**15CSE381 – COA Periodical Lab – 1**

24/07/2019

**SET 1**

P = (~A & ~B & ~C) | (~A & B & ~C) | (~A & ~B & C)

Q = (~A & ~B) | (~A & ~C)

Z = P + Q

Draw the Circuit diagram (4 marks), Truth Table (4 marks) and derive the logical equation for Z (4 marks). Implement the same using gate-level Verilog program (8 marks) and verify the output with the output of the truth table. Write the code using modules wherever applicable

**SET 2**

Design a combinational circuit with three inputs I3, I2 and I1 and two outputs O2 and O1 that behaves as follows. The outputs indicate the highest index of the inputs that is driven high. For example, if I3 is 0, I2 is 1 and I1 is 1, then O2, O1 would be 10 (i.e. the highest index of the inputs that is driven high is 2, hence the output 10, binary of 2). Specify the functions by filling out a complete truth table (4 marks) Using K map, derive the minimized logic equation (4 marks), draw the circuit diagram (4 marks) and implement the same in Verilog (8 marks