MIPS Superscaler Cycle Processor Emulator Project

Organization: CS-286, Computer Science, SIUE

Author: Mark McKenney

Description

In this project, you will create a simulator for a pipelined, super-scalar processor with cache. Your simulator will support the instruction set described in Project 1, and must be able to load a binary MIPS file and execute it. Furthermore, your simulator will produce the disassembled program code (exactly as you did in Project 1), and will produce a cycle-by-cycle simulation showing the processor state at each cycle. The processor state includes the contents of registers, buffers, cache, and data memory at each cycle. You do not need to implement exception/interrupt handling

Implementation

You may use any programming language that you like. You MUST include instructions in a README file that indicate how to compile (if necessary) and run your program. You MUST include a **Makefile** that will compile your code (if necessary).

It is highly recommended that in each cycle, your program executes each pipeline stage in REVERSE order. That is, first handle the WB stage, then the MEM/ALU stages, then the ISSUE stage, then the IF stage. By executing the pipelines in this order, you will ensure that the cache is updated in the proper order, and you will not have collisions in the buffers between pipeline stages.

Execution

Your program must accept command line arguments for execution. The following arguments must be supported (Executable named "mipssim"):

mipssim -i INPUTFILENAME -o OUTPUTFILENAME

Your program will produce 2 output files. One named **OUTPUTFILE-NAME_pipeline.txt**, which contains the simulation output, and one named **OUTPUTFILENAME_dis.txt**, which contains the disassembled program code for the input MIPS program.

Your program will be graded with the sample input and output provided to you

Expected Output

Sample inputs and expected outputs are provided for testing. The most simple program is t1.bin and they are progressively more complex in the following order: t1.bin, t2.bin, t3.bin, t4.bin, sample.bin

One note: depending on when in the clock cycle you update cache, your program may end up with 2 cache lines switched from the provided output for t3.bin and t4.bin. This is OK.

Details

Instruction format: The instruction format is exactly the same as in Project 1

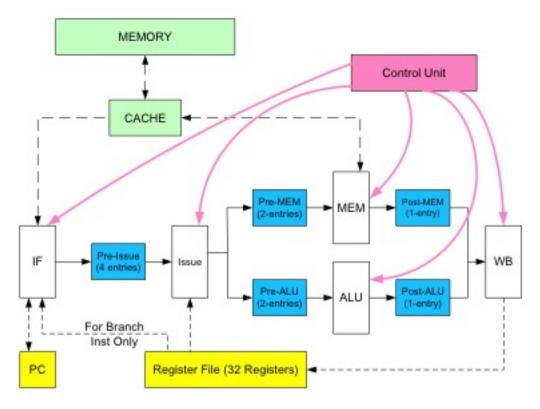


Figure 1: The processor datapath for this project.

White boxes represent functional units, blue boxes represent buffers (structured as queues) between the functional units, yellow boxes represent registers, and green boxes represent memory units. The various components are discussed in detail below:

Instruction Fetch (IF)

Instruction fetch can fetch and decode up to two instructions at each clock cycle. Instructions are always fetched and decoded in program order. The following conditions must be met before instructions can be fetched:

- 1. If the fetch unit is stalled, no instruction can be fetched at the current cycle (no pre-fetching). The fetch unit can be stalled due to a branch instruction or a cache miss (cache is described below)
- 2. If there is no room in the pre-issue buffer, no instructions can be fetched at the current cycle
- 3. If there is only one empty slot in the pre-issue buffer, only one instruction will be fetched

The IF unit can only fetch and decode an instruction if it is in the cache. If the instruction to be fetched is in the cache, the entire fetch and decode process takes only 1 clock cycle. If the instruction to be fetched is not in the cache, the cache unit will fetch the instruction from memory and it will be in the cache at the next clock cycle. If the first instruction to be fetched is not in the cache, the second instruction cannot be fetched even if it is in the cache.

If a branch instruction (J, JR, BEQ, BLTZ) is fetched along with its next (in order) instruction, the next instruction will be discarded (it needs to be re-fetched based on the branch outcome).

If a branch instruction is fetched, the fetch unit will try to read all the argument registers in order to calculate the target address. If all registers are ready, or the target is immediate, the PC will be updated at the end of the cycle. Otherwise, the IF unit stalls until all argument registers are available. Therefore, if all registers are ready for a branch instruction, then no stalls are introduced.

A register can be written and read in the same clock cycle. Assume writes take place in the first half of the cycle, and reads take place in the second half of the cycle.

When a BREAK instruction is fetched, no more instructions will be fetched. Branch, BREAK, NOP, and invalid instructions will all be fetched, but will not be written into the Pre-Issue Buffer (They are completely handled by IF). However, entries must be available in the Pre-Issue Buffer for any instruction to be fetched.

Pre-Issue Buffer:

The pre-issue buffer has 4 entries, each entry can store a single instruction. The instructions are sorted in their program order (entry 0 always contains the oldest instruction and entry 3 contains the newest).

Issue Unit:

The issue unit follows the basic scoreboarding algorithm to issue instructions. It can issue up to two instructions, out of order, per clock cycle. When an instruction is issued, it moves out of the pre-issue buffer and into either the pre-mem buffer or the pre-ALU buffer. The issue unit searches from entry 0 to entry 3 (IN THAT ORDER) of the pre-issue buffer and issues instructions if:

1. No structural hazards exist (there is room in the pre-mem/pre-ALU destination buffer)

- 2. No WBW hazards exist active instructions (issued but not finished, or earlier no-issued instructions)
- 3. No WBR hazards exist with earlier not-issued instructions (do not check for WBR hazards with instructions that have already been issued. In other words, you only need to check the earlier instructions in the preissue buffer and not in later buffers in the pipeline)
- 4. No RBW hazards (true data dependencies) exist with active instructions (all operands are ready)
- 5. A load instruction must wait for all previous stores to be issued
- 6. Store instructions must be issued in order

Remember, registers can be written and read in the same cycle.

Note

ADD R3, R2, R1 ADD R3, R4, R5

Note that in the above instructions, the second instruction will not be issued until the first instruction has written back R3 in the write-back stage (due to the WBW Hazard). The issue unit does not attempt to determine special cases in which WBW, RBW, or WBR hazards will be avoided.

Pre-ALU Queue:

The pre-ALU buffer has two entries. Each entry can store an instruction with its operands. The buffer is managed as a FIFO queue

ALU:

The ALU handles all non-memory instructions (everything except LW and SW and branch instructions that are handled in the IF stage). All ALU operations take one clock cycle. When the ALU finishes, the instruction is moved from the pre-ALU buffer to the post-ALU buffer. The ALU can only fetch one instruction from the pre-ALU buffer per clock cycle.

Post-ALU buffer:

The post-ALU buffer has one entry that can store the instruction with the destination register ID and the result of the ALU operation

Pre-Mem Queue:

The pre-mem buffer has two entries. Each entry can store an instruction with its address and data (for SW). It is managed as a FIFO queue.

MEM Unit:

The MEM unit handles LW and SW operations.

For LW, it takes one cycle to finish if it hits in the cache. If it misses in the cache, then the operation cannot be performed and must be retried in the next cycle. In this case, the operation remains in the pre-mem buffer. When a cache hit occurs, the operation finishes and the instruction, destination register, and data will be written to the post-MEM buffer.

A SW takes one cycle to finish if it hits in the cache. If it misses in the cache, then the operation cannot be performed and must be retried in the next cycle. In this case, the operation remains in the pre-mem buffer. When a cache hit occurs, the SW instruction finshes. The SW instruction never goes into the post-MEM buffer.

Write Back Unit:

The WB unit can execute two write-backs in one cycle. It fetches the contents of the post-ALU and post-MEM buffers and updates the register file.

PC:

The PC holds the address of the next instruction. It should be initialized to 96.

Register File:

There are 32 registers. Assume sufficient read/write ports to perform all necessary operations during a single clock cycle.

Notes on Pipeline:

- 1. The execution finishes when a BREAK instruction is fetched and the pipeline is empty (all other instructions have finished)
- 2. No data forwarding
- 3. No delay slot will be used for branching
- 4. Different instructions finish in different stages:
 - NOP, Branch, BREAK, Jumps: only use IF stage
 - SW only uses IF, issue, MEM stages
 - LW uses all stages on MEM pipeline: IF, issue, MEM, WB stages
 - ALU ops use all stages on ALU pipeline: IF, issue, ALU, WB stages

Cache Description:

The cache is uniform (holds both data and instructions) and is a 2-way associative cache with 4 sets. Each cache line/block contains 2 data words (1 word = 32 bits = 4 bytes). Because each cache line/block is 64 bits wide, all memory fetch operations will return two words (64 bits). The cache is organized as follows:

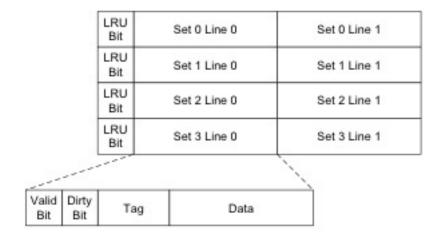


Figure 2: Cache diagram for the project.

Note that since all address are word aligned , the lower two bits will be discarded when calculating which set data will be written to in cache. Furthermore, since each cache line is 2 words wide, memory is effectively two word aligned, so the lower three bits of a memory address are discarded when calculating which cache set data should be written to.

There are sufficient ports of cache so that the IF and MEM unit can access the cache at the same cycle without any port conflict. If the two units are accessing the same set at the same time, assume MEM will be executed at the first half of the cycle and IF will be executed at the second half of the cycle.

Note that the IF unit can only execute 1 memory read per cycle. Therefore, if the IF unit is attempting to fetch the instructions as 100 and 104, and neither are in cache, then a memory read for the words at address 96 and 100 can be initiated. The memory read for the words at addresses 104 and 108 must be initiated during the next clock cycle.

All the bits will be initialized as 0. (The LRU bit is initialized to 0 also.) When a valid line exists, the valid bit will be turned on (set to be 1).

The dirty bit will be turn on when the pipeline writes to any part of the line.

It takes 1 cycle to get data from main memory to cache. Assume bypassing is used here so that both the cache and the request unit (IF or MEM) can get the data at the same cycle. For example, if IF requests a data in cycle 5 and it is a miss the IF and cache will get the data in cycle 6.

The write-back from cache to main memory takes no time (for simplification).

All dirty blocks will be written back at the cycle the simulation is finished.

Output Format

At the end of a clock cycle, the processor, cache, and memory state will be output.

If any entry in a buffer/queue is empty, no content should be printed. Only instructions are printed, not addresses or values computed. The instruction should be printed as it was for Project 1.

Every cache line must be printed, even if it is empty. Furthermore, the cache values should be printed as a bit string.

The output format is as follows:

```
20 hyphens and a new line
Cycle[value]:
<black_line>
Pre-Issue Buffer:
<tab>Entry 0:<tab>[instruction]
<tab>Entry 1:<tab>[instruction]
<tab>Entry 2:<tab>[instruction]
<tab>Entry 3:<tab>[instruction]
Pre_ALU Queue:
<tab>Entry 0:<tab>[instruction]
<tab>Entry 1:<tab>[instruction]
Post_ALU Queue:
<tab>Entry 0 :<tab>[instruction]
Pre_MEM Queue:
<tab>Entry 0:<tab>[instruction]
<tab>Entry 1:<tab>[instruction]
Post_MEM Queue:
<tab> Entry 0:<tab>[instruction]
< blank_line >
Registers
R00:< tab >< int(R0) >< tab >< int(R1) > ... < tab >< int(R7) >
R08: < tab > < int(R8) > < tab > < int(R15) >
R16:< tab >< int(R16) >< tab >< int(R17) > . . < tab >< int(R23) >
R24:< tab >< int(R24) >< tab >< int(R25) >..< tab >< int(R31) >
<black line>
Cache
Set 0: LRU=<Value>
<tab>Entry 0: [(valid bit, dirty bit, int(tag))<word0,word1>]
<tab>Entry 1: [(valid bit, dirty bit, int(tag))<word0,word1>]
. . .
Set 3: LRU=<Value>
<tab>Entry 0: [(valid bit, dirty bit, int(tag))<word0,word1>]
<tab>Entry 1: [(valid bit, dirty bit, int(tag))<word0,word1>]
<black line>
Data
< firstDataAddress >:< tab >< show 8 data words as ints w/tabs in between >
..... < continue until the last data word >
```

Grading

A valid attempt that compiles successfully and produces simulation files for at least 10 clock cycles (even if the files do NOT match the expected output for those 10 cycles) will receive 72 points. Note that it is not sufficient for those 10 cycles to attempt to re-execute the same instruction. At the very least, it should fetch successive instructions. Your basic program should also disassemble the programs correctly (you should already have a working disassembler).

Each **simulation file** that matches the expected output provided in the following files will receive 7 points. Therefore, to get 100 percent you must match the pipeline output for each of the 4 binary files provided.

We expect your simulation file to EXACTLY match ours. We will use the diff program to verify exactness. We will use diff -wbB to suppress white space differences.

Becuase cache can be accessed both in IF and MEM stages, you may run into an issue where the LRU bit in your implementation is switched for a cache line from the expected output. To avoid this, take a look at the videos on how I implement cache misses. In general, a cache miss should simply record the memory address that was missed in a list. At the beginning of each clock cycle, the first thing to do should be to updated the cache based on that miss list. If you treat the list as a FIFO queue (cache is updated in the order the misses occurred in the last clock cycle), then your cache will match the expected output.

```
Page 1 of 1
EX_readBinaryFile.cpp
#include <iostream>
#include <unistd.h>
#include <fcntl.h>
#include <iomanip>
using namespace std;
int main()
           char buffer[4];
           int i;
char * iPtr;
iPtr = (char*)(void*) &i;
           int FD = open("test2.bin", O_RDONLY);
           int amt = 4;
           while( amt != 0 )
{
                       amt = read(FD, buffer, 4);
if( amt == 4)
                                   iPtr[0] = buffer[3];
iPtr[1] = buffer[2];
                                   iPtr[2] = buffer[1];
                                   iPtr[3] = buffer[0];
cout << "i = " <<hex<< i << endl;</pre>
                       }
            }
```

```
EX_readBinaryFile.java
                                                                                               Page 1 of 1
import java.io.BufferedInputStream;
import java.io.DataInputStream;
import java.io.File;
import java.io.FileInputStream;
import java.io.FileNotFoundException;
import java.io.IOException;
class EX_readBinaryFile
    public static void main(String[] args) throws IOException, FileNotFoundException
         File file = new File("test1.bin");
         byte[] fileData = new byte[(int) file.length()];
DataInputStream dis = new DataInputStream(new FileInputStream(file));
         dis.readFully(fileData);
         dis.close();
          for( int i = 0; i < fileData.length; i+=4 )
               int x = 0;
              x = x \mid ((fileData[i] \& 0x000000FF) << 24);
              x = x | ((fileData[i+1] & 0x000000FF) << 16);
x = x | ((fileData[i+2] & 0x000000FF) << 8);
x = x | (fileData[i+3] & 0x000000FF);
               System.out.println(x);
               System.out.println((x>>26) & 0x0000003F);
               System.out.println(((x << 6)>>27) & 0x = 0 = 0 = 0
              System.out.println( Integer.toHexString(x) );
          }
    }
```

```
EX_readBinaryFile.py
                                                                                         Page 1 of 1
import sys
import os
import struct
# convert ints to signed
def imm16BitUnsignedTo32BitSignedConverter( num ):
         negBitMask = 0x00008000
         # if the 16th bit is 1, the 16 bit value is negative if( negBitMask & num ) > 0 :
                  # put 1s in the upper 16 bits
                  num = num | 0xFFFF0000 # now perform a 2's complement conversion
                  # flip the bits using XOR
num = num ^ 0xffffffff
                   # add 1
                  num = num + 1
                   \ensuremath{\text{\#}} num is now the positive version of the number
                  \mbox{\#} multiply by -1 to get a signed integer with the negative number num = num * -1
         return num
# how to read binary file and get ints
inFile = open( sys.argv[1], 'rb' )
# get the file length
inFileLen = os.stat( sys.argv[1] )[6]
inFileWords = inFileLen / 4
instructions = []
address = []
# read the words from the file
for i in range( inFileWords ) :
         instructions.append( struct.unpack('>I', inFile.read(4))[0] )
address.append( 96 + (i*4) )
         \ensuremath{\text{\#}} use I to hold the current instruction
         I = instructions[ len(instructions)-1 ]
         # get IMMEDIATE bits
         IMM = ((I << 16) \& 0xffffffff ) >> 16
         IMM = imm16BitUnsignedTo32BitSignedConverter( IMM )
         print bin(I)
         print IMM
         # get the opcode bits
         OP = I >> 26
         print OP
         # get the RS bits
         RS = ((I << 6) \& 0xFFFFFFFF) >> 27
         print RS
         print '----'
inFile.close()
```

```
b2t.c
                                                                          Page 1 of 1
/****************
This program converts a binary file to a file
containing string representations of the 1's and 0's
in the binfary file.
// gcc -o b2t b2t.c
// Usage ./a.out < inputfile > outputfile
#include<stdio.h>
main( int argc, char** argv)
    if ( argc >1 )
       fprintf(stderr, "Usage: ./a.out < input_txt > output_bin\n");
    char word[32];
    unsigned char vals[4];
   unsigned char w, div, b; unsigned char tot;
    w = 0;
    while( scanf( "%c", &tot) != EOF )
           div = 128;
           for( b=0; b<8; b++ )
               if( tot >= div)
               {
                   printf( "1" );
                   tot -= div;
               else
               printf( "0");
div = div/2;
           }
          w ++;
if ( w == 4 )
          {
              printf("\n");
              w = 0;
    }
```

```
t2b.c
                                                                              Page 1 of 1
/****************
This program converts a text file containing text
strings of 1's and 0's to a binary file.
for example, the text string:
000000010000000011111111110101010
would result in the following binary sequence (written as hex here) in the output file:
0100FFAA
 ***********************************
// gcc -o t2b t2b.c
// Usage ./a.out < inputfile > outputfile
#include<stdio.h>
main( int argc , char **argv )
    if(argc > 1)
    fprintf(stderr, "Usage: ./a.out < input_txt > output_bin\n");
    char word[32];
    unsigned char vals[4];
    int w, mul, b;
    unsigned char tot ;
    while( scanf(" %s", word ) > 0 )
        for( w=0; w<4; w++ )
            mul = 128;
tot = 0;
            for( b=0; b<8; b++ )
                tot += (word[w*8+b]=='1')*mul;
                mul = mul/2;
            fputc( tot, stdout);
       }
    }
```

t1_dis.txt Page 1 of 1 1 00011 00000 00001 00000 00010 000000 96 R1, 128(R0) LW R1, R1, #-8 R1, 128(R0) R1, #8 1 01000 00001 00001 11111 11111 111000 100 ADDI 1 01011 00000 00001 00000 00010 000000 104 SW 1 00001 00001 00000 00000 00000 000010 BLTZ1 00010 00000 00000 00000 00000 011000 112 #96 Invalid Instruction 0 00000 00000 00000 00000 00000 000000 116 0 00000 00000 00000 00000 00000 000000 120 Invalid Instruction 1 00000 00000 00000 00000 00000 001101 124 BREAK 128 16 132

```
t1_pipeline.txt
                                      Page 1 of 8
Cycle:1
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
        Ω
           0
                0
                    0
                        0
                            0
                                0
R08:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
Entry
Data
128:
   4
       16
Cycle:2
Pre-Issue Buffer:
   Entry 0:
            [ LW
               R1, 128(R0)]
   Entry 1:
Entry 2:
            [ADDI R1, R1, #-8]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
```

```
Page 2 of 8
t1_pipeline.txt
Post_MEM Queue:
   Entry 0:
Registers
       0
                            0
R00:
   0
                  0
                     0
                         0
R08:
   0
       0
                  0
                         0
                            0
R16:
   0
       0
          0
                  0
                     0
                         0
                            0
R24:
                            0
   0
       0
          0
                     0
                         0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Dat.a
   4
       16
128:
Cycle:3
Pre-Issue Buffer:
   Entry 0:
Entry 1:
          [ADDI R1, R1, #-8]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
              R1, 128(R0)]
   Entry 0:
          [LW
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       0
          0
              0
                  0
                     0
                         0
                            0
R08:
   Ω
       Ω
          0
              Ω
                  0
                     Ω
                         Ω
                            0
R16:
   Ω
          Ω
              Ω
                     Ω
                            Ω
       Ω
                  0
                         Ω
                            0
R24:
   0
       0
          0
              0
                  0
                     0
                         0
Cache
Set 0: LRU=1
   Entry
Set 1: LRU=0
```

```
t1_pipeline.txt
                         Page 3 of 8
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
128:
  4
     16
Cycle:4
Pre-Issue Buffer:
        [ADDI
          R1, R1, #-8]
  Entry 0:
          R1, 128(R0)]
  Entry 1:
        [SW
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
        [ LW
          R1, 128(R0)]
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     Ω
        0
          Ω
             Ω
                0
                  Ω
                     0
R08:
  0
     Ω
        0
          0
             0
                0
                  Ω
                     0
R16:
  0
     0
        0
          0
             0
                0
                  0
                     0
R24:
  0
     0
        0
          0
             0
                0
                  0
                     0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Data
```

```
t1_pipeline.txt
                                       Page 4 of 8
128: 4 16
Cycle:5
Pre-Issue Buffer:
           [ADDI R1, R1, #-8]
[SW R1, 128(R0)]
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
            [LW
               R1, 128(R0)]
Registers
       0
R00:
            0
                    0
                        0
                            0
                                0
R08:
    0
            0
                    0
                            0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Data
   4
       16
128:
Cycle:6
Pre-Issue Buffer:
    Entry 0:
Entry 1:
           ſsw
                R1, 128(R0)1
    Entry 2:
    Entry 3:
Pre_ALU Queue:
           [ADDI R1, R1, #-8]
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
```

```
t1_pipeline.txt
                                 Page 5 of 8
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
R08:
   0
      0
          0
                     0
                        0
                            0
R16:
          0
              0
                            0
   0
      0
                 0
                     0
                        0
R24:
   0
                            0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
   4
128:
      16
Cycle:7
Pre-Issue Buffer:
             R1, 128(R0)]
   Entry 0:
          [SW
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
          [ADDI
   Entry 0:
             R1, R1, #-8]
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       4
          Ω
              Ω
                 Ω
                     Ω
                        Ω
                            Ω
R08:
   Ω
          Ω
                            Ω
      Ω
              Ω
                 0
                     Ω
                        Ω
R16:
   0
      0
          0
              0
                 0
                     0
                        0
                            0
R24:
   0
      0
          0
              0
                 0
                     0
                        0
                            0
Cache
Set 0: LRU=0
   Entry
```

```
Page 6 of 8
t1_pipeline.txt
Set 1: LRU=1
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
128:
  4
     16
Cycle:8
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
          R1, 128(R0)1
       [SW
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  Ω
     -4
       Ω
          Ω
            Ω
               Ω
                  Ω
                    Ω
R08:
  0
     0
       0
          0
            0
               0
                  0
                    0
R16:
  0
     Ω
       0
          0
            0
               0
                  Ω
                    0
R24:
  0
     0
       0
          0
            0
               0
                  0
                    0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
```

```
t1_pipeline.txt
                                   Page 7 of 8
Data
128:
   4
     16
Cycle:9
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
                         0
R08:
   0
       0
           0
              0
                  0
                      0
                         0
                             0
R16:
   0
R24:
   0
                             0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Set 3: LRU=0
   Entry
Entry
Data
  4 16
128:
Cvcle:10
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
```

```
t1_pipeline.txt
                      Page 8 of 8
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
 0
    -4
             0
                  0
         0
           0
      0
R08:
    0
                  0
  0
             0
                0
R16:
  0
    0
      0
         0
           0
             0
                0
                  0
R24:
                  0
  0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
128:
  -4
    16
```

t2_dis.txt Page 1 of 1 1 00011 00000 00001 00000 00010 000000 LW R1, 128(R0) 1 00011 00000 00010 00000 00010 100000 100 LW R2, 160(R0) 1 01011 00000 00001 00000 00010 000100 104 SW R1, 132(R0) 1 00011 00000 00011 00000 00011 000000 R3, 192(R0) R1, 164(R0) R4, 196(R0) 1 01011 00000 00001 00000 00010 100100 SW 112 1 00011 00000 00100 00000 00011 000100 116 LW 1 00001 00100 00000 11111 11111 111101 120 BLTZ R4, #-12 1 00000 00000 00000 00000 00000 001101 124 BREAK 00000000000000000000000000000000011 128 3 1111111111111111111111111111111111111 132 -5 0 136 140 0 144 0 148 Ω 0 152 156 0 160 4 164 -6 168 0 172 0 176 0 180 0 184 0 188 0 -2 196 0

```
t2_pipeline.txt
                                      Page 1 of 12
Cycle:1
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
   Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R08:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                        0
                            0
                                0
R24:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
Entry
Data
128:
    3
        -5
            0
                    0
                        0
                            0
                                0
                                0
160:
    4
        -6
    -2
192:
Cycle:2
Pre-Issue Buffer:
                R1, 128(R0)]
            [T.W
    Entry 0:
                R2, 160(R0)]
    Entry 1:
            [LW
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
```

```
t2_pipeline.txt
                                       Page 2 of 12
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        0
                     0
                         0
                             0
                                 0
R08:
                                 0
    0
        0
            0
                0
                    0
                         0
                             0
R16:
    0
            0
                0
                         0
                             0
                                 0
        0
                     0
                                 0
R24:
    0
        0
            0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
128:
    3
        -5
            0
                0
                     0
                         0
                             0
                                 0
        -6
                     Ω
                                 Ω
160:
    4
            0
                             0
    -2
192:
        0
Cycle:3
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                R1, 128(R0)]
            [LW
                R2, 160(R0)1
    Entry 1:
            [LW
Post_MEM Queue:
    Entry 0:
Registers
        0
                     Ω
                                 0
R00:
    0
            0
                0
                         0
                             Ω
R08:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R16:
    0
        Ω
            0
                0
                     0
                         0
                             Ω
                                 0
R24:
    0
        0
                0
                     0
                         0
                             0
                                 0
Cache
Set 0: LRU=1
```

```
t2_pipeline.txt
                              Page 3 of 12
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
128:
   3
      -5
         Ω
            Ω
                0
                   0
                      Ω
                         0
160:
      -6
         0
            0
                0
                   0
                      0
                         0
192:
   -2
      0
Cycle:4
Pre-Issue Buffer:
         [SW
            R1, 132(R0)]
   Entry 0:
   Entry 1:
            R3, 192(R0)]
         [LW
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
            R1, 128(R0)]
   Entry 0:
         [LW
   Entry 1:
         [LW
            R2, 160(R0)]
Post_MEM Queue:
   Entry 0:
Registers
R00:
      0
                0
                      0
R08:
   0
      0
         0
            0
                0
                   0
                      0
                         0
R16:
      0
         0
            0
                      0
                         0
   0
                         0
R24:
   0
      0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
0: [\,(1\,,0\,,3\,)<1010110000000001000000010000100\,,1000110000000110000000110000000>]
   Entry
Set 2: LRU=0
   Entry
Set 3: LRU=0
```

```
t2_pipeline.txt
                                   Page 4 of 12
   Entry
Entry
Data
128:
   3
       -5
           0
                  0
                      0
                          0
                              0
160:
   4
       -6
                  0
                              0
           0
                          0
192:
   -2
       0
Cycle:5
Pre-Issue Buffer:
               R1, 132(R0)]
           [SW
   Entry 0:
               R3, 192(R0)]
   Entry 1:
           [LW
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [LW
               R2, 160(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
           [LW
               R1, 128(R0)]
Registers
R00:
       0
           0
               0
                  0
                      0
                          0
                              0
   0
R08:
   0
       0
           0
               0
                  0
                      0
                          0
                              0
R16:
   0
       0
           0
               0
                  0
                      0
                          0
                              0
R24:
   Ω
               Ω
                  Ω
                              Ω
       0
           0
                      Ω
                          0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
   3
       -5
                          0
128:
           Ω
               0
                  Ω
                      0
                              Ω
160:
   4
       -6
           0
               0
                  0
                      0
                          0
                              0
192:
   -2
       Ω
Cycle:6
Pre-Issue Buffer:
   Entry 0:
           [LW
               R3, 192(R0)]
```

```
t2_pipeline.txt
                                          Page 5 of 12
    Entry 1:
             [SW
                 R1, 164(R0)]
    Entry 2:
             [LW
                 R4, 196(R0)]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [ LW
                 R2, 160(R0)]
             ſSW
                 R1, 132(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        3
R00:
    0
             0
                  Ω
                      Ω
                          0
                               Ω
                                   0
R08:
    0
        0
             0
                  0
                      0
                          0
                               0
                                   0
R16:
    0
        0
             0
                  0
                      0
                          0
                               0
                                   0
R24:
    0
        Ω
             Ω
                  Ω
                      Ω
                          Ω
                               Ω
                                   Ω
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
128:
         -5
160:
    4
         -6
             0
                      0
                                   0
192:
    -2
        0
Cycle:7
Pre-Issue Buffer:
                 R1, 164(R0)]
R4, 196(R0)]
             [SW
    Entry 0:
    Entry 1:
             [LW
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
                 R1, 132(R0)]
    Entry 0:
             [SW
    Entry 1:
             [LW
                 R3, 192(R0)]
Post_MEM Queue:
    Entry 0:
             [LW
                  R2, 160(R0)]
```

```
t2_pipeline.txt
                                   Page 6 of 12
Registers
R00:
   0
       3
           0
              0
                  0
                      0
                         0
                             0
R08:
   0
       0
           0
              0
                  0
                      0
                         0
                             0
R16:
   0
       0
           0
                          0
                             0
                             0
R24:
   0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
128:
   3
       -5
           0
              0
                  0
                      0
                          0
                             0
160:
   4
       -6
           0
                  0
                             0
       0
   -2
192:
Cvcle:8
Pre-Issue Buffer:
   Entry 0:
           [LW
              R4, 196(R0)]
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [LW
              R3, 192(R0)]
   Entry 1:
              R1, 164(R0)]
           [SW
Post_MEM Queue:
   Entry 0:
Registers
R00:
       3
           4
              0
                  0
                      0
                         0
                             0
   0
R08:
   0
       0
           0
              0
                  0
                      0
                         0
                             0
R16:
   0
       0
           0
              Ω
                  0
                      Ω
                         0
                             Ω
R24:
   0
           Ω
              Ω
                  Ω
                             Ω
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
```

```
Page 7 of 12
t2_pipeline.txt
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Dat.a
     -5
128:
  3
        Ω
           Ω
              Ω
                 0
                   Ω
                      Ω
160:
  4
     -6
        0
           0
              0
                 0
                   0
                      0
  -2
192:
     0
Cycle:9
Pre-Issue Buffer:
  Entry 0:
        [LW
           R4, 196(R0)]
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
           R3, 192(R0)]
  Entry 0:
        M.T l
  Entry 1:
        [SW
           R1, 164(R0)]
Post_MEM Queue:
  Entry 0:
Registers
R00:
  Ω
     3
        4
           Ω
              Ω
                 Ω
                   Ω
                      Ω
R08:
  0
     0
        0
           0
              0
                 0
                   0
                      0
R16:
  0
     Ω
        0
           0
              0
                 0
                   Ω
                      0
R24:
  0
     0
        0
           0
              0
                   0
                      0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
```

```
t2_pipeline.txt
                                       Page 8 of 12
Data
128:
    3
        -5
            0
                0
                     0
                         0
                             0
                                 0
160:
    4
        -6
            0
                             0
                                 0
192:
    -2
        0
Cycle:10
Pre-Issue Buffer:
    Entry 0:
Entry 1:
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
            [SW
                R1, 164(R0)]
    Entry 1:
            [LW
                R4, 196(R0)]
Post_MEM Queue:
    Entry 0:
            [LW
                R3, 192(R0)]
Registers
R00: 0
            4
                0
                     0
                             0
                                 0
R08:
    0
        0
            0
                     0
                         0
                                 0
R16:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R24:
    0
        0
                     0
                                 0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
128:
    3
        -5
            0
                0
                     0
                         0
                             0
                                 0
160:
    4
        -6
            0
                0
                     0
                         0
                             0
                                 0
    -2
       0
192:
Cycle:11
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
```

```
t2_pipeline.txt
                                         Page 9 of 12
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
             [SW
                 R1, 164(R0)]
    Entry 0:
    Entry 1:
                 R4, 196(R0)]
             [LW
Post_MEM Queue:
    Entry 0:
Registers
        3
                 -2
                          0
                              0
                                   0
R00:
             4
                      0
    0
R08:
                 0
    0
        0
                                   0
             0
                      0
                          0
                              0
R16:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
    Ω
                 Ω
                      Ω
                                   Ω
R24:
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
    3
        - 5
128:
             Ω
                 Ω
                      Ω
                          Ω
                              Ω
                                   Ω
160:
    4
        -6
             0
                 0
                      0
                          0
                              0
                                   0
    - 2
192:
        Ω
Cycle:12
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [T.W
                 R4, 196(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        3
             4
                 -2
                      0
                          0
                              0
                                   0
R08:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
R16:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
R24:
    0
        0
             0
                              0
                                   0
```

t2_pipeline.txt Page 10 of 12 Cache Set 0: LRU=0 Entry Entry Set 1: LRU=1 Entry Entry Set 2: LRU=1 Entry Entry Set 3: LRU=1 Entry Entry 128: 3 160: 4 -6 0 0 0 -2 192: 0 Cycle:13 Pre-Issue Buffer: Entry 0: Entry 1: Entry 2: Entry 3: Pre_ALU Queue: Entry 0: Entry 1: Post_ALU Queue: Entry 0: Pre_MEM Queue: Entry 0: Entry 1: Post_MEM Queue: Entry 0: [LW R4, 196(R0)] Registers 3 R00: 0 -2 0 R08: 0 0 0 0 0 0 0 0 R16: 0 0 0 0 0 0 0 0 R24: 0 Cache Set 0: LRU=1 Entry Entry Set 1: LRU=1 Entry $0: [\,(1\,,0\,,3\,)\,<\bar{10}10110000000001000000010000100\,,1000110000000110000000110000000]$ Set 2: LRU=1

```
Page 11 of 12
t2_pipeline.txt
Entry
Set 3: LRU=1
   Entry
Entry
Dat.a
      3
         0
                  0
                     0
                        0
   3
            0
               0
128:
160:
      -6
                        0
   4
         0
            0
               0
                  0
                     0
192:
   -2
      0
Cycle:14
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
      3
                     0
                        0
         4
            -2
               0
                  0
R00:
   0
R08:
            0
   0
      0
         0
               0
                  0
                     0
                        0
R16:
   0
      Ω
         0
            Ω
               0
                  Ω
                     0
                        0
R24:
   0
      0
         0
            0
               0
                  0
                     0
                        0
Cache
Set 0: LRU=1
   Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
128:
   3
      3
         0
            0
               0
                  0
                     0
                        0
160:
   4
      -6
         0
               0
                     0
                        0
192:
   -2
      0
```

```
t2_pipeline.txt
                              Page 12 of 12
Cycle:15
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
  0
      3
            -2
                0
                   0
                      0
                         0
                0
R08:
   0
      0
         0
            0
                   0
                      0
                         0
R16:
   0
      0
         0
            0
                0
                   0
                      0
                         0
R24:
   0
      0
                         0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Data
128:
160:
   4
      3
         0
                0
                   0
                      0
                         0
192:
```

t3_dis.txt Page 1 of 1 1 00011 00000 00001 00000 00010 001000 LW R1, 136(R0) 1 00011 00001 00010 00000 00010 001000 100 LW R2, 136(R1) 1 00011 00010 00011 00000 00010 001000 104 LW R3, 136(R2) 1 00000 00001 00011 00100 00000 100000 ADD R4, R1, R3 1 00000 00100 00010 00011 00000 100000 112 ADD R3, R4, R2 R1, R2, #-5 R3, R2, #-5 1 01000 00010 00001 11111 11111 111011 116 ADDI 1 01000 00010 00011 11111 11111 111011 120 ADDI R1, 136(R0) R3, #-36 1 01011 00000 00001 00000 00010 001000 SW 124 1 00001 00011 00000 11111 11111 110111 BLTZ 128 1 00000 00000 00000 00000 00000 001101 132 BREAK 12 136 140 0 144 0 20 148 152 0 -5 156

```
t3_pipeline.txt
                                      Page 1 of 15
Cycle:1
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R08:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
Entry
Data
136:
    12
       0
            0
                20
                    0
                        -5
Cycle:2
Pre-Issue Buffer:
    Entry 0:
                R1, 136(R0)]
            [ LW
    Entry 1:
Entry 2:
            [LW
                R2, 136(R1)]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
```

```
Page 2 of 15
t3_pipeline.txt
Post_MEM Queue:
   Entry 0:
Registers
       0
                             0
R00:
   0
          0
                  0
                     0
                         0
R08:
   0
       0
                  0
                         0
                             0
R16:
   0
       0
           0
              0
                  0
                     0
                         0
                             0
R24:
                             0
   0
       0
           0
                     0
                         0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Dat.a
   12
              20
                     -5
       0
           Ω
                  Ω
136:
Cycle:3
Pre-Issue Buffer:
   Entry 0:
Entry 1:
           [LW
              R2, 136(R1)]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
              R1, 136(R0)]
   Entry 0:
           [LW
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       0
           0
              0
                  0
                     0
                         0
                             0
R08:
   Ω
       Ω
           0
              Ω
                  0
                     Ω
                         Ω
                             0
R16:
   Ω
           Ω
              Ω
                     Ω
                         Ω
                             Ω
       Ω
                  0
                             0
R24:
   0
       0
           0
              0
                  0
                     0
                         0
Cache
Set 0: LRU=1
   Entry
Set 1: LRU=0
```

```
t3_pipeline.txt
                          Page 3 of 15
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
136:
  12
     0
        0
           20
             0
                -5
Cycle:4
Pre-Issue Buffer:
        [LW
           R2, 136(R1)]
  Entry 0:
  Entry 1:
        [LW
           R3, 136(R2)]
  Entry 2:
        [ADD
           R4, R1, R3]
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
        [ LW
           R1, 136(R0)]
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     Ω
        0
           Ω
             Ω
                0
                   Ω
                      0
R08:
  0
     Ω
        0
           0
             0
                0
                   Ω
                      0
R16:
  0
     0
        0
           0
             0
                0
                   0
                      0
R24:
  0
     0
        0
           0
             0
                0
                   Ω
                      0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Data
```

```
t3_pipeline.txt
                                        Page 4 of 15
136: 12 0
           0
                20 0 -5
Cycle:5
Pre-Issue Buffer:
                R2, 136(R1)]
    Entry 0:
            [LW
    Entry 1:
            [LW
                R3, 136(R2)]
    Entry 2:
            [ADD
                R4, R1, R3]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
            [LW
                R1, 136(R0)]
Registers
R00:
        0
            0
                 0
                     0
                         0
                             0
                                  0
R08:
    0
        0
            0
                 0
                     0
                         0
                             0
                                  0
R16:
    0
        0
            0
                 0
                     0
                         0
                             0
                                  0
R24:
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
   12
                 20
                         -5
136:
Cycle:6
Pre-Issue Buffer:
                R3, 136(R2)]
    Entry 0:
Entry 1:
            M.T ]
            R4, R1, R3]
            [ADD
                R3, R4, R2]
    Entry 2:
                R1, R2, #-5]
    Entry 3:
            [ADDI
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
            [LW R2, 136(R1)]
```

```
t3_pipeline.txt
                                   Page 5 of 15
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
       12
R00:
   0
R08:
   0
       0
           0
                  0
                      0
                          0
                              0
R16:
       0
               0
                              0
   0
           0
                  0
                      0
                          0
R24:
   0
                              0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
   12
                      -5
      0
           0
               20
                  0
136:
_____
Cycle:7
Pre-Issue Buffer:
               R3, 136(R2)]
   Entry 0:
           [LW
   Entry 1:
           [ADD
               R4, R1, R3]
   Entry 2:
           [ADD
               R3, R4, R2]
   Entry 3:
           [ADDI
               R1, R2, #-5]
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [LW
              R2, 136(R1)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       12
           Ω
               Ω
                  Ω
                      Ω
                          Ω
                              Ω
R08:
   Ω
       Ω
                              Ω
           0
               Ω
                  0
                      Ω
                          0
R16:
   0
       0
           0
               0
                  0
                      0
                          0
                              0
R24:
   0
       0
           0
               0
                  0
                      0
                          0
                              0
Cache
Set 0: LRU=1
   Entry
```

```
Page 6 of 15
t3_pipeline.txt
Set 1: LRU=0
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
136:
  12
     0
        0
           2.0
              0
                 -5
Cycle:8
Pre-Issue Buffer:
  Entry 0:
        [LW
           R3, 136(R2)]
  Entry 1:
        [ADD
           R4, R1, R3]
           R3, R4, R2]
  Entry 2:
        [ADD
  Entry 3:
        [ADDI
           R1, R2, #-5]
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
           R2, 136(R1)]
  Entry 0:
        [LW
Registers
R00:
  0
     12
        Ω
           Ω
              Ω
                 Ω
                   Ω
                      Ω
R08:
  0
     0
        0
           0
              0
                 0
                   0
                      0
R16:
  0
     Ω
        0
           0
              0
                 0
                   Ω
                      0
R24:
  0
     0
        0
           0
              0
                 0
                   0
                      0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
```

```
t3_pipeline.txt
                                       Page 7 of 15
Data
136:
   12
      0
            0
                20
                    0
                         -5
Cycle:9
Pre-Issue Buffer:
    Entry 0:
            [ADD
                R4, R1, R3]
                R3, R4, R2]
    Entry 1:
            [ADD
    Entry 2:
Entry 3:
            [ADDI
                R1, R2, #-5]
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
            [LW
                R3, 136(R2)]
    Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
        12
            20
                0
                     0
                         0
                             0
R08:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R16:
        0
            0
    0
R24:
    0
        0
                                 0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
   12 0
            0
                20
                     0
                        -5
136:
Cvcle:10
Pre-Issue Buffer:
            R4, R1, R3]
    Entry 0:
            [ADD
                R3, R4, R2]
    Entry 1:
                R1, R2, #-5]
    Entry 2:
            [ADDI
            [ADDI R3, R2, #-5]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
```

```
t3_pipeline.txt
                                      Page 8 of 15
    Entry 0:
            [LW
                R3, 136(R2)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
        12
            20
                        0
                                0
R08:
        0
                                0
    0
            0
                0
                    0
                        0
                            0
R16:
    0
            0
                0
                        0
                                0
        0
                    0
                            0
R24:
    0
        0
            0
                    0
                                0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
   12 0
            0
                2.0
                    0
                        -5
136:
Cycle:11
Pre-Issue Buffer:
    Entry 0:
            [ADD
                R4, R1, R3]
    Entry 1:
            [ADD
                R3, R4, R2]
    Entry 2:
            [ADDI
                R1, R2, #-5]
   Entry 3:
            [ADDI
                R3, R2, #-5]
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
   Entry 1:
Post_MEM Queue:
            [LW
               R3, 136(R2)1
   Entry 0:
Registers
R00:
       12
            2.0
                Ω
                    Ω
                        Ω
                            Ω
                                Ω
   Ω
R08:
        0
    0
            0
                0
                    0
                        0
                            0
                                0
R16:
    0
        Ω
            0
                0
                    Ω
                        0
                            Ω
                                0
R24:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=1
    Entry
```

```
Page 9 of 15
t3_pipeline.txt
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
136:
  12
    0
       Ο
          2.0
             Ω
                - 5
Cycle:12
Pre-Issue Buffer:
  Entry 0:
        [ADD
          R3, R4, R2]
  Entry 1:
        [ADDI
          R3, R2, #-5]
  Entry 2:
        [SW
          R1, 136(R0)]
  Entry 3:
Pre_ALU Queue:
  Entry 0:
        [ADD
          R4, R1, R3]
        [ADDI
          R1, R2, #-5]
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     12
        20
          -5
             0
                0
                  0
                     0
R08:
  0
     Ω
        0
          Ω
             0
                0
                  Ω
                     0
R16:
  0
     0
        0
          0
             0
                0
                  0
                     0
R24:
  0
     0
        0
          0
                0
                  Ω
                     0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
```

```
t3_pipeline.txt
                                       Page 10 of 15
Data
136:
    12
       0
            0
                 20
                     0
                         -5
Cycle:13
Pre-Issue Buffer:
    Entry 0:
            [ADD
                 R3, R4, R2]
    Entry 1:
            [ADDI
                 R3, R2, #-5]
    Entry 2:
                R1, 136(R0)]
            [SW
    Entry 3:
Pre_ALU Queue:
    Entry 0:
            [ADDI
                R1, R2, #-5]
    Entry 1:
Post_ALU Queue:
                R4, R1, R3]
    Entry 0:
            [ ADD
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        12
            20
                 -5
                     0
                         0
                             0
                                  0
R08:
    0
        0
                                  0
                     0
R16:
    0
        0
            0
                 0
                         0
                             0
                                  0
R24:
    0
                                  0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Set 2: LRU=0
    Entry
Set 3: LRU=1
    Entry
Entry
Data
   12 0
                20
                     0
                         -5
136:
            0
Cycle:14
Pre-Issue Buffer:
                R3, R2, #-5]
            [ ADDI
    Entry 0:
    Entry 1:
            [SW
                R1, 136(R0)]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
            [ADD
                R3, R4, R2]
    Entry 1:
Post_ALU Queue:
    Entry 0:
            [ADDI
                R1, R2, #-5]
```

```
t3_pipeline.txt
                                     Page 11 of 15
Pre_MEM Queue:
    Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
       12
           20
               -5
                       0
                           0
                               0
   0
R08:
    0
       0
               0
                   0
                       0
                           0
                               0
           0
R16:
    0
       0
           0
               0
                               0
                   0
                       0
                           0
R24:
   0
       0
           0
                       0
                               0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Dat.a
   12
       0
           Ω
               2.0
                   Ω
                       - 5
136:
Cvcle:15
Pre-Issue Buffer:
   Entry 0:
           [ADDI
               R3, R2, #-5]
    Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
           [ADD
               R3, R4, R2]
Pre_MEM Queue:
   Entry 0:
           [SW
               R1, 136(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
                   7
   0
       15
           2.0
               -5
                       0
                           0
                               0
R00:
R08:
    0
       Ω
           0
               Ω
                   0
                       0
                           Ω
                               0
R16:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
    0
       Ω
           0
               Ω
                   0
                       Ω
                           Ω
                               0
Cache
Set 0: LRU=0
```

```
t3_pipeline.txt
                       Page 12 of 15
  Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
136:
  12
    0
       0
          20
            0
               -5
Cycle:16
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
       [ADDI R3, R2, #-5]
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     15
       20
          27
               0
                 Ω
                    0
R08:
  0
     0
       0
          0
            0
               0
                 0
                    0
R16:
  0
     0
       0
          0
            0
               0
                 0
                    0
R24:
     0
                    0
  0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=0
  Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
```

```
t3_pipeline.txt
                               Page 13 of 15
20
                   -5
136:
Cycle:17
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
         [ADDI R3, R2, #-5]
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00: 0
      15
         20
            27
R08:
   0
      0
R16:
   0
      0
          0
                0
R24:
   0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
  12 0
         0 20 0
                    -5
136:
Cvcle:18
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
  Entry 0:
   Entry 1:
Post_ALU Queue:
```

```
t3_pipeline.txt
                                     Page 14 of 15
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
        15
            20
                15
                        0
                            0
                                0
R08:
    0
        0
            0
                    0
                                0
                0
                        0
                            0
R16:
    0
        0
            0
                0
                                0
                    0
                        0
                            0
R24:
    0
                                0
        0
            0
                0
                        0
                            0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
   12
       0
                2.0
                    0
                        -5
136:
            0
Cycle:19
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
        15
            20
                                0
R00:
    0
                15
                        0
                            Ω
R08:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R16:
    0
        Ω
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
        0
                            0
Cache
Set 0: LRU=0
```

Page 15 of 15 t3_pipeline.txt Entry Set 1: LRU=0 Entry Entry Set 2: LRU=0 Entry Entry Set 3: LRU=1 Entry Entry Data 136: 15 0 0 20 0 -5

t4_dis.txt Page 1 of 1 1 00011 00000 00001 00000 00010 010000 96 LW R1, 144(R0) 1 00011 00000 00010 00000 00010 010100 100 LW R2, 148(R0) 1 00000 00011 00001 00011 00000 100000 104 ADD R3, R3, R1 1 00000 00011 00010 00011 00000 100000 ADD R3, R3, R2 1 01000 00010 00010 11111 11111 111111 112 ADDI R2, R2, #-1 1 00001 00010 00000 00000 00000 000001 116 BLTZ R2, #4 1 00010 00000 00000 00000 00000 011010 120 J #104 R1, R1, #-1 R1, #4 1 01000 00001 00001 11111 11111 111111 ADDI 124 1 00001 00001 00000 00000 00000 000001 BLTZ 128 1 00010 00000 00000 00000 00000 011001 #100 132 J 1 01011 00000 00011 00000 00010 010000 SW R3, 144(R0) 136 1 00000 00000 00000 00000 00000 001101 140 BREAK 144 1 148

```
t4_pipeline.txt
                                      Page 1 of 37
Cycle:1
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
       Ω
           0
                0
                    0
                        0
                            0
                                0
R08:
    0
       0
            0
                0
                    0
                        0
                            0
                                0
R16:
    0
       0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
       0
            0
                0
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
Entry
Data
144:
   1
       1
Cycle:2
Pre-Issue Buffer:
   Entry 0:
               R1, 144(R0)]
            [ LW
   Entry 1:
Entry 2:
           [LW
               R2, 148(R0)]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
```

```
Page 2 of 37
t4_pipeline.txt
Post_MEM Queue:
   Entry 0:
Registers
       0
                            0
R00:
   0
                  0
                     0
                         0
R08:
   0
       0
                  0
                         0
                            0
R16:
   0
       0
          0
              0
                  0
                     0
                         0
                            0
R24:
                            0
   0
       0
          0
                     0
                         0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Dat.a
   1
144:
      1
Cycle:3
Pre-Issue Buffer:
   Entry 0:
Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
              R1, 144(R0)]
   Entry 0:
          [LW
   Entry 1:
          [LW
              R2, 148(R0)]
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       0
          0
              0
                  0
                     0
                         0
                            0
R08:
   Ω
       Ω
          0
              Ω
                  0
                     Ω
                         Ω
                            0
R16:
   Ω
          Ω
              Ω
                     Ω
                         Ω
                            Ω
       Ω
                  0
                            0
R24:
   0
       0
          0
              0
                  0
                     0
                         0
Cache
Set 0: LRU=1
   Entry
Set 1: LRU=0
```

```
t4_pipeline.txt
                         Page 3 of 37
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
144:
  1
     1
Cycle:4
Pre-Issue Buffer:
        [ADD
          R3, R3, R1]
  Entry 0:
  Entry 1:
        [ADD R3, R3, R2]
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
          R1, 144(R0)]
        [LW
  Entry 1:
          R2, 148(R0)]
        [LW
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     Ω
        0
          Ω
             Ω
                0
                   Ω
                     0
R08:
  0
     Ω
        0
          0
             0
                0
                   Ω
                     0
R16:
  0
     0
        0
          0
             0
                0
                   0
                     0
R24:
  0
     0
        0
          0
             0
                0
                   Ω
                     0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Data
```

```
t4_pipeline.txt
                                       Page 4 of 37
144: 1 1
Cycle:5
Pre-Issue Buffer:
           [ADD R3, R3, R1]
    Entry 0:
    Entry 1:
            [ADD
                R3, R3, R2]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                R2, 148(R0)]
            [LW
    Entry 1:
Post_MEM Queue:
    Entry 0:
            [LW
                R1, 144(R0)]
Registers
R00:
       0
            0
                0
                    0
                        0
                            0
                                 0
R08:
    0
       0
            0
                0
                    0
                        0
                            0
                                 0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                 0
R24:
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
   1
       1
144:
Cycle:6
Pre-Issue Buffer:
                R3, R3, R2]
    Entry 0:
Entry 1:
            [ ADD
               R2, R2, #-1]
            [ADDI
    Entry 2:
    Entry 3:
Pre_ALU Queue:
           [ADD R3, R3, R1]
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
```

```
t4_pipeline.txt
                                       Page 5 of 37
    Entry 1:
Post_MEM Queue:
   Entry 0:
            [LW
                R2, 148(R0)]
Registers
R00:
    0
                     0
R08:
    0
        0
            0
                     0
                         0
                             0
                                 0
R16:
            0
                                 0
    0
        0
                0
                     0
                         0
                             0
R24:
    0
                                 0
Cache
Set 0: LRU=1
    Entry
0: [\,(1\,,0\,,3\,)\,<\,\bar{100011000000001000000010010000}\,,\,100011000000001001000000010010100>\,]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
    1
144:
      1
Cycle:7
Pre-Issue Buffer:
    Entry 0:
            [ ADD
                R3, R3, R2]
    Entry 1:
            [ADDI
                R2, R2, #-1]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
            [ADD
                R3, R3, R1]
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        1
            1
                Ω
                     Ω
                         Ω
                             Ω
                                 Ω
R08:
    Ω
        Ω
            Ω
                                 Ω
                Ω
                     0
                         Ω
                             Ω
R16:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R24:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
Cache
Set 0: LRU=1
    Entry
```

```
Page 6 of 37
t4_pipeline.txt
Set 1: LRU=1
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
144:
  1
     1
Cycle:8
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
       [ADD
          R3, R3, R2]
  Entry 1:
       [ADDI R2, R2, #-1]
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  Ω
     1
       1
          1
             Ω
               Ω
                  Ω
                     Ω
R08:
  0
     0
       0
          0
             0
               0
                  0
                     0
R16:
  0
     Ω
       0
          0
             0
               0
                  Ω
                     0
R24:
  0
     0
       0
          0
             0
               0
                  0
                     0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
```

```
t4_pipeline.txt
                                          Page 7 of 37
Data
144:
    1
       1
Cycle:9
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
             [ADDI R2, R2, #-1]
    Entry 1:
Post_ALU Queue:
             [ADD R3, R3, R2]
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         1
R08:
    0
         0
             0
                      0
                           0
                               0
                                    0
R16:
R24:
    0
         0
                                    0
Cache
Set 0: LRU=1
    Entry
0: [\,(1\,,0\,,3\,)\,<\bar{100011000000001000000010010000}\,,100011000000001001000000010010100>\,]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
   1 1
144:
Cvcle:10
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
             [ADDI R2, R2, #-1]
Pre_MEM Queue:
```

```
Page 8 of 37
t4_pipeline.txt
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       1
                     0
                             0
R08:
       0
              0
                             0
   0
          0
                 0
                     0
                         0
R16:
   0
          0
              0
                     0
                         0
                             0
       0
                  0
R24:
   0
       0
          0
                             0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
   1 1
144:
Cycle:11
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
       1
          Ω
              2
                  Ω
                     Ω
                         Ω
                             Ω
   Ω
R08:
       0
              0
   0
          0
                  0
                     0
                         0
                             0
R16:
   0
       Ω
          0
              0
                  0
                     0
                         Ω
                             0
R24:
   0
       0
          0
              0
                  0
                     0
                         0
                             0
Cache
Set 0: LRU=1
   Entry
```

```
Page 9 of 37
t4_pipeline.txt
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
144:
  1
     1
Cycle:12
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     1
        0
           2
              0
                 0
                   0
                      0
R08:
  0
     Ω
        0
           0
              0
                 0
                   0
                      0
R16:
  0
     0
        0
           0
              0
                 0
                   0
                      0
R24:
  0
     0
        0
                 0
                   0
                      0
Cache
Set 0: LRU=1
  Entry
0: [\,(1\,,0\,,3\,)\,<\,1000110000000010000000100100000\,,\,10001100000001001000000010010000\,]
  Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
```

```
t4_pipeline.txt
                                   Page 10 of 37
Data
144:
   1
      1
Cycle:13
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       1
          0
              2
                  0
                      0
                          0
                              0
R08:
   0
      0
                          0
R16:
   0
       0
           0
                      0
                          0
                              0
R24:
   0
                              0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Set 2: LRU=0
   Entry
Set 3: LRU=1
   Entry
Entry
Data
   1 1
144:
Cycle:14
Pre-Issue Buffer:
           [ ADD
              R3, R3, R1]
   Entry 0:
   Entry 1:
           [ADD
              R3, R3, R2]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
```

```
t4_pipeline.txt
                                          Page 11 of 37
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
         1
             0
                  2
                      0
                           0
                               0
                                    0
    0
R08:
    0
         0
             0
                  0
                           0
                                    0
                      0
                               0
R16:
    0
             0
         0
                  Ω
                      0
                           0
                               0
                                    0
    0
             0
                                    0
R24:
         0
                  0
                      0
                           0
                               0
Cache
Set 0: LRU=1
    Entry
0: [\,(1\,,0\,,3\,)\,<\,\hat{100011000000000100100000010010000}\,,\,1000110000000010000000010010100>\,]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
    1
144:
        1
Cycle:15
Pre-Issue Buffer:
    Entry 0:
             [ADD
                  R3, R3, R2]
    Entry 1:
             [ADDI R2, R2, #-1]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
             [ADD
                  R3, R3, R1]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
    0
         1
             0
                  2.
                      0
                           0
                               0
                                    0
R00:
R08:
    0
         Ω
             0
                  0
                      0
                           0
                               Ω
                                    0
R16:
    0
         0
             0
                  0
                      0
                           0
                               0
                                    0
R24:
    0
         Ω
             0
                  Ω
                      0
                           0
                               Ω
                                    0
Cache
Set 0: LRU=1
```

```
t4_pipeline.txt
                                 Page 12 of 37
Set 1: LRU=1
   Entry
0: [(1,0,3)<100000001100001000110000100000,1000000011000100001100000100000]
   Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
144:
   1
Cycle:16
Pre-Issue Buffer:
          [ADD R3, R3, R2]
[ADDI R2, R2, #-1]
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
              R3, R3, R1]
          [ ADD
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       1
          Ω
                 0
                     0
                        Ω
                            0
R08:
   0
       0
          0
              0
                 0
                     0
                        0
                            0
R16:
   0
       0
          0
              0
                 0
                     0
                        0
                            0
R24:
                            0
       0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
0 \colon [\: (1,0,3) < \bar{1000000001100001100001100000100000}\:, 100000000110001000011000001000000>\:]
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
```

```
Page 13 of 37
t4_pipeline.txt
144:
Cycle:17
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
Entry 3:
Pre_ALU Queue:
   Entry 0:
         [ADD R3, R3, R2]
          [ADDI R2, R2, #-1]
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
     0
0
R00: 0
R08:
   0
                            0
         0
R16:
   0
                 0
                     0
                        0
                            0
R24:
   0
                            0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
  1
144:
      1
Cvcle:18
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
          [ADDI R2, R2, #-1]
   Entry 1:
Post_ALU Queue:
```

```
t4_pipeline.txt
                                      Page 14 of 37
    Entry 0:
            [ADD
                R3, R3, R2]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
        1
            0
                3
                    0
                        0
                            0
                                 0
    0
R08:
    0
        0
                0
                                 0
            0
                    0
                        0
                            0
R16:
    0
                                 0
        0
            0
                0
                    0
                        0
                             0
R24:
    0
                                 0
        0
            0
                0
                    0
                        0
                             0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
    1
144:
        1
Cycle:19
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
            [ADDI
               R2, R2, #-1]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
                                 0
R00:
    0
        1
            Ω
                3
                    Ω
                        0
                            Ω
R08:
    0
        0
            0
                0
                    0
                        0
                             0
                                 0
R16:
    0
        Ω
            0
                0
                    0
                        0
                             0
                                 0
R24:
    0
        0
                             0
Cache
Set 0: LRU=1
```

```
Page 15 of 37
t4_pipeline.txt
0: [\,(1\,,0\,,3\,)<1000110000000010000000100100000\,,10001100000001001000000100100100>\,]
  Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
1
    1
144:
Cycle:20
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre ALU Oueue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     1
        -1
           3
             0
                0
                   0
                      0
R08:
  0
     0
        0
           0
             0
                0
                   0
                      0
                      0
R16:
  0
     0
                   0
R24:
  0
     0
        0
                0
                   0
                      0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
```

```
t4_pipeline.txt
                                Page 16 of 37
   Entry
144:
  1
     1
Cycle:21
Pre-Issue Buffer:
   Entry 0:
          [ADDI R1, R1, #-1]
   Entry 1:
Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
   0
      1
          -1
R08:
   0
      0
                 0
                    0
                        0
                           0
R16:
   0
      0
          0
                 0
                    0
                        0
                           0
R24:
   0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
Entry
Set 3: LRU=1
   Entry
Entry
Data
144:
   1
      1
Cvcle:22
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
          [ADDI R1, R1, #-1]
   Entry 1:
```

```
t4_pipeline.txt
                                      Page 17 of 37
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
        1
            -1
                    0
                         0
                             0
                                 0
    0
R08:
            0
                0
    0
        0
                    0
                         0
                             0
                                 0
R16:
            0
                0
                                 0
    0
        0
                    0
                         0
                             0
R24:
    0
        0
            0
                         0
                             0
                                 0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
144:
    1
       1
Cycle:23
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
            [ADDI R1, R1, #-1]
Pre_MEM Queue:
    Entry 0:
Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        1
            -1
                3
                    0
                        0
                             0
                                 0
R08:
    0
        Ω
            Ω
                0
                    0
                         0
                             Ω
                                 0
R16:
    0
        0
            0
                0
                    0
                         0
                             0
                                 0
R24:
    0
        0
            0
                0
                    0
                         0
                             0
                                 0
Cache
Set 0: LRU=0
```

```
t4_pipeline.txt
                      Page 18 of 37
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
  1
144:
Cycle:24
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
    0
       -1
         3
            0
              0
                0
                   0
R08:
    0
  0
R16:
  0
    0
       0
         0
              0
                 0
                   0
R24:
  0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
```

```
Page 19 of 37
t4_pipeline.txt
Data
144:
  1
Cycle:25
Pre-Issue Buffer:
   Entry 0:
Entry 1:
   Entry 2:
Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      0
         -1
                0
                       0
                          0
R08:
   0
      0
         0
                0
                   0
                       0
                          0
R16:
   0
      0
         0
                0
                   0
                       0
                          0
R24:
   0
                   0
                          0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Dat.a
144:
  1
     1
Cycle:26
Pre-Issue Buffer:
   Entry 0:
          [LW
             R2, 148(R0)]
   Entry 1:
         [ADD
            R3, R3, R1]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
```

```
t4_pipeline.txt
                                             Page 20 of 37
     Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
     Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
         0
                                  0
R00:
              -1
                   3
                        0
                             0
                                       0
    0
R08:
              0
     0
                   0
                                       0
         0
                        0
                             0
                                  0
R16:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
    0
                                       Ω
R24:
         0
Cache
Set 0: LRU=1
    Entry
0: [\,(1\,,0\,,3\,)\,<\,1000110000000010000000100100000\,,\,10001100000001001000000010010000]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
144:
    1
        1
Cycle:27
Pre-Issue Buffer:
    Entry 0:
              [ADD
                   R3, R3, R2]
     Entry 1:
              [ADDI
                   R2, R2, #-1]
     Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
              [ADD
                   R3, R3, R1]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                   R2, 148(R0)]
              [LW
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
     0
         Ω
              -1
                   3
                        0
                             0
                                  Ω
                                       0
R08:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R16:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R24:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
Cache
```

```
Page 21 of 37
t4_pipeline.txt
Set 0: LRU=1
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
1
     1
144:
Cycle:28
Pre-Issue Buffer:
         [ADD
            R3, R3, R2]
   Entry 0:
   Entry 1:
         [ADDI R2, R2, #-1]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
         [ ADD
            R3, R3, R11
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
         [LW
            R2, 148(R0)]
Registers
R00:
      0
         -1
                0
                      0
R08:
   0
      0
         0
            0
                0
                   0
                      0
                         0
R16:
      0
         0
            0
                   0
                      0
                         0
   0
         0
            0
                         0
R24:
   0
      0
                0
                   0
                      0
Cache
Set 0: LRU=1
   Entry
0: [\ (1,0,3) < \bar{10001100000000100100000010010000}, 10001100000000100100000010010100>]
   Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
```

```
t4_pipeline.txt
                                   Page 22 of 37
   Entry
Entry
144:
   1
Cycle:29
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
           [ADD R3, R3, R2]
[ADDI R2, R2, #-1]
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       0
                              0
R08:
   0
       0
                  0
                              0
R16:
   0
           0
               0
                      0
                          0
                              0
       0
                   0
R24:
   0
       0
                              0
Cache
Set 0: LRU=1
   Entry
0: [\,(1,0,3)<\hat{100011000000001000000010010000},1000110000000100100000010010100>\,]
   Entry
Set 1: LRU=1
   Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
   1 1
144:
Cycle:30
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
```

```
t4_pipeline.txt
                                       Page 23 of 37
    Entry 0:
            [ADDI
                R2, R2, #-1]
    Entry 1:
Post_ALU Queue:
    Entry 0:
            [ADD
                R3, R3, R2]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        0
                                 0
R00:
                3
                    0
                         0
                             0
   0
R08:
    0
        0
            0
                Ω
                    0
                         0
                             0
                                 0
R16:
    Ω
            Ω
                Ω
                                 Ω
        Ω
                    Ω
                         Ω
                             Ω
R24:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
Cache
Set 0: LRU=1
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
144:
   1
       1
Cycle:31
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
            [ADDI R2, R2, #-1]
    Entry 0:
Pre MEM Oueue:
    Entry 0:
Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        0
R00:
    0
            1
                4
                     0
                         0
                             0
                                 0
R08:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R16:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R24:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
```

```
Page 24 of 37
t4_pipeline.txt
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
144:
  1
Cycle:32
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
     0
        0
              0
                 0
                    0
                       0
R08:
  0
     0
                       0
                    0
                       0
R16:
  0
     0
        0
                 0
                    0
R24:
  0
Cache
Set 0: LRU=1
  Entry
0: [\,(1\,,0\,,3\,)\,<\,1000110000000010000000100100000\,,\,10001100000001001000000010010000\,]
  Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
```

```
t4_pipeline.txt
                              Page 25 of 37
Set 3: LRU=1
Data
  1
     1
144:
Cvcle:33
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
      0
R00:
  0
                         0
R08:
   0
      0
            0
                         0
         0
                0
                   0
                      0
        0
R16:
   0
      0
            0
               0
                   0
                      0
                         0
R24:
   0
      0
         0
            0
                0
                   0
                      0
                         0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
   1
144:
     1
Cycle:34
Pre-Issue Buffer:
   Entry 0:
         [ADD
            R3, R3, R1]
   Entry 1:
         [ADD R3, R3, R2]
   Entry 2:
   Entry 3:
```

```
t4_pipeline.txt
                                             Page 26 of 37
Pre_ALU Queue:
     Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         0
              0
                   4
                        0
                             0
                                  0
                                       0
R08:
     Ω
                                       Ω
         Ω
              Ω
                   Ω
                        Ω
                             Ω
                                  Ω
R16:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R24:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
Cache
Set 0: LRU=1
    Entry
0: [\,(1\,,0\,,3\,)\,<\,1000110000000010000000100100000\,,\,10001100000001001000000010010000\,]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
144:
    1
Cycle:35
Pre-Issue Buffer:
    Entry 0:
              [ADD
                   R3, R3, R2]
     Entry 1:
              [ADDI
                  R2, R2, #-1]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
              [ADD
                   R3, R3, R1]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         0
              0
                        0
                             0
                                  0
                                       0
R08:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R16:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R24:
     0
         0
              0
                                  0
                                       0
```

t4_pipeline.txt Page 27 of 37 Cache Set 0: LRU=1 Entry Entry Set 1: LRU=1 Entry Entry Set 2: LRU=0 Entry Entry Set 3: LRU=1 Entry Entry 144: 1 Cycle:36 Pre-Issue Buffer: R3, R3, R2] [ADD Entry 0: [ADDI R2, R2, #-1] Entry 1: Entry 2: Entry 3: Pre_ALU Queue: Entry 0: Entry 1: Post_ALU Queue: Entry 0: [ADD R3, R3, R1] Pre_MEM Queue: Entry 0: Entry 1: Post_MEM Queue: Entry 0: Registers R00: 0 0 0 0 0 0 R08: 0 0 0 0 0 0 0 R16: 0 0 0 0 0 0 0 R24: 0 0 0 0 0 0 0 Cache Set 0: LRU=1 Entry $0: [\ (1\,,0\,,3\,)\,<\,\bar{10000110000000001001000000010010000}\,,\,1000110000000010000000010010100>\,]$ Set 1: LRU=1 Entry Entry Set 2: LRU=0 Entry

```
Page 28 of 37
t4_pipeline.txt
Set 3: LRU=1
   Entry
Entry
Data
  1
144:
Cvcle:37
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
         [ ADD
            R3, R3, R2]
           R2, R2, #-1]
   Entry 1:
         [ADDI
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
      0
         0
            4
               0
                  0
                     0
                         0
R08:
   0
      0
         0
            0
               0
                  0
                     0
                         0
R16:
   0
      0
         0
            0
               0
                  Ω
                     0
                         0
R24:
   Ω
            Ω
                         Ω
      Ω
               0
                     Ω
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Dat.a
144:
   1
     1
Cycle:38
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
```

```
t4_pipeline.txt
                                             Page 29 of 37
    Entry 3:
Pre_ALU Queue:
    Entry 0:
              [ADDI
                  R2, R2, #-1]
    Entry 1:
Post_ALU Queue:
                   R3, R3, R2]
    Entry 0:
              [ADD
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
         Ω
ROO:
              Ω
                        Ω
                             Ω
                                  Ω
                                       Ω
    0
R08:
    0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R16:
    0
         Ω
              0
                   0
                        0
                             0
                                  0
                                       0
R24:
    0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
0 \colon [\: (1,0,3) < \bar{1000000001100001100001100000100000}\:, 100000000110001000011000001000000>\:]
    Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
144:
    1
        1
Cycle:39
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
              [ADDI R2, R2, #-1]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         Ω
              0
                   4
                        0
                             0
                                  0
                                       0
R08:
    0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R16:
    0
         0
```

```
t4_pipeline.txt
                       Page 30 of 37
 0 0
R24:
      0
         Ο
            0
              0
                 Ω
                    Ω
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
144:
  1
Cvcle:40
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
     0
                 0
                    0
  0
       -1
            0
R08:
  0
     0
                 0
                    0
R16:
  0
     0
       0
          0
            0
               0
                 0
                    0
R24:
  0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
```

```
t4_pipeline.txt
                           Page 31 of 37
Set 3: LRU=1
  Entry
Entry
Data
  1
144:
     1
Cycle:41
Pre-Issue Buffer:
        [ADDI R1, R1, #-1]
   Entry 0:
   Entry 1:
   Entry 2:
  Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     0
        -1
              0
                 0
                    0
                        0
R08:
         0
   0
     0
           Ω
               0
                  0
                     0
                        0
R16:
         Ω
            Ω
                        Ω
   0
     Ω
               0
                  Ω
                     Ω
R24:
   0
                        0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
144:
  1
     1
Cvcle:42
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
```

```
t4_pipeline.txt
                                     Page 32 of 37
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
           [ADDI R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
       0
                       0
                           0
                               0
R00:
   0
           -1
                   0
R08:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
R16:
    0
       0
            0
               0
                   0
                       0
                           0
                               0
R24:
    0
       0
                               0
Cache
Set 0: LRU=0
    Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
144:
   1
Cycle:43
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
   Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
           [ADDI R1, R1, #-1]
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       0
            -1
                    0
R08:
    0
```

```
t4_pipeline.txt
                         Page 33 of 37
R16:
  0
     0
                   0
                      Ω
R24:
  0
     0
                      0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Data
144:
  1
    1
Cycle:44
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     -1
        -1
R08:
  0
     0
        0
          0
             0
                0
                   0
                      0
R16:
     0
        0
                      0
  0
                0
                   0
R24:
  0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
```

```
Page 34 of 37
t4_pipeline.txt
Entry
Set 3: LRU=1
  Entry
Entry
Dat.a
  1
     1
144:
Cycle:45
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
              0
                 0
                    0
                       0
R00:
  0
     -1
        -1
     Ω
R08:
  Ω
        Ω
                       Ω
           Ω
              Ω
                 Ω
                    Ω
        0
R16:
  0
     0
           0
              0
                 0
                    0
                       0
R24:
  0
     0
        0
           0
              0
                 0
                    0
                       0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
144:
  1
     1
Cycle:46
Pre-Issue Buffer:
        [SW
           R3, 144(R0)]
  Entry 0:
```

```
t4_pipeline.txt
                                         Page 35 of 37
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        -1
             -1
                 4
                      0
                          0
                               Ω
                                   0
R08:
    0
        0
             0
                 0
                      0
                          0
                               0
                                   0
R16:
    0
        0
             0
                 Ω
                      0
                          0
                               0
                                   0
R24:
    0
        Ω
             Ω
                      Ω
                          Ω
                               Ω
                                   Ω
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
0:[(1,0,3)<100000001100001000110000100000,1000000011000100001100000100000>]
    Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
144:
    1
Cycle:47
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
             [SW
    Entry 0:
                 R3, 144(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00: 0
        -1
             -1
                      0
                          0
                               0
                                   0
```

```
t4_pipeline.txt
                           Page 36 of 37
R08:
   0
     0
        0
           0
              0
                 0
                    0
                       0
R16:
   0
     0
        0
           0
              0
                 0
                    0
                       0
R24:
   0
     0
        0
              0
                 0
                    0
                       0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
  1
144:
Cycle:48
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
   Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
   Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
      -1
        -1
              0
                 0
                    0
                       0
R08:
   0
     0
                       0
              0
                 0
                    0
R16:
   0
     0
        0
              0
                 0
                    0
                       0
R24:
   0
                       0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
```

```
t4_pipeline.txt
             Page 37 of 37
Set 3: LRU=1
 Entry
Entry
Data
144:
 4
  1
```

sample_bin.txt Page 1 of 1

```
Page 1 of 1
sample_dis.txt
0 01000 00000 00001 00000 00000 001010
                                Invalid Instruction
 01000 00000 00001 00000 00000 001010
                           100
                                ADDI
                                      R1, R0, #10
 01011 00000 00001 00000 00100 001100
                           104
                                SW
                                      R1, 268(R0)
0 00010 10000 00000 00000 00000 000000
                                Invalid Instruction
 00011 00000 00001 00000 00100 001100
                           112
                                LW
                                      R1, 268(R0)
 00001 00001 00000 00000 00000 001100
                           116
                                BLTZ
                                      R1, #48
 00000 00000 00001 01010 00010 000000
                           120
                                SLL
                                      R10, R1,
                                      R3, 176(R10)
00011 01010 00011 00000 00010 110000
                                LW
                           124
 00011 01010 00100 00000 00011 011100
                                      R4, 220(R10)
                           128
                                LW
1 00011 00000 00101 00000 00100 001000
                                      R5, 264(R0)
                           132
                                LW
 00001 00011 00000 00000 00000 000010
                                BLTZ
                                      R3, #8
                           136
 00000 00100 00101 00110 00000 100010
                           140
                                SUB
                                      R6, R4, R5
 00010 00000 00000 00000 00000 100110
                           144
                                      #152
                                ıΤ
1 00000 00100 00101 00110 00000 100000
                                ADD
                                      R6, R4, R5
                           148
                                      R6, 176(R10)
1
 01011 01010 00110 00000 00010 110000
                           152
                                SW
1 01000 00001 00001 11111 11111 111111
                           156
                                ADDT
                                      R1, R1, #-1
1
 01011 00000 00001 00000 00100 001100
                           160
                                SW
                                      R1, 268(R0)
1 00010 00000 00000 00000 00000 011100
                           164
                                J
                                      #112
                                Invalid Instruction
0 \ 00000 \ 00000 \ 00000 \ 00000 \ 00000 \ 00000
                           168
1 00000 00000 00000 00000 00000 001101
                           172
                                BREAK
176
                                -1
180
                                 -2
184
                                -3
188
                                1
00000000000000000000000000000011
                           196
200
                                0
204
                                0
208
212
                                -5
0000000000000000000000000000000110
                           216
                                6
220
                                0
224
                                0
228
                                0
232
                                0
236
                                0
240
                                0
244
                                0
248
                                0
252
                                0
256
                                0
260
                                0
264
                                1
```

```
sample_mips.txt
                                                                                          Page 1 of 1
         ; Initially PC is set to 96 ; Data section is right after the code section
         .global _main
_main:
                  R1, R0, #10
R1, VAR_i(R0)
         ADDI
                                    ; init i
         SW
                                    ; store i
FOR_0:
                  R1, VAR_i(R0)
R1, END_FOR_0
         LW
         BLTZ
                                    ; i >= 0?
                                    ; get correct word boundary; read A[i]
                  R10, R1, #2
R3, A(R10)
R4, B(R10)
         SLL
         LW
         LW
                                     ; read B[i]
                  R5, C(R0)
         LW
                                     ; read C
                  R3, ELSE_0
R6, R4, R5
                                    ; A[i] >= 0 ?
; B[i] - C
         BLTZ
         SUB
                  TAIL_0
ELSE_0:
         ADD
                  R6, R4, R5
                                    ; B[i] + C
TAIL_0:
         SW
                  R6, A(R10)
                                    ; rewrite A[i]
                  R6, A(R10)
R1, R1, #-1
R1, VAR_i(R0)
                                    ; i--
         ADDI
         SW
         J
                  FOR_0
END_FOR_0:
         BREAK
Α:
         .word -1, -2, -3, 1, 2, 3, 0, 0, 5, -5, 6
в:
         .word 0, 0, 0, 0, 0, 0, 0, 0, 0, 0
; let C be 1
         .word 1
VAR_i:
; for var i
         .word 0
```

```
sample_pipeline.txt
                                     Page 1 of 157
Cycle:1
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
       0
            0
                0
                    0
                        0
                            0
                                0
R08:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                        0
                            0
                                0
R24:
    0
       0
            0
                0
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
Entry
Data
176:
    -1
        -2
            -3
                1
                            0
                                0
    5
208:
        -5
                0
                                0
   0
240:
Cycle:2
Pre-Issue Buffer:
            [ADDI R1, R0, #10]
   Entry 0:
    Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
```

```
Page 2 of 157
sample_pipeline.txt
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        0
                     0
                         0
                             0
                                 0
R08:
                                 0
    0
        0
            0
                0
                     0
                         0
                             0
R16:
    0
            0
                0
                         0
                             0
                                 0
        0
                     0
                                 0
R24:
    0
        0
            0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
            -3
                1
                     2
                         3
                             0
                                 0
    5
208:
        -5
            6
                Ω
                     Ω
                         Ω
                                 Ω
                             0
        0
240:
    0
            0
                0
                     0
                         0
                             1
                                 0
Cycle:3
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
            [ADDI
                R1, R0, #10]
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        0
                                 0
R00:
    0
            0
                0
                     0
                         0
                             0
R08:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R16:
    0
        Ω
            0
                0
                     0
                         0
                             Ω
                                 0
R24:
    0
        0
                         0
                             0
                                 0
Cache
Set 0: LRU=1
```

```
Page 3 of 157
sample_pipeline.txt
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
176:
  -1
     -2
        -3
          1
             2
                3
                  0
                     0
208:
  5
     -5
        6
          0
             0
                0
                  0
                     0
240:
  0
     0
                     0
Cycle:4
Pre-Issue Buffer:
        [SW
          R1, 268(R0)]
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
          R1, R0, #10]
  Entry 0:
        [ADDI
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
     0
                  0
R08:
  0
     0
        0
          0
                  0
                     0
R16:
     0
        0
                  0
                     0
  0
                     0
R24:
  0
     0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
  Entry
Set 3: LRU=0
```

```
Page 4 of 157
sample_pipeline.txt
   Entry
Entry
Data
176:
   -1
       -2
           -3
              1
                      3
                         0
                             0
208:
   5
       -5
           6
              0
                  0
                      0
                             0
                         0
                             0
240:
   0
       0
Cycle:5
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [SW
              R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
       10
           0
              0
                  0
                      0
                         0
                             0
   0
R08:
   0
       0
           0
              0
                  0
                      0
                         0
                             0
R16:
   0
       0
           0
              0
                  0
                      0
                         0
                             0
R24:
   Ω
              Ω
                             Ω
       0
           0
                  0
                      0
                         0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
       - 2
                  2
                         0
                             Ω
176:
   -1
           -3
              1
208:
   5
       -5
           6
              0
                  0
                      0
                         0
                             0
240:
   0
       Ω
           0
              Ω
                  0
                      Ω
                         1
                             0
Cycle:6
Pre-Issue Buffer:
   Entry 0:
           [LW
              R1, 268(R0)]
```

```
Page 5 of 157
sample_pipeline.txt
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
            [SW
                R1, 268(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        10
R00:
    0
            0
                0
                    0
                        0
                            Ω
                                0
R08:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
        Ω
            Ω
                    Ω
                            Ω
                                Ω
Cache
Set 0: LRU=1
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
176:
            -3
                            0
208:
    5
        -5
            6
                0
                    0
                        0
                            0
                                0
240:
    0
        0
Cycle:7
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
               R1, 268(R0)]
            [LW
    Entry 1:
Post_MEM Queue:
    Entry 0:
```

```
Page 6 of 157
sample_pipeline.txt
Registers
R00:
   0
       10
           0
              0
                  0
                      0
                         0
                             0
R08:
   0
       0
           0
              0
                  0
                      0
                         0
                             0
R16:
       0
           0
                         0
                             0
       0
                             0
R24:
   0
                      0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
       -2
           -3
              1
                  2
                      3
                         0
                             0
208:
   5
       -5
           6
              0
                  0
                      0
                         0
                             0
       0
   0
              0
                  0
                      0
                             0
240:
           0
Cycle:8
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
           [LW
              R1, 268(R0)]
Registers
R00:
       10
           0
              0
                  0
                      0
                         0
                             0
   0
R08:
   0
       0
           0
              0
                  0
                      0
                         0
                             0
R16:
   0
       0
           0
              Ω
                  0
                      Ω
                         0
                             0
R24:
   0
           Ω
              Ω
                  Ω
                             Ω
       0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
```

```
Page 7 of 157
sample_pipeline.txt
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Dat.a
     - 2
176:
  -1
        -3
          1
             2
                3
                  Ω
                     Ω
208:
  5
     -5
        6
          0
             0
                0
                  0
                     0
240:
  0
     0
        0
          0
             0
                0
                  1
                     0
Cycle:9
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  Ω
     10
        Ω
          Ω
             Ω
                Ω
                  Ω
                     Ω
R08:
  0
     0
        0
          0
             0
                0
                  0
                     0
R16:
  0
     Ω
        0
          0
             0
                0
                  0
                     0
R24:
  0
     0
                   0
                     0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
```

```
sample_pipeline.txt
                                      Page 8 of 157
Data
176:
    -1
        -2
            -3
                1
                         3
                             0
                                 0
208:
    5
        -5
            6
                0
                    0
                         0
                             0
                                 0
240:
    0
        0
Cycle:10
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00: 0
        10
                             0
                                 0
R08:
    0
        0
            0
                                 0
R16:
    0
        0
            0
                    0
                         0
                             0
                                 0
R24:
    0
        0
                                 0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
            -3
                1
                    2
                         3
                             0
                                 0
        -5
    5
208:
            6
                0
                    0
                         0
                             0
                                 0
        0
    Ω
                Ω
                    Ω
                                 Ω
240:
            Ω
                         Ω
Cycle:11
Pre-Issue Buffer:
    Entry 0:
            [SLL
                R10, R1, #2]
                R3, 176(R10)]
    Entry 1:
            [LW
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
```

```
sample_pipeline.txt
                                         Page 9 of 157
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        10
                 0
                          0
                              0
                                   0
R00:
             0
                      0
    0
R08:
    0
        0
                                   0
             0
                 0
                      0
                          0
                              0
R16:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
    Ω
                                   Ω
R24:
        0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
        - 2
                              0
176:
    -1
             -3
                 1
                      2
                          3
                                   Ω
208:
    5
        -5
             6
                 0
                      0
                          0
                              0
                                   0
240:
    0
        0
             0
                 0
                      0
                          0
                              1
                                   0
Cycle:12
Pre-Issue Buffer:
    Entry 0:
             [LW
                 R3, 176(R10)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
             [SLL
                 R10, R1, #2]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        10
             0
                 0
                      0
                          0
                              0
                                   0
R08:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
R16:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
R24:
    0
        0
             0
                               0
                                   0
```

```
sample_pipeline.txt
                                 Page 10 of 157
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
0: [\,(1\,,0\,,3\,)<10000000000000010101000010000000\,,100011010100001100000010110000>]
   Entry
176:
       -2
          -3
                         0
                             0
   -1
208:
   5
       -5
          6
              0
                  0
                     0
                         0
                             0
240:
   0
       0
                             0
Cycle:13
Pre-Issue Buffer:
              R3, 176(R10)]
          [LW
   Entry 0:
              R4, 220(R10)]
   Entry 1:
          [T.W
              R5, 264(R0)]
   Entry 2:
          [LW
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
          [SLL
              R10, R1, #2]
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       10
                             0
R08:
   0
       0
          0
              0
                  0
                     0
                         0
                             0
R16:
       0
          0
              0
                         0
                             0
   0
                  0
                     0
R24:
   0
                             0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
```

```
Page 11 of 157
sample_pipeline.txt
Entry
Set 3: LRU=1
   Entry
Entry
Dat.a
       -2
                           0
    -1
           -3
                   2
                       3
                               0
176:
               1
208:
   5
       -5
           6
               0
                   0
                       0
                           0
                               0
240:
   0
       0
           0
               0
                   0
                       0
                               0
                           1
Cycle:14
Pre-Issue Buffer:
   Entry 0:
           [LW
               R5, 264(R0)]
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
               R3, 176(R10)]
           [LW
   Entry 1:
           [LW
               R4, 220(R10)]
Post_MEM Queue:
   Entry 0:
Registers
           0
                       0
                           0
                               0
       10
               0
                   0
R00:
   0
R08:
           40
   0
       0
               0
                   0
                       0
                           0
                               0
R16:
   0
       0
           Ω
               Ω
                   0
                       Ω
                           0
                               0
R24:
   0
       0
           0
               0
                   0
                       0
                           0
                               0
Cache
Set 0: LRU=0
   Entry
1: [\,(1,0,4)<\overline{10}001101010001000000000011011100\,,100011000000010100000001000010000]
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
    -1
       -2
           -3
               1
                   2
                       3
                           0
                               0
208:
   5
       -5
           6
               0
                   0
                       0
                           0
                               0
240:
   0
       0
           0
               0
                   0
                       0
                               0
```

```
sample_pipeline.txt
                                      Page 12 of 157
Cycle:15
Pre-Issue Buffer:
            [LW
                R5, 264(R0)]
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                R3, 176(R10)]
            [T.W
                R4, 220(R10)]
    Entry 1:
            [LW
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        10
            0
                0
                     0
                         0
                             0
                                 0
R08:
    0
        0
            40
                0
                     0
                         0
                             0
                                 0
R16:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R24:
    0
        0
                                 0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Data
176:
            -3
208:
    5
        -5
            6
                0
                     0
                         0
                             0
                                 0
        0
                                 0
240:
    0
Cycle:16
Pre-Issue Buffer:
    Entry 0:
Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
            [LW
                R4, 220(R10)]
```

```
sample_pipeline.txt
                                      Page 13 of 157
    Entry 1:
            [LW
                R5, 264(R0)]
Post_MEM Queue:
   Entry 0:
            [LW
                R3, 176(R10)]
Registers
R00:
    0
        10
                    0
R08:
    0
        0
            40
                0
                    0
                         0
                             0
                                 0
R16:
        0
            0
                0
                                 0
    0
                    0
                         0
                             0
R24:
    0
            0
                    0
                         0
                                 0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
    -1
        -2
            -3
                    2
                         3
                             0
                                 0
                1
176:
208:
    5
        -5
            6
                    0
                         0
                0
                             0
                                 0
        Ω
    Ω
                         Ω
                                 Ω
240:
            0
                Ω
                    0
                             1
        ____
Cycle:17
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
                R4, 220(R10)]
R5, 264(R0)]
    Entry 0:
            [LW
    Entry 1:
            [LW
Post_MEM Queue:
    Entry 0:
Registers
        10
            0
                6
                    0
                         0
                             0
                                 0
R00:
    0
R08:
    0
        Ω
            40
                0
                    0
                         0
                             Ω
                                 0
R16:
    0
        0
            0
                0
                    0
                         0
                             0
                                 0
R24:
    0
        0
            0
                Ω
                    0
                         0
                             0
                                 0
Cache
Set 0: LRU=0
```

```
Page 14 of 157
sample_pipeline.txt
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
176:
   -1
     -2
        -3
           1
              2
                 3
                    0
                       0
208:
  5
     -5
        6
           0
              0
                 0
                    0
                       0
240:
  0
     0
        0
           0
              0
                 0
                       0
Cycle:18
Pre-Issue Buffer:
  Entry 0:
        [SUB
           R6, R4, R5]
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
        [LW
           R5, 264(R0)]
  Entry 1:
Post_MEM Queue:
  Entry 0:
        [LW
           R4, 220(R10)]
Registers
R00:
  0
     10
        0
           6
              0
                 0
                    0
                       0
R08:
     0
        40
                       0
  0
R16:
  0
     0
        0
           0
              0
                 0
                    0
                       0
R24:
  0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=1
  Entry
Set 3: LRU=0
```

```
Page 15 of 157
sample_pipeline.txt
Entry
Data
176:
           -3
208:
   5
       -5
           6
                  0
                         0
                             0
       0
240:
   0
           0
                  0
                             0
                         1
Cvcle:19
Pre-Issue Buffer:
           SUB
              R6, R4, R5]
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
           [LW
              R5, 264(R0)]
Registers
                  0
R00:
   0
       10
              6
                      0
                             0
R08:
   0
       0
           40
              0
                  0
                     0
                             0
                         0
R16:
   0
       0
           0
              0
                  0
                     0
                         0
                             0
                             0
R24:
   0
       0
           0
              0
                  0
                      0
                         0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
       - 2
           -3
              1
                  2
                     3
                         0
                             0
   5
208:
       -5
           6
              0
                  0
                     0
                         0
                             Ω
240:
   0
       0
           0
              0
                  0
                     0
                         1
                             0
Cvcle:20
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
```

```
Page 16 of 157
sample_pipeline.txt
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
              [SUB
                   R6, R4, R5]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
         10
              0
                                  0
                                       0
R00:
    0
                        0
R08:
    0
         0
              40
                   0
                        0
                             0
                                  0
                                       0
R16:
    0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R24:
    0
         0
              0
                                       0
Cache
Set 0: LRU=1
    Entry
1: [\,(1,0,4)<\overline{10}001101010001000000000011011100\,,100011000000010100000001000010000]
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
         -2
              -3
                   1
                        2
                             3
                                  0
                                       0
208:
    5
         -5
              6
                        0
                                       0
240:
    0
         0
              0
                        0
                             0
                                       0
Cycle:21
Pre-Issue Buffer:
              [SW
                   R6, 176(R10)]
    Entry 0:
                   R1, R1, #-1]
    Entry 1:
              [ADDI
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
Entry 1:
Post_ALU Queue:
                   R6, R4, R5]
    Entry 0:
              [SUB
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
```

```
sample_pipeline.txt
                                    Page 17 of 157
R00:
    0
       10
           0
                   0
                           0
                               0
R08:
    0
       0
           40
               0
                   0
                       0
                           0
                               0
R16:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
        0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
                           0
176:
    -1
            -3
                               0
208:
    5
        -5
           6
               0
                   0
                       0
                               0
                           0
240:
    0
       0
           0
               0
                               0
Cvcle:22
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
   Entry 3:
Pre_ALU Queue:
    Entry 0:
           [ADDI
               R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [SW
               R6, 176(R10)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
       10
    0
           0
               6
                   0
                       1
                           -1
                               0
R08:
    0
       0
           40
               0
                       0
                           0
                               0
                   0
R16:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
    0
       0
           Ω
                   Ω
                               Ω
Cache
Set 0: LRU=1
    Entry
Entry
1: [\,(1,0,4)<\overline{10}001101010001000000000011011100\,,100011000000010100000001000010000]
Set 1: LRU=0
```

```
Page 18 of 157
sample_pipeline.txt
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
        -3
           1
              2
                 3
                    0
                       0
176:
   -1
     - 2
   5
208:
     -5
        6
           0
              0
                 0
                    0
                       0
240:
   0
     0
        0
              0
                       0
Cycle:23
Pre-Issue Buffer:
        [SW
           R1, 268(R0)]
   Entry 0:
   Entry 1:
   Entry 2:
  Entry 3:
Pre_ALU Queue:
   Entry 0:
  Entry 1:
Post_ALU Queue:
        [ADDI
           R1, R1, #-1]
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     10
        Ω
           6
              0
                    -1
                       0
R08:
   0
     Ω
        40
           0
              0
                 Ω
                    Ω
                       0
R16:
   0
     0
        0
           0
              0
                 0
                    0
                       0
R24:
   0
     0
        0
           Ω
              0
                 0
                    Ω
                       0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=0
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
```

```
sample_pipeline.txt
                                       Page 19 of 157
176:
    -1
        -2
            -3
                     2
                             0
                                  0
208:
    5
        -5
            6
                 0
                     0
                         0
                             0
                                  0
240:
    0
        0
            0
                 0
                     0
                         0
                                  0
Cycle:24
Pre-Issue Buffer:
    Entry 0:
            [LW
                 R1, 268(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
            [SW
                 R1, 268(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        9
            0
                 6
                     0
                         1
                              -1
                                  0
R08:
    0
        0
            40
                 0
                         0
                             0
                                  0
                     0
R16:
    0
        0
            0
                 0
                     0
                         0
                             0
                                  0
R24:
    0
            0
                                  0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
            -3
                             0
                                  0
                 1
                     2
                         3
208:
    5
        -5
            6
                 0
                     0
                         0
                             0
                                  0
        0
240:
    0
            0
                 0
                     0
                         0
                             1
                                  0
Cvcle:25
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
```

```
Page 20 of 157
sample_pipeline.txt
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [LW
                 R1, 268(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
        9
             0
                      0
                                   0
    0
                 6
                          1
                               -1
R08:
        0
             40
                          0
                               0
    0
                 0
                      0
                                   0
R16:
                 0
                               0
                                   0
    0
        0
             0
                      0
                          0
R24:
    0
        0
             0
                 0
                      0
                          0
                               0
                                   0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
             -3
                 1
                      2
                          3
                               Ω
                                   Ω
    5
208:
        -5
             6
                 Ω
                      Ω
                          Ω
                               0
                                   0
240:
    0
        0
             0
                 0
                      0
                          0
                               1
                                   0
Cycle:26
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre MEM Oueue:
    Entry 0:
Entry 1:
Post_MEM Queue:
                 R1, 268(R0)]
    Entry 0:
             [LW
Registers
        9
R00:
    0
             Ω
                 6
                      Ω
                          1
                               -1
                                   0
R08:
    0
        0
             40
                 0
                      0
                          0
                               0
                                   0
R16:
    0
        0
             0
                 0
                      0
                          0
                               0
                                   0
R24:
    0
        0
             0
                 0
                      0
                          0
                               0
                                   0
```

```
Page 21 of 157
sample_pipeline.txt
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
176:
  -1
     -2
        -3
             2
                  Ω
                     0
208:
  5
     -5
240:
  0
     0
             0
                     0
Cvcle:27
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
     9
                     0
R00:
  0
                   -1
R08:
  0
     0
        40
                     0
R16:
  0
     0
        0
          0
             0
                0
                  0
                     0
R24:
  0
        0
                     0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
```

```
Page 22 of 157
sample_pipeline.txt
1: [\ (1\,,0\,,4\,)\,<\,\bar{10}001000000000000000000000000100110\,,\,100000001000010100110000001000000\,>\,]
Set 3: LRU=0
   Entry
Entry
Data
176:
    -1
       - 2
           -3
               1
                       3
                           0
                               0
   5
       -5
           6
                   0
                       0
208:
               0
                               0
                           0
   0
       0
                               0
           0
240:
Cvcle:28
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
       9
                               Ω
ROO:
           Ω
               6
                   Ω
                           -1
   0
       0
           40
                       0
                           0
R08:
   0
               0
                   0
                               0
R16:
   0
       0
           0
               0
                   0
                       0
                           0
                               0
                               Ω
R24:
   0
       0
           0
Cache
Set 0: LRU=0
   Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
       - 2
176:
    -1
           -3
               1
                   2
                       3
                           Ω
                               Ω
208:
   5
       -5
           6
               0
                   0
                       0
                           0
                               0
240:
   0
       Ω
           0
               Ω
                   0
                       Ω
                           1
                               0
Cycle:29
```

```
sample_pipeline.txt
                                       Page 23 of 157
Pre-Issue Buffer:
    Entry 0:
             [SLL
                 R10, R1, #2]
                 R3, 176(R10)]
    Entry 1:
             [LW
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        9
R00:
    0
             Ω
                 6
                     Ω
                         1
                              -1
                                  Ω
R08:
    0
        0
             40
                 0
                     0
                         0
                              0
                                  0
R16:
    0
        0
             0
                 0
                     0
                         0
                              0
                                  0
R24:
    0
        0
             0
                 0
                     0
                         0
                              0
                                  0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
176:
    -1
        -2
             -3
                         3
                              0
                                  0
                 1
        -5
             6
208:
                     0
                                  0
240:
    0
        0
             0
                     0
                         0
                              1
                                  0
Cycle:30
Pre-Issue Buffer:
    Entry 0:
                 R3, 176(R10)]
             [LW
    Entry 1:
Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
             [SLL
                 R10, R1, #2]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
```

```
Page 24 of 157
sample_pipeline.txt
Post_MEM Queue:
    Entry 0:
Registers
         9
                                     0
R00:
    0
              0
                   6
                       0
                                 -1
                                 0
R08:
    0
         0
              40
                       0
                                     0
R16:
    0
         0
              0
                   0
                       0
                            0
                                 0
                                     0
R24:
              0
                                     0
    0
         0
                            0
                                 0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Set 3: LRU=1
    Entry
Entry
Dat.a
         - 2
                       2
                                 Ω
                                     Ω
176:
     -1
              -3
                  1
                            3
    5
         -5
              6
                       0
                            0
208:
                   0
                                     0
                                 0
    0
         0
                   0
                       0
                            0
                                     0
240:
              0
                                 1
Cycle:31
Pre-Issue Buffer:
    Entry 0:
              [LW
                  R3, 176(R10)]
    Entry 1:
              [LW
                  R4, 220(R10)]
    Entry 2:
              [LW
                  R5, 264(R0)]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
              [SLL
                  R10, R1, #2]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
         9
R00:
              Ω
                   6
                       Ω
                            1
                                 -1
                                     Ω
    0
R08:
    0
         0
              40
                            0
                                 0
                   0
                       0
                                     0
R16:
    0
         Ω
              0
                   0
                       0
                            0
                                 Ω
                                     0
R24:
    0
         0
              0
                   0
                       0
                            0
                                 0
                                     0
Cache
Set 0: LRU=1
    Entry
0: [\ (1\,,0\,,4\,) < 100011010101010100010000000011011100\,,1000110000000101000000010000010000>]
```

```
Page 25 of 157
sample_pipeline.txt
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
176:
  -1
     - 2
        -3
           1
              2
                 3
                    Λ
                       Ω
208:
  5
     -5
        6
           0
              0
                 0
                    0
                       0
240:
  0
     Ω
        0
           Ω
              0
                 Ω
                    1
                       0
Cycle:32
Pre-Issue Buffer:
  Entry 0:
        [LW
           R5, 264(R0)]
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
           R3, 176(R10)]
        [T.W
  Entry 1:
        [LW
           R4, 220(R10)]
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     9
        0
           6
              0
                 1
                    -1
                       0
R08:
  0
     0
        36
           0
              0
                 0
                    0
                       0
        0
                       0
R16:
  0
     0
                    0
R24:
  0
     0
        0
           0
              0
                 0
                    0
                       0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
```

```
sample_pipeline.txt
                                    Page 26 of 157
   Entry
-2
                           0
                               0
176:
    -1
           -3
               1
                   2
       -5
208:
                               0
240:
    0
       0
Cvcle:33
Pre-Issue Buffer:
               R5, 264(R0)]
   Entry 0:
           [LW
   Entry 1:
Entry 2:
   Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
           [LW
               R3, 176(R10)]
   Entry 1:
           [LW
               R4, 220(R10)]
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       9
           0
               6
                   0
                               0
R08:
    0
       0
           36
               0
                   0
                               0
R16:
    0
           0
               0
                   0
                       0
                           0
                               0
       0
R24:
    0
       0
           0
                               0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
    -1
       - 2
           - 3
               1
                   2
                       3
                           Ω
                               Ω
    5
       -5
208:
           6
               0
                   0
                       0
                               0
                           0
    Ω
       Ω
               0
240:
           0
                   0
                       Ω
                           1
                               0
Cycle:34
Pre-Issue Buffer:
   Entry 0:
    Entry 1:
    Entry 2:
```

```
Page 27 of 157
sample_pipeline.txt
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
     Entry 0:
               [LW
                    R4, 220(R10)]
                    R5, 264(R0)]
     Entry 1:
               [LW
Post_MEM Queue:
                    R3, 176(R10)]
    Entry 0:
               [LW
Registers
          9
               Ω
                         Ω
R00:
                    6
                              1
                                        Ω
     0
                                   - 1
R08:
               36
                              0
                                   0
     0
          0
                    0
                         0
                                        0
R16:
     0
          Ω
               0
                    0
                         0
                              0
                                   Ω
                                        0
R24:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
Cache
Set 0: LRU=1
     Entry
0: [\ (1\,,0\,,4\,) < 100011010101010100010000000011011100\,,1000110000000101000000010000010000>]
     Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
     Entry
Entry
Data
176:
     -1
          - 2
               -3
                    1
                         2
                              3
                                   0
                                        0
208:
     5
          -5
               6
                    0
                         0
                              0
                                   0
                                        0
240:
     0
          0
               0
                                        0
Cycle:35
Pre-Issue Buffer:
     Entry 0:
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
     Entry 0:
Pre_MEM Queue:
     Entry 0:
               [LW
                    R4, 220(R10)]
    Entry 1:
               [LW
                    R5, 264(R0)]
Post_MEM Queue:
    Entry 0:
Registers
R00:
          9
               0
                    -5
                         0
                             1
                                        0
```

```
sample_pipeline.txt
                                         Page 28 of 157
R08:
    0
         0
             36
                      0
                           0
                               0
                                    0
R16:
    0
         0
             0
                  0
                      0
                           0
                               0
                                    0
R24:
    0
         0
             0
                      0
                           0
                               0
                                    0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
0: [\,(1\,,0\,,3\,)\,<\bar{10}000000000000000101101000010000000\,,10001101010000110000010110000>\,]
    Entry
Data
176:
         -2
             -3
                  1
                           3
                               0
                                    0
    -1
         -5
             6
208:
                  0
                      0
                           0
                               0
                                    0
240:
    0
         0
             0
                           0
                                    0
Cycle:36
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [LW
                  R5, 264(R0)]
    Entry 1:
Post_MEM Queue:
                  R4, 220(R10)]
    Entry 0:
             [LW
Registers
R00:
    0
         9
             0
                  -5
                      0
                           1
                                    0
                                -1
R08:
         0
                  0
                           0
                               0
    0
             36
                      0
                                    0
R16:
    0
             0
                  0
                           0
                               0
                                    0
         0
                      0
R24:
    0
         0
             0
                  0
                      0
                           0
                               0
                                    0
Cache
Set 0: LRU=0
    Entry
0: [\,(1\,,0\,,4)\,<\,10001101010001000000000011011100\,,\,100011000000010100000001000010000]
Set 1: LRU=1
    Entry
```

```
Page 29 of 157
sample_pipeline.txt
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Dat.a
      - 2
                     Ω
176:
   -1
         -3
            1
               2
                  3
                        Ω
   5
      -5
         6
               0
                  0
208:
            0
                     0
                        0
      Ω
240:
   Ω
         0
            Ω
               0
                  Ω
                     1
                        0
Cycle:37
Pre-Issue Buffer:
   Entry 0:
         [ADD
            R6, R4, R5]
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
         [LW
            R5, 264(R0)1
Registers
      9
            -5
R00:
   0
         Λ
               0
                  1
                     -1
                        0
R08:
   0
      Ω
         36
            Ω
               0
                  0
                     Ω
                        0
R16:
   0
      Ω
         0
            0
               Ω
                  0
                     Ω
                        0
R24:
   0
      0
         0
            0
               0
                  0
                     0
                        0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
176:
   -1
      -2
         -3
            1
               2
                  3
                     0
                        0
```

```
sample_pipeline.txt
                                       Page 30 of 157
208:
   5
       -5
                     0
                         0
                             0
                                  0
        0
240:
    0
                                  0
Cycle:38
Pre-Issue Buffer:
    Entry 0:
            [SW
                 R6, 176(R10)]
                R1, R1, #-1]
    Entry 1:
            [ADDI
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
            [ADD
                R6, R4, R5]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        9
            0
R08:
    0
        0
            36
                 0
                     0
                         0
                             Ω
                                  0
R16:
                             0
    0
R24:
    0
        0
                                  0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
                             0
176:
    -1
        -2
            -3
                 1
                     2
                         3
                                  0
        -5
            -1
208:
    5
                 0
                     0
                         0
                             0
                                  0
240:
    0
        0
                     0
                                  0
Cvcle:39
Pre-Issue Buffer:
                 R6, 176(R10)]
    Entry 0:
            [SW
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
            [ADDI
                R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
```

```
sample_pipeline.txt
                                               Page 31 of 157
     Entry 0:
               [ADD
                    R6, R4, R5]
Pre_MEM Queue:
     Entry 0:
     Entry 1:
Post_MEM Queue:
     Entry 0:
Registers
R00:
          9
               0
                    -5
                         0
                              1
                                         0
     0
                                    -1
R08:
     0
          0
                    0
                              0
                                   0
                                         0
               36
                         0
R16:
     0
               0
                    0
                                         0
          0
                         0
                              0
                                   0
R24:
     0
                                         0
          0
               0
                              0
                                   0
Cache
Set 0: LRU=0
     Entry
0: [\,(1\,,0\,,4\,)\,<\,100011010101010100010000000011011100\,,\,1000110000000101000000010000010000>\,]
     Entry
Set 1: LRU=0
     Entry
Entry
Set 2: LRU=1
     Entry
Entry
Set 3: LRU=0
     Entry
Entry
Data
176:
          - 2
                                         0
     -1
               -3
                         2
                                   Λ
208:
     5
          -5
               -1
                    0
                         0
                              0
                                   0
                                         0
     0
          Ω
                    0
240:
               0
                         0
                              Ω
                                   1
                                         0
Cycle:40
Pre-Issue Buffer:
     Entry 0:
               [SW
                    R1, 268(R0)]
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
                   R1, R1, #-1]
     Entry 0:
               [ADDI
Pre_MEM Queue:
     Entry 0:
                    R6, 176(R10)]
               [SW
     Entry 1:
Post_MEM Queue:
     Entry 0:
Registers
R00:
     0
          9
               Ω
                    -5
                         0
                                         0
                    0
                              0
R08:
     0
          0
               36
                         0
                                   0
                                         0
R16:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                         0
R24:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                         0
Cache
```

```
Page 32 of 157
sample_pipeline.txt
Set 0: LRU=1
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
0: [\,(1\,,0\,,4\,)\,<\bar{10}001000000000000000000000000100110\,,10000000100001010011000000100000>\,]
   Entry
Set 3: LRU=0
   Entry
Entry
176:
   -1
       -2
           -3
                          0
                              0
208:
   5
       -5
           -1
               0
                   0
                       0
                          0
                              0
240:
   0
       0
Cycle:41
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [SW
               R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
       8
                   0
                              0
R08:
   0
       0
                          0
                              0
           36
                   0
                       0
R16:
   0
       0
           0
                   0
                       0
                          0
                              0
R24:
   0
       0
           0
                   0
                       0
                          0
                              0
Cache
Set 0: LRU=1
   Entry
Set 1: LRU=0
   Entry
Set 2: LRU=0
   Entry
0: [\,(1\,,0\,,4\,)\,<\,10001000000000000000000000000100110\,,\,100000001000010100110000001000000>\,]
```

```
Page 33 of 157
sample_pipeline.txt
Set 3: LRU=0
   Entry
Entry
Data
    -1
       -2
           -3
               1
                   2
                       3
                           0
                               0
176:
       -5
208:
    5
           -1
               0
                   0
                       0
                           0
                               0
    0
       0
           0
                               0
240:
                   0
Cycle:42
Pre-Issue Buffer:
               R1, 268(R0)]
   Entry 0:
           [LW
    Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
       8
R00:
           0
                   0
                               0
   0
               -5
                       1
                           1
R08:
    Ω
       Ω
           36
               Ω
                       Ω
                           Ω
                               Ω
                   0
           0
               0
                               0
R16:
    0
       0
                   0
                       0
                           0
R24:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
0: [\,(1,0,3)<\hat{10000000000000000010101000010000000}\,,10001101010000110000010110000>\,]
   Entry
Data
176:
    -1
       -2
           -3
               1
                   2
                       3
                           Ω
                               0
    5
       -5
           -1
208:
               0
                   0
                       0
                           0
                               0
240:
    0
       0
           0
               0
                   0
                       0
                           1
                               0
Cycle:43
```

```
sample_pipeline.txt
                                     Page 34 of 157
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
            [LW
                R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
        8
            0
                -5
                    0
                            1
                                0
                Ω
R08:
    Ω
        Ω
            36
                    0
                        Ω
                            Ω
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
        0
            0
                    0
                            0
                                0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
                            0
                                0
208:
        -5
                            0
                                0
240:
Cycle:44
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
   Entry 2:
Entry 3:
Pre_ALU Queue:
   Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
```

```
sample_pipeline.txt
                                 Page 35 of 157
   Entry 0:
          [LW
              R1, 268(R0)]
Registers
R00:
       8
          0
              -5
                  0
                            0
R08:
   0
          36
                            0
       0
              0
                  0
                     0
                         0
R16:
   0
       0
          0
                  0
                     0
                         0
                            0
R24:
   0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
       - 2
          -3
                         0
                            0
              1
       -5
   5
          -1
208:
              Ω
                  Ω
                     Ω
                            Ω
                         Ω
   0
       0
                            0
240:
Cycle:45
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
       8
R00:
   0
          Ω
              -5
                  Ω
                     1
                         1
                            Ω
R08:
   Ω
          36
              Ω
                     Ω
                         Ω
                            Ω
       Ω
                  0
              0
                            0
R16:
   0
       0
          0
                  0
                     0
                         0
R24:
   0
       0
          0
              0
                  0
                     0
                         0
                            0
Cache
Set 0: LRU=1
   Entry
```

```
Page 36 of 157
sample_pipeline.txt
Set 1: LRU=0
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
      -2
          -3
             1
                 2
                       Ω
                           0
   5
208:
      -5
          -1
             Ω
                 Ω
                    Ω
                       Ω
                           0
240:
   0
      0
          0
             0
                 0
                    0
                       1
                           0
Cycle:46
Pre-Issue Buffer:
          [SLL
             R10, R1, #2]
   Entry 0:
   Entry 1:
          [LW
             R3, 176(R10)]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      8
          Ω
             -5
                 0
                           0
R08:
   0
      0
          36
             0
                 0
                    0
                       0
                           0
R16:
   0
      0
          0
             0
                 0
                    0
                       0
                           0
R24:
                           0
      0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Set 2: LRU=1
   Entry
Set 3: LRU=1
   Entry
0: [\,(1,0,3)\,<\,1000000000000000010101000010000000\,,\,100011010000011000000101100000\,>\,]
```

```
sample_pipeline.txt
                                     Page 37 of 157
Data
                            0
176:
            -3
208:
        -5
                    0
    5
            -1
                            0
                                0
240:
Cycle:47
Pre-Issue Buffer:
                R3, 176(R10)]
    Entry 0:
Entry 1:
            [LW
    Entry 2:
Entry 3:
Pre_ALU Queue:
                R10, R1, #2]
    Entry 0:
            [SLL
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        8
            0
                -5
                    0
                                0
R08:
    0
        0
            36
                0
                        0
                            0
                                0
                    0
R16:
    0
        0
            0
                    0
                        0
                            0
                                0
R24:
    0
                        0
                                0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
        - 2
                    2
                        3
                            0
                                Ω
176:
    -1
            -3
                1
        -5
    5
208:
            -1
                Ω
                    Ω
                        Ω
                                Ω
                            0
        0
240:
    0
            0
                0
                                0
                    0
                        0
                            1
Cycle:48
Pre-Issue Buffer:
    Entry 0:
            [LW
                R3, 176(R10)]
    Entry 1:
            [LW
                R4, 220(R10)]
    Entry 2:
            [LW
                R5, 264(R0)]
    Entry 3:
```

```
sample_pipeline.txt
                                             Page 38 of 157
Pre_ALU Queue:
     Entry 0:
    Entry 1:
Post_ALU Queue:
              [SLL
    Entry 0:
                  R10, R1, #2]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
     0
         8
              0
                   -5
                        0
                             1
                                       0
                                  1
R08:
     Ω
              36
                   Ω
                             Ω
                                  Ω
                                       Ω
         Ω
                        0
                   0
R16:
     0
         0
              0
                        0
                             0
                                  0
                                       0
R24:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
0: [\,(1,0,3)<\hat{10000000000000000010101000010000000}\,,10001101010000110000010110000>\,]
    Entry
Data
176:
     -1
         -2
              -3
                   1
                        2
                             3
                                  Ω
                                       Ω
208:
     5
         -5
              -1
                   0
                        0
                             0
                                  0
                                       0
240:
     0
         0
                        0
                                       0
Cycle:49
Pre-Issue Buffer:
                   R5, 264(R0)]
    Entry 0:
              [LW
     Entry 1:
     Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                   R3, 176(R10)]
              [LW
    Entry 1:
              [LW
                   R4, 220(R10)]
Post_MEM Queue:
    Entry 0:
Registers
R00:
     0
R08:
     0
              32
```

```
sample_pipeline.txt
                                     Page 39 of 157
R16:
    0
        0
                            Ω
                                0
R24:
    0
        0
                                0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
   Entry
0:[(1,0,4)<100001000110000000000000000001,10000001010011001100000100010>]
    Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
    Entry
0: [\,(1,0,3)\,<\,100000000000000010101000010000000\,,\,1000110101000001100000010110000>\,]
Data
176:
    -1
208:
    5
        -5
            -1
                    0
                        0
                                0
    0
240:
Cvcle:50
Pre-Issue Buffer:
   Entry 0:
Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
            [LW
                R4, 220(R10)]
    Entry 1:
            [LW
                R5, 264(R0)]
Post_MEM Queue:
            [LW
   Entry 0:
                R3, 176(R10)]
Registers
R00:
        8
            0
                -5
                    0
                                0
    0
R08:
    0
        0
            32
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
        0
            0
                0
                    0
                        0
                                0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
   Entry
Entry
```

```
Page 40 of 157
sample_pipeline.txt
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
   -1
       - 2
           -3
              1
                  2
                      3
                         0
                             0
   5
           -1
208:
       - 5
              Ω
                  Ω
                      Ω
                             Ω
                         0
       0
   0
           0
                             0
240:
              0
                  0
                      0
                         1
Cycle:51
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [LW
              R4, 220(R10)]
   Entry 1:
           [LW
              R5, 264(R0)]
Post_MEM Queue:
   Entry 0:
Registers
       8
           Ω
              5
                  Ω
                             Ω
R00:
   0
                      1
                         1
R08:
   0
       0
           32
              0
                  0
                      0
                         0
                             0
R16:
   0
       0
           0
              Ω
                  0
                      0
                         Ω
                             0
R24:
   0
       0
           Ω
              Ω
                  Ω
                      Ω
                         0
                             0
Cache
Set 0: LRU=0
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Set 3: LRU=1
   Entry
0: [\,(1\,,0\,,3\,)<100000000000000010101000010000000\,,10001101010000110000010110000>]
   Entry
Data
176:
   -1
208:
   5
       -5
                             0
```

```
sample_pipeline.txt
                                     Page 41 of 157
240: 0 0
                       0 1
            0
                    0
Cycle:52
Pre-Issue Buffer:
    Entry 0:
            [SUB
                R6, R4, R5]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
   Entry 0:
Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                R5, 264(R0)]
            [LW
    Entry 1:
Post_MEM Queue:
                R4, 220(R10)]
    Entry 0:
            [LW
Registers
R00:
        8
            0
                    0
                                 0
R08:
    0
        0
            32
                0
                    0
                        0
                            0
                                 0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                 0
R24:
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Data
176:
    -1
        -2
            -3
                            0
                                 0
208:
    5
        -5
            -1
                0
                    0
                        0
                            0
                                 0
    0
        0
            0
240:
                0
                    0
                                 0
Cycle:53
Pre-Issue Buffer:
            [SUB R6, R4, R5]
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
```

```
Page 42 of 157
sample_pipeline.txt
Pre_MEM Queue:
     Entry 0:
     Entry 1:
Post_MEM Queue:
               [LW
                    R5, 264(R0)]
    Entry 0:
Registers
R00:
          8
               0
                    5
                         0
                              1
                                   1
                                        0
     0
R08:
     0
          0
               32
                    0
                         0
                              0
                                   0
                                        0
R16:
     0
               0
                    0
                              0
                                   0
                                        0
          0
                         0
R24:
     0
               0
                    0
                         0
                              0
                                        0
          0
                                   0
Cache
Set 0: LRU=0
     Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
     Entry
0: [\,(1,0,3)<\hat{10000000000000000010101000010000000}\,,10001101010000110000010110000>\,]
     Entry
Data
     -1
          - 2
               -3
                    1
                         2
                              3
                                   Ω
                                        Ω
176:
     5
          -5
208:
               -1
                    0
                         0
                              0
                                   0
                                        0
240:
     0
          0
               0
                                        0
Cycle:54
Pre-Issue Buffer:
     Entry 0:
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
               [SUB
                    R6, R4, R5]
     Entry 1:
Post_ALU Queue:
     Entry 0:
Pre_MEM Queue:
    Entry 0:
Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
     0
          8
               0
                    5
                         0
                              1
                                   1
                                        0
R08:
     0
          0
               32
                    0
                         0
                              0
                                   Ω
                                        0
R16:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
R24:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
Cache
Set 0: LRU=0
```

```
Page 43 of 157
sample_pipeline.txt
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
0: [\,(1,0,3)\,<\,100000000000000010101000010000000\,,\,1000110101000001100000010110000>\,]
   Entry
Data
176:
   -1
      -5
208:
   5
            0
               0
                      0
                         0
240:
   0
      Ω
               Ω
                         0
Cycle:55
Pre-Issue Buffer:
            R6, 176(R10)]
   Entry 0:
         [SW
            R1, R1, #-1]
   Entry 1:
         [ADDI
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
         [SUB
            R6, R4, R5]
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      8
         0
               0
                         0
R08:
   0
      0
         32
                   0
                      0
                         0
   0
            0
                         0
R16:
      0
         0
                   0
                      0
R24:
   0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
```

```
Page 44 of 157
sample_pipeline.txt
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
             -3
                     2
                          3
                              0
                                  0
208:
    5
        -5
                 0
                     0
                          0
                              0
                                  0
             -1
240:
    0
        0
             0
                 0
                     0
                                  0
Cycle:56
Pre-Issue Buffer:
             ſSW
                 R1, 268(R0)]
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
             [ADDI
                 R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [SW
                 R6, 176(R10)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        8
             0
                     0
                              -1
                                  0
R08:
    0
                 0
                          0
                              0
        0
             32
                     0
                                  0
R16:
    0
             Ω
                 Ω
                          Ω
                              Ω
                                  Ω
        0
                     0
R24:
    0
        0
             0
                          0
                                  0
                     0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
0: [\,(1\,,0\,,4\,)\,<\,1000100000000000000000000000100110\,,\,100000001000010100110000001000000\,>\,]
    Entry
Set 3: LRU=1
    Entry
Data
176:
    -1
        -2
             -3
                 1
                     2
                          3
                              0
                                  0
208:
    5
        -5
             -1
                 Ω
                     0
                          0
                              0
                                  0
        0
240:
    0
                                  0
Cycle:57
Pre-Issue Buffer:
```

```
Page 45 of 157
sample_pipeline.txt
    Entry 0:
            [SW
                 R1, 268(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
            [ADDI
                R1, R1, #-1]
Pre_MEM Queue:
    Entry 0:
Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        8
            0
                 5
                     0
                             -1
                                  0
R08:
    0
        0
            32
                 0
                     0
                         0
                             0
                                  0
R16:
    0
        Ω
            Ω
                 Ω
                     0
                         0
                             Ω
                                  0
R24:
    0
        0
            0
                 0
                     0
                         0
                              0
                                  0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Data
176:
        -2
            -3
                              0
                                  0
208:
    5
        -5
            -1
                     0
240:
    0
        0
                     0
                                  0
Cycle:58
Pre-Issue Buffer:
    Entry 0:
            [LW
                R1, 268(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
                 R1, 268(R0)]
    Entry 0:
            [SW
    Entry 1:
Post_MEM Queue:
    Entry 0:
```

```
sample_pipeline.txt
                                       Page 46 of 157
Registers
R00:
    0
        7
             0
                 5
                     0
                                  0
R08:
    0
        0
             32
                          0
                              0
                                  0
R16:
    0
                 0
                              0
                                  0
        0
             0
                     0
                         0
R24:
    0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
             -3
                 1
                         3
                              0
                                  0
    5
        -5
208:
             -1
                     0
                         0
                 0
                              0
                                  0
        0
             0
                                  Ω
240:
    Ω
                 Ω
                     Ω
                         Ω
                              1
Cycle:59
Pre-Issue Buffer:
    Entry 0:
Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                 R1, 268(R0)]
             [LW
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        7
R00:
    0
             0
                 5
                     0
                         1
                              -1
                                  0
                              Ω
R08:
    Ω
        Ω
             32
                 Ω
                     0
                         Ω
                                  Ω
R16:
    Ω
             Ω
                 Ω
                         Ω
                                  Ω
        Ω
                     0
                              Ω
R24:
                 0
                                  0
    0
        0
             0
                     0
                          0
                              0
Cache
Set 0: LRU=1
    Entry
Entry
1: [\,(1\,,0\,,4\,)\,<\,100011010101010100010000000011011100\,,\,1000110000000101000000010000010000>\,]
Set 1: LRU=0
```

```
Page 47 of 157
sample_pipeline.txt
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
176:
  -1
     -2
        -3
           1
             2
                3
                   0
                      0
208:
  5
     -5
        -1
           0
             0
                0
                   0
                      0
     Ω
240:
  Ω
                      Ω
Cycle:60
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
        [LW
           R1, 268(R0)]
Registers
R00:
  0
     7
        0
           5
             0
                1
                   -1
                      0
R08:
  0
     Ω
        32
           Ω
             0
                0
                   Ω
                      0
R16:
  0
     0
        0
           0
             0
                0
                   0
                      0
R24:
  0
     0
        0
             0
                0
                   Ω
                      0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
```

```
sample_pipeline.txt
                                    Page 48 of 157
Data
176:
       -2
           -3
                           0
                               0
208:
    5
       -5
240:
   0
       0
Cycle:61
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
Entry 2:
    Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
       7
                           -1
                               0
                           0
R08:
    0
       0
           32
                   0
                       0
                               0
R16:
    0
       0
           0
                   0
                       0
                           0
                               0
R24:
    0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
                               0
176:
    -1
       -2
               1
                   2
                           0
    5
208:
       - 5
           -1
               Ω
                   Ω
                       Ω
                           Ω
                               0
240:
    Ω
Cycle:62
Pre-Issue Buffer:
   Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
```

```
Page 49 of 157
sample_pipeline.txt
     Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
         7
                                       0
R00:
              0
                        0
    0
                                  -1
R08:
     0
         0
              32
                   0
                        0
                             Ω
                                  0
                                       0
     Ω
              Ω
                   Ω
                             Ω
                                       Ω
R16:
         Ω
                        Ω
                                  Ω
R24:
    0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
Cache
Set 0: LRU=1
    Entry
1: [\,(1\,,0\,,4\,)\,<\,100011010101010100010000000011011100\,,\,1000110000000101000000010000010000>\,]
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
     -1
         -2
              -3
                   1
                        2
                             3
                                  0
                                       0
208:
     5
         -5
              -1
                   0
                        0
                             0
                                  0
                                       0
240:
     0
         0
              0
                   0
                        0
                             0
                                       0
Cycle:63
Pre-Issue Buffer:
              [SLL
                   R10, R1, #2]
    Entry 0:
    Entry 1:
                   R3, 176(R10)]
              [LW
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
     0
         7
              0
                   5
                        0
                             1
                                  -1
                                       0
R08:
     0
         0
              32
                   0
                        0
                             0
                                  0
                                       0
R16:
     0
         0
                                       0
```

```
sample_pipeline.txt
                              Page 50 of 157
R24:
   0
     0
         0
                Ω
                   Ω
                      0
                          Ω
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
      -2
         -3
                2
                   3
                      0
                          0
208:
   5
      -5
         -1
             0
                0
                   0
                      0
                          0
240:
   0
      0
                0
                          0
Cycle:64
Pre-Issue Buffer:
             R3, 176(R10)]
         M.T l
   Entry 0:
             R4, 220(R10)]
   Entry 1:
         [LW
   Entry 2:
             R5, 264(R0)]
         [LW
   Entry 3:
Pre_ALU Queue:
   Entry 0:
         [SLL
             R10, R1, #2]
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      7
         0
                0
                       -1
                          0
R08:
   0
      0
         32
             0
                      0
                          0
                0
R16:
   0
      0
         0
             0
                0
                   0
                      0
                          0
R24:
   0
      0
         0
                          0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
```

```
Page 51 of 157
sample_pipeline.txt
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
      -2
                2
                       0
                          0
   -1
          -3
             1
                    3
176:
208:
   5
      -5
          -1
             0
                0
                    0
                       0
                          0
      0
   Ω
                          Ω
240:
Cycle:65
Pre-Issue Buffer:
   Entry 0:
          [LW
             R3, 176(R10)]
   Entry 1:
          [LW
             R4, 220(R10)]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
          [SLL
             R10, R1, #2]
Pre_MEM Queue:
   Entry 0:
          [LW
             R5, 264(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
      7
          0
                0
                       -1
                          0
   0
             5
                    1
R08:
      Ω
          32
             Ω
                    Ω
                       Ω
   0
                0
                          0
R16:
   0
      Ω
          0
             0
                0
                    0
                       Ω
                          0
R24:
   0
          Ω
                    Ω
                       Ω
                          0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
      -2
176:
   -1
          -3
             1
                2
                    3
                       Ω
                          0
208:
   5
      -5
             0
                0
                    0
                       0
                          0
240:
   0
                0
                          0
```

```
sample_pipeline.txt
                                      Page 52 of 157
Cycle:66
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                R3, 176(R10)]
            [ LW
    Entry 1:
            [LW
                R4, 220(R10)]
Post_MEM Queue:
    Entry 0:
            [LW
                R5, 264(R0)]
Registers
R00:
    0
        7
            Ω
                5
                     0
                         1
                             -1
                                 0
R08:
    0
        0
            28
                0
                     0
                         0
                             0
                                 0
R16:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R24:
    0
        0
            0
                Ω
                     0
                         0
                             Ω
                                 0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
            -3
                1
                             0
                                 0
    5
208:
        -5
            -1
                0
                             0
                                 0
240:
    0
Cvcle:67
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
```

```
Page 53 of 157
sample_pipeline.txt
    Entry 0:
             [LW
                 R3, 176(R10)]
    Entry 1:
             [LW
                 R4, 220(R10)]
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        7
             0
                      0
                               -1
                                   0
R08:
        0
             28
                 0
                          0
                              0
                                   0
    0
                      0
R16:
    0
             0
                 0
                          0
                              0
                                   0
        0
                      0
                 0
                                   0
R24:
    0
        0
             0
                      0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        - 2
             -3
                      2
                              0
                                   0
                 1
    5
        -5
             -1
                 Ω
                      Ω
                          Ω
                                   Ω
208:
                              Ω
        0
240:
    0
                      0
                          0
                              1
                                   0
Cycle:68
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                 R4, 220(R10)]
             [LW
    Entry 1:
Post_MEM Queue:
    Entry 0:
             [LW
                 R3, 176(R10)1
Registers
        7
             Ω
                 5
                      Ω
R00:
    0
                          1
                              -1
                                   Ω
R08:
    0
        0
             28
                 0
                      0
                          0
                              0
                                   0
R16:
    0
        Ω
             0
                 0
                      0
                          0
                              Ω
                                   0
R24:
    0
        0
             0
                      0
                          0
                              0
                                   0
Cache
Set 0: LRU=0
    Entry
```

```
Page 54 of 157
sample_pipeline.txt
Entry
1: [\,(1,0,4)<\overline{10}001101010001000000000011011100\,,100011000000010100000001000010000]
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
      -2
         -3
            1
               2
                   3
                      0
                         0
208:
   5
      -5
            0
               0
                   0
                      0
                         0
         -1
240:
   0
      0
         0
                         7
Cycle:69
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
         [LW
            R4, 220(R10)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
      7
               0
   0
R08:
   0
      0
         28
            0
               0
                   0
                      0
                         0
R16:
   0
      0
            0
                      0
                         0
                      0
                         0
R24:
   0
      0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
```

```
Page 55 of 157
sample_pipeline.txt
    Entry
Entry
Data
176:
    -1
        -2
            -3
                1
                         3
                             0
                                 0
208:
    5
        -5
            -1
                0
                     0
                         0
                             0
                                 0
                                 7
240:
    0
        0
Cycle:70
Pre-Issue Buffer:
            [SUB
                R6, R4, R5]
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
            [LW
                R4, 220(R10)]
Registers
R00:
    0
        7
            0
                0
                     0
                         1
                                 0
                             -1
R08:
    0
        0
            28
                0
                     0
                         0
                             0
                                 0
R16:
    0
            0
        0
                0
                     0
                         0
                             0
                                 0
R24:
    0
            Ω
                Ω
                     Ω
                                 Ω
        Ω
                         0
                             0
Cache
Set 0: LRU=0
    Entry
Entry
1: [\,(1,0,4)<1000110101010100010000000011011100\,,1000110000000101000000010000010000>]
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
                             0
                                 Ω
176:
    -1
        - 2
            -3
                1
                     2
208:
    5
        -5
            -1
                0
                     0
                         0
                             0
                                 0
                                 7
240:
    0
        Ω
            Ω
                Ω
                     Ω
                         Ω
Cycle:71
Pre-Issue Buffer:
    Entry 0:
```

```
Page 56 of 157
sample_pipeline.txt
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
             [SUB
                 R6, R4, R5]
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
         7
             Ω
R00:
    0
                  0
                      0
                           1
                                -1
                                    0
R08:
    0
         0
             28
                  0
                      0
                           0
                               0
                                    0
R16:
    0
         0
             0
                  0
                      0
                           0
                                0
                                    0
R24:
    0
         Ω
             Ω
                                Ω
                                    Ω
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
0:[(1,0,4)<100001000110000000000000000001,10000001010011001100000100010>]
    Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
176:
                               0
208:
    -1
                  0
                      0
                           0
                                0
                                    0
240:
    0
         0
Cycle:72
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
             [SUB R6, R4, R5]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
```

```
Page 57 of 157
sample_pipeline.txt
Registers
R00:
    0
        7
            0
                 0
                     0
                         1
                              -1
                                  0
R08:
    0
        0
            28
                 0
                     0
                         0
                              0
                                  0
R16:
    0
        0
                              0
                                  0
        0
                              0
                                  0
R24:
    0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
1: [\,(1\,,0\,,4\,)\,<\,10001000000000000000000000000100110\,,\,100000001000010100110000001000000>\,]
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
            -3
                 1
                     2
                         3
                              0
                                  0
208:
    -1
        1
            -1
                 0
                     0
                         0
                              0
                                  0
    0
            0
                                  7
        0
                     0
                         0
240:
Cvcle:73
Pre-Issue Buffer:
                 R6, 176(R10)]
            [SW
    Entry 0:
    Entry 1:
            [ADDI
                 R1, R1, #-1]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        7
R00:
            0
                 0
                     0
                         1
                                  0
    0
                              -1
R08:
    0
        0
            28
                 0
                     0
                         0
                              0
                                  0
R16:
    0
        Ω
            Ω
                 Ω
                     0
                         Ω
                              Ω
                                  0
R24:
    Ω
                                  Ω
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
```

```
Page 58 of 157
sample_pipeline.txt
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
      -2
         -3
             1
                2
                   3
                       Ω
                          Ω
208:
   -1
      1
         -1
             0
                0
                   0
                       0
                          0
7
240:
   0
      0
         0
             0
                0
Cycle:74
Pre-Issue Buffer:
   Entry 0:
         [SW
             R1, 268(R0)]
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
         [ADDI
             R1, R1, #-1]
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
             R6, 176(R10)]
         [SW
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
      7
R00:
   Ω
         Ω
             Ω
                Ω
                   1
                       -1
                          Ω
R08:
   0
      0
         28
             0
                0
                   0
                       0
                          0
R16:
   0
      Ω
         0
             0
                0
                   0
                       0
                          0
R24:
   0
      0
         0
             0
                0
                   0
                       0
                          0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
1: [\,(1,0,4)<1000100000000000000000000000100110\,,10000000100001010011000000100000>]
Set 3: LRU=0
   Entry
Entry
```

```
sample_pipeline.txt
                                       Page 59 of 157
Data
176:
    -1
        -2
             -3
                 1
                     2
                         3
                              0
                                  0
208:
    -1
            -1
                 0
                     0
                         0
                              0
                                  0
240:
    0
        0
Cycle:75
Pre-Issue Buffer:
                 R1, 268(R0)]
R1, 268(R0)]
    Entry 0:
Entry 1:
             [SW
             [LW
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
             [ADDI
                R1, R1, #-1]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00: 0
        7
                                  0
R08:
    0
        0
             28
                     0
                         0
                              0
                                  0
R16:
    0
        0
             0
                 0
                     0
                         0
                              0
                                  0
R24:
    0
        0
                                  0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
            -3
                 1
                     2
                         3
                              0
                                  0
    -1
            -1
208:
        1
                 0
                     0
                         0
                              0
                                  0
    0
                                  7
240:
        Ω
             Ω
                     Ω
                         Ω
                 Ω
Cycle:76
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
```

```
sample_pipeline.txt
                                         Page 60 of 157
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
             [SW
                  R1, 268(R0)]
    Entry 0:
    Entry 1:
                 R1, 268(R0)]
             [LW
Post_MEM Queue:
    Entry 0:
Registers
         6
             0
                  0
R00:
                      0
                           1
                                    0
    0
                               -1
R08:
                               0
    0
             28
                           0
                                    0
        0
                  0
                      0
R16:
    0
         0
             0
                  0
                      0
                           0
                               0
                                    0
    Ω
             Ω
                      Ω
                                    Ω
R24:
         0
                  0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
                               0
176:
    -1
         -2
             -3
                  1
                      2
                           3
                                    Ω
208:
    -1
        1
             -1
                  0
                      0
                           0
                               0
                                    0
240:
    0
         0
             0
                  Ω
                      0
                           0
                               1
                                    7
Cycle:77
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
                 R1, 268(R0)]
    Entry 0:
             [SW
                  R1, 268(R0)]
    Entry 1:
             [LW
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         6
             0
                  0
                      0
                           1
                               -1
                                    0
R08:
    0
        0
             28
                  0
                      0
                           0
                               0
                                    0
R16:
    0
         0
             0
                  0
                      0
                           0
                               0
                                    0
R24:
    0
         0
             0
                  0
                                    0
```

```
Page 61 of 157
sample_pipeline.txt
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
1: [\,(1,0,4)<1000100000000000000000000000100110\,,10000000100001010011000000100000>]
Set 3: LRU=0
   Entry
Entry
176:
          -3
                       0
                           0
208:
   -1
          -1
             0
                0
                       0
                           0
240:
   0
      0
Cycle:78
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
          [LW
             R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      6
R08:
   0
      0
          28
             0
                0
                    0
                       0
                           0
R16:
          0
             0
                       0
                           0
   0
      0
                0
                    0
R24:
   0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
```

```
Page 62 of 157
sample_pipeline.txt
Entry
Set 3: LRU=0
   Entry
Entry
Dat.a
                          0
   -1
       -2
           -3
                  2
                      3
                             0
176:
               1
208:
   -1
           -1
               0
                  0
                      0
       1
                          0
                             0
   0
240:
       0
           0
               0
                  0
                      0
                             7
                          1
Cycle:79
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
           [LW
              R1, 268(R0)1
Registers
           0
               0
                  0
       6
                      1
                             0
R00:
   0
                          -1
R08:
                          0
   0
       0
           28
               0
                  0
                      0
                             0
R16:
   0
       Ω
           Ω
               Ω
                  0
                      Ω
                          Ω
                             0
R24:
   0
       0
           0
               0
                  0
                      0
                          0
                             0
Cache
Set 0: LRU=1
   Entry
1: [\,(1,0,4)<\overline{10}001101010001000000000011011100\,,100011000000010100000001000010000]
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
       -2
           -3
              1
                  2
                      3
                          0
                             0
208:
   -1
       1
           -1
               0
                  0
                      0
                          0
                             0
240:
   0
       0
               0
                  0
                      0
```

```
sample_pipeline.txt
                                         Page 63 of 157
Cycle:80
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         6
             0
                  0
                      0
                               -1
                                    0
R08:
    0
         0
             28
                  0
                      0
                           0
                               0
                                    0
R16:
    0
         0
             0
                  0
                           0
                               0
                                    0
R24:
    0
         0
                                    0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
1: [\,(1,0,4)<1000100000000000000000000000100110\,,10000000100001010011000000100000>]
Set 3: LRU=0
    Entry
Data
176:
    -1
             -3
                                    0
7
208:
    -1
         1
             -1
                  0
                      0
                           0
                               0
    0
240:
Cycle:81
Pre-Issue Buffer:
    Entry 0:
Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
```

```
sample_pipeline.txt
                                         Page 64 of 157
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         6
R08:
    0
         0
             28
                  0
                          0
                               0
                                   0
R16:
             0
                  0
                               0
                                   0
    0
        0
                      0
                          0
R24:
    0
                                   0
Cache
Set 0: LRU=1
    Entry
Entry
1: [\,(1,0,4)<10001101010001000000000011011100\,,100011000000010100000010000010000]
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
    -1
         -2
             -3
                      2
                          3
                               0
                                   0
                 1
176:
208:
    -1
             -1
                  0
                      0
                          0
        1
                               0
                                   0
    Ω
        Ω
             Ω
                          Ω
                                   7
240:
                  Ω
                      0
                               1
Cycle:82
Pre-Issue Buffer:
    Entry 0:
             [SLL
                 R10, R1, #2]
    Entry 1:
             [LW
                 R3, 176(R10)]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
    0
         6
             0
                 0
                                   0
R00:
                      0
                          1
                               -1
R08:
    0
        Ω
             28
                 0
                      0
                          0
                               Ω
                                   0
R16:
    0
        0
             0
                  0
                      0
                          0
                               0
                                   0
R24:
    0
        Ω
             0
                  Ω
                      0
                           Ω
                               0
                                   0
Cache
Set 0: LRU=1
```

```
Page 65 of 157
sample_pipeline.txt
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
176:
   -1
     -2
         -3
            1
               2
                  3
                     0
                        0
208:
   -1
     1
        -1
            0
               0
                  0
                     0
                        0
240:
   0
     0
         0
            0
               0
                  0
                        7
Cycle:83
Pre-Issue Buffer:
  Entry 0:
         [LW
            R3, 176(R10)]
           R4, 220(R10)]
R5, 264(R0)]
  Entry 1:
         [LW
  Entry 2:
         [LW
  Entry 3:
Pre_ALU Queue:
  Entry 0:
         [SLL
           R10, R1, #2]
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     6
         0
            0
               0
                     -1
                        0
R08:
   0
      0
                     0
         28
                        0
R16:
   0
      0
         0
            0
                  0
                     0
                        0
R24:
   0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
```

```
Page 66 of 157
sample_pipeline.txt
Entry
Data
176:
   -1
           -3
208:
   -1
           -1
                  0
                              0
                              7
240:
   0
       0
                          1
Cvcle:84
Pre-Issue Buffer:
              R3, 176(R10)]
           [LW
   Entry 0:
   Entry 1:
              R4, 220(R10)1
           [LW
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
           [SLL
              R10, R1, #2]
Pre_MEM Queue:
   Entry 0:
           [LW
              R5, 264(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       6
                  0
                          -1
                              0
R08:
   0
       0
           28
               0
                      0
                          0
                              0
                  0
R16:
   0
       0
           0
               0
                  0
                      0
                          0
                              0
                      0
                              0
R24:
   0
       0
           0
               0
                  0
                          0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
   -1
           -3
              1
                  2
                      3
                          0
                              0
       -2
208:
   -1
       1
           -1
               0
                  0
                      0
                          0
                              0
240:
   0
       0
           0
               0
                  0
                      0
                          1
                              7
Cvcle:85
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
```

```
Page 67 of 157
sample_pipeline.txt
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
                 R3, 176(R10)]
R4, 220(R10)]
    Entry 0:
             [LW
    Entry 1:
             [LW
Post_MEM Queue:
                 R5, 264(R0)]
             [LW
    Entry 0:
Registers
        6
             0
                 0
                     0
                                   0
R00:
    0
                          1
                              -1
R08:
    0
        0
             24
                 0
                     0
                          0
                              Ω
                                   0
R16:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
R24:
    0
        0
             0
                 0
                      0
                          0
                                   0
Cache
Set 0: LRU=0
    Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
             -3
                 1
                      2
                          3
                              0
                                   -1
208:
    -1
             -1
                              0
                                   0
240:
    0
        0
             0
                          0
Cycle:86
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [LW
                 R3, 176(R10)]
    Entry 1:
             [LW
                 R4, 220(R10)]
Post_MEM Queue:
    Entry 0:
Registers
```

```
sample_pipeline.txt
                                    Page 68 of 157
R00:
   0
       6
           0
               0
                   0
                               0
R08:
   0
       0
           24
               0
                   0
                       0
                           0
                               0
R16:
   0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
    -1
           -3
                               -1
208:
    -1
           -1
               0
                   0
                       0
                               0
       1
                           0
240:
   0
       0
Cvcle:87
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [LW
               R4, 220(R10)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
           [LW
               R3, 176(R10)]
Registers
R00:
           0
                   0
   0
       6
               0
                       1
                           -1
                               0
R08:
   0
       0
           24
               0
                   0
                       0
                           0
                               0
R16:
   0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
   Ω
       0
           Ω
                   Ω
                               Ω
Cache
Set 0: LRU=0
   Entry
Entry
1: [\,(1,0,4)<\overline{10}001101010001000000000011011100\,,100011000000010100000001000010000]
Set 1: LRU=0
```

```
Page 69 of 157
sample_pipeline.txt
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
          -3
             1
                    3
                       0
176:
   -1
      - 2
                 2
                           -1
208:
   -1
      1
          -1
             Ω
                 0
                    0
                       0
                           Ω
240:
   0
      0
          0
                 0
                    0
                       1
                           6
Cycle:88
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
             R4, 220(R10)]
          [ LW
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      6
          Ω
             Ω
                 Ω
                    1
                        -1
                           0
R08:
   0
      Ω
          24
             0
                 0
                    Ω
                        Ω
                           0
R16:
   0
      0
          0
             0
                 0
                    0
                        0
                           0
R24:
   0
      Ω
          0
             Ω
                 0
                    0
                        Ω
                           0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
0: [\,(1\,,0\,,3\,)\,<\bar{10}0000000000000010101000010000000\,,100011010100001100000010110000>\,]
   Entry
Data
```

```
sample_pipeline.txt
                                       Page 70 of 157
176:
    -1
        -2
            -3
                     2
                              0
                                  -1
208:
    -1
        1
            -1
                 0
                     0
                         0
                              0
                                  0
240:
    0
        0
            0
                     0
                         0
                                  6
Cycle:89
Pre-Issue Buffer:
    Entry 0:
            [SUB
                 R6, R4, R5]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
            [LW
                 R4, 220(R10)]
Registers
R00:
    0
        6
            0
                 0
                     0
                         1
                              -1
                                  0
R08:
    0
        0
            24
                         0
                              0
                                  0
                     0
R16:
    0
        0
            0
                 0
                     0
                         0
                              0
                                  0
R24:
    0
                                  0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
            -3
                              0
        -2
                 1
                     2
                         3
                                  -1
208:
    -1
        1
            -1
                 0
                     0
                         0
                              0
                                  0
    0
        0
240:
            0
                 0
                     0
                         0
                              1
                                  6
Cvcle:90
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
            [SUB
                 R6, R4, R5]
    Entry 1:
```

```
Page 71 of 157
sample_pipeline.txt
Post_ALU Queue:
     Entry 0:
Pre_MEM Queue:
     Entry 0:
     Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
          6
               0
                         0
                                        0
     0
                                   -1
R08:
                              0
                                   0
     0
                    0
          0
               24
                         0
                                        0
R16:
               0
                    0
                                   0
                                        0
     0
          0
                         0
                              0
R24:
     0
          0
               0
                              0
                                   0
                                        0
Cache
Set 0: LRU=0
     Entry
Entry
Set 1: LRU=0
     Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
     Entry
0: [\,(1,0,3)<\hat{100000000000000000010101000010000000}\,,10001101010000110000010110000>\,]
     Entry
Data
176:
     -1
          -2
               -3
                    1
                         2
                              3
                                   0
                                        -1
208:
     -1
          1
               -1
                    0
                         0
                              Ω
                                   0
                                        Ω
240:
     0
          0
               0
                    0
                         0
                              0
                                   1
                                        6
Cycle:91
Pre-Issue Buffer:
     Entry 0:
               [SW
                    R6, 176(R10)]
     Entry 1:
               [ADDI
                    R1, R1, #-1]
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
               [SUB
                   R6, R4, R5]
    Entry 0:
Pre MEM Oueue:
    Entry 0:
Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
          6
R00:
     0
               0
                    0
                         0
                              1
                                   -1
                                        0
R08:
     0
          0
               24
                    0
                         0
                              0
                                   0
                                        0
R16:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
R24:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
```

```
Page 72 of 157
sample_pipeline.txt
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
176:
   -1
     -2
        -3
              2
                    Ω
                       -1
208:
  -1
        -1
240:
  0
     0
        0
           0
              0
                       6
Cvcle:92
Pre-Issue Buffer:
  Entry 0:
        [SW
           R1, 268(R0)1
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
           R1, R1, #-1]
        [ADDI
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
        [SW
           R6, 176(R10)]
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     6
        0
              0
                    -1
                       0
R08:
  0
     0
        24
                       0
R16:
  0
     0
        0
           0
              0
                 0
                    0
                       0
R24:
  0
        0
                       0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
```

```
Page 73 of 157
sample_pipeline.txt
Set 3: LRU=0
   Entry
Entry
Data
176:
    -1
           -3
               1
                       3
                           0
                               -1
       -2
                   0
                       0
                               0
208:
    -1
       1
           -1
               0
                           0
    0
240:
                               6
Cvcle:93
Pre-Issue Buffer:
    Entry 0:
           [SW
               R1, 268(R0)]
    Entry 1:
    Entry 2:
   Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
           [ADDI
               R1, R1, #-1]
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
                               Ω
ROO:
       6
           Ω
               Ω
                   Ω
                           -1
   0
                       0
                           0
R08:
    0
       0
           24
               0
                   0
                               0
R16:
           0
    0
       0
               0
                   0
                       0
                           0
                               0
R24:
    0
       0
           0
                               0
Cache
Set 0: LRU=1
    Entry
Entry
1: [\ (1\,,0\,,4\,)\,<\,10\,0011010101000100000000011011100\,,1000110000000101000000100001000010000]
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
    -1
       -2
           -3
               1
                   2
                       3
                           Ω
                               -1
208:
    -1
       1
           -1
               0
                   0
                       0
                           0
                               0
240:
    0
       Ω
           Ω
                   0
                       Ω
                           1
                               6
Cycle:94
```

```
sample_pipeline.txt
                                        Page 74 of 157
Pre-Issue Buffer:
    Entry 0:
             [LW
                 R1, 268(R0)]
    Entry 1:
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
Entry 1:
             [SW
                 R1, 268(R0)]
Post_MEM Queue:
    Entry 0:
Registers
        5
R00:
    0
             Ω
                 Ω
                     Ω
                          1
                              -1
                                  Ω
R08:
    0
        0
             24
                 0
                     0
                          0
                              0
                                  0
R16:
    0
        0
             0
                 0
                     0
                          0
                              0
                                  0
R24:
    0
        0
             0
                 0
                     0
                          0
                              0
                                  0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
176:
    -1
             -3
                          3
                              0
        -2
                 1
                                  -1
208:
    -1
             -1
                     0
240:
    0
        0
             0
                     0
                          0
                              1
                                  6
Cycle:95
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [SW
                 R1, 268(R0)]
    Entry 1:
             [LW
                 R1, 268(R0)]
```

```
Page 75 of 157
sample_pipeline.txt
Post_MEM Queue:
    Entry 0:
Registers
         5
                                     0
R00:
    0
                       0
                                -1
         0
                                0
R08:
    0
              24
                       0
                                     0
R16:
    0
         0
              0
                  0
                       0
                           0
                                0
                                     0
R24:
              0
                  0
                                     0
    0
         0
                           0
                                0
Cache
Set 0: LRU=1
    Entry
Entry
1: [\,(1\,,0\,,4\,)\,<\,\bar{10}0011010101010100010000000011011100\,,\,100011000000010100000001000010000\,]
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Dat.a
                       2
                                Ω
176:
    -1
         - 2
             -3
                  1
                           3
                                     -1
             -1
                           0
                                     0
208:
    -1
         1
                  0
                       0
                                0
    0
         0
              0
                  0
                           0
                                     6
240:
                       0
                                1
Cycle:96
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
              [LW
                  R1, 268(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
         5
              Ω
                  Ω
                       Ω
                           1
                                -1
                                     Ω
    0
R08:
    0
         0
                           0
                                0
              24
                  0
                       0
                                     0
R16:
    0
         Ω
              0
                  0
                       0
                           0
                                Ω
                                     0
R24:
    0
         0
              0
                  0
                       0
                            0
                                0
                                     0
Cache
Set 0: LRU=1
    Entry
```

```
Page 76 of 157
sample_pipeline.txt
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   _ 1
      - 2
         -3
            1
                2
                   3
                      Λ
                          -1
208:
   -1
      1
         -1
             0
                0
                   0
                      0
                          0
240:
   0
      Ω
         Ω
            Ω
                0
                   0
                      1
                          6
Cycle:97
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
         [LW
            R1, 268(R0)]
Registers
R00:
   0
      5
         0
             0
                0
                   1
                      -1
                          0
R08:
   0
      0
         24
             0
                0
                   0
                      0
                          0
      0
         0
                          0
R16:
   0
                      0
R24:
   0
      0
         0
             0
                0
                   0
                      0
                          0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
0: [\,(1\,,0\,,4\,)\,<\,10001000000000000000000000100110\,,\,100000001000010100110000001000000\,]
   Entry
Set 3: LRU=0
```

```
sample_pipeline.txt
                                        Page 77 of 157
    Entry
0
176:
    -1
        -2
             -3
                                   -1
             -1
208:
    -1
240:
    0
        0
Cycle:98
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
                                   0
        0
R08:
    0
             24
                                   0
R16:
    0
             0
                 0
                          0
                              0
                                   0
        0
                      0
R24:
    0
        0
                                   0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
0: [\,(1\,,0\,,4\,)\,<\,10001000000000000000000000000100110\,,\,100000001000010100110000001000000\,>\,]
    Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        - 2
             -3
                 1
                      2
                          3
                              Ω
                                   -1
    -1
        1
             -1
208:
                 0
                      0
                          0
                              0
                                   0
    Ω
        Ω
240:
                      0
                              1
                                   6
Cycle:99
Pre-Issue Buffer:
    Entry 0:
             [SLL
                 R10, R1, #2]
    Entry 1:
             [LW
                 R3, 176(R10)]
    Entry 2:
```

```
sample_pipeline.txt
                                        Page 78 of 157
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        5
             Ω
R00:
                 Ω
                     Ω
                          1
                              -1
                                   Ω
    0
R08:
        0
                          0
                              0
    0
             24
                 0
                      0
                                   0
R16:
    0
        Ω
             0
                 0
                      0
                          0
                              Ω
                                   0
R24:
    0
        0
             0
                 0
                          0
                              0
                                   0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
             -3
                 1
                      2
                          3
                              0
                                   -1
208:
    -1
        1
             -1
                 0
                      0
                          0
                              0
                                   0
240:
    0
        0
             0
                      0
                                   6
Cycle:100
Pre-Issue Buffer:
    Entry 0:
             [LW
                 R3, 176(R10)]
                 R4, 220(R10)]
    Entry 1:
             [LW
    Entry 2:
             [LW
                 R5, 264(R0)]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
             [SLL
                 R10, R1, #2]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
        5
             0
                 0
                      0
                         1
                                   0
```

```
sample_pipeline.txt
                                     Page 79 of 157
R08:
    0
        0
            24
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
0: [\,(1,0,3)<\hat{10}00000000000000010101000010000000,10001101010000110000010110000>\,]
Data
176:
        -2
            -3
                1
                        3
                            0
    -1
                                -1
            -1
                                0
208:
    -1
                0
                    0
                            0
240:
    0
        0
            0
                    0
                        0
                                6
Cycle:101
Pre-Issue Buffer:
                R3, 176(R10)]
            [ LW
    Entry 0:
                R4, 220(R10)]
    Entry 1:
            [LW
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
            [SLL
                R10, R1, #2]
Pre_MEM Queue:
    Entry 0:
            [LW
                R5, 264(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        5
            0
                0
                    0
                        1
                                0
                            -1
R08:
        0
                            0
    0
            24
                0
                    0
                        0
                                0
R16:
    0
            0
                0
                        0
                            0
                                0
        0
                    0
R24:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
```

```
Page 80 of 157
sample_pipeline.txt
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Dat.a
176:
   -1
       -2
          -3
              1
                 2
                     3
                        Ω
                            -1
   -1
          -1
                 0
                     0
                            0
208:
       1
              Ω
                        0
240:
   Ω
       Ω
                 Ω
                     Ω
                        1
                            6
Cycle:102
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
          [LW
              R3, 176(R10)]
   Entry 1:
          [LW
              R4, 220(R10)]
Post_MEM Queue:
              R5, 264(R0)]
   Entry 0:
          [LW
Registers
       5
R00:
   0
          Ω
              Λ
                 Λ
                     1
                        -1
                            0
R08:
   0
       Ω
          20
              Ω
                 0
                     0
                        Ω
                            0
R16:
   0
       Ω
          Ω
              0
                 Ω
                     0
                        Ω
                            0
R24:
   0
       0
          0
              0
                 0
                     0
                        0
                            0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
0: [\,(1,0,3)<\hat{100000000000000000010101000010000000}\,,10001101010000110000010110000>\,]
   Entry
176:
   -1
       -2
          -3
              1
                 2
                     3
                            -1
```

```
sample_pipeline.txt
                                           Page 81 of 157
   -1
       1
208:
              -1
                       0
                            0
                                 0
                                      0
240:
    0
        0
              0
                                      6
Cycle:103
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
                  R3, 176(R10)]
    Entry 0:
              [LW
    Entry 1:
              [LW
                  R4, 220(R10)]
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         5
              0
                   0
                       0
                                      0
R08:
    0
         0
              20
                   0
                       0
                            0
                                 0
                                      0
R16:
              0
                   0
                                 0
    0
R24:
    0
         0
                                      0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
0: [\,(1\,,0\,,4\,)\,<\,10001000000000000000000000000100110\,,\,100000001000010100110000001000000\,>\,]
    Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
         -2
              -3
                   1
                       2
                            3
                                 -1
                                      -1
             -1
208:
    -1
         1
                   0
                       0
                            0
                                 0
                                      0
240:
    0
         0
                                      6
Cycle:104
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
```

```
sample_pipeline.txt
                                         Page 82 of 157
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [LW
                 R4, 220(R10)]
    Entry 1:
Post_MEM Queue:
                 R3, 176(R10)]
    Entry 0:
             [LW
Registers
             0
R00:
        5
                 0
                      0
                          1
                                   0
    0
                               -1
R08:
    0
        0
             2.0
                          0
                               0
                                   0
                 0
                      0
R16:
    0
                          0
                                   0
        0
             0
                 0
                      0
                               0
R24:
    0
                                   0
        0
             0
                 0
                      0
                          0
                               0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
             -3
                      2
                               -1
                                   -1
208:
    -1
        1
             -1
                 0
                      0
                          0
                               0
                                   0
    0
        0
240:
             0
                 0
                      0
                          0
                                   6
Cycle:105
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                 R4, 220(R10)]
             [LW
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        5
             Ω
                 3
                      0
                               -1
                                   0
                          0
                               0
R08:
    0
        0
             20
                 0
                      0
                                   0
R16:
    0
        0
             0
                 0
                      0
                          0
                               0
                                   0
R24:
    0
        0
             0
                 0
                      0
                          0
                               0
                                   0
Cache
```

```
Page 83 of 157
sample_pipeline.txt
Set 0: LRU=1
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
0: [\,(1\,,0\,,4\,)\,<\bar{10}001000000000000000000000000100110\,,10000000100001010011000000100000>\,]
   Entry
Set 3: LRU=1
   Entry
Entry
176:
   -1
          -3
                       -1
                           -1
208:
   -1
      1
          -1
             0
                 0
                    0
                       0
                           0
240:
   0
      0
Cycle:106
Pre-Issue Buffer:
          [SUB
             R6, R4, R5]
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
          [LW
             R4, 220(R10)]
Registers
R00:
      5
          0
             3
                 0
                           0
R08:
   0
      0
          20
                    0
                       0
                           0
                 0
R16:
   0
      0
          0
                 0
                    0
                       0
                           0
R24:
   0
      0
          0
             0
                 0
                    0
                           0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
```

```
Page 84 of 157
sample_pipeline.txt
Set 3: LRU=1
   Entry
Entry
Data
   -1
      -2
          -3
             1
                 2
                    3
                           -1
176:
                        -1
          -1
208:
   -1
      1
             0
                 0
                    0
                        0
                           0
   0
      0
240:
                           6
                        1
Cycle:107
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
          [SUB
             R6, R4, R5]
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
      5
R00:
          0
                 0
                           0
   0
             3
                    1
                        -1
                        Ω
R08:
   Ω
      Ω
          2.0
             Ω
                    Ω
                           Ω
                 0
          0
                        0
                           0
R16:
   0
      0
             0
                 0
                    0
R24:
   0
      0
          0
             0
                 0
                    0
                        0
                           0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
   -1
      -2
          -3
             1
                 2
                    3
                        -1
                           -1
   -1
      1
          -1
                        0
                           0
208:
             0
                 0
                    0
240:
   0
      0
          0
             0
                 0
                    0
                        1
                           6
Cycle:108
```

```
Page 85 of 157
sample_pipeline.txt
Pre-Issue Buffer:
    Entry 0:
            [SW
                 R6, 176(R10)]
    Entry 1:
            [ADDI
                R1, R1, #-1]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
            [SUB
                R6, R4, R5]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        5
            0
                     0
                              -1
                                  0
R08:
    Ω
        Ω
            20
                 Ω
                     0
                         Ω
                              Ω
                                  0
R16:
    0
        0
            0
                 0
                     0
                         0
                              0
                                  0
R24:
    0
        0
            0
                 0
                     0
                              0
                                  0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
208:
                                  0
    -1
240:
Cycle:109
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
                R1, R1, #-1]
            [ADDI
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
            [SW
                 R6, 176(R10)]
    Entry 1:
Post_MEM Queue:
```

```
sample_pipeline.txt
                                 Page 86 of 157
   Entry 0:
Registers
R00:
       5
                             0
R08:
   0
       0
           20
                             0
                  0
                     0
                         0
R16:
   0
       0
                  0
                     0
                         0
                             0
R24:
   0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
                  2
       -2
           -3
              1
                         -1
                             -1
   -1
           -1
                     Ω
208:
              Ω
                  Ω
                             Ω
       1
   0
       0
           0
              0
                  0
                             6
240:
Cycle:110
Pre-Issue Buffer:
              R1, 268(R0)]
   Entry 0:
           [SW
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
           [ADDI
   Entry 0:
              R1, R1, #-1]
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
       5
R00:
   0
           Ω
              3
                  Ω
                     1
                         -1
                             Ω
R08:
   Ω
       Ω
           2.0
              Ω
                     Ω
                         Ω
                             Ω
                  0
              0
                             0
R16:
   0
       0
           0
                  0
                     0
                         0
R24:
   0
       0
           0
              0
                  0
                     0
                         0
                             0
Cache
Set 0: LRU=0
   Entry
```

```
Page 87 of 157
sample_pipeline.txt
Set 1: LRU=1
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
      -2
          -3
             1
                2
                       -1
                          -1
      1
208:
   -1
         -1
             Ω
                Ω
                    Ω
                       Ω
                          Ω
240:
   0
      0
          0
             0
                0
                    0
                       1
                          6
Cycle:111
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
          [SW
             R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      4
          Ω
                0
                          0
R08:
   0
      0
          20
             0
                0
                    0
                       0
                          0
R16:
   0
      0
          0
             0
                0
                    0
                       0
                          0
R24:
                          0
      0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
0: [\,(1,0,3)\,<\,1000000000000000010101000010000000\,,\,100011010000011000000101100000\,>\,]
```

```
sample_pipeline.txt
                                  Page 88 of 157
Data
176:
           -3
208:
                   0
   -1
           -1
240:
Cycle:112
Pre-Issue Buffer:
               R1, 268(R0)]
   Entry 0:
Entry 1:
           [LW
   Entry 2:
Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
                   0
                          -1
                              0
R08:
   0
       0
           20
               0
                   0
                      0
                          0
                              0
R16:
   0
       0
           0
                   0
                      0
                          0
                              0
R24:
   0
                              0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
                   2
                      3
176:
   -1
       - 2
           -3
               1
                          - 1
                              -1
   -1
208:
       1
           -1
               Ω
                   Ω
                      Ω
                          Ω
                              Ω
   0
240:
       0
           0
               0
                   0
                      0
                              6
                          1
Cycle:113
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
```

```
sample_pipeline.txt
                                       Page 89 of 157
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
            [LW
                R1, 268(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        4
            0
                 3
                     0
                         1
                              -1
                                  0
R08:
    Ω
            2.0
                 Ω
                         Ω
                              Ω
                                  Ω
        0
                     0
R16:
    0
        0
            0
                 0
                     0
                         0
                              0
                                  0
R24:
    0
        0
            0
                 0
                     0
                         0
                              0
                                  0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
            -3
                 1
                     2
                         3
                              -1
                                  -1
208:
    -1
            -1
                 0
                     0
                         0
                              0
                                  0
240:
    0
                 0
                     0
                         0
Cycle:114
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
                 R1, 268(R0)]
    Entry 0:
            [LW
Registers
R00:
    0
            0
                     0
R08:
    0
        0
            20
```

```
sample_pipeline.txt
                                   Page 90 of 157
R16:
   0
       0
                           Ω
                               Ω
R24:
   0
       0
                               0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
0:[(1,0,4)<100001000110000000000000000001,10000001010011001100000100010>]
   Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
0: [\,(1,0,3)\,<\,100000000000000010101000010000000\,,\,1000110101000001100000010110000>\,]
Data
176:
    -1
                               -1
208:
    -1
           -1
                   0
                       0
                               0
   0
240:
Cvcle:115
Pre-Issue Buffer:
   Entry 0:
Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
                   0
                           -1
                               0
   0
R08:
   0
       0
           20
               0
                   0
                       0
                           0
                               0
R16:
   0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
   0
       0
           0
                       0
                               0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
```

```
Page 91 of 157
sample_pipeline.txt
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
       - 2
           -3
              1
                  2
                      3
                         -1
                             -1
           -1
                         Ω
208:
   -1
              Ω
                  Ω
                      Ω
                             Ω
       1
   0
       0
           0
240:
              0
                  0
                      0
                         1
                             6
Cycle:116
Pre-Issue Buffer:
   Entry 0:
           [SLL
              R10, R1, #2]
   Entry 1:
           [LW
              R3, 176(R10)]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
       4
           Ω
              3
                             Ω
R00:
   0
                  0
                      1
                         -1
R08:
   0
       Λ
           20
              0
                  0
                      0
                         Ω
                             0
R16:
   0
       0
           0
              Ω
                  0
                      0
                         Ω
                             0
R24:
   0
       0
           Ω
              Ω
                  Ω
                      Ω
                             0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Set 3: LRU=1
   Entry
0: [\,(1\,,0\,,3\,)<100000000000000010101000010000000\,,10001101010000110000010110000>]
Data
176:
   -1
208:
   -1
       1
                         Ω
                             Ω
```

```
sample_pipeline.txt
                                      Page 92 of 157
240: 0 0
                        0 1
            0
                   0
Cycle:117
Pre-Issue Buffer:
                R3, 176(R10)]
    Entry 0:
            [LW
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
Entry 1:
            [SLL
                R10, R1, #2]
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
                    0
                                 0
R08:
    0
        0
            20
                0
                        0
                             0
                                 0
R16:
    0
        0
            0
                0
                    0
                        0
                             0
                                 0
R24:
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Data
176:
    -1
            -3
                             -1
                                 -1
            -1
208:
    -1
                0
                    0
                        0
       0
    0
            0
240:
                0
                    0
                                 6
Cycle:118
Pre-Issue Buffer:
            [LW
                R3, 176(R10)]
    Entry 0:
    Entry 1:
            [LW
                R4, 220(R10)]
    Entry 2:
            [LW
                R5, 264(R0)]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
            [SLL
               R10, R1, #2]
```

```
sample_pipeline.txt
                                               Page 93 of 157
Pre_MEM Queue:
     Entry 0:
     Entry 1:
Post_MEM Queue:
     Entry 0:
Registers
R00:
          4
                    3
                         0
                                   -1
                                        0
     0
R08:
     0
          0
               20
                    0
                         0
                              0
                                   0
                                        0
R16:
     0
          0
               0
                    0
                              0
                                   0
                                        0
                         0
R24:
     0
               0
                    0
                              0
                                        0
          0
Cache
Set 0: LRU=1
     Entry
0: [\,(1\,,0\,,4\,)\,<\,\hat{1000110101000100000000011011100}\,,\,1000110000000101000000010000010000\}
     Entry
Set 1: LRU=0
     Entry
Entry
Set 2: LRU=1
     Entry
Entry
Set 3: LRU=1
     Entry
Entry
Data
     -1
               -3
                    1
                         2
                              -1
176:
          - 2
                                   - 1
                                        -1
208:
     -1
          1
               -1
                    0
                         0
                              0
                                   0
                                        0
240:
     0
          0
               0
                         0
                                        6
Cycle:119
Pre-Issue Buffer:
     Entry 0:
               [LW
                    R5, 264(R0)]
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
     Entry 0:
Pre_MEM Queue:
                    R3, 176(R10)]
     Entry 0:
Entry 1:
               [LW
               [LW
                    R4, 220(R10)]
Post_MEM Queue:
     Entry 0:
Registers
R00:
     0
          4
               0
                    3
                         0
                              1
                                   -1
                                        0
R08:
     0
          0
               16
                    0
                         0
                              0
                                   Ω
                                        0
R16:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
R24:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
Cache
Set 0: LRU=1
```

```
Page 94 of 157
sample_pipeline.txt
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
0: [\,(1,0,3)\,<\,100000000000000010101000010000000\,,\,1000110101000001100000010110000>\,]
   Entry
Data
176:
   -1
                         0
208:
   -1
              0
                  0
                             0
240:
   0
       Ω
                  Ω
                             6
Cycle:120
Pre-Issue Buffer:
   Entry 0:
           [LW
              R5, 264(R0)]
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
              R3, 176(R10)]
   Entry 0:
           [LW
   Entry 1:
           [LW
              R4, 220(R10)]
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       4
           0
                  0
                             0
R08:
   0
       0
          16
                     0
                         0
                             0
              0
                  0
   0
              0
                         0
                             0
R16:
       0
           0
                  0
                     0
R24:
   0
Cache
Set 0: LRU=1
   Entry
0: [\,(1\,,0\,,4)\,<\bar{10}001101010101000100000000011011100\,,1000110000000101000000100000100000]
   Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
```

```
Page 95 of 157
sample_pipeline.txt
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
            -3
                          -1
                              -1
                                  -1
208:
    -1
                 0
                     0
                         0
                              0
                                  0
            -1
240:
    0
        0
Cycle:121
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
            [LW
                 R4, 220(R10)]
    Entry 1:
            [LW
                 R5, 264(R0)]
Post_MEM Queue:
    Entry 0:
            [LW
                 R3, 176(R10)]
Registers
R00:
    0
        4
            0
                 3
                     0
                              -1
                                  0
R08:
    0
            16
                 0
                         0
                              0
        0
                     0
                                  0
R16:
    0
            Ω
                 Ω
                         Ω
                                  Ω
        0
                     0
                              Ω
            0
R24:
    0
        0
                     0
                         0
                                  0
Cache
Set 0: LRU=0
    Entry
0: [\ (1\,,0\,,4\,)\,<\,\bar{10}0011010101000100000000011011100\,,1000110000000101000000010000010000>\,]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Data
176:
    -1
        -2
            -3
                 1
                     2
                         -1
                              -1
                                  -1
208:
    -1
        1
            -1
                 Ω
                     0
                         Ω
                              Ω
                                  Ω
    Ω
240:
        Ω
Cycle:122
Pre-Issue Buffer:
```

```
Page 96 of 157
sample_pipeline.txt
      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
                        R4, 220(R10)]
R5, 264(R0)]
     Entry 0:
Entry 1:
                  [LW
                  [LW
Post_MEM Queue:
      Entry 0:
Registers
R00:
      0
            4
                  0
                        2
                              0
                                          -1
                                                 0
R08:
      0
            0
                  16
                        0
                              0
                                    0
                                          0
                                                 0
R16:
      0
            Ω
                  0
                        Ω
                              0
                                    0
                                          Ω
                                                 0
R24:
      0
            0
                  0
                        0
                              0
                                    0
                                           0
                                                 0
Cache
Set 0: LRU=0
      Entry
0: [\,(1\,,0\,,4\,)\,<\bar{10}001101010001000000000011011100\,,100011000000010100000001000010000]
      Entry
Set 1: LRU=1
      Entry
Entry
Set 2: LRU=1
      Entry
Entry
1: [\,(1,0,4)<1000100000000000000000000000100110\,,100000001000010100110000001000000>]
Set 3: LRU=1
      Entry
0: [\,(1,0,3)\,<\,1000000000000000010101000010000000\,,\,100011010000011000000101100000\,>\,]
      Entry
Data
176:
      -1
                  -3
                                     -1
208:
      -1
                              0
240:
      0
           0
                              0
                                                 6
Cycle:123
Pre-Issue Buffer:
      Entry 0:
                  [SUB
                       R6, R4, R5]
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:
                  [LW
                        R5, 264(R0)]
      Entry 1:
Post_MEM Queue:
      Entry 0:
                  [LW
                        R4, 220(R10)]
```

```
sample_pipeline.txt
                                        Page 97 of 157
Registers
R00:
    0
        4
             0
                 2
                      0
                                   0
R08:
    0
        0
             16
                          0
                              0
                                   0
R16:
    0
                 0
                              0
                                   0
        0
             0
                      0
                          0
R24:
    0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
             -3
                 1
                          -1
                              -1
                                   -1
                          0
                              0
208:
    -1
             -1
                 0
                      0
                                   0
        1
    0
             0
        Ω
                 Ω
240:
                      Ω
Cycle:124
Pre-Issue Buffer:
    Entry 0:
Entry 1:
             [SUB
                 R6, R4, R5]
             [SW
                 R6, 176(R10)]
    Entry 2:
             [ADDI
                 R1, R1, #-1]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                 R5, 264(R0)]
             [LW
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        4
             0
                 2
                      0
                          1
                              -1
                                   0
R08:
    Ω
        Ω
             16
                 Ω
                      0
                          Ω
                              Ω
                                   0
R16:
    Ω
                 Ω
                          Ω
                                   Ω
        Ω
             Ω
                      0
                              Ω
R24:
                 0
                                   0
    0
        0
             0
                      0
                          0
                              0
Cache
Set 0: LRU=0
    Entry
0: [\,(1\,,0\,,4\,)\,<\bar{10}001101010001000000000011011100\,,100011000000010100000001000010000]
    Entry
Set 1: LRU=1
```

```
Page 98 of 157
sample_pipeline.txt
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
0: [\,(1\,,0\,,3\,)\,<\bar{10}0000000000000010101000010000000\,,100011010100001100000010110000>\,]
    Entry
Data
176:
    -1
       -2
           -3
               1
                   2
                       -1
                           -1
                               -1
208:
    -1
       1
           -1
               0
                   0
                       0
                           0
                               0
240:
    Ω
       Λ
                               4
Cycle:125
Pre-Issue Buffer:
    Entry 0:
           [SUB
               R6, R4, R5]
               R6, 176(R10)]
    Entry 1:
           [SW
    Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
           [ADDI
              R1, R1, #-1]
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
           [LW
               R5, 264(R0)]
Registers
R00:
   0
       4
           0
               2
                   0
                       1
                           -1
                               0
R08:
    0
       Ω
           16
               Ω
                   0
                       0
                           Ω
                               0
R16:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
    0
       0
           0
                   0
                       0
                           Ω
                               0
Cache
Set 0: LRU=0
   Entry
0: [\,(1\,,0\,,4\,)\,<\,\hat{10}\,001101010101000100000000011011100\,,\,100011000000010100000001000010000]
   Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
```

```
sample_pipeline.txt
                                        Page 99 of 157
Data
176:
    -1
        -2
             -3
                          -1
                                   -1
    -1
208:
240:
    0
        0
Cycle:126
Pre-Issue Buffer:
    Entry 0:
             [SW
                 R6, 176(R10)]
    Entry 1:
Entry 2:
                 R1, 268(R0)]
             [SW
    Entry 3:
Pre_ALU Queue:
             SUB
                 R6, R4, R5]
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
             [ADDI
                 R1, R1, #-1]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
             0
                      0
                              -1
                                   0
R08:
    0
        0
             16
                 0
                      0
                          0
                              0
                                   0
R16:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
R24:
    0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
             -3
                 1
                      2
                          -1
                              -1
                                   -1
                          Ω
                              Ω
208:
    -1
        1
             -1
                 Ω
                      Ω
                                   Ω
    0
240:
Cycle:127
Pre-Issue Buffer:
                 R6, 176(R10)]
    Entry 0:
             [SW
    Entry 1:
             [SW
                 R1, 268(R0)]
    Entry 2:
             [LW
                 R1, 268(R0)]
    Entry 3:
Pre_ALU Queue:
```

```
Page 100 of 157
sample_pipeline.txt
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
             [SUB
                 R6, R4, R5]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        3
                                   0
R00:
             0
                      0
    0
                               -1
R08:
    0
        0
             16
                 Ω
                      0
                          0
                               0
                                   0
    Ω
                 Ω
                                   Ω
R16:
        Ω
             Ω
                      Ω
                          Ω
                               Ω
R24:
    0
        0
             0
                 0
                      0
                          0
                               0
                                   0
Cache
Set 0: LRU=1
    Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
             -3
                 1
                      2
                          -1
                               -1
                                   -1
208:
    -1
        1
             -1
                 0
                      0
                          0
                               0
                                   0
240:
    0
        0
             0
                 0
                      0
                          0
                                   4
Cycle:128
Pre-Issue Buffer:
             [SW
                 R1, 268(R0)]
    Entry 0:
    Entry 1:
                 R1, 268(R0)]
             [LW
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
                 R6, 176(R10)]
    Entry 0:
             [SW
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        3
             0
                 2
                      0
                          1
                               -1
                                   0
R08:
    0
        0
             16
                 0
                      0
                          0
                               0
                                   0
R16:
    0
        0
                                   0
```

```
sample_pipeline.txt
                            Page 101 of 157
     0
R24:
  0
         0
               Ω
                  Ω
                      Ω
                         Ω
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
      -2
         -3
            1
               2
                   -1
                      -1
                         -1
208:
   -1
         -1
            0
               0
                   0
                      0
                         0
240:
   0
      0
         0
               0
Cycle:129
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
         [SW
            R1, 268(R0)]
   Entry 1:
            R1, 268(R0)]
         [LW
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      3
         0
            2
               0
                      -1
                         0
R08:
   0
      0
         16
            0
                   0
                      0
                         0
               0
R16:
   0
      0
         0
            0
               0
                   0
                      0
                         0
R24:
   0
      0
         0
                         0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
```

```
Page 102 of 157
sample_pipeline.txt
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
               2
176:
   -1
      -2
         -3
            1
                   -1
                      -1
                         -1
208:
   -1
         -1
            Ω
               0
                  0
                      0
                         0
      1
   Ω
240:
Cycle:130
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
         [LW
            R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
      3
         0
               0
                      -1
                         0
   0
            2
                  1
R08:
         16
                  Ω
                      Ω
   0
      Ω
            Ω
               0
                         0
R16:
   0
      Ω
         0
            0
               0
                  0
                      Ω
                         0
R24:
   0
                  Ω
                      Ω
                         Ω
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
      -2
         -3
            1
               2
                   -1
                      -1
                         -1
208:
   -1
            0
               0
                   0
                      0
                         0
240:
   Ω
      Ω
```

```
Page 103 of 157
sample_pipeline.txt
Cycle:131
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
   Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
            [LW
                R1, 268(R0)]
Registers
R00:
    0
        3
            Ω
                2
                    0
                        1
                            -1
                                0
R08:
    0
        0
            16
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
        0
            0
                Ω
                    0
                        0
                            Ω
                                0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
            -3
                1
                        -1
                            -1
                                -1
208:
    -1
            -1
   0
240:
Cvcle:132
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
```

```
Page 104 of 157
sample_pipeline.txt
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        3
                              -1
                                  0
R08:
    0
        0
            16
                 0
                         0
                              0
                                  0
                     0
R16:
    0
            0
                 0
                         0
                              0
                                  0
        0
                     0
            0
                                  0
R24:
    0
        0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
            -3
                 1
                     2
                         -1
                              -1
                                  -1
        1
                         Ω
208:
            -1
                 0
                     Ω
                              Ω
                                  Ω
    -1
240:
    0
        0
                 0
                     0
                         0
                              1
                                  4
Cycle:133
Pre-Issue Buffer:
    Entry 0:
            [SLL
                 R10, R1, #2]
    Entry 1:
            [LW
                 R3, 176(R10)]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        3
R00:
    0
            Ω
                     Ω
                         1
                              -1
                                  0
R08:
    0
        0
            16
                 0
                     0
                         0
                              0
                                  0
R16:
    0
        Ω
            0
                 0
                     0
                         0
                              Ω
                                  0
R24:
    0
        0
            0
                         0
                              0
                                  0
Cache
Set 0: LRU=0
    Entry
```

```
Page 105 of 157
sample_pipeline.txt
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
0: \hbox{\tt [(1,0,3)<1000000000000000010101000010000000,10001101010000110000010110000>]}
   Entry
Data
176:
   -1
       -2
           -3
              1
                  2
                      -1
                         -1
                             -1
208:
   -1
           -1
              0
                  0
                      0
                          0
                             0
240:
   0
       0
           0
                             4
Cycle:134
Pre-Issue Buffer:
           [LW
              R3, 176(R10)]
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
              R10, R1, #2]
           [SLL
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
R08:
   0
       0
           16
                      0
                          0
                             0
R16:
   0
       0
           0
              0
                         0
                             0
                             0
R24:
   0
       0
                          0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
1: [\,(1\,,0\,,4\,)\,<\,10001000000000000000000000000100110\,,\,100000001000010100110000001000000>\,]
Set 3: LRU=1
```

```
Page 106 of 157
sample_pipeline.txt
    Entry
Entry
Data
176:
    -1
           -3
               1
                   2
                       -1
                           -1
                               -1
208:
    -1
           -1
               0
                   0
                       0
                           0
                               0
       1
240:
   0
       0
Cvcle:135
Pre-Issue Buffer:
           [T.W
               R3, 176(R10)]
   Entry 0:
               R4, 220(R10)]
R5, 264(R0)]
   Entry 1:
           [ LW
   Entry 2:
           [LW
    Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
           [SLL
               R10, R1, #2]
Pre_MEM Queue:
    Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       3
           0
               2
                   0
                               0
                       1
                           -1
R08:
    0
       0
           16
               0
                   0
                       0
                           0
                               0
R16:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
   0
           Ω
               Ω
                               Ω
       Ω
                   0
                       Ω
                           0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
                   2
176:
    -1
       -2
           -3
               1
                       -1
                           -1
                               -1
208:
    -1
       1
           -1
               0
                   0
                       0
                           0
                               0
240:
    Ω
       Ω
           Ω
               Ω
                   Ω
                       Ω
                               4
Cycle:136
Pre-Issue Buffer:
   Entry 0:
           [LW
               R5, 264(R0)]
```

```
Page 107 of 157
sample_pipeline.txt
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
     Entry 0:
Pre_MEM Queue:
     Entry 0:
                [LW
                     R3, 176(R10)]
                     R4, 220(R10)]
     Entry 1:
                ſLW
Post_MEM Queue:
     Entry 0:
Registers
          3
R00:
     0
                Ω
                     2
                           Ω
                                1
                                     -1
                                           Ω
R08:
     0
          0
                12
                     0
                           0
                                0
                                     0
                                           0
R16:
     0
          0
                0
                     0
                           0
                                0
                                     0
                                           0
R24:
     0
          Ω
                Ω
                     Ω
                           Ω
                                Ω
                                     Ω
                                           Ω
Cache
Set 0: LRU=1
     Entry
0: [\,(1\,,0\,,4\,)\,<\,\hat{10}\,001101010101000100000000011011100\,,\,1000110000000101000000010000100000]
     Entry
Set 1: LRU=1
     Entry
0:[(1,0,4)<100001000110000000000000000001,10000001010011001100000100010>]
     Entry
Set 2: LRU=1
     Entry
Entry
Set 3: LRU=1
     Entry
Entry
176:
                -3
                                -1
                                     -1
                                           -1
208:
     -1
                -1
                     0
                           0
                                0
                                     0
                                           0
240:
     0
          0
Cycle:137
Pre-Issue Buffer:
                [LW
                     R5, 264(R0)]
     Entry 0:
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
     Entry 0:
Pre_MEM Queue:
                     R3, 176(R10)]
     Entry 0:
                [LW
     Entry 1:
                [LW
                     R4, 220(R10)]
Post_MEM Queue:
     Entry 0:
```

```
Page 108 of 157
sample_pipeline.txt
Registers
R00:
     0
         3
              Ω
                   2
                        0
                             1
                                  -1
                                       0
R08:
     0
         0
              12
                   0
                        0
                             0
                                  0
                                       0
R16:
         0
              0
                                  0
                                       0
R24:
         0
                                  0
                                       0
     0
Cache
Set 0: LRU=1
    Entry
0: [\,(1\,,0\,,4\,)\,<\bar{10}0011010101010100010000000011011100\,,100011000000010100000010000100000]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
1: [\,(1\,,0\,,4\,)\,<\,10001000000000000000000000000100110\,,\,100000001000010100110000001000000>\,]
Set 3: LRU=1
    Entry
Entry
Data
176:
     -1
         -2
              -3
                   1
                        2
                             -1
                                  -1
                                       -1
208:
     -1
         1
              -1
                   0
                        0
                             0
                                  0
                                       0
    0
              0
         0
                        0
                             0
                                       4
240:
                                  1
Cvcle:138
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
     Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
     Entry 0:
               [LW
                   R4, 220(R10)]
    Entry 1:
                   R5, 264(R0)]
              [LW
Post_MEM Queue:
    Entry 0:
              [LW
                   R3, 176(R10)]
Registers
R00:
         3
              0
                   2
                        0
                             1
                                       0
    0
                                  -1
R08:
     0
         0
              12
                   0
                        0
                             0
                                  0
                                       0
R16:
     0
         Ω
              Ω
                   Ω
                        0
                             Ω
                                  Ω
                                       0
R24:
    0
              Ω
                        Ω
                                       Ω
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
```

```
Page 109 of 157
sample_pipeline.txt
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
0: [\,(1,0,3)<\hat{100000000000000000010101000010000000}\,,10001101010000110000010110000>\,]
    Entry
Dat.a
176:
    -1
        -2
            -3
                 1
                     2
                         -1
                              -1
                                  -1
208:
    -1
        1
            -1
                 0
                     0
                         0
                              0
                                  0
240:
    0
        0
            0
                 0
                     0
                         0
                              1
                                  4
Cycle:139
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                R4, 220(R10)]
            M.T l
                R5, 264(R0)]
    Entry 1:
            ſLW
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        3
            Ω
                 1
                     Ω
                         1
                              -1
                                  Ω
R08:
    0
        0
            12
                 0
                     0
                         0
                             0
                                  0
R16:
    0
        Ω
            0
                 0
                     0
                         0
                              Ω
                                  0
R24:
    0
        0
            0
                 0
                     0
                         0
                              0
                                  0
Cache
Set 0: LRU=1
    Entry
0: [\,(1\,,0\,,4\,)\,<\,100011010101010100010000000011011100\,,\,1000110000000101000000010000010000>\,]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
0: [\,(1,0,3)\,<\,1000000000000000010101000010000000\,,\,100011010000011000000101100000\,>\,]
    Entry
```

```
sample_pipeline.txt
                                            Page 110 of 157
Data
176:
     -1
         -2
              -3
                   1
                        2
                             -1
                                  -1
                                       -1
208:
     -1
              -1
                   0
                        0
                             0
                                  0
                                       0
240:
     0
         0
Cycle:140
Pre-Issue Buffer:
    Entry 0:
Entry 1:
              [SUB
                   R6, R4, R5]
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
              [LW
                   R5, 264(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
              [LW
                   R4, 220(R10)]
Registers
R00: 0
              0
                        0
R08:
     0
         0
              12
                        0
                             0
                                  0
                                       0
R16:
    0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R24:
    0
         0
              0
                        0
                             0
                                       0
Cache
Set 0: LRU=1
    Entry
0: [\,(1,0,4)<\hat{1000110101000100000000011011100}\,,1000110000000101000000010000010000>\,]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
     -1
         -2
              -3
                   1
                        2
                             -1
                                  -1
                                       -1
     -1
              -1
208:
         1
                   0
                        0
                             0
                                  0
                                       0
    0
240:
         Ο
              Ω
                        Ω
                             Ω
                                       3
                                  1
Cycle:141
Pre-Issue Buffer:
     Entry 0:
              [SUB
                  R6, R4, R5]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
```

```
sample_pipeline.txt
                                         Page 111 of 157
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
             [LW
                  R5, 264(R0)]
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
         3
             0
R00:
                  1
                      0
                           1
                                    0
    0
                                -1
R08:
             12
                                0
    0
         0
                  0
                           0
                                    0
                      0
R16:
    0
         0
             0
                  0
                      0
                           0
                                0
                                    0
    Ω
             Ω
                                    Ω
R24:
         0
                  0
                      0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
         -2
             -3
                  1
                      2
                           -1
                                -1
                                    -1
208:
    -1
         1
             -1
                  0
                      0
                           0
                                0
                                    0
240:
    0
         Ω
             0
                  Ω
                      0
                           0
                                1
                                    3
Cycle:142
Pre-Issue Buffer:
    Entry 0:
             [SUB
                  R6, R4, R5]
                  R6, 176(R10)]
    Entry 1:
             [SW
    Entry 2:
                  R1, R1, #-1]
             [ADDI
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
             [LW
                  R5, 264(R0)]
Registers
R00:
    0
         3
             0
                  1
                      0
                           1
                                -1
                                    0
R08:
    0
         0
             12
                  0
                      0
                           0
                                0
                                    0
R16:
    0
         0
             0
                  0
                      0
                           0
                                0
                                    0
R24:
    0
         0
             0
                  0
                      0
                                    0
```

```
Page 112 of 157
sample_pipeline.txt
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
1: [\,(1,0,4)<1000100000000000000000000000100110\,,10000000100001010011000000100000>]
Set 3: LRU=1
   Entry
Entry
176:
          -3
                    -1
                           -1
208:
   -1
          -1
             0
                 0
                        0
240:
   0
      0
Cycle:143
Pre-Issue Buffer:
          [SW
             R6, 176(R10)]
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
          [SUB
             R6, R4, R5]
   Entry 1:
          [ADDI
             R1, R1, #-1]
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
      3
R00:
   0
R08:
   0
      0
          12
             0
                 0
                    0
                        0
                           0
R16:
          0
                        0
                           0
   0
      0
                 0
                    0
R24:
   0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
```

```
Page 113 of 157
sample_pipeline.txt
Entry
Set 3: LRU=1
   Entry
Entry
Dat.a
                   2
   -1
       -2
           -3
                       -1
176:
               1
                           -1
                               -1
   -1
           -1
                       0
                           0
208:
               0
                   0
                               0
       1
   0
240:
       0
           0
               0
                   0
                       0
                               3
                           1
Cycle:144
Pre-Issue Buffer:
   Entry 0:
           [SW
               R6, 176(R10)]
   Entry 1:
           [SW
               R1, 268(R0)]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
           [ADDI
               R1, R1, #-1]
   Entry 1:
Post_ALU Queue:
   Entry 0:
           [SUB
               R6, R4, R5]
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
       3
           0
               1
                   0
                               0
R00:
   0
                       1
                           -1
R08:
                           0
   0
       0
           12
               0
                   0
                       0
                               0
R16:
   0
       Ω
           Ω
               Ω
                   0
                       Ω
                           Ω
                               0
R24:
   0
       0
           0
               0
                   0
                       0
                           0
                               0
Cache
Set 0: LRU=0
   Entry
0: [\ (1,0,4) < 10001101010001000000000011011100 \ , 1000110000000101010000000100000100000]
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
   -1
       -2
           -3
               1
                   -1
                       -1
                           -1
                               -1
208:
   -1
       1
           -1
               0
                   0
                       0
                           0
                               0
240:
   0
       0
           0
               0
                   0
                       0
```

```
sample_pipeline.txt
                                           Page 114 of 157
Cycle:145
Pre-Issue Buffer:
                 R1, 268(R0)]
R1, 268(R0)]
              [SW
    Entry 0:
    Entry 1:
              [LW
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
              [ADDI R1, R1, #-1]
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                  R6, 176(R10)]
              [SW
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
   0
         3
              0
                   1
                        0
                                 -1
                                      0
R08:
    0
         0
              12
                   0
                       0
                            0
                                 0
                                      0
R16:
    0
         0
              0
                   0
                        0
                            0
                                 0
                                      0
R24:
    0
         0
                                      0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
1: [\,(1,0,4)<1000100000000000000000000000100110\,,10000000100001010011000000100000>]
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
              -3
                       -1
                            -1
                                      -1
         1
              -1
208:
    -1
                   0
                        0
                            0
                                 0
                                      0
    0
240:
Cycle:146
Pre-Issue Buffer:
    Entry 0:
Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [SW R1, 268(R0)]
```

```
sample_pipeline.txt
                                    Page 115 of 157
   Entry 1:
           [LW
               R1, 268(R0)]
Post_MEM Queue:
   Entry 0:
Registers
       2
R00:
    0
                   0
R08:
    0
       0
           12
               0
                   0
                       0
                           0
                               0
R16:
           0
               0
                           0
                               0
    0
       0
                   0
                       0
R24:
   0
                               0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
    -1
       -2
           -3
               1
                       -1
                           -1
176:
                   -1
                               -1
208:
    -1
           -1
               0
                   0
                       0
                           0
                               0
       1
    Ω
       Ω
           Ω
                   Ω
                       Ω
                               3
240:
               Ω
                           1
Cycle:147
Pre-Issue Buffer:
   Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [LW
               R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
   0
       2
           0
               1
                   0
                               0
R00:
                       1
                           -1
R08:
    0
       Ω
           12
               0
                   0
                       Ω
                           Ω
                               0
R16:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
    0
       Ω
           Ω
               Ω
                   0
                       Ω
                               0
Cache
Set 0: LRU=0
```

```
Page 116 of 157
sample_pipeline.txt
  Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
176:
  -1
     -2
        -3
           1
              -1
                 -1
                    -1
                       -1
208:
  -1
     1
        -1
           0
              0
                 0
                    0
                       0
240:
  0
     0
        0
           0
              0
                 0
                       3
Cycle:148
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
        [LW
           R1, 268(R0)]
Registers
R00:
  0
     2
        0
           1
              0
                 1
                    -1
                       0
R08:
  0
     0
        12
                    0
                       0
R16:
  0
     0
        0
           0
              0
                 0
                    0
                       0
R24:
  0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
```

```
Page 117 of 157
sample_pipeline.txt
Entry
Data
176:
    -1
            -3
                    -1
                        -1
208:
    -1
            -1
                            0
240:
    0
        0
                            1
                                3
Cvcle:149
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        2
R00:
    0
                             -1
                                 0
R08:
    0
        0
            12
                0
                    0
                        0
                            0
                                 0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                 0
                        0
                                 0
R24:
    0
        0
            0
                0
                    0
                            0
Cache
Set 0: LRU=0
    Entry
0: [\ (1\,,0\,,4\,)<\bar{1000110101010100010000000011011100}\,,1000110000000101000000010000010000>]
    Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
            -3
                1
                        -1
                            -1
        - 2
                    -1
                                 -1
208:
    -1
        1
            -1
                Ω
                    Ω
                        Ω
                            0
                                 Ω
240:
    0
        0
            0
                0
                    0
                        0
                            1
                                 3
Cycle:150
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
```

```
sample_pipeline.txt
                                     Page 118 of 157
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
        2
            0
                1
                                 0
R00:
    0
                    0
                            -1
R08:
    0
        0
            12
                0
                    0
                        0
                            Ω
                                 0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                 0
R24:
    0
        0
            0
                                 0
Cache
Set 0: LRU=0
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
            -3
                1
                    -1
                        -1
                            -1
                                -1
                            0
208:
    -1
            -1
                    0
                                 0
240:
    0
        0
            0
                    0
                        0
                                 3
Cycle:151
Pre-Issue Buffer:
            [SLL
    Entry 0:
                R10, R1, #2]
                R3, 176(R10)]
    Entry 1:
            [LW
    Entry 2:
    Entry 3:
Pre_ALU Queue:
   Entry 0:
Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
```

```
sample_pipeline.txt
                                    Page 119 of 157
R00:
   0
        2
            Ω
                1
                    0
                                0
R08:
    0
        0
           12
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
        0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
0: [\ (1,0,3)<\bar{1000000000000000001011000010000000},100011010000110000010110000>]
   Entry
Data
176:
    -1
            -3
                    -1
                        -1
                            -1
                                -1
208:
    -1
            -1
                0
                    0
                        0
                            0
                                0
       1
240:
   0
       0
            0
                0
                    0
Cvcle:152
Pre-Issue Buffer:
            [LW
               R3, 176(R10)]
   Entry 0:
    Entry 1:
            [LW
               R4, 220(R10)]
    Entry 2:
            [LW
               R5, 264(R0)]
   Entry 3:
Pre_ALU Queue:
   Entry 0:
           [SLL
               R10, R1, #2]
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
        2
    0
            0
                1
                    0
                        1
                            -1
                                0
R08:
    0
        0
            12
                0
                        0
                            0
                                0
                    0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
    Ω
        0
            Ω
                                Ω
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
```

```
Page 120 of 157
sample_pipeline.txt
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
          -3
              1
176:
   -1
       - 2
                 -1
                     -1
                        -1
                            -1
208:
   -1
       1
          -1
              Ω
                 Ω
                     Ω
                        Ω
                            Ω
240:
   0
       0
          0
                     0
                            3
Cycle:153
Pre-Issue Buffer:
          [LW
              R3, 176(R10)]
   Entry 0:
   Entry 1:
          [LW
              R4, 220(R10)]
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
          [SLL
              R10, R1, #2]
   Entry 0:
Pre_MEM Queue:
   Entry 0:
              R5, 264(R0)]
          [ LW
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       2
          Ω
              1
                 Ω
                     1
                        -1
                            0
R08:
   0
       Ω
          12
              0
                 0
                     Ω
                        Ω
                            0
R16:
   0
       0
          0
              0
                 0
                     0
                        0
                            0
R24:
   0
       Ω
          0
              Ω
                 0
                     0
                        Ω
                            0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
0: [\,(1,0,3)\,<\,1000000000000000010101000010000000\,,\,100011010000011000000101100000\,>\,]
   Entry
Data
```

```
sample_pipeline.txt
                                            Page 121 of 157
    -1
176:
         -2
              -3
                        -1
                             -1
                                       -1
         1
                                  0
208:
     -1
              -1
                   0
                        0
                             0
                                       0
240:
     0
         0
                        0
                             0
                                  1
                                       3
Cycle:154
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
     Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
                   R3, 176(R10)]
     Entry 0:
              [LW
    Entry 1:
              [LW
                   R4, 220(R10)]
Post_MEM Queue:
    Entry 0:
              [LW
                   R5, 264(R0)]
Registers
R00:
     0
         2
              0
                        0
                                  -1
                                       0
R08:
     0
         0
              8
                   0
                        0
                                  0
                                       0
R16:
     0
         0
              0
                   0
                        0
                             0
                                  0
                                       0
R24:
    0
              0
                        0
                                       0
Cache
Set 0: LRU=1
    Entry
0: [\,(1\,,0\,,4\,)\,<\,100011010101010100010000000011011100\,,\,1000110000000101000000010000010000>\,]
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
     -1
              -3
                             -1
                                  -1
          -2
                   1
                        -1
                                       -1
208:
     -1
         1
              -1
                   0
                        0
                             0
                                  0
                                       0
     0
              0
240:
         0
                   0
                        0
                             0
                                  1
                                       3
Cvcle:155
Pre-Issue Buffer:
     Entry 0:
     Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
     Entry 0:
    Entry 1:
```

```
Page 122 of 157
sample_pipeline.txt
Post_ALU Queue:
     Entry 0:
Pre_MEM Queue:
     Entry 0:
               [LW
                    R4, 220(R10)]
     Entry 1:
Post_MEM Queue:
    Entry 0:
               [LW
                    R3, 176(R10)]
Registers
R00:
          2
               0
                    1
                         0
                                        0
     0
                              1
                                   -1
R08:
                              0
                                   0
     0
          0
                    0
               8
                         0
                                        0
R16:
                    0
                                        0
     0
          0
               0
                         0
                              0
                                   0
R24:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
Cache
Set 0: LRU=1
     Entry
Entry
Set 1: LRU=1
     Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
0: [\,(1,0,3)<\hat{10000000000000000010101000010000000}\,,10001101010000110000010110000>\,]
     Entry
Data
176:
     -1
          -2
               -3
                    1
                         -1
                              -1
                                   -1
                                        -1
               -1
                         Ω
                              Ω
208:
     -1
          1
                    Ω
                                   0
                                        Ω
240:
     0
          0
               0
                    0
                         0
                              0
                                   1
                                        3
Cycle:156
Pre-Issue Buffer:
     Entry 0:
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
    Entry 0:
Pre MEM Oueue:
    Entry 0:
Entry 1:
                    R4, 220(R10)]
               [LW
Post_MEM Queue:
    Entry 0:
Registers
          2
R00:
     0
               0
                    -3
                         0
                              1
                                   -1
                                        0
R08:
     0
          0
               8
                    0
                         0
                              0
                                   0
                                        0
R16:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
R24:
     0
          0
               0
                    0
                         0
                              0
                                   0
                                        0
```

```
Page 123 of 157
sample_pipeline.txt
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
176:
  -1
     -2
        -3
              -1
                 -1
208:
  -1
        -1
240:
  0
     0
        0
           0
              0
                       3
Cvcle:157
Pre-Issue Buffer:
  Entry 0:
        [ ADD
           R6, R4, R51
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
        [LW
           R4, 220(R10)]
Registers
     2
        0
              0
R00:
  0
           -3
                    -1
                       0
R08:
  0
     0
        8
              0
                 0
                       0
R16:
  0
     0
        0
           0
              0
                 0
                    0
                       0
R24:
  0
                       0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=0
```

```
Page 124 of 157
sample_pipeline.txt
1: [\ (1\,,0\,,4\,)\,<\,\bar{10}001000000000000000000000000100110\,,\,100000001000010100110000001000000\,>\,]
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
            -3
                1
                        -1
                            -1
        -2
                    -1
                                -1
                    0
                        0
                            0
                                0
208:
    -1
        1
            -1
                0
    0
240:
Cvcle:158
Pre-Issue Buffer:
    Entry 0:
            [SW
                R6, 176(R10)]
    Entry 1:
            [ADDI
                R1, R1, #-1]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
            [ADD
                R6, R4, R5]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        2
                                Ω
ROO:
            Ω
                -3
                    Ω
                            -1
    0
        0
                        0
                            0
R08:
    0
                0
            8
                    0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
        Ω
            0
                                0
Cache
Set 0: LRU=0
    Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
            -3
                1
                    -1
                        -1
                            -1
                                -1
208:
    -1
        1
            -1
                0
                    0
                        0
                            0
                                0
240:
    0
        Ω
            Ω
                Ω
                    Ω
                        Ω
                            1
                                3
Cycle:159
```

```
sample_pipeline.txt
                                        Page 125 of 157
Pre-Issue Buffer:
    Entry 0:
             [SW
                  R6, 176(R10)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
             [ADDI
                 R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
                 R6, R4, R5]
             [ ADD
    Entry 0:
Pre_MEM Queue:
    Entry 0:
Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
        2
R00:
    0
             Ω
                  - 3
                      Ω
                          1
                               -1
                                   Ω
R08:
    0
        0
             8
                  0
                      0
                          0
                               0
                                   0
R16:
    0
        0
             0
                  0
                      0
                          0
                               0
                                   0
R24:
    0
        0
             0
                  0
                      0
                          0
                               0
                                   0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
176:
    -1
             -3
                           -1
         -2
                 1
                      -1
                               -1
                                   -1
                               0
208:
    -1
             -1
240:
    0
        0
             0
                      0
                          0
                               1
                                   3
Cycle:160
Pre-Issue Buffer:
    Entry 0:
             [SW
                 R1, 268(R0)]
    Entry 1:
Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
             [ADDI
                  R1, R1, #-1]
Pre_MEM Queue:
    Entry 0:
             [SW
                  R6, 176(R10)]
    Entry 1:
```

```
Page 126 of 157
sample_pipeline.txt
Post_MEM Queue:
   Entry 0:
Registers
        2
                                0
R00:
    0
            0
                -3
                    0
                            0
R08:
    0
        0
            8
                    0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
                                0
    0
        0
            0
                        0
                            0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
   Entry
Entry
Dat.a
            -3
176:
    -1
        - 2
                1
                    -1
                        -1
                            -1
                                -1
            -1
                    0
                        0
                            0
208:
    -1
        1
                0
                                0
    0
       0
            0
                0
                                3
240:
                    0
Cycle:161
Pre-Issue Buffer:
    Entry 0:
            [LW
                R1, 268(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
    Entry 0:
            [SW
                R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
        1
            Ω
                -3
                    Ω
                        1
                            1
                                Ω
    0
R08:
    0
        0
                0
                        0
                            0
            8
                    0
                                0
R16:
    0
        Ω
            0
                0
                    Ω
                        0
                            Ω
                                0
R24:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=1
    Entry
```

```
Page 127 of 157
sample_pipeline.txt
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
  Entry
Entry
Data
176:
  _ 1
     - 2
        -3
           1
             -1
                -1
                   -1
                      -1
208:
  -1
     1
        -1
           0
             0
                0
                   0
                      0
240:
  0
     Ω
        Ω
           Ω
             Ω
                0
                   1
                      3
Cycle:162
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
          R1, 268(R0)1
        [LW
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
     1
        0
           -3
             0
                1
                   1
                      0
R08:
  0
     0
        8
           0
             0
                0
                   0
                      0
     0
                      0
R16:
  0
        0
R24:
  0
     0
        0
           0
             0
                0
                   0
                      0
Cache
Set 0: LRU=1
  Entry
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=0
```

```
sample_pipeline.txt
                                  Page 128 of 157
   Entry
176:
   -1
       -2
           -3
                  -1
                      -1
                          -1
                              -1
           -1
208:
   -1
240:
   0
Cvcle:163
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
           [LW
              R1, 268(R0)]
Registers
R00:
   0
           0
               -3
                  0
                              0
R08:
   0
       0
           8
                  0
                          0
                              0
R16:
   0
           0
               0
                  0
                      0
                          0
                              0
       0
R24:
   0
       0
           0
                  0
                              0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
           -3
              1
                  -1
                      -1
                          -1
                             -1
   -1
       1
           -1
                  0
                      0
                          0
208:
              0
                              0
   Ω
       Ω
240:
                          1
                              3
Cycle:164
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
```

```
sample_pipeline.txt
                                     Page 129 of 157
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
ROO:
        1
            Ω
                -3
                    Ω
                        1
                                 Ω
    0
                            1
R08:
                0
                        0
                            0
    0
        0
            8
                    0
                                 0
R16:
    0
        Ω
            0
                0
                    0
                        0
                            Ω
                                 0
R24:
    0
        0
            0
                0
                    0
                        0
                             0
                                 0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=0
    Entry
Entry
Data
176:
    -1
        -2
            -3
                1
                    -1
                        -1
                            -1
                                 -1
208:
    -1
        1
            -1
                0
                    0
                        0
                             0
                                 0
240:
    0
        0
            0
                                 3
Cycle:165
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
        1
            0
                -3
                    0
                        1
                            1
```

```
sample_pipeline.txt
                               Page 130 of 157
R08:
   0
      0
          8
             0
                 0
                    0
                        0
                           0
R16:
   0
      0
          0
             0
                 0
                    0
                        0
                           0
R24:
   0
      0
          0
             0
                 0
                    0
                        0
                           0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
      -2
          -3
             1
                    -1
                        -1
   -1
                 -1
                           -1
          -1
                        0
208:
   -1
             0
                 0
                    0
240:
   0
      0
Cycle:166
Pre-Issue Buffer:
          [SLL
             R10, R1, #2]
   Entry 0:
             R3, 176(R10)]
   Entry 1:
          [LW
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      1
          0
             -3
                 0
                    1
                        1
                           0
R08:
      0
             0
                        0
   0
          8
                 0
                    0
                           0
R16:
   0
          0
             0
                    0
                        0
                           0
      0
                 0
R24:
   0
      0
          0
             0
                 0
                    0
                        0
                           0
Cache
Set 0: LRU=1
   Entry
Set 1: LRU=0
   Entry
```

```
sample_pipeline.txt
                               Page 131 of 157
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
0:[(1,0,3)<10000000000000000010101000010000000,10001101010000110000010110000>]
   Entry
Dat.a
176:
   -1
      - 2
          -3
             1
                 -1
                    -1
                        -1
                           -1
   -1
          -1
                 0
                    0
                        0
208:
      1
             0
                           0
240:
   Ω
      Ω
          Ω
             Ω
                 Ω
                    Ω
                        1
                           3
Cycle:167
Pre-Issue Buffer:
   Entry 0:
          [LW
             R3, 176(R10)]
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
          [SLL
             R10, R1, #2]
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
      1
          0
             -3
                 0
                    1
                        1
                           0
R08:
   0
      0
          8
             Ω
                 0
                    0
                        0
                           0
R16:
   0
      Ω
          0
             0
                 Ω
                    0
                        Ω
                           0
R24:
   0
      0
          0
             0
                 0
                    0
                        0
                           0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
176:
   -1
      -2
          -3
             1
                 -1
                    -1
                           -1
```

```
sample_pipeline.txt
                                      Page 132 of 157
   -1
       1
208:
            -1
                     0
                        0
                             0
                                  0
240:
    0
       0
            0
                                  3
Cycle:168
Pre-Issue Buffer:
    Entry 0:
            [LW
                R3, 176(R10)]
                R4, 220(R10)]
R5, 264(R0)]
    Entry 1:
            [LW
    Entry 2:
Entry 3:
            [LW
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
            [SLL
                R10, R1, #2]
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        1
                     0
                                  0
R08:
    0
        0
            8
                 0
                     0
                         0
                             0
                                  0
R16:
        0
    0
R24:
    0
        0
                                  0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
            -3
                1
                     -1
                         -1
                             -1
                                  -1
            -1
208:
    -1
        1
                 0
                     0
                         0
                             0
                                  0
240:
    0
        0
Cycle:169
Pre-Issue Buffer:
                R5, 264(R0)]
    Entry 0:
            [LW
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
```

```
sample_pipeline.txt
                                         Page 133 of 157
    Entry 0:
Pre_MEM Queue:
    Entry 0:
             [LW
                  R3, 176(R10)]
    Entry 1:
                  R4, 220(R10)]
             [LW
Post_MEM Queue:
    Entry 0:
Registers
R00:
         1
             0
                  -3
                      0
                           1
                                    0
    0
                               1
R08:
    0
         0
                  0
                           0
                               0
                                    0
             4
                      0
R16:
    0
             0
                  0
                                    0
         0
                      0
                           0
                               0
R24:
    0
                                    0
         0
             0
                  0
                      0
                           0
                               0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
         -2
             -3
                  1
                      -1
                           -1
                               -1
                                    -1
208:
    -1
         1
             -1
                  0
                      0
                           0
                               0
                                    0
    Ω
240:
         Ω
             0
                  0
                      0
                                    3
Cycle:170
Pre-Issue Buffer:
    Entry 0:
             [LW
                  R5, 264(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                  R3, 176(R10)]
             [ LW
    Entry 1:
             [LW
                  R4, 220(R10)]
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         1
             0
                  -3
                      0
                               1
                                    0
                  0
                           0
R08:
    0
         0
             4
                      0
                               0
                                    0
R16:
    0
         0
             0
                  0
                      0
                           0
                               0
                                    0
R24:
    0
         0
             0
                  0
                      0
                           0
                               0
                                    0
Cache
```

```
Page 134 of 157
sample_pipeline.txt
Set 0: LRU=0
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
0: [\,(1\,,0\,,3\,)\,<\bar{10}000000000000000101101000010000000\,,10001101010000110000010110000>\,]
   Entry
176:
   -1
          -3
                 -1
                    -1
                        -1
                           -1
208:
   -1
          -1
             0
                 0
                    0
                        Ω
                           0
240:
   0
      0
Cycle:171
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
          [LW
             R4, 220(R10)]
   Entry 1:
          [LW
             R5, 264(R0)]
Post_MEM Queue:
   Entry 0:
          [LW
             R3, 176(R10)]
Registers
R00:
      1
          0
             -3
                 0
                        1
                           0
  0
R08:
   0
      0
                        0
                           0
          4
             0
                 0
                    0
R16:
   0
      0
          0
                 0
                    0
                        0
                           0
R24:
   0
      0
          0
             0
                 0
                    0
                        0
                           0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
```

```
Page 135 of 157
sample_pipeline.txt
Set 3: LRU=1
   Entry
Entry
Data
       -2
          -3
             1
                 -1
                     -1
                        -1
                            -1
176:
   -1
          -1
208:
   -1
      1
              0
                 0
                    0
                        0
                            0
   0
      0
                    0
240:
                            3
                        1
Cycle:172
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
          [LW
             R4, 220(R10)]
   Entry 1:
          [LW
             R5, 264(R0)]
Post_MEM Queue:
   Entry 0:
Registers
R00:
          0
              -2
                 0
                            0
   0
      1
                    1
                        1
R08:
   Ω
      Ω
              Ω
                    Ω
                        Ω
                            Ω
          4
                 0
R16:
   0
          0
              0
                            0
      0
                 0
                    0
                        0
              0
R24:
   0
      0
          0
                 0
                    0
                        0
                            0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
   -1
       -2
          -3
             1
                 -1
                     -1
                        -1
                            -1
      1
   -1
          -1
                 0
                    0
                        0
                            0
208:
             0
240:
   0
      0
          0
             0
                 0
                    0
                        1
                            3
Cycle:173
```

```
Page 136 of 157
sample_pipeline.txt
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
                R5, 264(R0)]
            [LW
    Entry 1:
Post_MEM Queue:
            [LW
                R4, 220(R10)]
    Entry 0:
Registers
R00:
    0
        1
            0
                -2
                    0
                         1
                                 0
R08:
    Ω
        Ω
            4
                Ω
                     Ω
                         Ω
                             Ω
                                 0
R16:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R24:
    0
        0
            0
                Ω
                     0
                         0
                             Ω
                                 0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
208:
            -1
    -1
240:
Cycle:174
Pre-Issue Buffer:
            [ADD
                R6, R4, R5]
    Entry 0:
    Entry 1:
    Entry 2:
Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
```

```
sample_pipeline.txt
                                        Page 137 of 157
    Entry 0:
             [LW
                 R5, 264(R0)]
Registers
R00:
        1
             0
                 -2
                      0
                                   0
R08:
    0
                                   0
        0
             4
                 0
                      0
                          0
                               0
R16:
    0
        0
             0
                      0
                          0
                               0
                                   0
R24:
    0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
0: [\,(1\,,0\,,4\,)\,<\,10001000000000000000000000000100110\,,\,100000001000010100110000001000000\,>\,]
    Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        - 2
                          -1
             -3
                 1
                      -1
                               -1
                                   -1
    -1
             -1
                          Ω
                               Ω
208:
                 Ω
                      Ω
                                   Ω
        1
    0
        0
             0
                 0
                      0
                                   3
240:
Cycle:175
Pre-Issue Buffer:
                 R6, 176(R10)]
    Entry 0:
             [SW
    Entry 1:
             [ADDI
                 R1, R1, #-1]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
             [ADD
                 R6, R4, R5]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        1
             Ω
                 - 2
                      Ω
                          1
                              1
                                   Ω
R08:
    Ω
        Ω
                 Ω
                          Ω
                               Ω
                                   Ω
             4
                      0
                 0
R16:
    0
        0
             0
                      0
                          0
                               0
                                   0
R24:
    0
        0
             0
                 0
                      0
                          0
                               0
                                   0
Cache
Set 0: LRU=1
    Entry
```

```
Page 138 of 157
sample_pipeline.txt
Set 1: LRU=0
Entry
Set 2: LRU=1
   Entry
0: [\,(1\,,0\,,4\,)\,<\,1000100000000000000000000000100110\,,\,100000001000010100110000001000000\,>\,]
    Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
    -1
       -2
            1
                -1
                    -1
                        -1
                            -1
                                -1
208:
    -1
       1
            -1
                Λ
                    Ω
                        Ω
                            Ω
                                Ω
240:
    0
       0
            0
                0
                    0
                        0
                            1
                                3
Cycle:176
Pre-Issue Buffer:
            [SW
                R6, 176(R10)]
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
            [ADDI
                R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
                R6, R4, R5]
   Entry 0:
            [ ADD
Pre_MEM Queue:
    Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
    0
       1
            0
                -2
                    0
                                0
R08:
    0
       0
            4
                0
                    0
                        0
                            0
                                0
R16:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R24:
                                0
    0
        0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=0
   Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
    Entry
0: [\,(1,0,3)\,<\,1000000000000000010101000010000000\,,\,100011010000011000000101100000\,>\,]
```

```
Page 139 of 157
sample_pipeline.txt
Data
208:
   -1
           -1
240:
Cycle:177
Pre-Issue Buffer:
           [SW
               R1, 268(R0)]
   Entry 0:
Entry 1:
   Entry 2:
Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
           [ADDI R1, R1, #-1]
Pre_MEM Queue:
   Entry 0:
           [SW
               R6, 176(R10)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       1
           0
               -2
                   0
                               0
R08:
   0
       0
           4
               0
                   0
                       0
                           0
                               0
R16:
   0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
   0
                       0
                               0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
       - 2
           1
               -1
                   - 1
                       -1
                           -1
                               - 1
   -1
208:
       1
           -1
               Ω
                   Ω
                       Ω
                           Ω
                               Ω
   0
240:
       0
           0
               0
                   0
                               3
                       0
                           1
Cycle:178
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
```

```
sample_pipeline.txt
                                           Page 140 of 157
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
              [SW
                  R1, 268(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         0
              0
                   -2
                        0
                            1
                                      0
                                 1
R08:
    Ω
                   Ω
                            Ω
                                 Ω
                                      Ω
         Ω
              4
                        Ω
                   0
R16:
    0
         0
              0
                        0
                            0
                                 0
                                      0
R24:
    0
         0
              0
                   0
                        0
                            0
                                 0
                                      0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=0
    Entry
0: [\,(1,0,3)<\hat{100000000000000000010101000010000000}\,,10001101010000110000010110000>\,]
    Entry
Data
176:
     -1
              1
                   -1
                        -1
                            -1
                                 -1
                                      -1
208:
    -1
              -1
                   0
                        0
                            0
                                 0
                                      0
240:
    0
                        0
Cycle:179
Pre-Issue Buffer:
                  R1, 268(R0)]
    Entry 0:
              [LW
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
         0
R08:
    0
```

```
sample_pipeline.txt
                                   Page 141 of 157
R16:
   0
       0
                           Ω
                               Ω
R24:
    0
       0
                               0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
0:[(1,0,4)<100001000110000000000000000001,10000001010011001100000100010>]
    Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
0: [\,(1,0,3)\,<\,100000000000000010101000010000000\,,\,1000110101000001100000010110000>\,]
Data
176:
    -1
                   -1
                       -1
208:
    -1
           -1
    0
240:
Cvcle:180
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
    Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [LW
               R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
       0
           0
               -2
                   0
                               0
    0
R08:
    0
       0
           4
               0
                   0
                       0
                           0
                               0
R16:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
   0
       0
           0
                       0
                               0
                   0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
```

```
Page 142 of 157
sample_pipeline.txt
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
Data
176:
   -1
       - 2
          1
              -1
                  -1
                      -1
                         -1
                             -1
                  Ω
                      Ω
                         Ω
208:
   -1
       1
          -1
              Ω
                             Ω
   0
       0
                             3
240:
           0
              0
                  0
                      0
                         1
_____
Cycle:181
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
              R1. 268(R0)1
   Entry 0:
           LT.M
Registers
       Ω
           Ω
                  Ω
                             Ω
R00:
   0
              -2
                     1
                         1
R08:
   0
       0
           4
              Λ
                  0
                      0
                         0
                             0
R16:
   0
       0
           0
              Ω
                  0
                      0
                         Ω
                             0
R24:
   0
       0
           0
              Ω
                  0
                      Ω
                             0
Cache
Set 0: LRU=0
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
0: [\,(1\,,0\,,3\,)<10000000000000010101000010000000\,,100011010100001100000010110000>]
   Entry
Data
176:
   -1
                  -1
                      -1
208:
   -1
       1
```

```
Page 143 of 157
sample_pipeline.txt
240: 0 0
           0
               0
                   0
                       0
                         1
                               3
Cycle:182
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       0
               -2
                   0
                               0
               0
R08:
    0
       0
                       0
                           0
                               0
R16:
    0
       0
           0
               0
                   0
                       0
                           0
                               0
R24:
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Data
176:
    -1
               -1
                   -1
                       -1
                           -1
                               -1
           1
208:
    -1
           -1
                   0
                       0
      0
   0
           0
240:
Cycle:183
Pre-Issue Buffer:
           [SLL
              R10, R1, #2]
   Entry 0:
               R3, 176(R10)]
   Entry 1:
           [LW
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
```

```
sample_pipeline.txt
                                       Page 144 of 157
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
        0
             0
                 -2
                      0
                                   0
    0
                              1
R08:
    0
        0
             4
                 0
                      0
                          0
                              0
                                   0
R16:
    0
        0
             0
                 0
                          0
                              0
                                   0
                      0
R24:
    0
             0
                      0
                          0
                                   0
        0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
    -1
                          -1
176:
        - 2
             1
                 -1
                      - 1
                              - 1
                                   -1
208:
    -1
        1
             -1
                 0
                      0
                          0
                              0
                                   0
240:
    0
        0
             0
                      Ω
                          Ω
                                   3
Cycle:184
Pre-Issue Buffer:
    Entry 0:
             [LW
                 R3, 176(R10)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
             [SLL
                 R10, R1, #2]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        0
             0
                 -2
                      0
                          1
                              1
                                   0
R08:
    0
        0
             4
                 Ω
                      0
                          0
                              Ω
                                   0
R16:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
R24:
    0
        0
             0
                 0
                      0
                          0
                              0
                                   0
Cache
Set 0: LRU=0
```

```
Page 145 of 157
sample_pipeline.txt
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
0: [\,(1,0,3)\,<\,100000000000000010101000010000000\,,\,1000110101000001100000010110000>\,]
   Entry
Data
176:
   -1
                      -1
                  -1
               0
                          0
                      0
208:
   -1
           -1
                  0
                              0
240:
   0
       Ω
                  Ω
                      Ω
                              3
Cycle:185
Pre-Issue Buffer:
              R3, 176(R10)]
   Entry 0:
           [LW
              R4, 220(R10)]
R5, 264(R0)]
   Entry 1:
           [LW
   Entry 2:
           [LW
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
           [SLL
              R10, R1, #2]
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       0
           0
               -2
                  0
                              0
R08:
   0
       0
                      0
                          0
                              0
   0
               0
                              0
R16:
       0
           0
                      0
                          0
R24:
   0
Cache
Set 0: LRU=1
   Entry
0: [\,(1\,,0\,,4)\,<\bar{10}001101010101000100000000011011100\,,1000110000000101000000100000100000]
   Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
```

```
Page 146 of 157
sample_pipeline.txt
Set 3: LRU=1
   Entry
Entry
Data
176:
   -1
              -1
                  -1
                      -1
                         -1
                             -1
           1
208:
   -1
           -1
              0
                  0
                      0
                         0
240:
   0
       0
Cycle:186
Pre-Issue Buffer:
              R5, 264(R0)]
   Entry 0:
           [LW
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [LW
              R3, 176(R10)]
   Entry 1:
           [LW
              R4, 220(R10)]
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       0
           0
              -2
                  0
                             0
R08:
   0
              0
                      0
       0
           0
                  0
                         0
                             0
R16:
   Ω
           Ω
              Ω
                      Ω
                             Ω
       Ω
                  0
                         0
R24:
   0
           0
                  0
                      0
                             0
Cache
Set 0: LRU=1
   Entry
Entry
Set 1: LRU=1
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
   -1
       -2
           1
              -1
                  -1
                      -1
                         -1
                             -1
208:
   -1
       1
           -1
              Ω
                  Ω
                      Ω
                         Ω
                             Ω
   Ω
240:
       Ω
Cycle:187
Pre-Issue Buffer:
```

```
Page 147 of 157
sample_pipeline.txt
     Entry 0:
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
     Entry 0:
Pre_MEM Queue:
                      R4, 220(R10)]
R5, 264(R0)]
     Entry 0:
Entry 1:
                [LW
                [LW
Post_MEM Queue:
                [LW
                      R3, 176(R10)1
     Entry 0:
Registers
R00:
     0
           0
                0
                      -2
                            0
                                 1
                                       1
                                            0
R08:
     0
           0
                0
                      0
                            0
                                 0
                                       0
                                            0
R16:
     0
           Ω
                0
                      Ω
                            Ω
                                 0
                                       Ω
                                            0
R24:
     0
           0
                0
                      0
                            0
                                 0
                                       0
                                            0
Cache
Set 0: LRU=1
     Entry
0: [\,(1\,,0\,,4\,)\,<\bar{10}001101010001000000000011011100\,,100011000000010100000001000010000]
     Entry
Set 1: LRU=1
     Entry
Entry
Set 2: LRU=0
     Entry
Entry
Set 3: LRU=1
     Entry
0: [\,(1,0,3)\,<\,1000000000000000010101000010000000\,,\,100011010000011000000101100000\,>\,]
     Entry
Data
176:
                                 -1
208:
     -1
                -1
                            0
                                       0
240:
     0
          0
                            0
                                 0
                                            3
Cycle:188
Pre-Issue Buffer:
     Entry 0:
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
     Entry 0:
Pre_MEM Queue:
     Entry 0:
                [LW
                      R4, 220(R10)]
     Entry 1:
                [LW
                      R5, 264(R0)]
Post_MEM Queue:
     Entry 0:
```

```
sample_pipeline.txt
                                            Page 148 of 157
Registers
R00:
    0
         0
              0
                   -1
                        0
                                       0
R08:
    0
         0
                             0
                                  0
                                       0
R16:
    0
              0
                   0
                                       0
         0
                        0
                             0
                                  0
R24:
    0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=1
    Entry
Entry
Set 2: LRU=0
    Entry
Entry
Set 3: LRU=1
    Entry
0: [\ (1\,,0\,,3\,) < 10000000000000000101010000100000000\,,1000110101000001100000010110000>]
    Entry
Data
176:
    -1
              1
                   -1
                        -1
                             -1
                                  -1
                                       -1
                        0
                                  0
208:
     -1
                   0
                             0
                                       0
         1
              -1
    0
         Ω
              Ω
                   Ω
                                       3
240:
                        Ω
Cycle:189
Pre-Issue Buffer:
    Entry 0:
Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
                   R5, 264(R0)]
    Entry 0:
              [LW
    Entry 1:
Post_MEM Queue:
                   R4, 220(R10)]
    Entry 0:
              [LW
Registers
R00:
    0
         0
              0
                   -1
                        0
                             1
                                  1
                                       0
R08:
    Ω
         Ω
              0
                   Ω
                        Ω
                             Ω
                                  Ω
                                       0
R16:
    Ω
              Ω
                   Ω
                        Ω
                             Ω
                                       Ω
         0
                                  Ω
R24:
                   0
                                       0
    0
         0
              0
                        0
                             0
                                  0
Cache
Set 0: LRU=1
    Entry
0: [\,(1\,,0\,,4\,)\,<\bar{10}001101010001000000000011011100\,,100011000000010100000001000010000]
    Entry
Set 1: LRU=1
```

```
Page 149 of 157
sample_pipeline.txt
   Entry
Entry
Set 2: LRU=0
   Entry
Entry
Set 3: LRU=0
   Entry
0: [\,(1\,,0\,,3\,)\,<\bar{10}0000000000000010101000010000000\,,100011010100001100000010110000>\,]
   Entry
Data
176:
   -1
       -2
           1
               -1
                   -1
                       -1
                          -1
                              -1
208:
   -1
       1
           -1
               0
                   0
                          0
                              Λ
240:
   Ω
       Λ
           Λ
                   Λ
                              3
Cycle:190
Pre-Issue Buffer:
   Entry 0:
           [ADD
               R6, R4, R5]
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre MEM Oueue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
           [LW
               R5, 264(R0)]
Registers
R00:
   0
       0
           0
               -1
                   0
                       1
                          1
                              0
R08:
   0
       Ω
           0
               Ω
                   0
                       0
                          Ω
                              0
R16:
   0
       0
           0
               0
                   0
                       0
                          0
                              0
R24:
   0
       0
           0
               Ω
                   0
                       0
                          0
                              0
Cache
Set 0: LRU=1
   Entry
0: [\,(1\,,0\,,4\,)\,<\,\hat{10}001101010101000100000000011011100\,,\,1000110000000101000000010000100000]
   Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=0
   Entry
Entry
```

```
sample_pipeline.txt
                                      Page 150 of 157
Data
176:
        -2
                         -1
                                  -1
    -1
208:
            -1
240:
    0
Cycle:191
Pre-Issue Buffer:
    Entry 0:
            [SW
                 R6, 176(R10)]
    Entry 1:
Entry 2:
            [ADDI
                R1, R1, #-1]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
            [ ADD
                R6, R4, R5]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        0
                 -1
                     0
                                  0
R08:
    0
        0
            0
                     0
                         0
                             0
                                  0
R16:
    0
        0
            0
                 0
                     0
                         0
                             0
                                  0
R24:
    0
Cache
Set 0: LRU=1
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
            1
                 -1
                     -1
                         -1
                             -1
                                  -1
                 Ω
                     Ω
                         Ω
                             Ω
208:
    -1
        1
            -1
                                  Ω
    0
240:
Cycle:192
Pre-Issue Buffer:
                R6, 176(R10)]
    Entry 0:
            [SW
    Entry 1:
            [SW
                 R1, 268(R0)]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
```

```
Page 151 of 157
sample_pipeline.txt
     Entry 0:
                 [ADDI
                     R1, R1, #-1]
     Entry 1:
Post_ALU Queue:
     Entry 0:
                 [ADD
                      R6, R4, R5]
Pre_MEM Queue:
     Entry 0:
     Entry 1:
Post_MEM Queue:
     Entry 0:
Registers
           0
                                             0
R00:
                 0
                      -1
                            0
     0
R08:
     0
           0
                 0
                      0
                                  0
                                       0
                                             0
                            0
     Ω
                      Ω
                                             Ω
R16:
           Ω
                 0
                            0
                                  Ω
                                       Ω
R24:
     0
           0
                 0
                      0
                            0
                                  0
                                        0
                                             0
Cache
Set 0: LRU=0
     Entry
0: [\,(1\,,0\,,4\,)\,<\,1^{-}000110101010100010000000011011100\,,\,1000110000000101000000010000010000>\,]
Set 1: LRU=0
     Entry
Entry
Set 2: LRU=1
     Entry
0: [\,(1\,,0\,,4\,)\,<\,1000100000000000000000000000100110\,,\,100000001000010100110000001000000\,>\,]
     Entry
Set 3: LRU=1
     Entry
Entry
Data
176:
     -1
           -2
                 1
                      -1
                            -1
                                  -1
                                        -1
                                             -1
208:
     -1
           1
                 -1
                      0
                            0
                                  0
                                       0
                                             0
240:
     0
           0
                 0
                            0
                                  0
                                             3
Cycle:193
Pre-Issue Buffer:
                 [SW
                      R1, 268(R0)]
     Entry 0:
     Entry 1:
     Entry 2:
     Entry 3:
Pre_ALU Queue:
     Entry 0:
     Entry 1:
Post_ALU Queue:
     Entry 0:
                 [ADDI
                     R1, R1, #-1]
Pre_MEM Queue:
     Entry 0:
                 [SW
                      R6, 176(R10)]
     Entry 1:
Post_MEM Queue:
     Entry 0:
Registers
R00:
     0
           Ω
                 0
                      -1
                            0
                                  1
                                       1
                                             0
R08:
     0
           0
                 0
                      0
                            0
                                  0
                                        0
                                             0
R16:
     0
           0
                                             0
```

```
sample_pipeline.txt
                                Page 152 of 157
      0
R24:
   0
          0
                  Ω
                     Ω
                         Ω
                             Ω
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
   -1
       -2
          1
              -1
                  -1
                     -1
                         -1
                             -1
208:
   -1
          -1
                  0
                     0
                         0
                             0
240:
   0
       0
          0
                  0
Cycle:194
Pre-Issue Buffer:
              R1, 268(R0)]
          W.T ]
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
          [SW
              R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
   0
       -1
          0
              -1
                  0
                             0
R08:
   0
       0
                         0
                             0
          0
                  0
R16:
   0
       0
          0
              0
                  0
                     0
                         0
                             0
R24:
   0
                             0
Cache
Set 0: LRU=0
   Entry
0: [\,(1\,,0\,,4)\,<\,10001101010001000000000011011100\,,1000110000000101000000100000100000]
   Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
```

```
Page 153 of 157
sample_pipeline.txt
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
   -1
       -2
              -1
                  -1
                      -1
                         -1
                             -1
176:
          1
208:
   -1
          -1
              0
                  0
                      0
                         0
                             0
       1
   Ω
240:
Cycle:195
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
           [LW
              R1, 268(R0)]
   Entry 1:
Post_MEM Queue:
   Entry 0:
Registers
R00:
       -1
           0
              -1
                  0
                             0
   0
                      1
                         1
R08:
       0
              Ω
                      Ω
                         Ω
   0
           0
                  Ω
                             0
R16:
   0
       Ω
           0
              0
                  0
                      0
                         0
                             0
R24:
   0
                      Ω
                             0
Cache
Set 0: LRU=0
   Entry
0: [\ (1\,,0\,,4\,)\,<\,10\,0011010101000100000000011011100\,,1000110000000101000000100001000010000\}]
   Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
   -1
       -2
           1
              -1
                  -1
                      -1
                         -1
                             -1
208:
   -1
              0
                  0
                      0
                         0
                             0
240:
   0
       Ω
                  0
```

```
sample_pipeline.txt
                                    Page 154 of 157
_____
Cycle:196
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
   Entry 0:
   Entry 1:
Post_MEM Queue:
   Entry 0:
           [LW
               R1, 268(R0)]
Registers
R00:
    0
       -1
            0
                -1
                    0
                       1
                            1
                                0
R08:
    0
        0
            0
                0
                    0
                        0
                            0
                                0
R16:
    0
       0
            0
                0
                    0
                        0
                            0
                                0
R24:
    0
       0
            0
                Ω
                    0
                        0
                            0
                                0
Cache
Set 0: LRU=0
   Entry
Entry
Set 1: LRU=0
   Entry
Entry
Set 2: LRU=1
   Entry
Entry
Set 3: LRU=1
   Entry
Entry
Data
176:
    -1
                -1
                        -1
                            -1
                                -1
208:
    -1
           -1
   0
240:
Cvcle:197
Pre-Issue Buffer:
   Entry 0:
   Entry 1:
   Entry 2:
   Entry 3:
Pre_ALU Queue:
   Entry 0:
   Entry 1:
Post_ALU Queue:
   Entry 0:
Pre_MEM Queue:
```

```
Page 155 of 157
sample_pipeline.txt
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
R00:
    0
        -1
            0
                -1
                     0
                                 0
R08:
        0
                0
                         0
                             0
                                 0
    0
            0
                    0
R16:
    0
        0
            0
                0
                         0
                             0
                                 0
                     0
                                 0
R24:
    0
        0
            0
Cache
Set 0: LRU=0
    Entry
Entry
Set 1: LRU=0
    Entry
Entry
Set 2: LRU=1
    Entry
Entry
Set 3: LRU=1
    Entry
Entry
Data
176:
    -1
        -2
                -1
                         -1
                             -1
            1
                     -1
                                 -1
        1
                     Ω
                         Ω
208:
                Ω
                             Ω
                                 Ω
    -1
            -1
240:
    0
        0
            0
                     0
                         0
                             1
                                 3
Cycle:198
Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
Registers
                                 0
R00:
    0
        -1
            0
                -1
                     0
                         1
                             1
R08:
    0
        0
            0
                0
                     0
                         0
                             0
                                 0
R16:
    0
        Ω
            0
                0
                     0
                         0
                             Ω
                                 0
R24:
    0
        0
                         0
                             0
                                 0
Cache
Set 0: LRU=0
    Entry
```

```
Page 156 of 157
sample_pipeline.txt
Entry
Set 1: LRU=0
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
  Entry
Entry
Data
176:
  -1
     -2
       1
          -1
             -1
               -1
                  -1
                     -1
208:
  -1
       -1
          0
             0
               0
                  0
240:
  0
     0
       0
             0
Cycle:199
Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:
Registers
R00:
  0
R08:
  0
     0
       0
          0
               0
                  0
                     0
R16:
  0
     0
       0
          0
                  0
                     0
                     0
R24:
  0
     0
                  0
Cache
Set 0: LRU=0
  Entry
Entry
Set 1: LRU=1
  Entry
Entry
Set 2: LRU=1
  Entry
Entry
Set 3: LRU=1
```

sample_pipeline.txt

Page 157 of 157

Data 176: 208: 240: