Manarat International University (MIU)

Department of CSE (Evening)
Final Exam (Summer 2017)
Digital Logic Design (CSE-209)

Full Marks: 40 Time: 2.5 Hour

Answer any 5 (five) question. All questions are of equal value.

1. a. Design a combinational circuit using a ROM which accepts a 3-bit number and generates an output binary number equal to the square of the input number 3

   b. Implement a full adder circuit with a decoder and two OR gates. 5

2. a. Implement the following function with a multiplexer 3

$$F(A,B,C,D)=\sum(0,1,3,4,8,9,15)$$

   b. Design a combinational circuit for BCD adder. 5

3. a. Define sequential circuits. 1

   b. Explain different triggering methods. What is the difference between a latch and a flip-flop. 3

   c. Write down the truth table, characteristics table and excitation table of the D flip-flop. 4

4. a. Convert a SR flip-flop to a T flip-flop 3

   b. What is "*Racing*"? How do you remove *racing* in JK flip-flop. 2

   c. Explain master-slave operation of a JK flip-flop 3

5. a. Draw state table, state diagram and state equation for JK flip-flop 5

   b. Write down the design procedure for clocked sequential circuit. 3

6. a. A sequential circuit has 2 T flip-flops (A, B) and one input x. It is described by the following flip-flop input functions. 4

$$T_A = x$$
$$T_B = x.Q_A$$
$$y = Q_A.Q_B$$

   Derive the state table and the state diagrams

   b. For the following sequential circuit find the state table and state diagrams. 4

$$D_A = x.Q_A + Q_B$$
$$D_B = Q_A'.Q_B$$
$$y = x.Q_A + x' Q_B'$$