PSL Logic-Driven Digital Twin Model of MiCOM P642 Transformer Protection Relay

Department of Electrical Engineering

BTech. Project Presentation

Supervisor: Dr. Ravi Yadav

Presenter:
Mansi Choudhary (B22EE045)
Mahek Vanjani (B22EE088)

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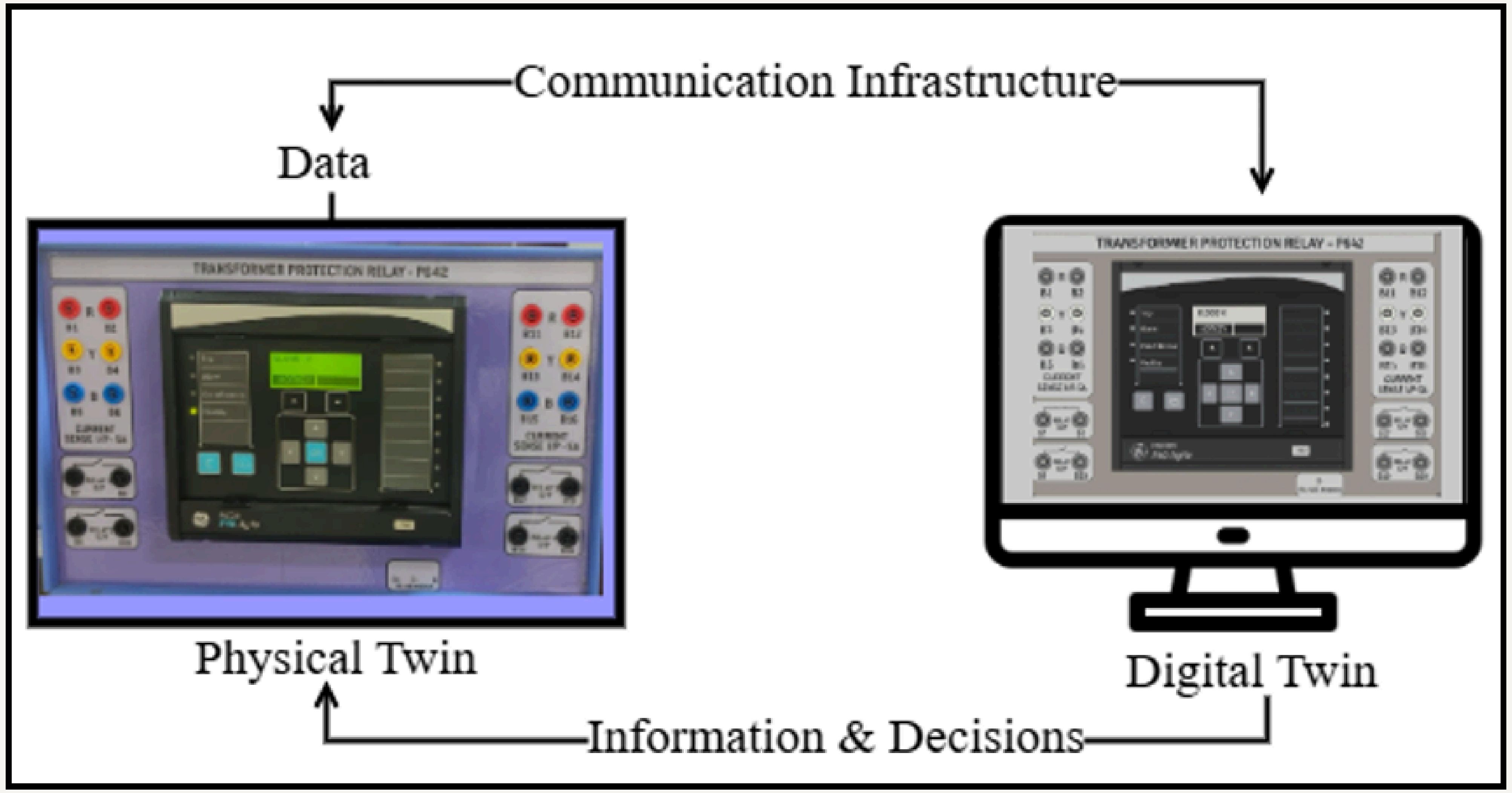


Overview

Motivation & Background

- Relay testing traditionally requires physical MiCOM P642 hardware, CT injection, wiring, and safety precautions.
- This process is slow, costly, and risky for the system.
- Digital twins allow hardware-free relay analysis, safe experimentation, and rapid validation.
- Motivation: Build a complete virtual replica of MiCOM P642 behaviour, including PSL logic, numerical Idiff protection, and trip responses.

Problem Statement and Objective

01

Problem Statement

There is no software-based digital twin that can replicate MiCOM P642's Idiff differential protection and PSL trip behaviour through black-box neural modelling without using physical relay hardware.

02

Objective

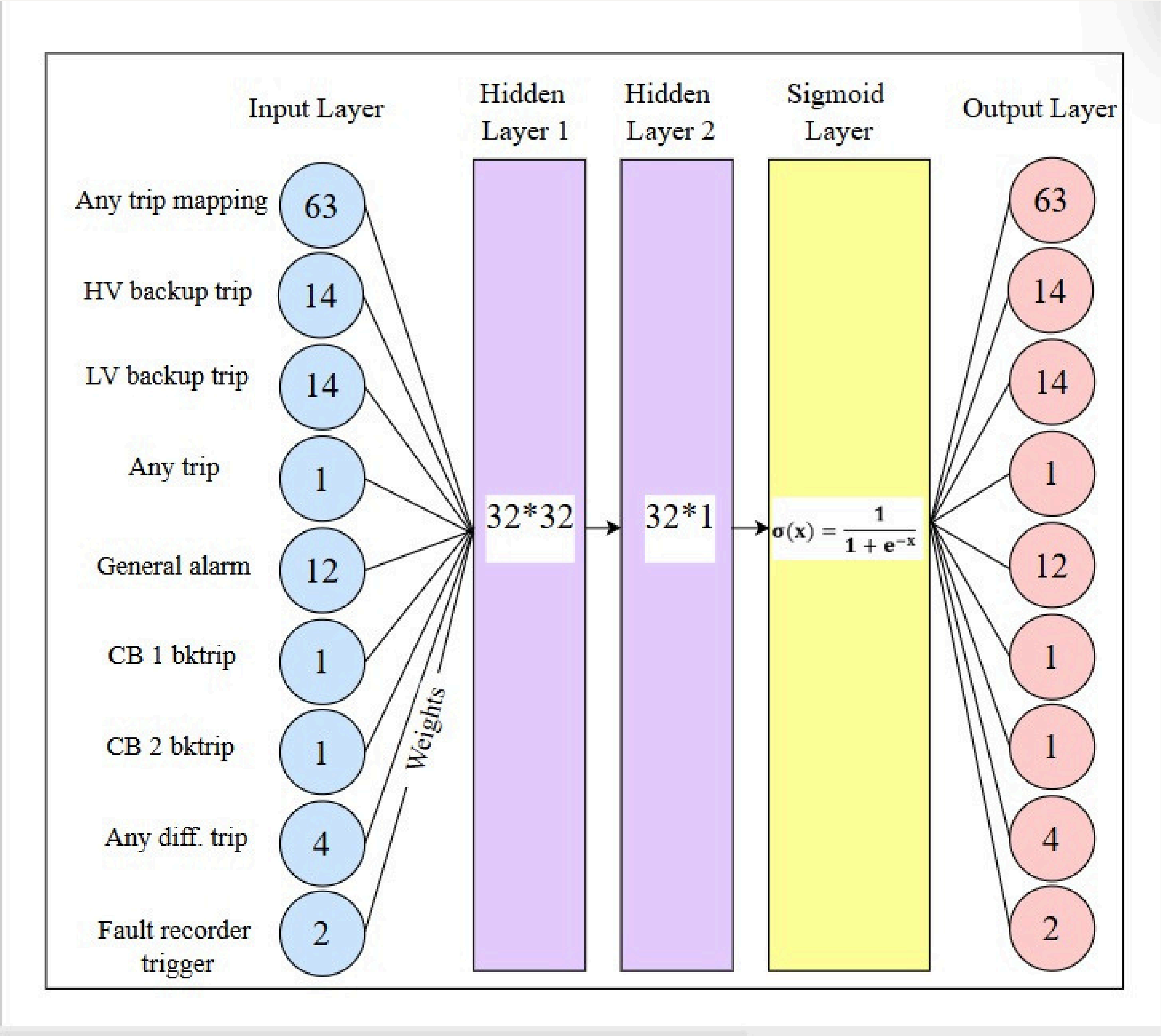
To create a software-based digital twin of the MiCOM P642 relay by modelling its Idiff differential protection and developing a black-box neural model that learns PSL trip behaviour, enabling relay testing and validation without physical hardware.

Literature Review

- Transformer differential protection uses Idiff–Ibias comparison, harmonic restraint, and slope characteristics to detect internal faults.
- MiCOM P642 uses PSL logic (DDBs, timers, gates) to combine protection outputs into final trip signals.
- Modbus communication enables real-time extraction of relay states for external analysis and testing.
- Prior research shows that black-box neural networks can learn relay behaviour, including trip logic and timing, without access to internal algorithms.
- Recent studies demonstrate the effectiveness of modular neural architectures for modelling complex protection logic, supporting digital twin development.

Methodology

Neural Network Architecture(Black Box Modelling)



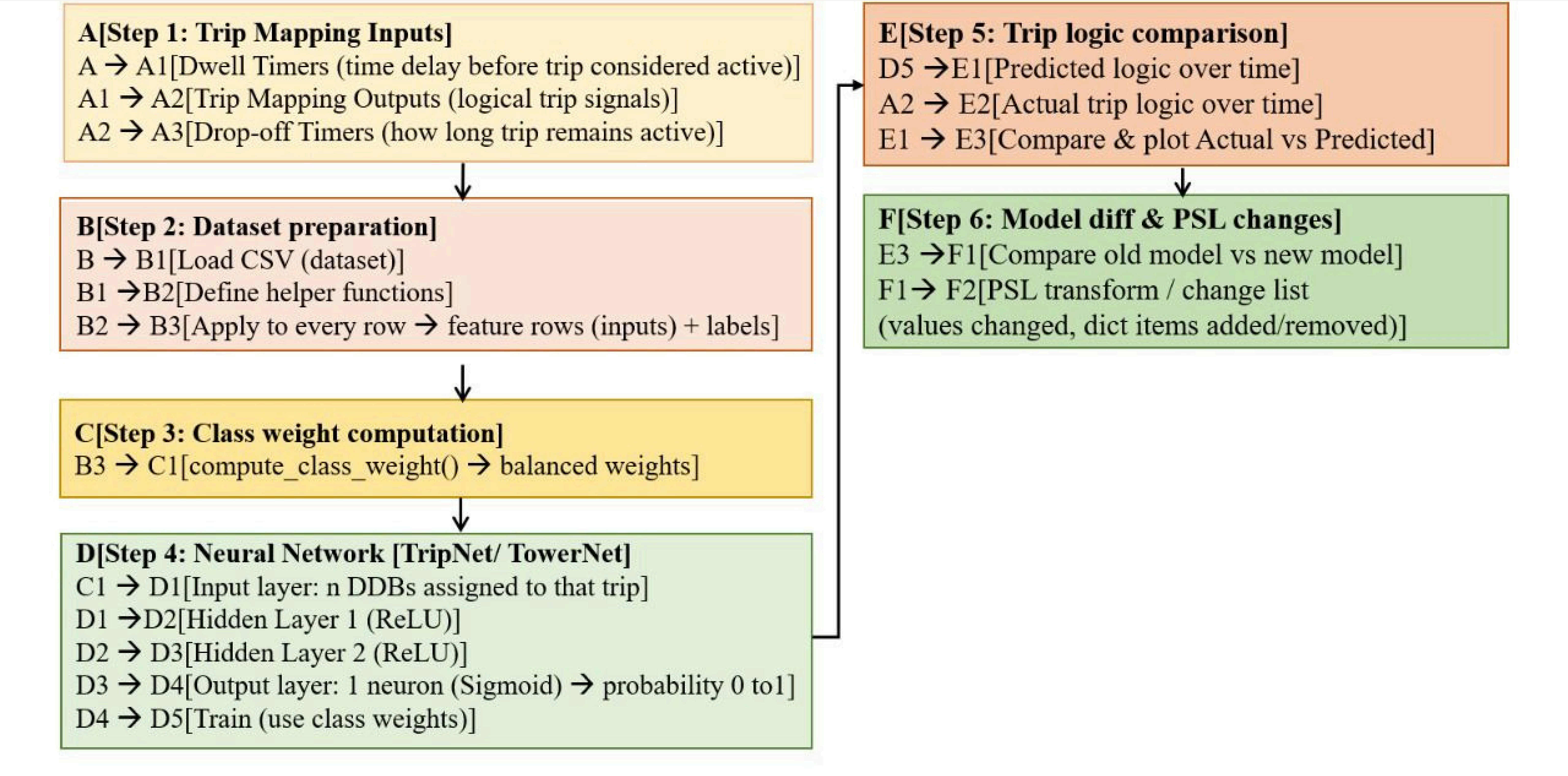
Neural Black-Box Modelling Framework:

- PSL trip mappings are converted into DDB-based inputs with dwell and drop-off timing.
- A hierarchical neural structure (TripNet–TowerNet) mirrors the relay's PSL logic.
- Each TripNet learns the behavior of an individual trip block using ReLU layers and a Sigmoid output.
- TowerNet aggregates all TripNet outputs to predict final multi-trip decision.
- Model predictions are validated using actual vs predicted trip curves over time.

Fine-Tuning Strategy:

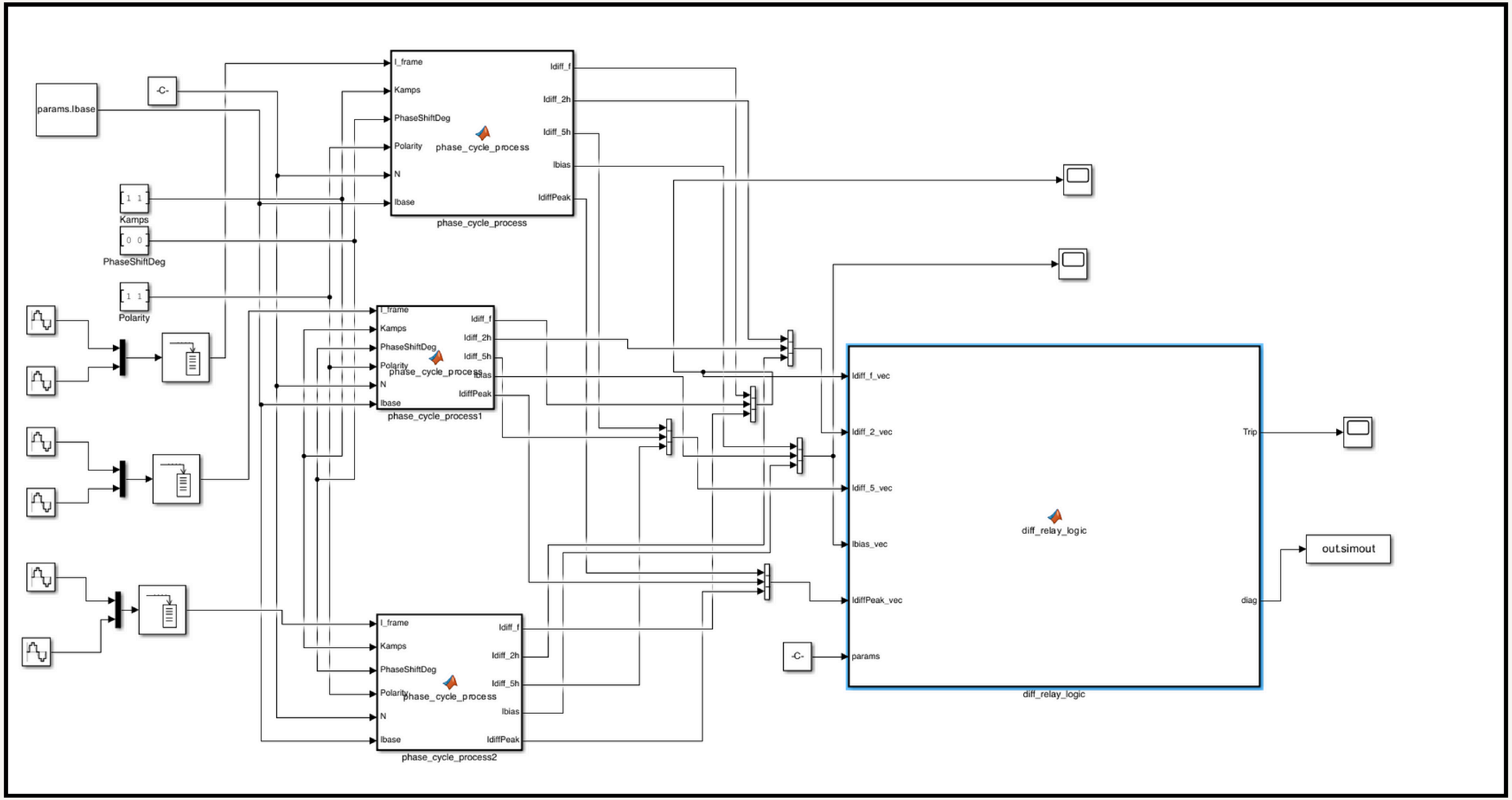
- PSL logic changes are detected automatically, and only affected TripNets are fine-tuned.
- TowerNet is retrained to realign global trip dependencies without full model retraining.

Methodology



Methodology

iDiff Trip Modelling in MATLAB/Simulink



Methodology

iDiff Trip Modelling in MATLAB/Simulink

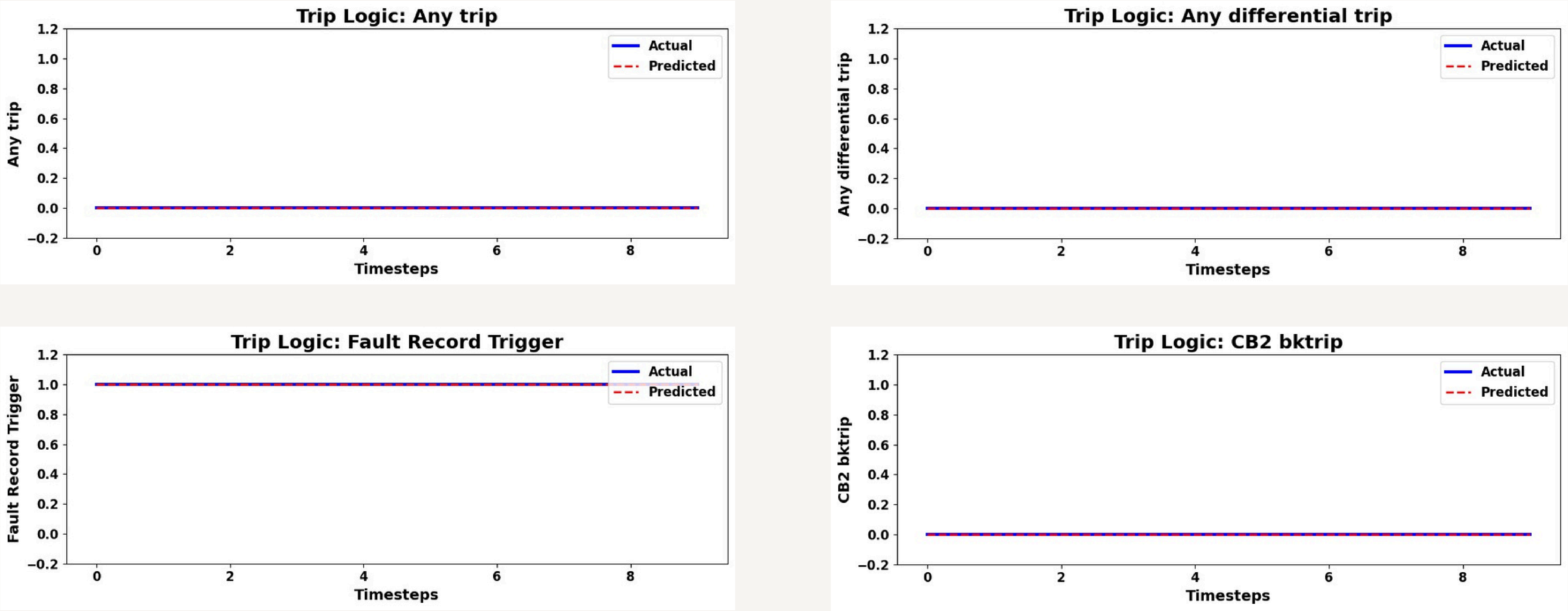
- Set Parameters: Configured sampling rate, slope settings, harmonic thresholds, and HS levels as per the MiCOM P642 manual.
- Generate Inputs: Created three-phase HV and LV CT currents for normal, fault, and inrush scenarios.
- Per-Cycle Processing: Used phase_cycle_process blocks to compute Idiff, Ibias, 2nd/5th harmonics, and peak Idiff for each phase.
- Vector Formation: Combined phase outputs into Idiff, Ibias, and harmonic vectors.
- Apply Relay Logic: Fed vectors into diff_relay_logic to apply triple-slope characteristic, harmonic blocking, and HS checks.
- Trip Output: Generated the final Trip signal based on protection criteria.

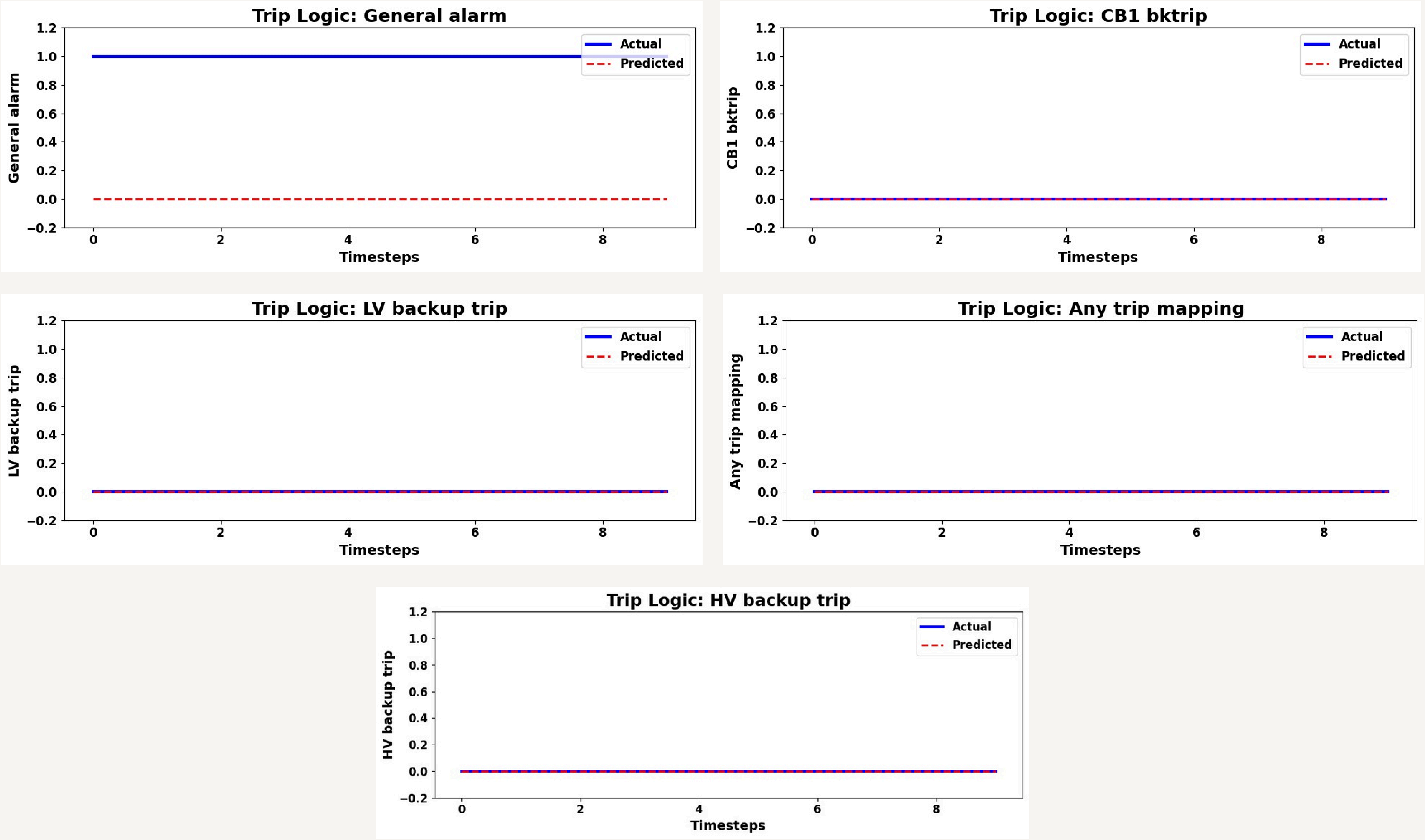
Results & Conclusions

Neural Network Evaluation Results:

- The accuracy of the model is currently around 85% accuracy using dataset consisting of 1000+ columns.

Actual v/s Predicted Trip Logic Comparison

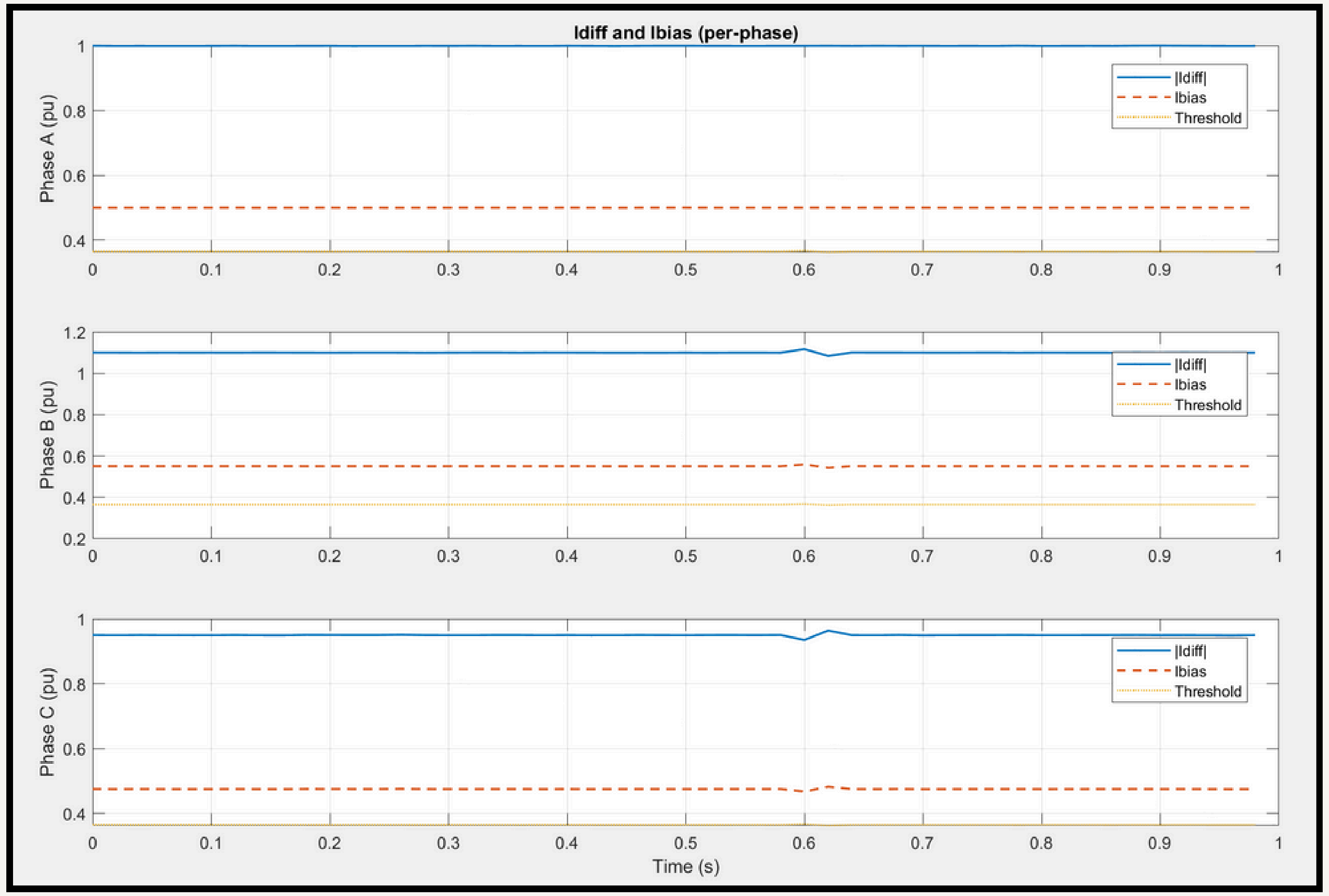


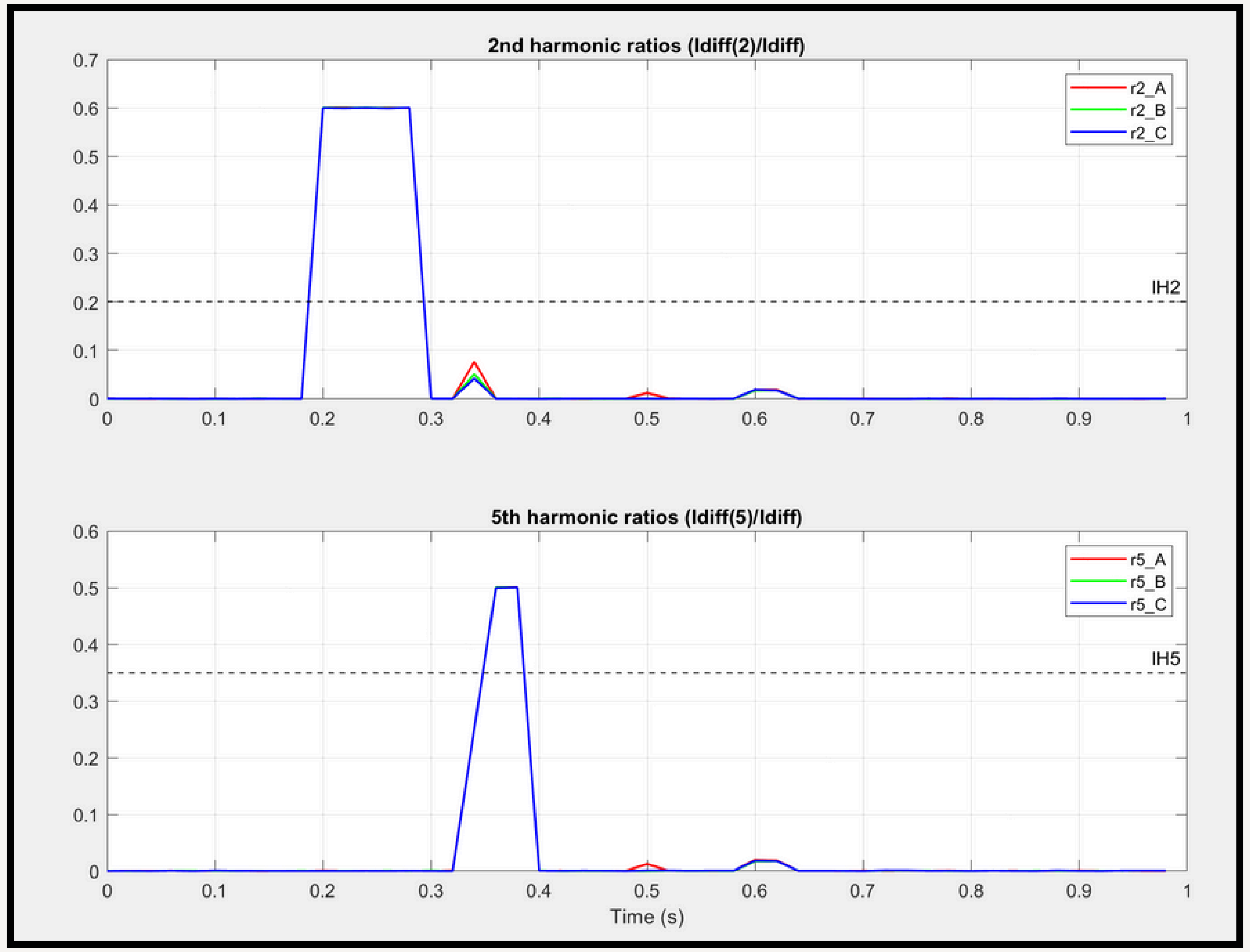


Trip Logic: General alarm
General alarm
Actual
Predicted
Timesteps
Trip Logic: CB1 bktrip
CB1 bktrip
Actual
Predicted
Timesteps
Trip Logic: LV backup trip
LV backup trip
Actual
Predicted
Timesteps
Trip Logic: Any trip mapping
Any trip mapping
Actual
Predicted
Timesteps
Trip Logic: HV backup trip
HV backup trip
Actual
Predicted
Timesteps

Results & Conclusions

iDiff Trip Modelling in MATLAB/Simulink



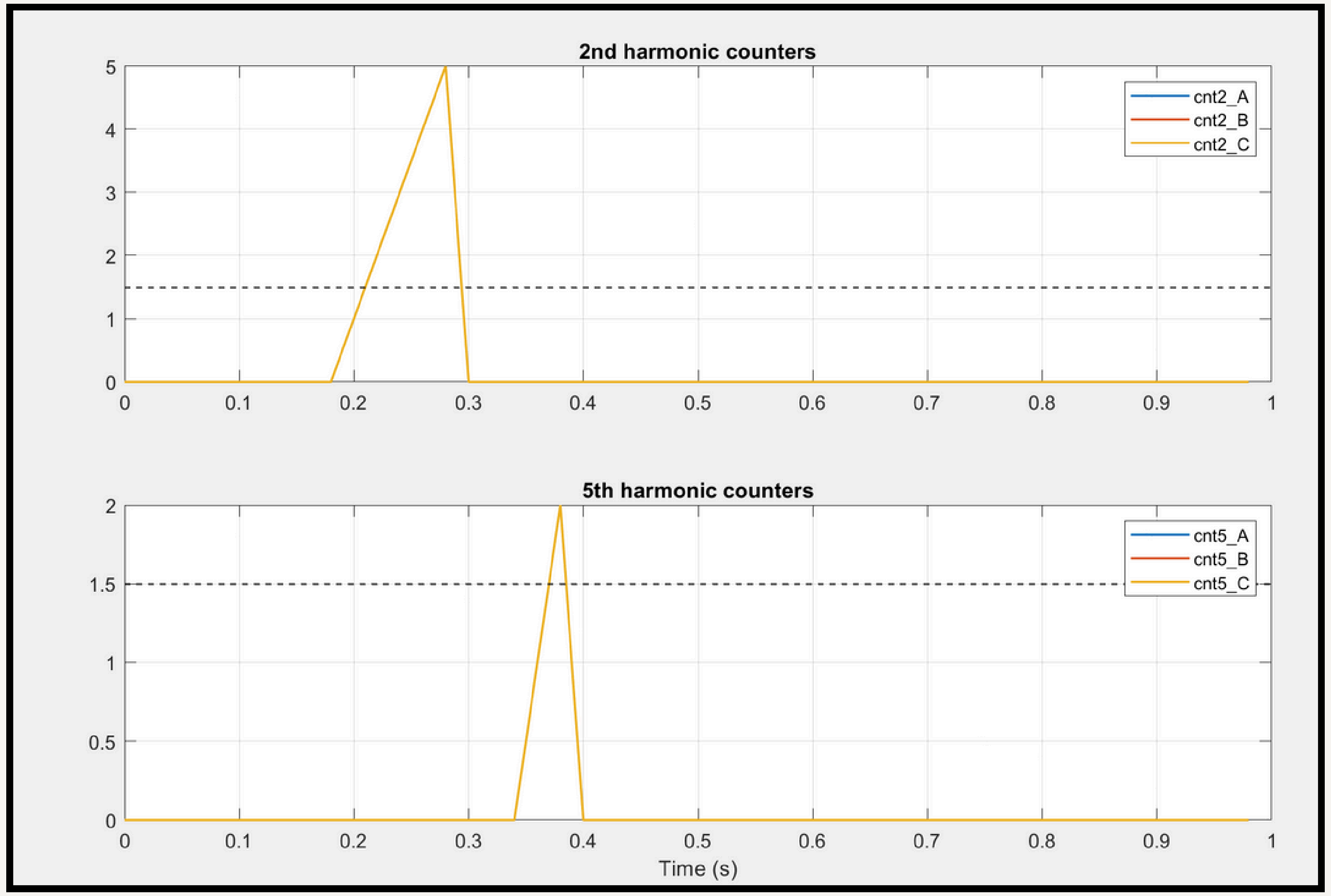


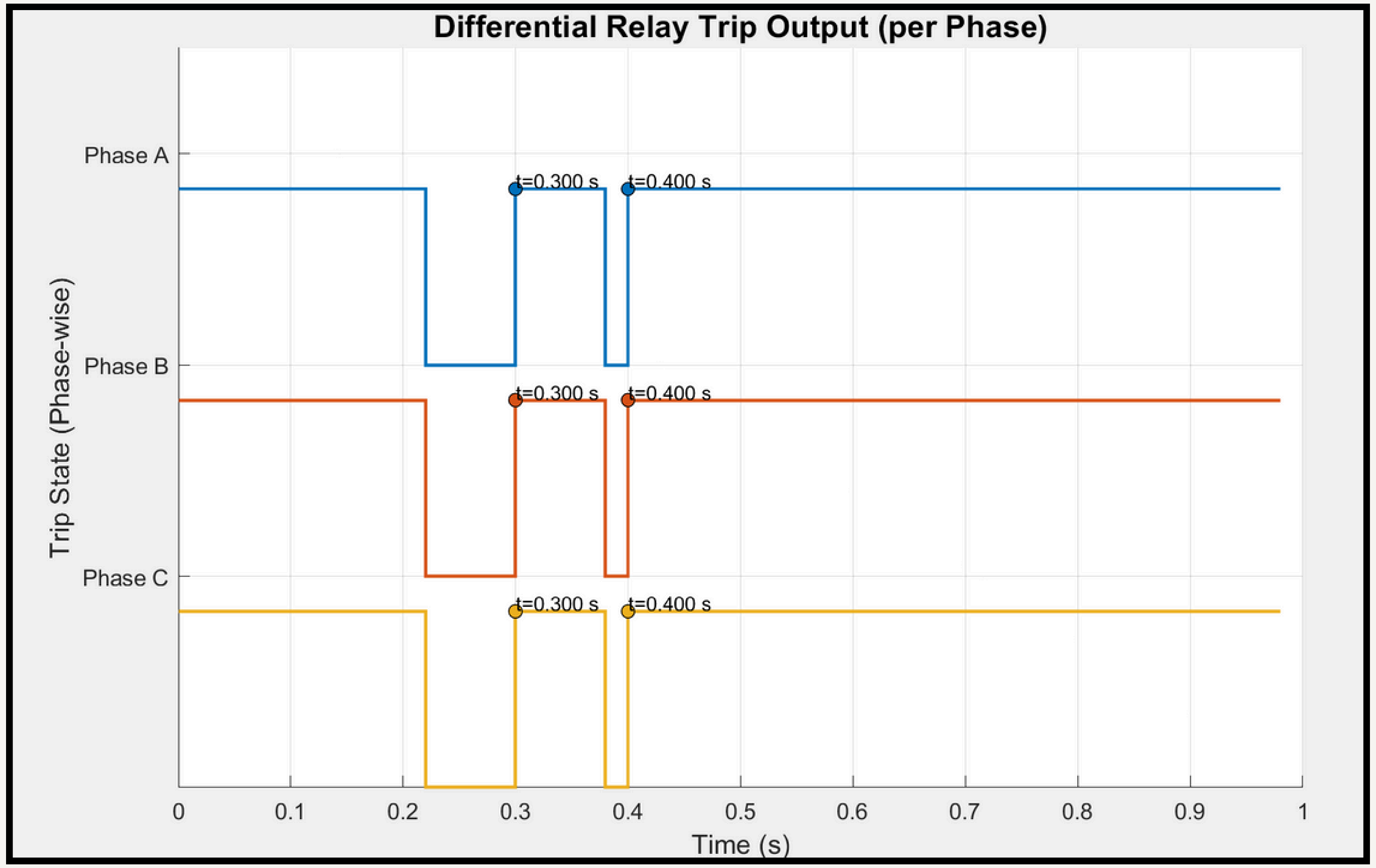
Idiff–Ibias Response: Idiff increases only during the internal fault window (0.30–0.40 s), while Ibias stays below threshold during normal and external conditions, showing stable behaviour.

Harmonic Ratios: 2nd harmonic rises during inrush and 5th harmonic during overfluxing, both correctly crossing their thresholds and activating blocking.

Results & Conclusions

iDiff Trip Modelling in MATLAB/Simulink



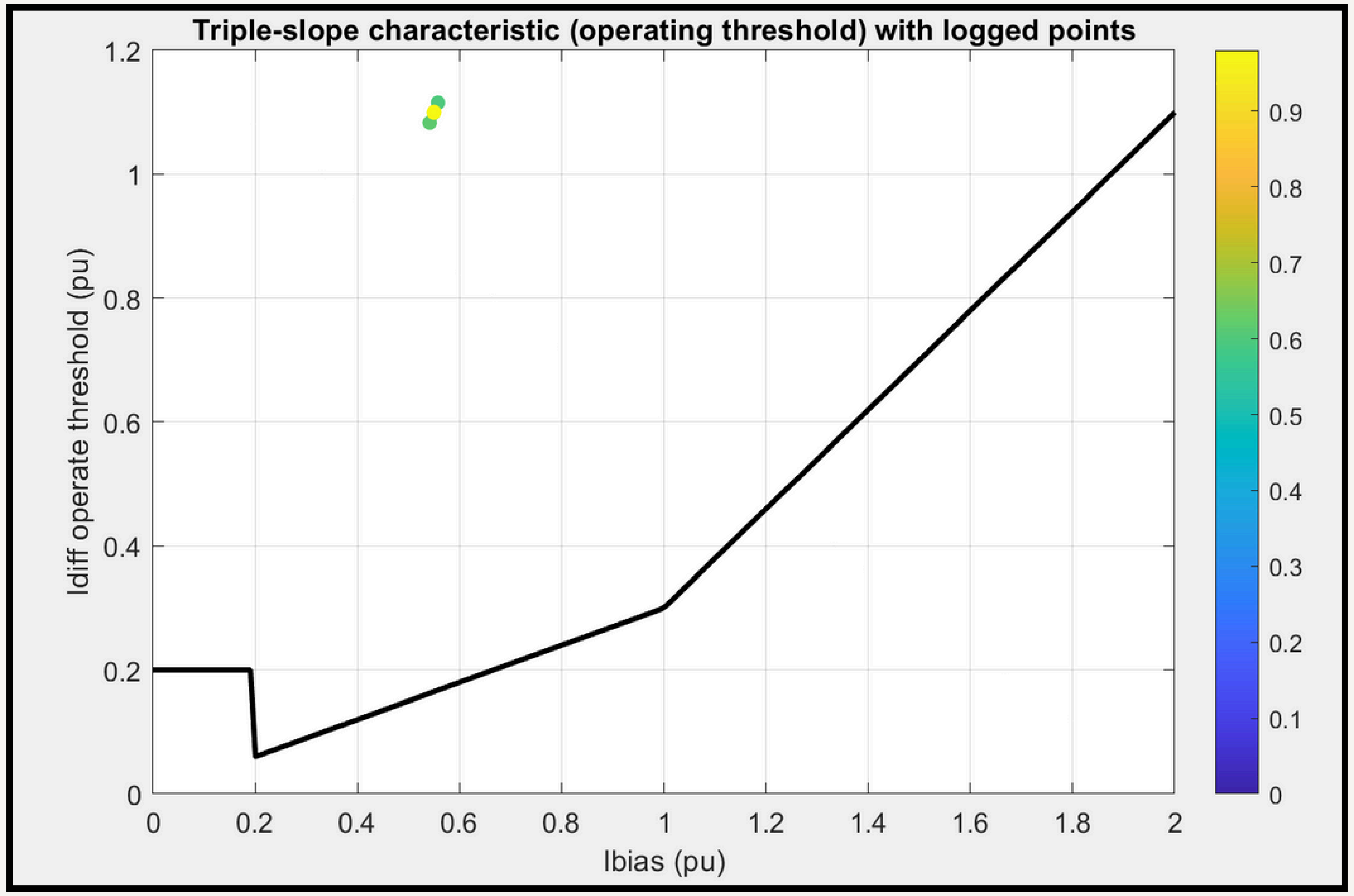


Harmonic Counters: Counters increase only during their respective harmonic events and reset immediately afterward, matching MiCOM blocking logic.

Trip Output: All phases trip at 0.30 s during the internal fault and reset at 0.40 s, confirming accurate fault detection and secure performance.

Results & Conclusions

iDiff Trip Modelling in MATLAB/Simulink



Slope Characteristic: Operating points fall in the trip region only during the fault, validating correct implementation of the triple-slope differential characteristic.

Limitations and Future Scope

Limitations

- Only Idiff protection is modelled; other relay functions are not included.
- Neural model does not capture full signal-processing behaviour.
- PSL timing and rare trip events need more data for higher accuracy.

Future Scope

- Add REF, thermal, and other protection functions to extend beyond Idiff.
- Implement full signal-processing layer (filtering, phasors, harmonics).
- Improve neural model accuracy using more data and rare-event cases.
- Add realistic CT-saturation and bias behaviour.

Acknowledgement and References

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[2] Y. Dong, Q. Chen, W. Ding, N. Shao, G. Chen, and G. Li, "State evaluation and fault prediction of protection system equipment based on digital twin technology," Applied Sciences, vol. 12, no. 15, p. 7539, 2022.

[3] F. Araujo-Vargas and G. Konstantinou, "Modular design and real-time simulators toward power system digital twins implementation," IEEE Transactions on Industrial Informatics, vol. 19, no. 1, pp. 52–61, 2022.

Thank You