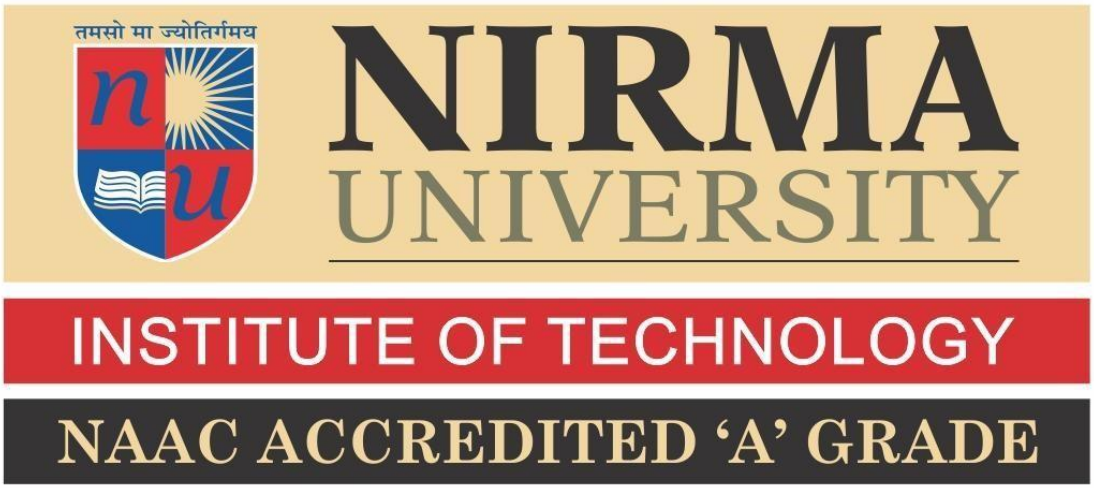

2EC501 VLSI DESIGN

SPECIAL ASSIGNMENT

ON

Two input OR gate using NMOS load and NMOS as a driver with a Propagation Delay of 2 ns

SUBMITTED TO

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Design Problem: Two input OR gate using NMOS load and NMOS as a driver with a Propagation Delay of 2 ns

2-Input OR Gate

Q1:Find out the optimized Boolean equation

- Total combination = 2^2= 4, so it has input in four combination 00, 01, 10, 11. And Boolean equation for OR-gate is,

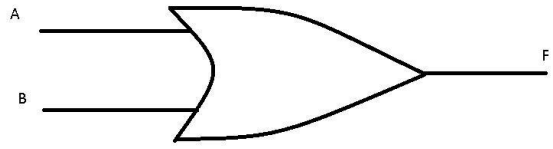
$$F = A + B$$

- Here in the above equation 'F' is the output while 'A' and 'B' are the inputs.

- Truth table for OR-gate is,

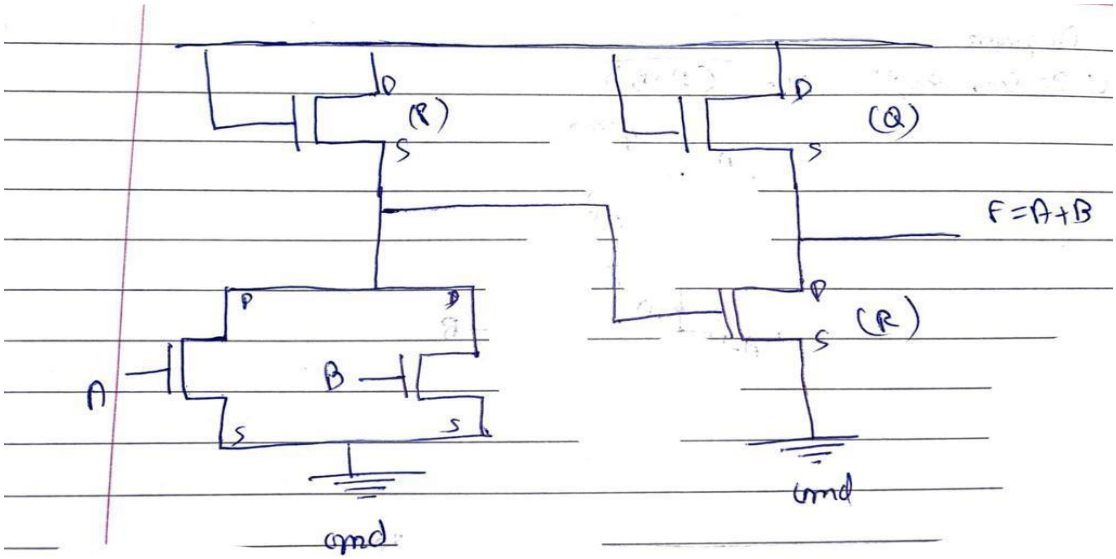
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

Q2:Draw the optimized gate level circuit diagram.

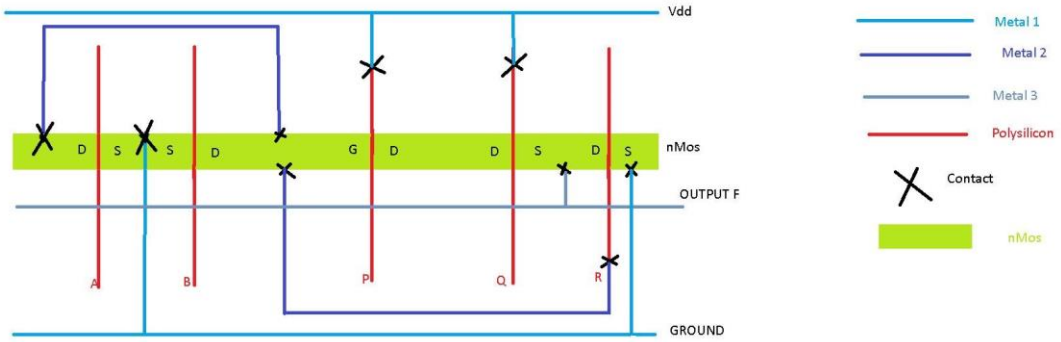


-2 Input OR Gate

Q3: Draw the transistor level schematic for CMOS/MOS implementation.



Q4: Draw stick diagram for above implementation level using proper colour code.

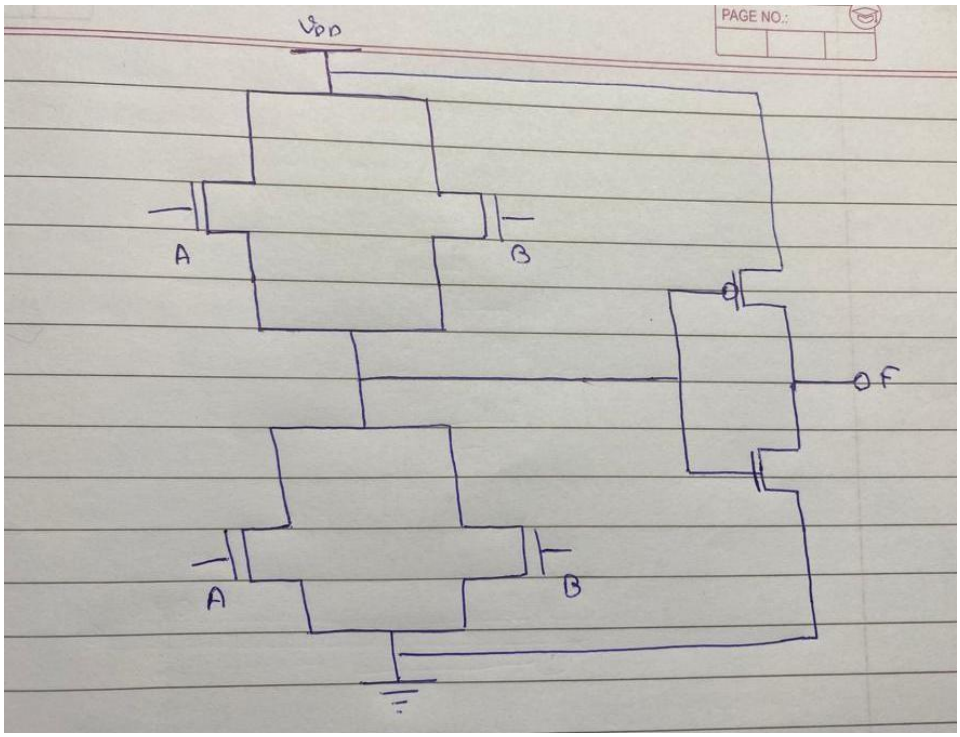


Q5: State the various level of VOL corresponding to various transistor statuses.

Vol depends on the no. of nmos connected to the ground, and output inverter is based at the inverter as well as nmos is weak at transmitting 1 so we will get

Vol>=0(slightly)

Q6: Find an equivalent CMOS inverter circuit.



Q7:A For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance? (Assume that all the transistors have been sized to give a worst-case output resistance of 20 K for the worst-case input pattern.)

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

OR Gate Truth Table

Here we can clearly see that we are getting low output at A=0 & B=0 and at zero nmos becomes an open circuit that means the value of the Resistance must be INFINITY.

Q8:For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?

Considering the above truth table we are getting high output values at three case

I. At A=0 & B=1
II. At A=1 & B=0
III. At A=1 & B=1

For Case I,

At A=0 & B=1, since transistor A is off the equivalent Resistance would be INFINITY even if transistor B is in on state.

For Case II,

At A=1 & B=0, same case as the above R=Infinity this time its transistor B which is in the off state.

For Case III,

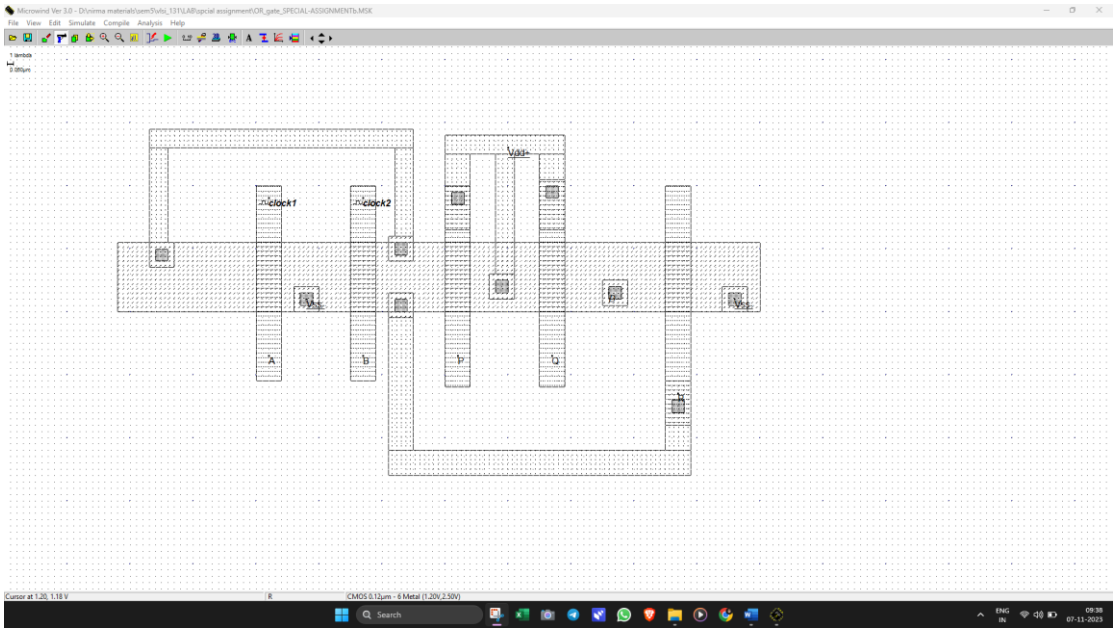
At A=1 & B=1, here since both the transistors are at on state we will assume their Resistance value to be 20k ohm each as given in the question.

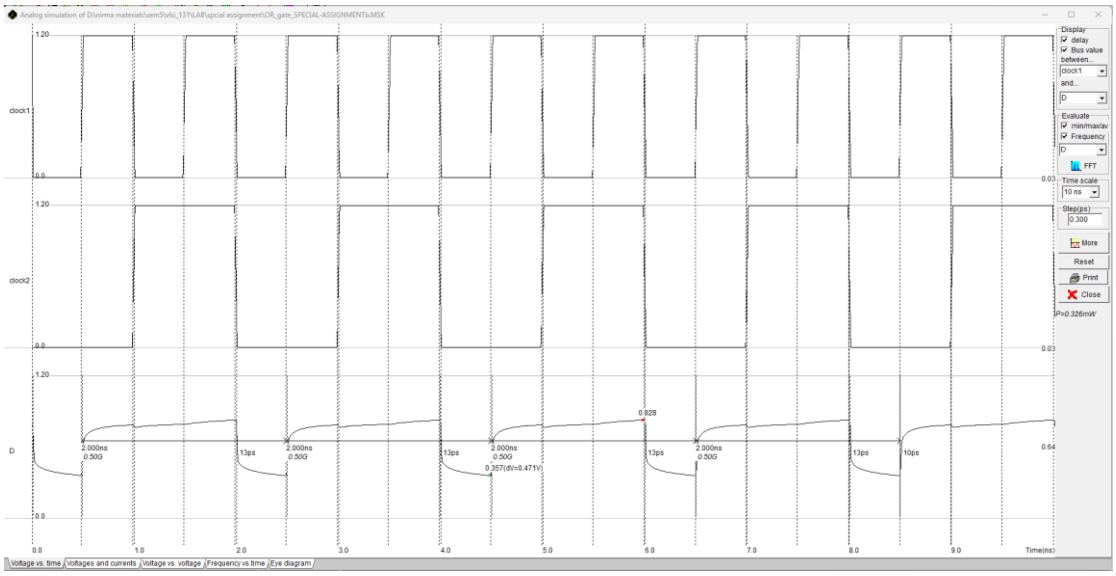
Since both are connected in parallel the Equivalent Resistance would be 20k

Req =20k ohm

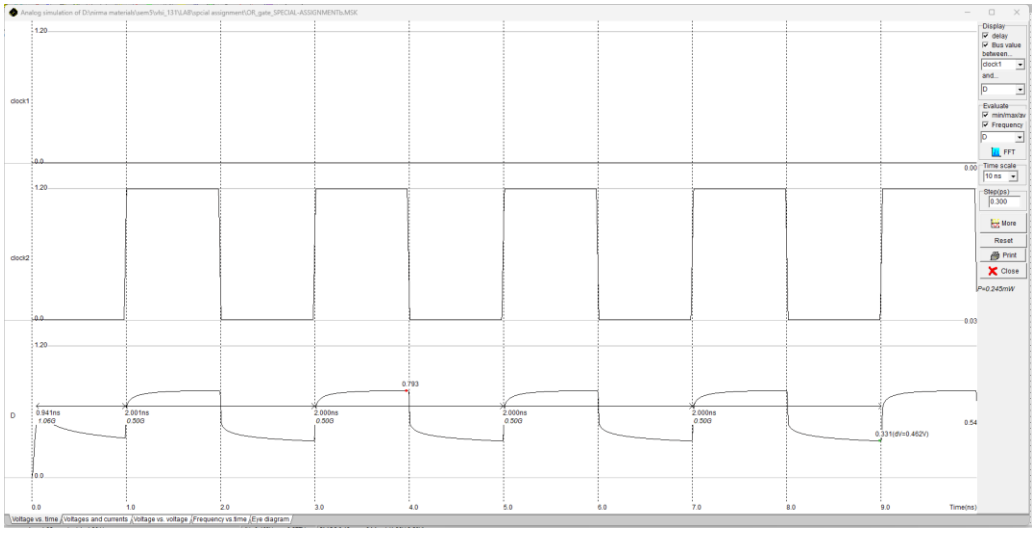
So here for the input A=1, B=1 we the lowest output resistance when Output is high.

Q9: Prepare the layout using Microwind tool.





Q10: Simulate it for various combinations of inputs.



Q11: Measure the rise time, fall time, propagation delay and other parameters.

τ(High time)= 0.91ns-0.18ns=0.80ns τ(Low time)= 199.41-198.83ns=0.624ns

Propagation delay= [τ(high-low) + τ(low-High)]/2= 2.249 ns

Conclusion:

In this assignment, OR gate is made, the target is to make an IC, for which basic components required are gates. So, by adjusting the capacitance and delaying the clock, a two-input OR gate was created using NMOS as the load and NMOS as the driver with a precise propagation delay of 2ns.