COMPUTER ORGANIZATION AND ARCHITECTURE
UNIT –III
TOPIC- ADDITION AND SUBTRACTION OF SIGNED MAGNITUDE DATA
PART-2

Addition and Subtraction of Signed Magnitude Data

Hardware Implementation

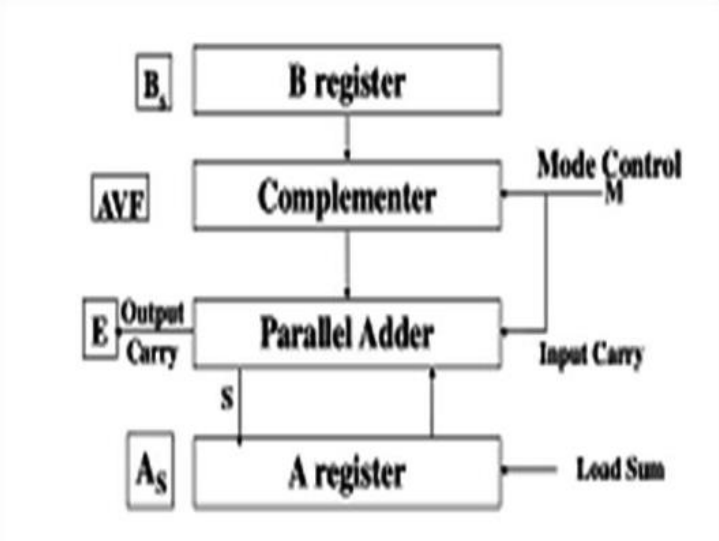

Figure: Hardware Implementation of signed magnitude addition and subtraction.

- Let A and B be the two registers that holds the magnitudes of the numbers and A_s and B_s be two flip flops that holds the corresponding sign.
- The result of the operation may be transferred to the third register or the result is transferred to A and A_s.
- First parallel adder is needed to perform micro operation: A+B. Second comparator circuit needed to establish if A<B,A>B or A==B.
- Third subtractor circuit is needed to perform the microoperation A-B and B-A.
- The hardware implementation of addition and subtraction in the above figure consist of registers A and B and the sign flip flops A_s and B_s.
- Subtraction is done by adding A to the 2's complement of B.
- The o/p carry is transferred to E.
- The add overflow flip flop(AVF) holds the overflow bit when A and B are added.
- The addition A+B is done through the parallel adder and the sum is transferred to A register.
- When the Mode bit M=0 the output of B register is transferred to the adder, the

input carry is 0 and the output of the adder is equal to sum A+B.

- When M=1, the 1's complement of B is applied to adder, the input carry is 1 and the output is equal to A+ B'+1.

Flow chart for Signed magnitude addition and subtraction

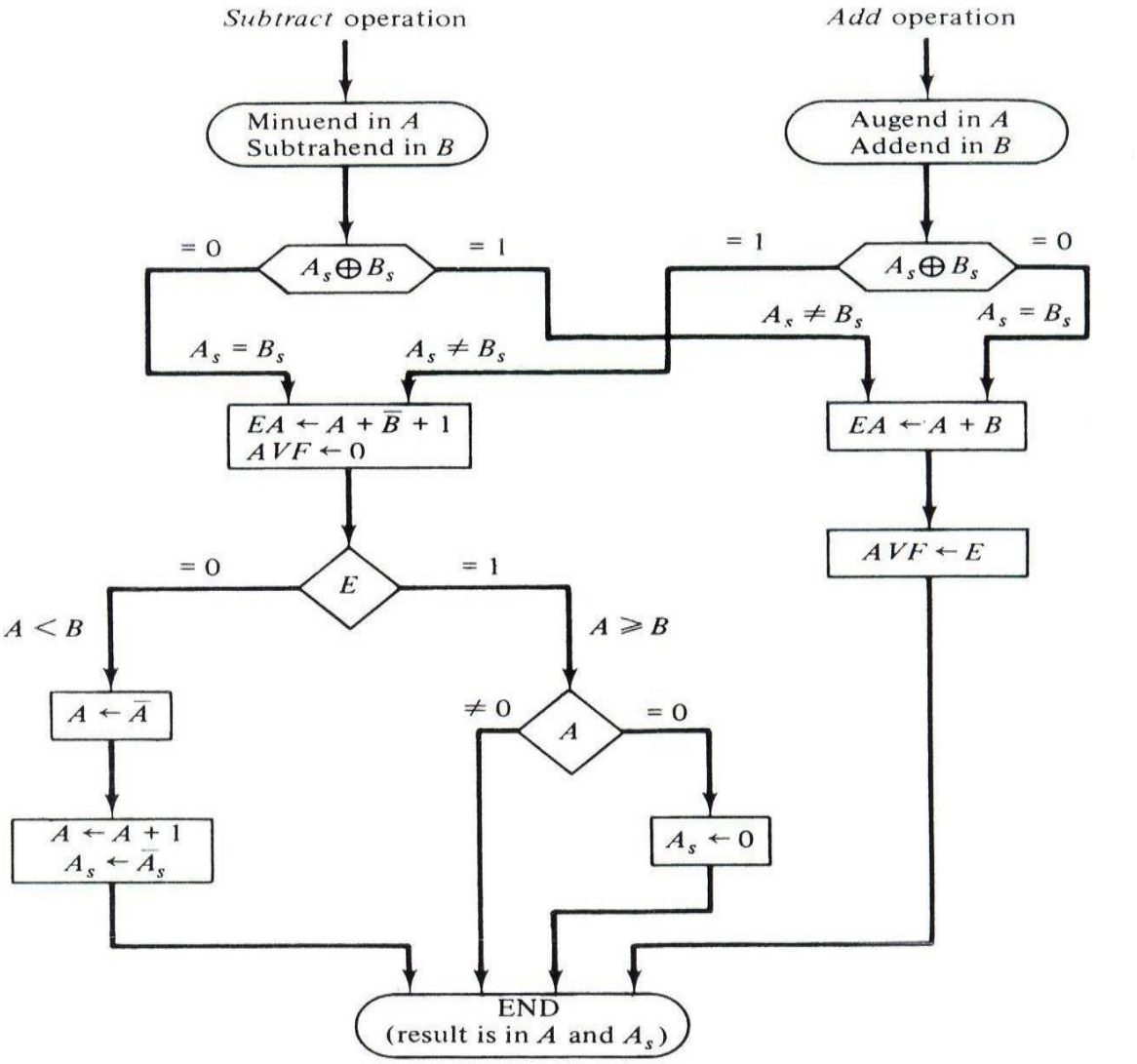

Figure 10-2 Flowchart for add and subtract operations.

- The two signs A, and B, are compared by an exclusive-OR gate.
- If the output of the exclusive-OR gate is 0 the signs are identical; If it is 1, the signs are different.
- For an add operation, identical signs dictate that the magnitudes be added.
- For a subtract operation, different signs dictate that the magnitudes be added.

- The magnitudes are added with a micro operation: EA←A + B, where EA is a register that combines E and A.
- The carry in E after the addition constitutes an overflow if it is equal to 1.
- The value of E is transferred into the add-overflow flip-flop AVF.

- The two magnitudes are subtracted if the signs are different for an add operation or identical for a subtract operation.

- The magnitudes are subtracted by adding A to the 2's complemented B. No overflow can occur if the numbers are subtracted so AVF is cleared to 0.

- If E=1, then the condition is A>=B and the number in A is the correct result.

- If E=0 then the condition is A<B and the number in A is taken 2’s complement which is the correct result.

- If the sign of the result is same as the sign of A, So no change in A_s is required.
- When A<B the sign of the result is the complement of the original sign of A.
- The final result is found in register A and its sign in A_s.

2 input XOR gate

A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0