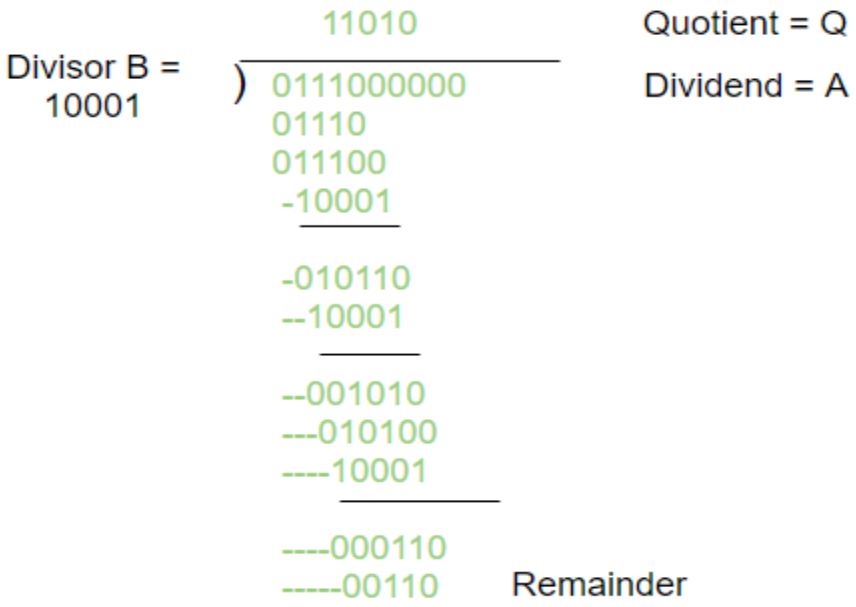
COMPUTER ORGANIZATION AND ARCHITECTURE
UNIT –III
TOPIC- DIVISION OF SIGNED MAGNITUDE DATA PART-1

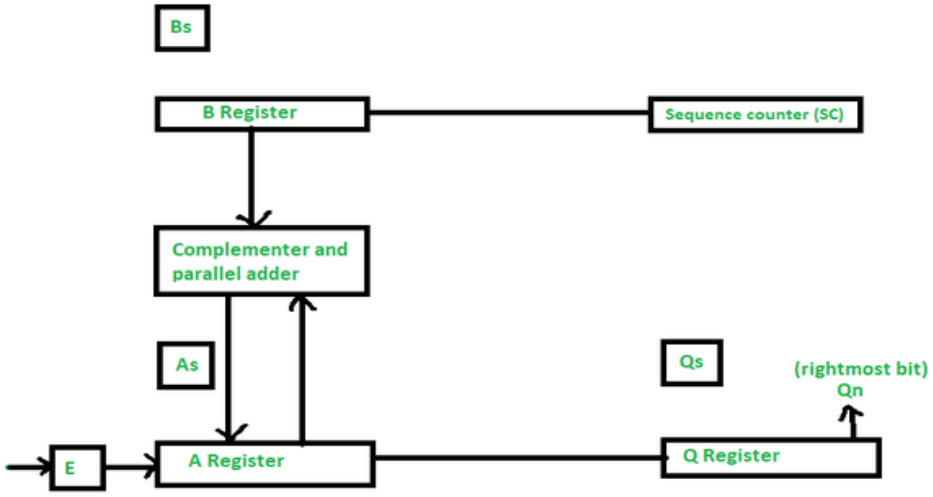
Signed magnitude Division

The Division of two fixed-point binary numbers in the signed-magnitude representation is done by the cycle of successive compare, shift, and subtract operations.



- First the bits of dividend are examined from left to right, until the set of bits examined represent the number greater than or equal to divisor.
- Until this event occurs 0's are placed in quotient from left to right.
- When the event occurs 1 is placed in the quotient and divisor is subtracted from the partial dividend. The result is referred as partial remainder.
- At each cycle of this process, an additional bits from the dividend are appended to the partial remainder, until the result is greater than or equal to the divisor.
- This process continues until all the bits of the dividend are exhausted.

Hardware Implementation:



- The hardware implementation of division is identical to multiplication.
- Here, the divisor is stored in the B register and the double-length dividend is stored in registers A and Q.
- Register EAQ is now shifted to the left with 0 inserted into Q_n and the previous value of E is lost. The dividend is shifted to the left and the divisor is subtracted by adding its 2's complement value.
- End carry gives the information about the relative magnitudes.

Divide overflow

- The division operation may result in a quotient with an overflow.
- The quotient is to be stored in a standard register, so the overflow bit will require one more flip flop for storing the sixth bit.
- The divide overflow condition must be avoided in normal computer operations because the entire quotient will be too long for transfer into a memory unit that has words of standard length.
- Provision to ensure that this condition is detected must be included in either the hardware or the software.
- When the dividend is twice as long as the divisor, the condition for overflow can be stated as follows: a divide overflow condition occurs if the high order half bits of the dividend constitute a number greater than or equal to the divisor.
- Another problem associated with division is the fact that a division by zero must be avoided.
- Overflow condition is usually detected when a special flip flop is set.(DVF)