COMPUTER ORGANIZATION AND ARCHITECTURE
UNIT –III
TOPIC- FLOATING POINT ADDITION & SUBTRACTION PART-1

Floating Point Addition & Subtraction

Introduction

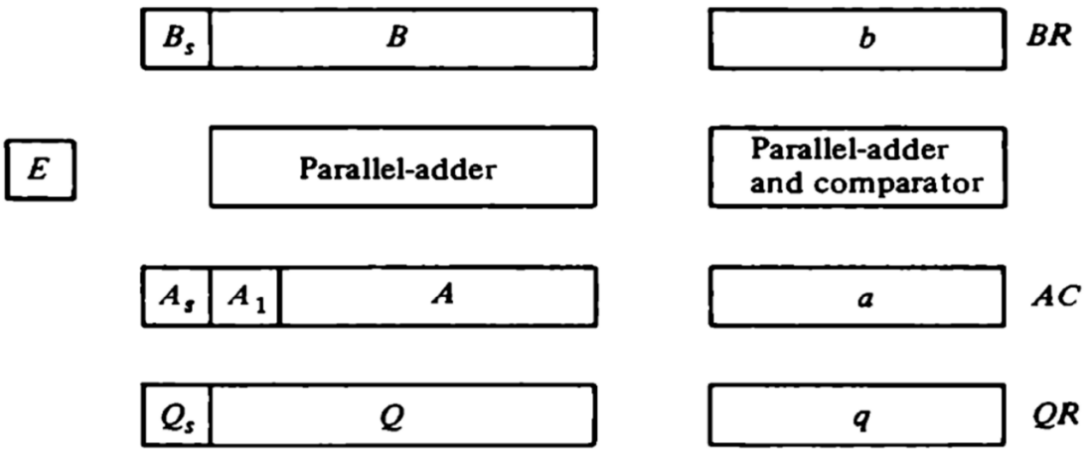
Floating point number in computer register consists of two parts: a mantissa m and exponent e which will be represented as m X r ^{e}

F = m x r^{e}
where m: Mantissa
r: Radix
e: Exponent

Number	Mantissa	Base	Exponent
9x10^8	9	10	8
110x2^7	110	2	7
4364.784	4364784	10	-3

Hardware Implementation

Figure 10-14 Registers for floating-point arithmetic operations.



- The register configuration for floating point operation is quite similar to the layout for fixed point operation.

- The same register and adder used for fixed point arithmetic are used for processing the mantissas.
- The difference lies in the way the exponents are handled.
- There are three registers BR, AC and QR.
- Each register is subdivided into two parts.
- The mantissa part has same upper case letters, the exponent part uses the corresponding lower case letters.
- A parallel adder adds the two mantissas and transfers the sum into A and the carry into E.
- A separate parallel adder is used for the exponents. Since the exponents are biased