PROJECT 1

EE739: - Processor Design

Department of Electrical Engineering

(IIT Bombay)

Submitted By: -

Harshad Bhausaheb Ugale (20307R008)

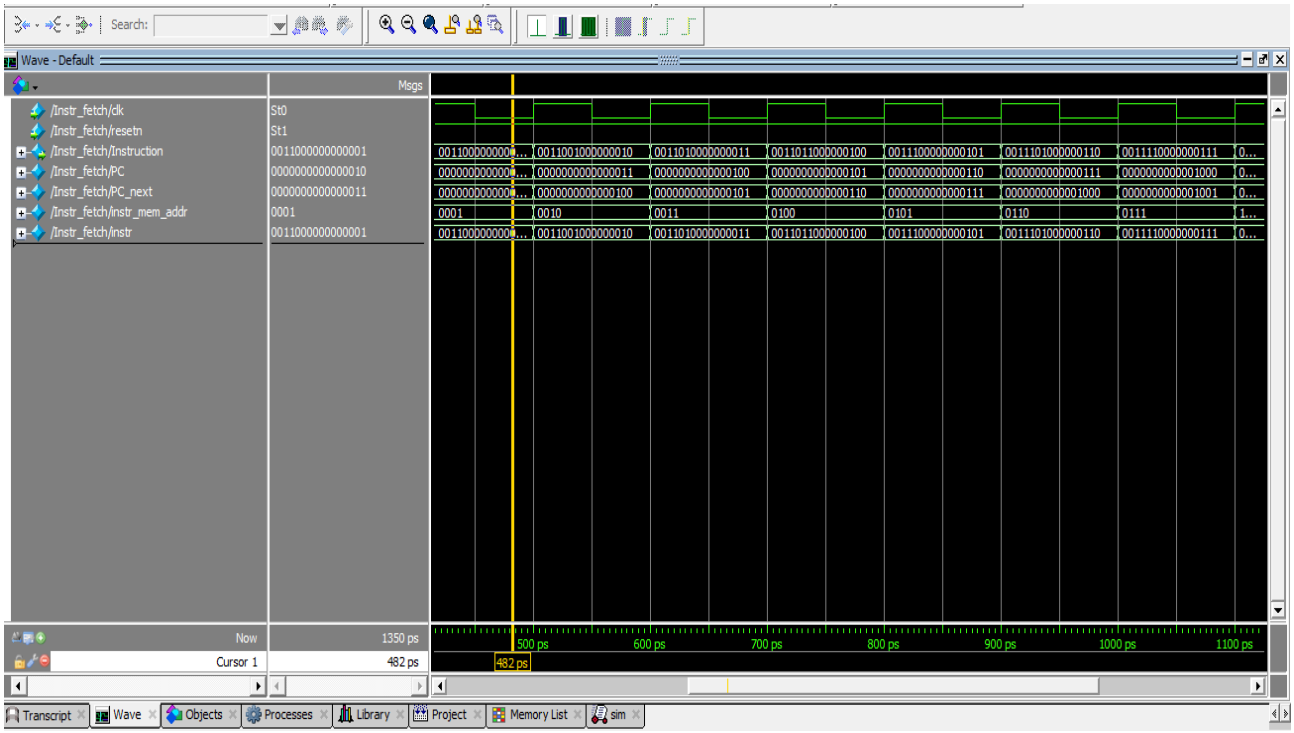
Mahesh Shahaji Patil (20307R010)

Introduction: -

IITB-RISC is a simple yet powerful microprocessor. It has 8 registers, each of 16 bits. The pipelined version of IITB-RISC follows standard six Pipeline stages - Instruction Fetch, Instruction Decode, Register Read, Execution, Memory Access and Write Back. The Data Path components in each stage is listed below along with the result obtained at each stage.

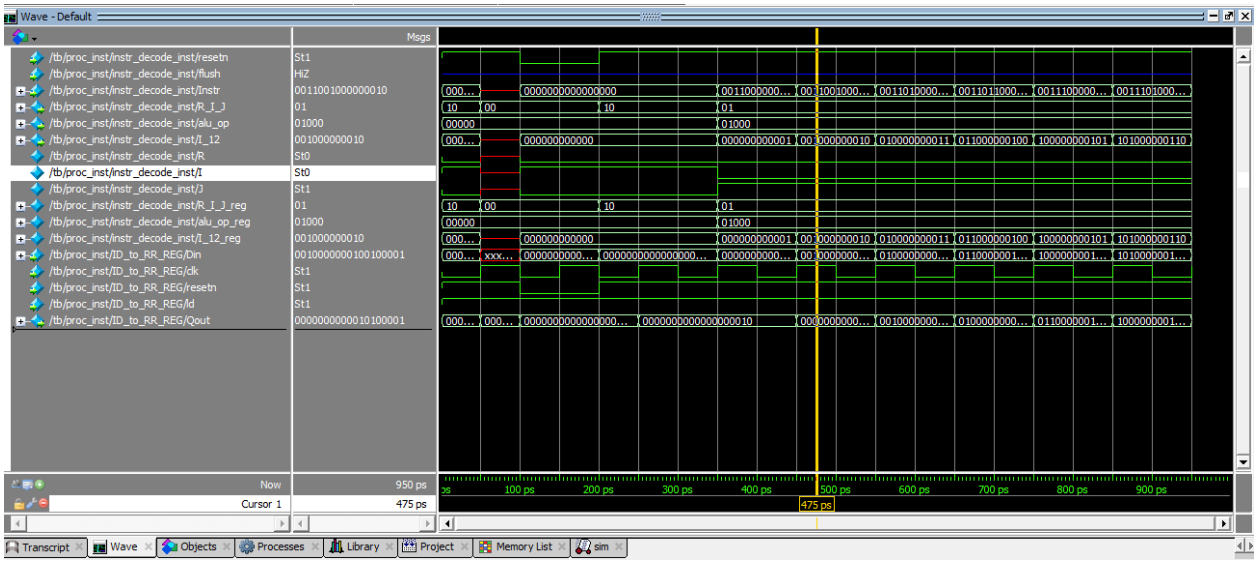
Instruction Fetch: -

This stage fetches the instruction from the instruction memory and stores it in the register placed in between the Instruction Fetch and Instruction Decode stage (IF_to_ID_Reg) so that on the next clock it has to be pass on the decode stage.



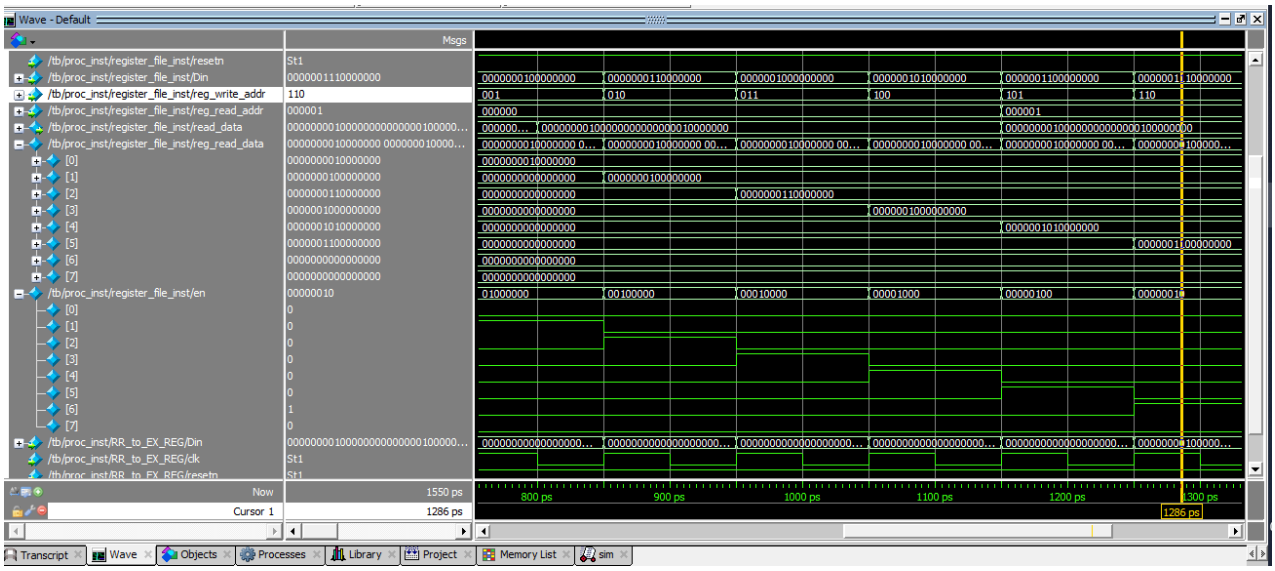
Instruction Decode: -

This stage decodes the instruction came as input from the fetch stage and stores it in the register placed in between the Instruction Decode and Register Read stage (ID_to_RR_Reg) so that on the next clock it has to be pass on the register read stage.



Register Read: -

This stage reads the registers from register file which have been already written by the Write Back stage in the previous execution of the jump type load instructions. The results obtained from the register read stage are stored in the register placed in between the Register Read and Execution stage (RR_to_EX_Reg) so that on the next clock it has to be pass on the Execution stage.

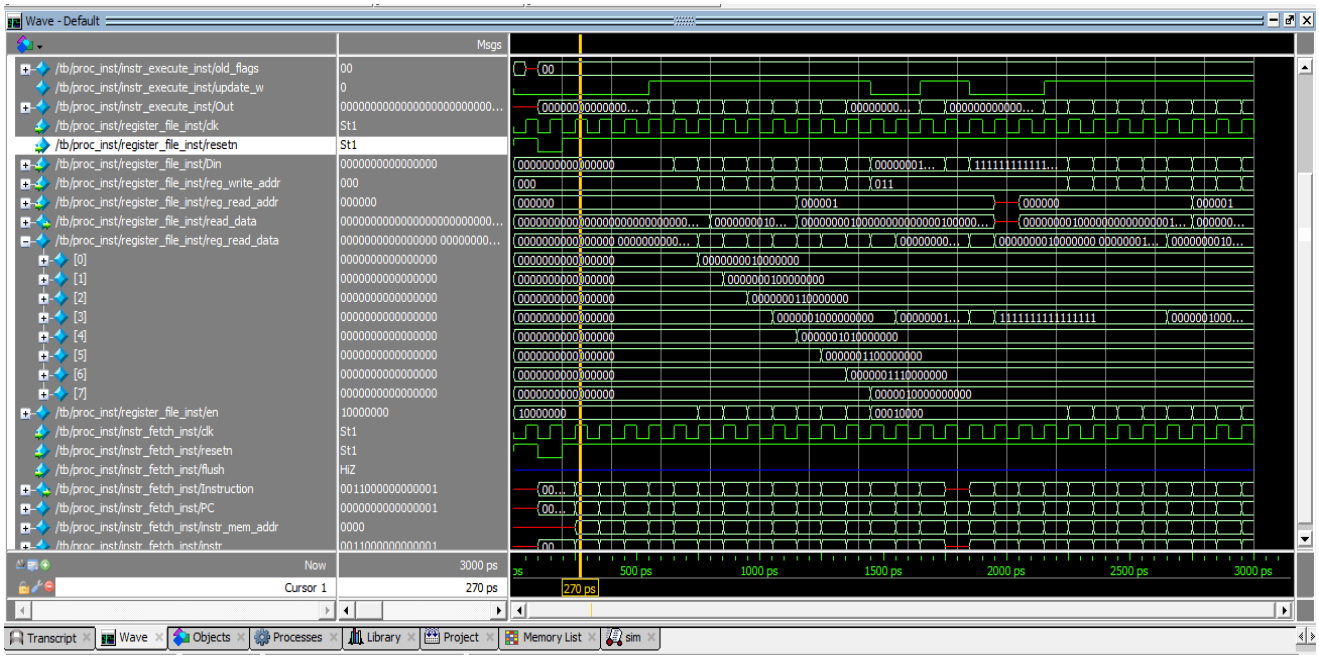


Execution: -

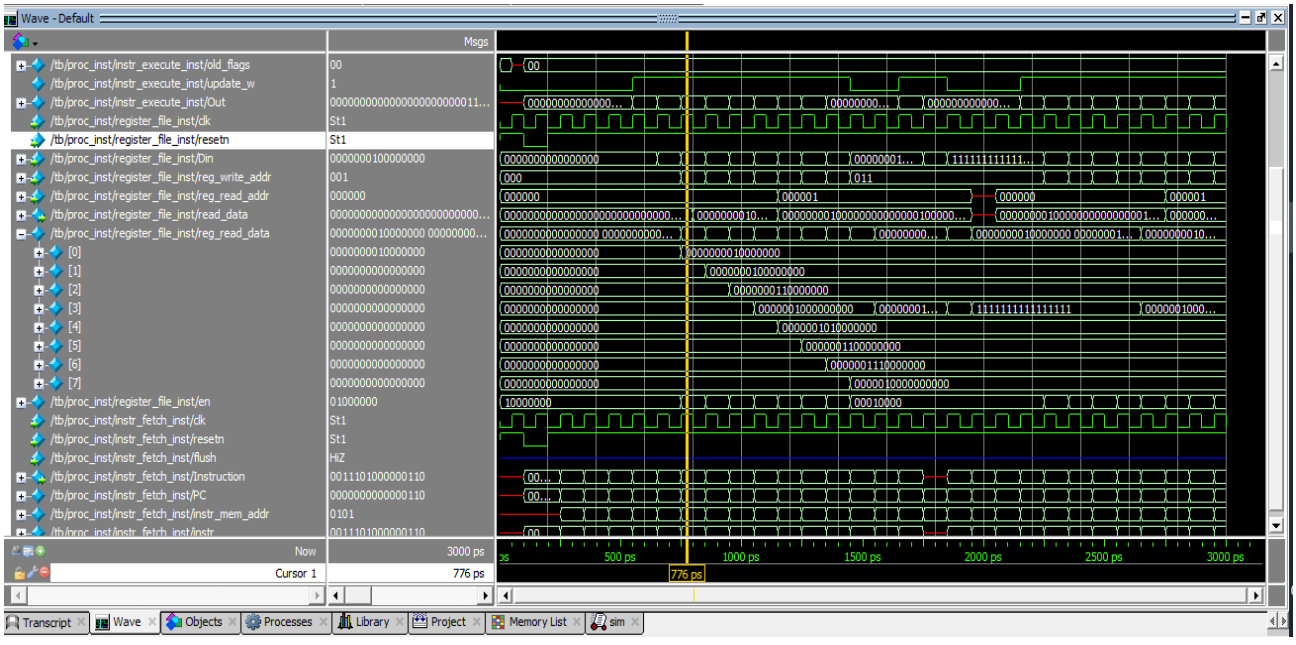
In this stage the execution of the instruction takes place according to the operands defined in the instruction like whether it is ADD, ADC, NDU, LHI, LW, SW, etc. and the results have been produced. The execution stage contains mostly the ALU operations.

LHI R0, 000000001 (1st Instruction From program_instr.hex)

Input: -

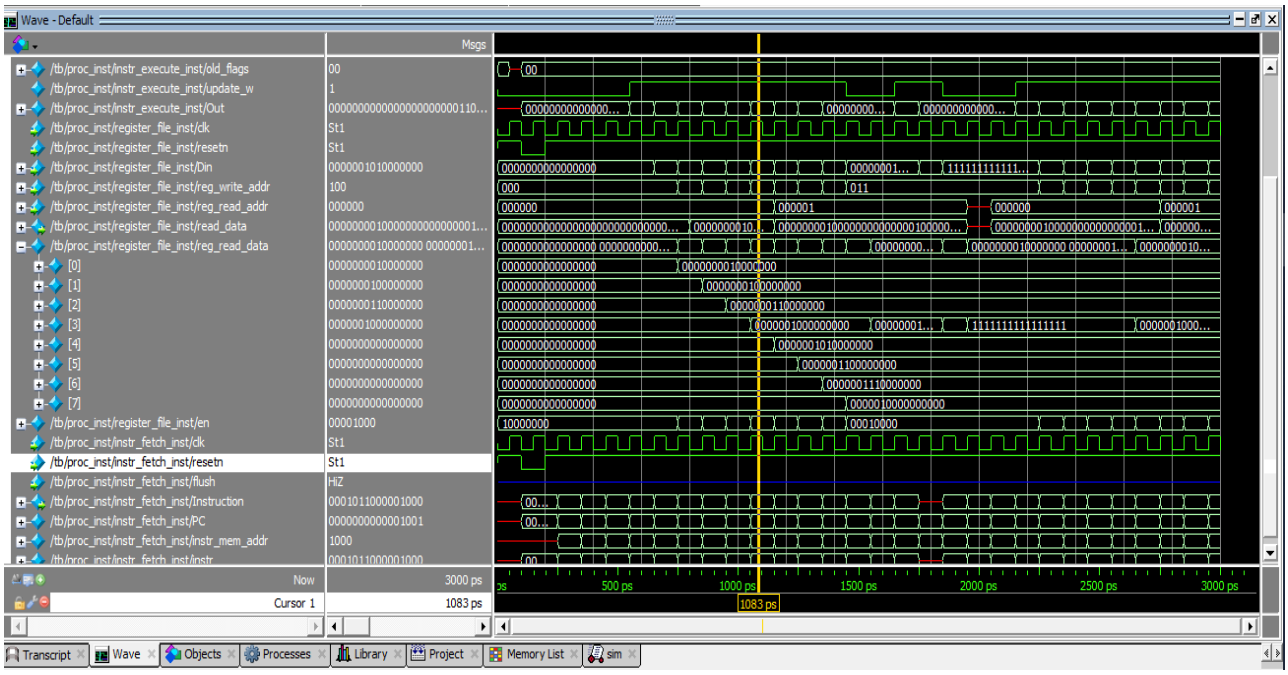


Output: -

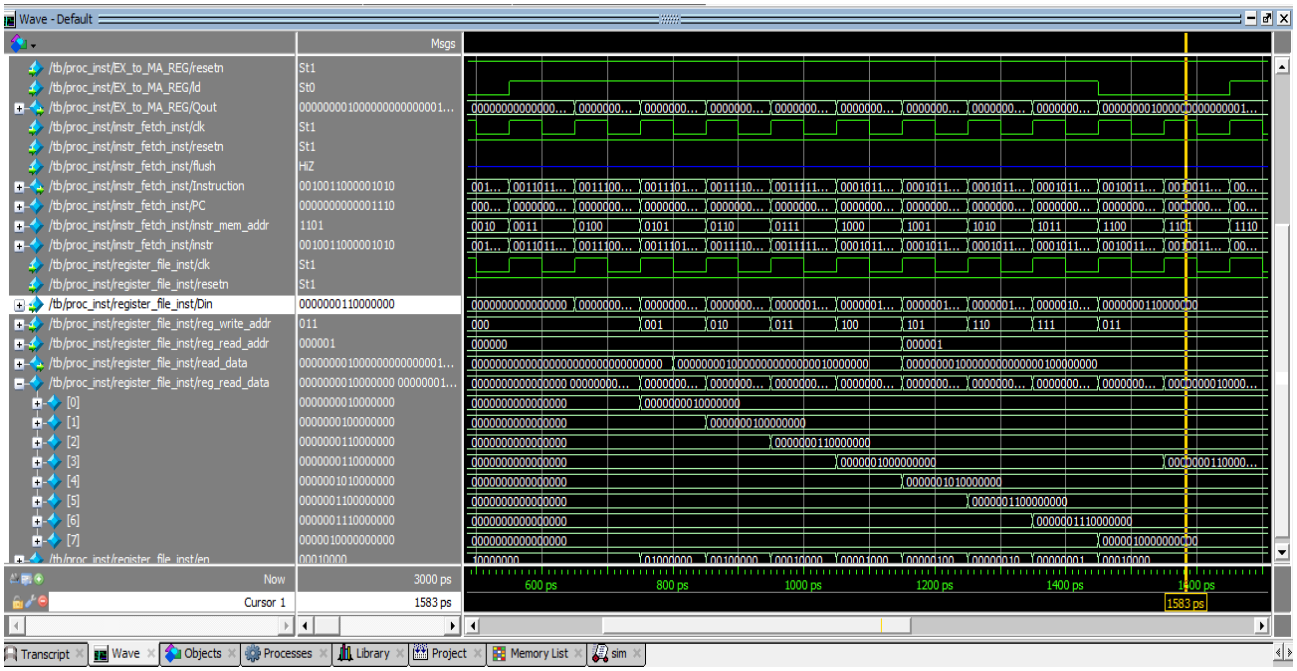


ADD R3, R0, R1 Instruction: -

Input: -

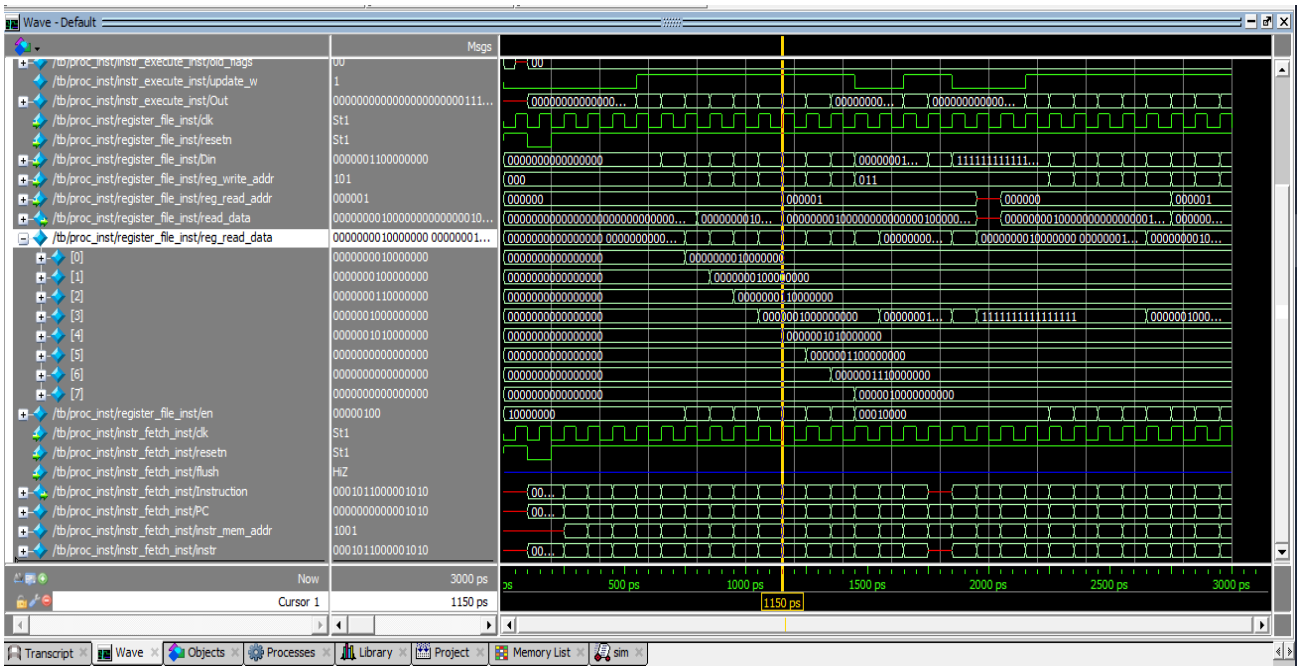


Output: -

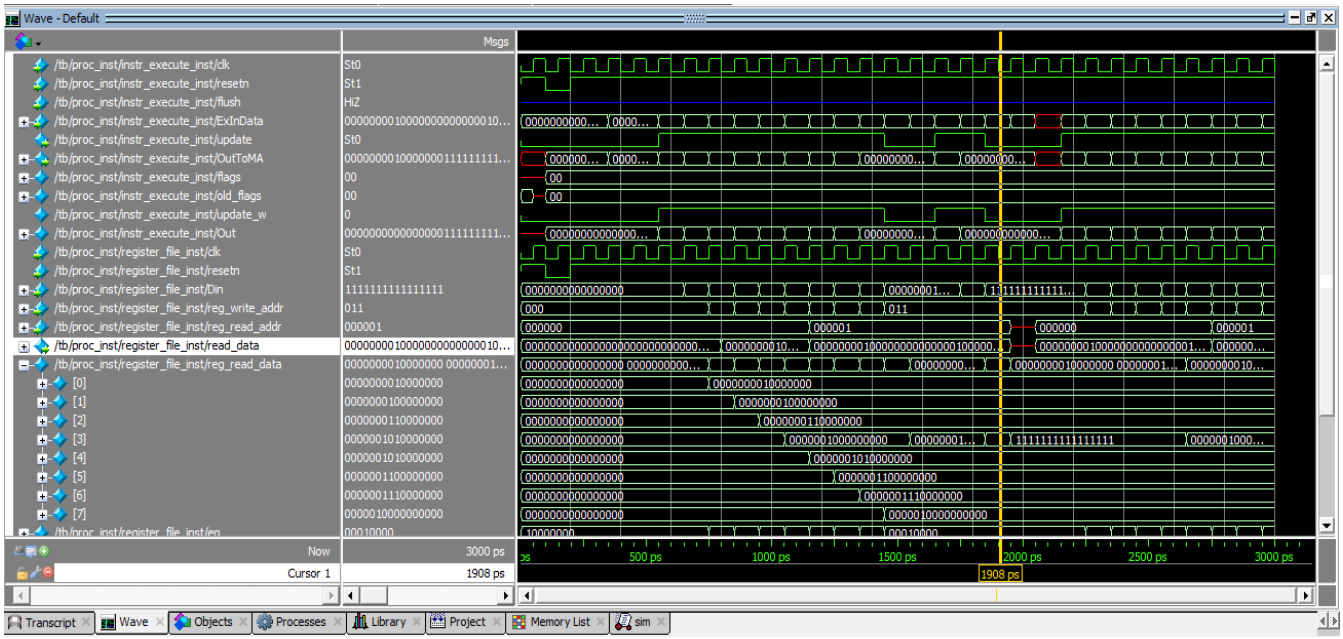


ADC R4, R0, R1 Instruction: -

Input: -

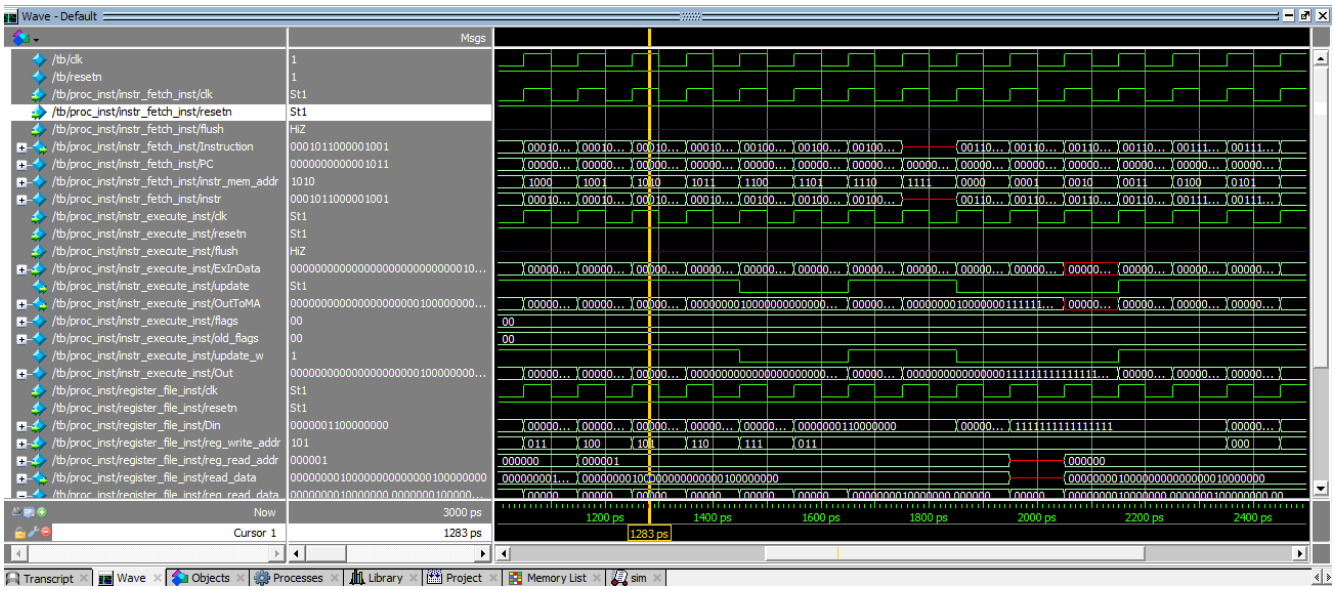


Output: -

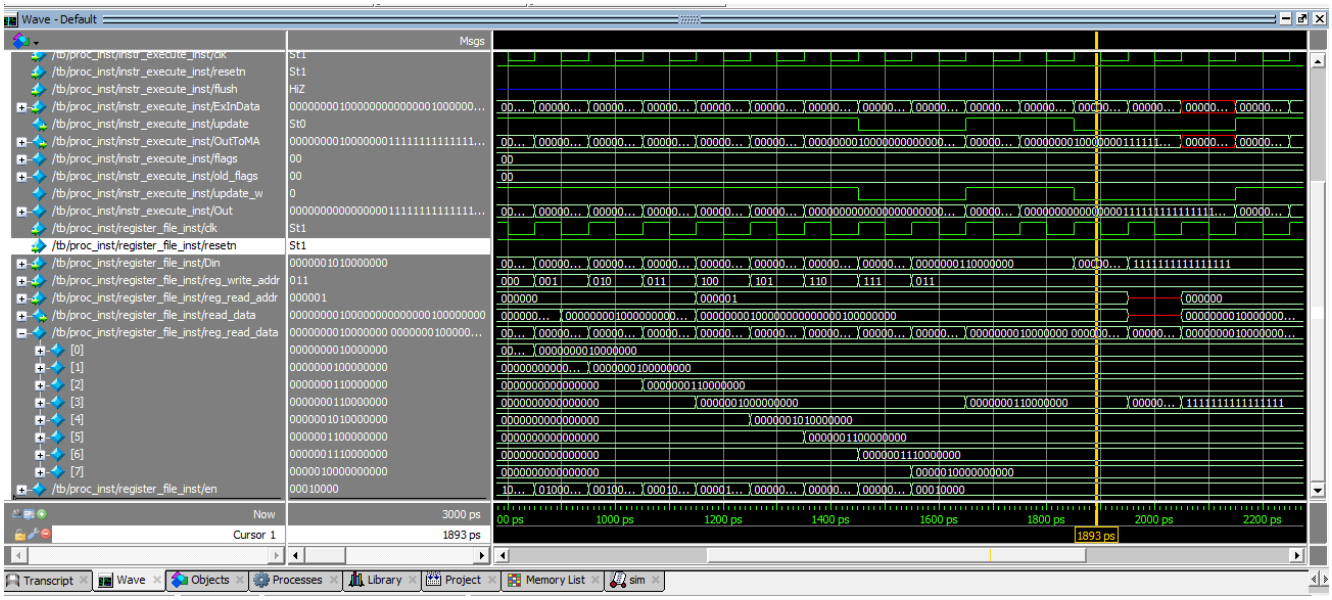


ADZ R5, R0, R1 Instruction: -

Input: -

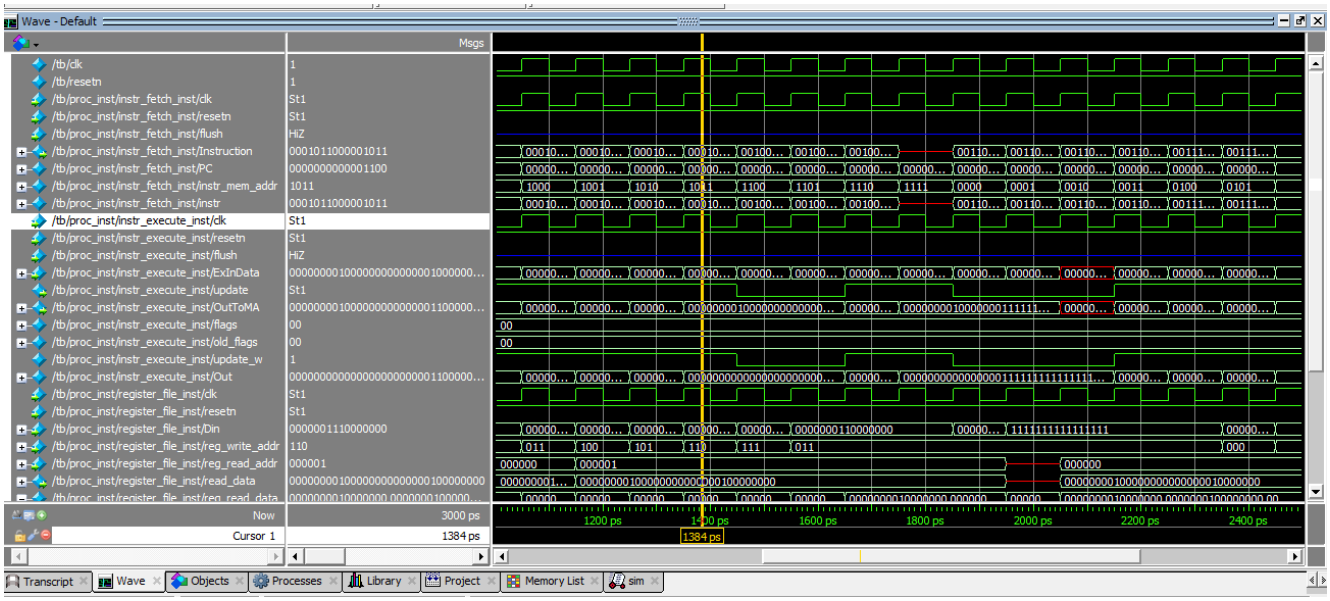


Output: -

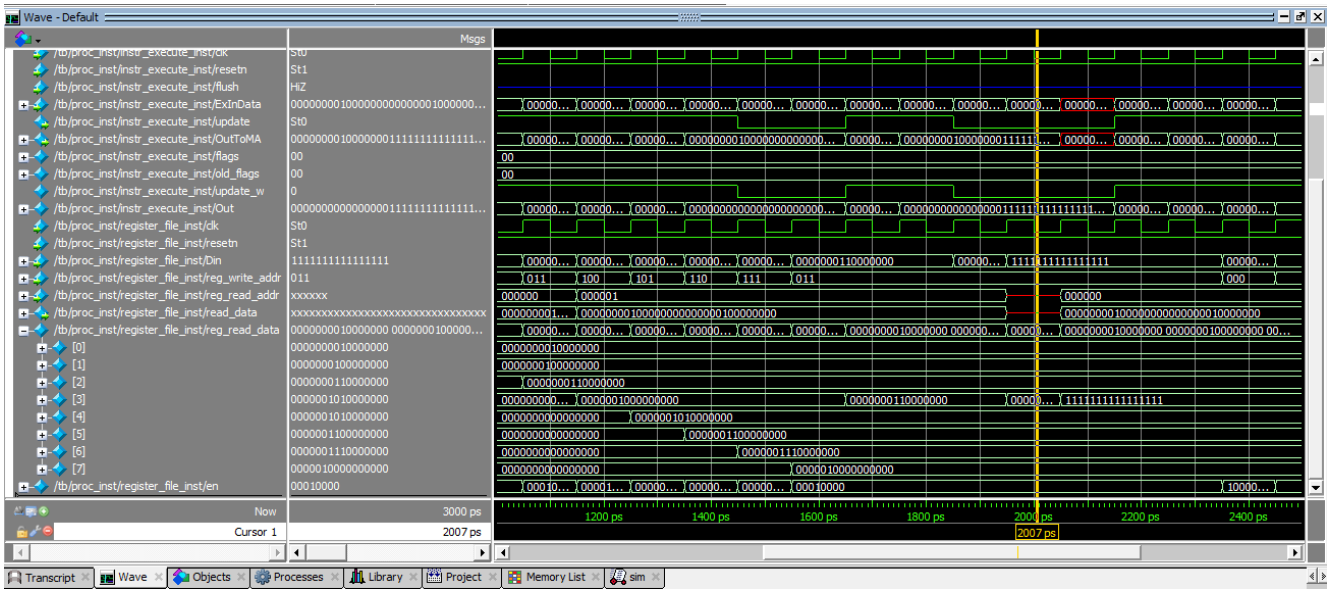


ADL R6, R0, R1 Instruction: -

Input: -

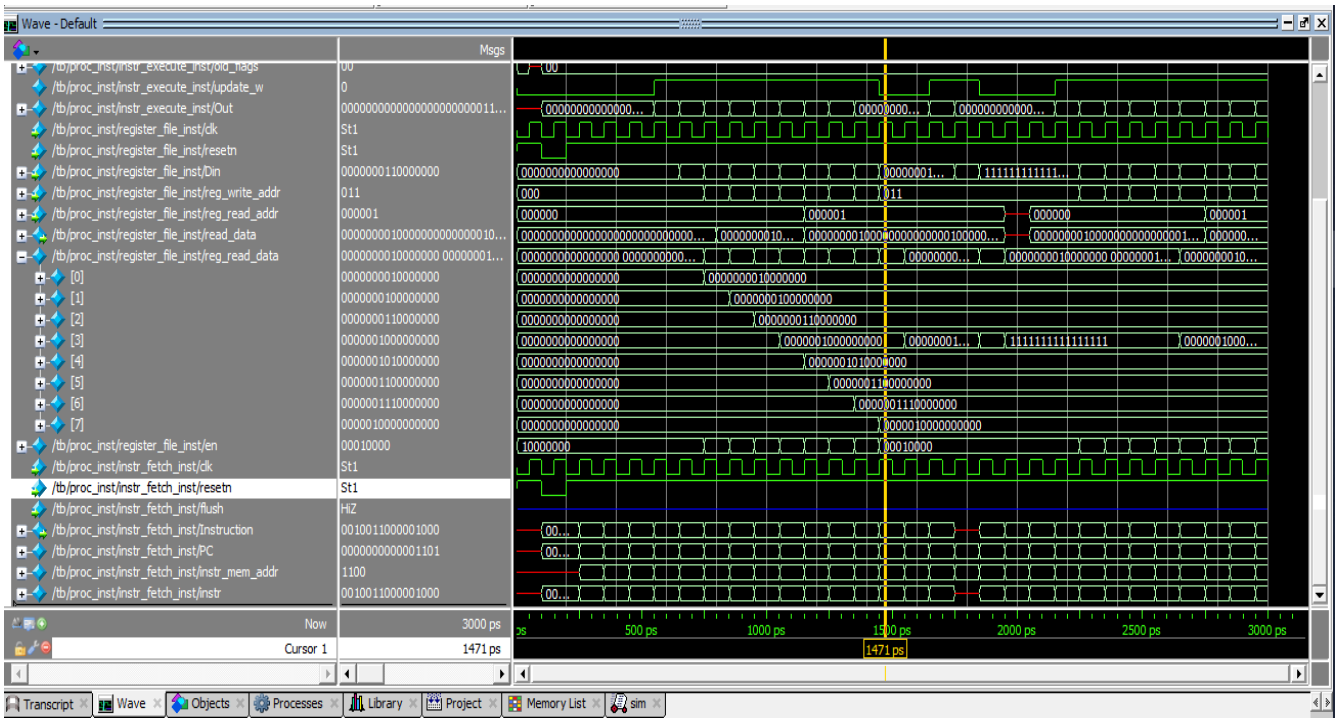


Output: -

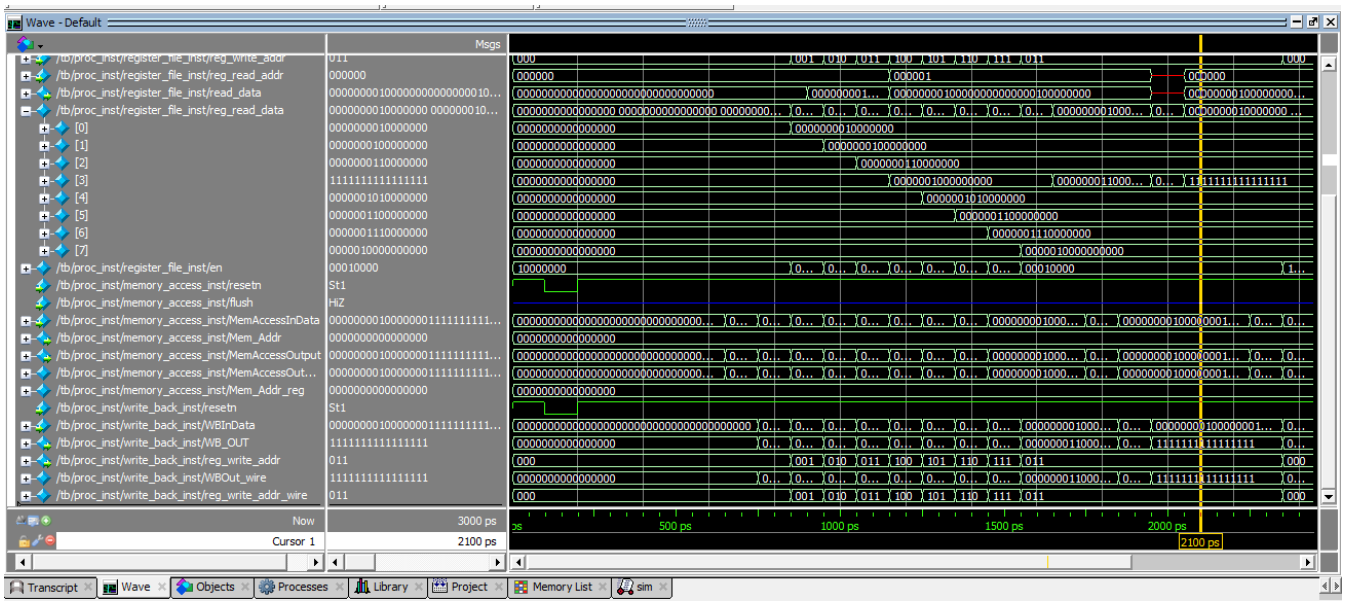


NDU R3, R0, R1 Instruction: -

Input: -

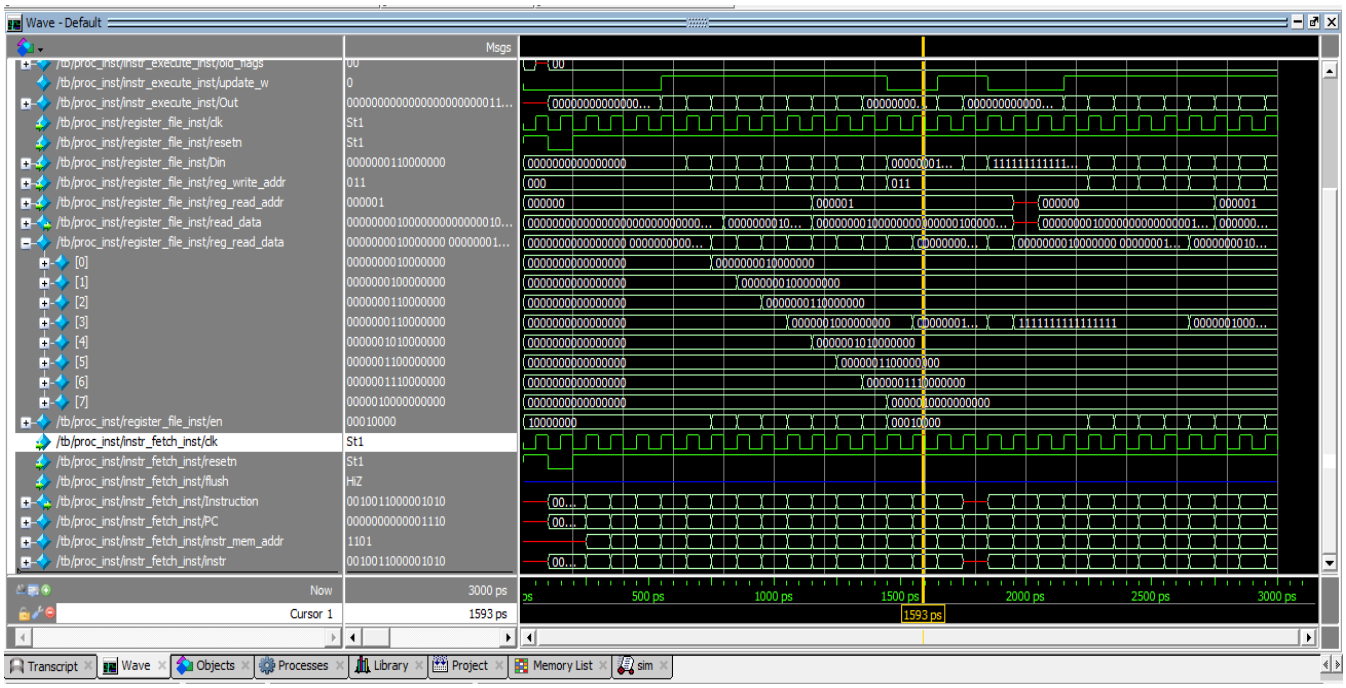


Output: -

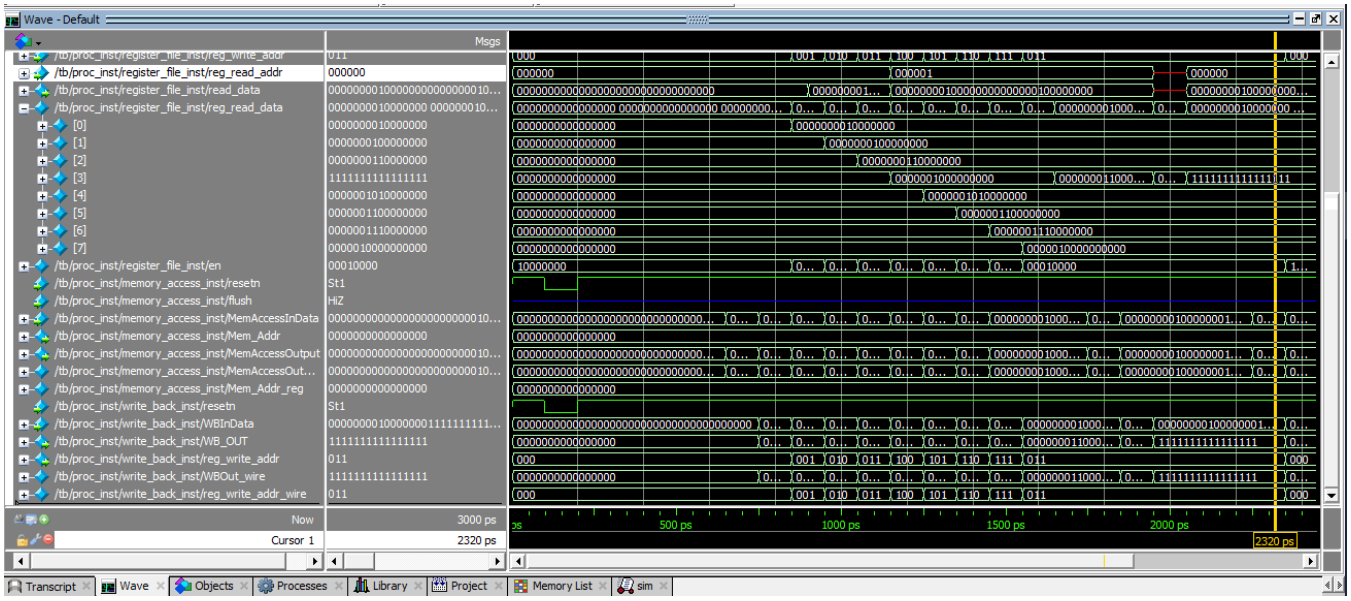


NDC R2, R0, R1 Instruction: -

Input: -

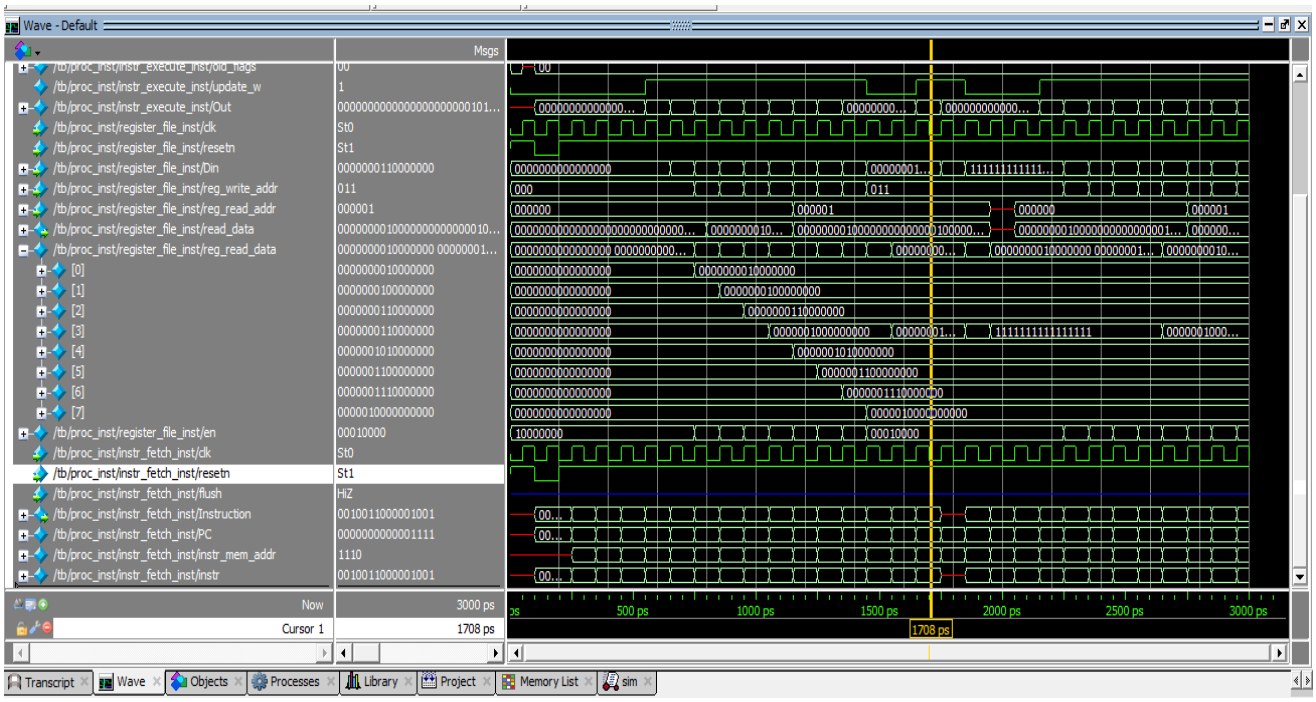


Output: -

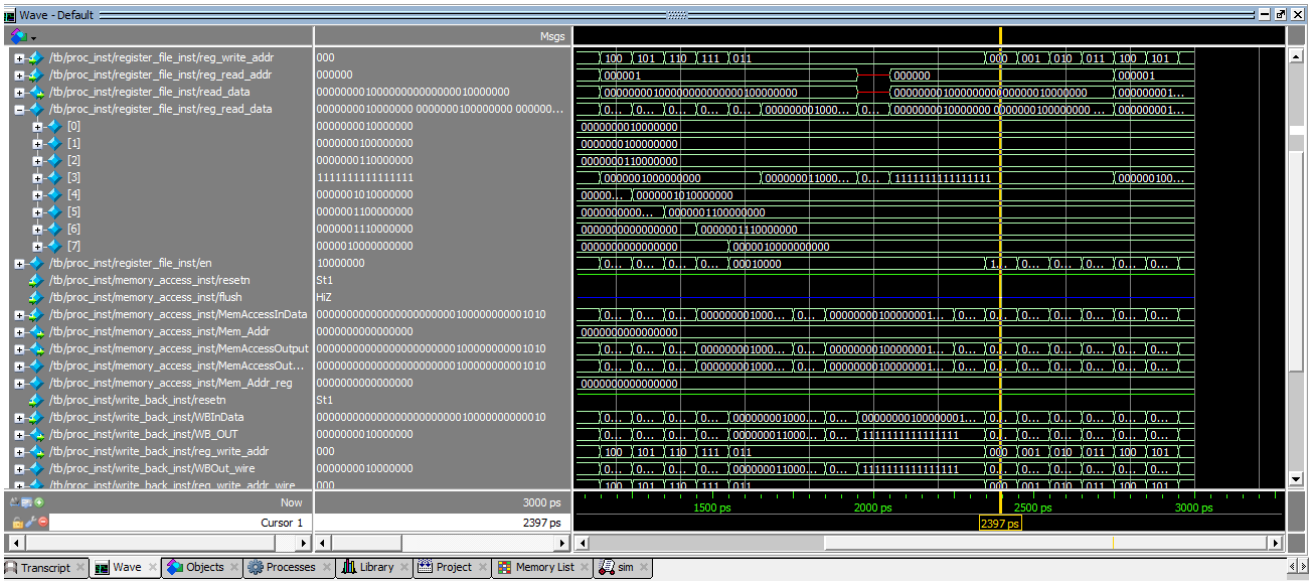


NDZ R4, R0, R1 Instruction: -

Input: -



Output: -



Memory Access: -

In this stage, the access of the memory can be done in the store instruction as specified by instruction. If we write to data into memory or store it, then we can form the address of it using the instruction and then store it using the write back stage.

Write Back: -

With the help of this we can write the data into the register file or into the memory with the help of the address being specified by the bits in the instruction.

Conclusion: -

We have designed and verified the IITB-RISC, 16-bit computer, standard 6 stage pipelined, 8 registers with 16-bit each processor and it has been optimized by performance.

The Raw Datapath Designed for the same: -