Ahsanullah University of Science & Technology

Department of Computer Science & Engineering

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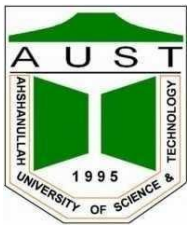


LAB REPORT

Course No: CSE 3110
Course Title: Digital System Design Lab

Experiment Number: 01

Name of the Experiment: Designing a 4-bit ALU (Arithmetic and Logic Unit)

Group No: V
Group Members

Simanta Sarker	18.01.04.010
Shawly Rohman	18.01.04.013
Atanu Kumar Saha	17.02.04.003
Mahin Opu	17.02.04.006
Faisal Ahmmed Tonmoy	17.02.04.025

Introduction:

In this experiment, we made a 4-bit Arithmetic Logic Unit (ALU) using a 4-bit full adder and basic gates. In this experiment, if S2 = 0 then the ALU will perform the arithmetic operation, and if the S2 = 1 then the ALU will perform the logical operation. So, depending on the value of S2 the ALU will perform a logical or arithmetic operation.

Problem Statement:

S2	S1	S0	Output	Function
0	0	0	Ai-Bi-1	Subtract with Borrow
0	0	1	Ai	Transfer A
0	1	0	Ai + 1	Increment A
0	1	1	Ai + Bi + 1	Add with Carry
1	0	X	Ai’	Complement A
1	1	X	Ai | Bi	OR

Function Generation:

S2	S1	S0	Z	X	Y	Output	Function
0	0	0	0	Ai	Bi’	Ai-Bi-1	Subtract with Borrow
0	0	1	0	Ai	0	Ai	Transfer A
0	1	0	1	Ai	0	Ai + 1	Increment A
0	1	1	1	Ai	Bi	Ai + Bi + 1	Add with Carry
1	0	X	0	Ai’	0	Ai’	Complement A
1	1	X	0	Ai | Bi	0	Ai | Bi	OR

$X = \overline{S2}\ Ai + S2\ \overline{S1}\ \overline{Ai} + S2\ S1(A+B)$

$Y = \overline{S2}\ \overline{S1}\ \overline{S0}\ \overline{Bi} + \overline{S2}\ S1\ S0\ Bi$
$= \overline{S2}\ (\overline{S1}\ \overline{S0}\ \overline{Bi} + S1\ S0\ Bi)$

K-Map Simplification:

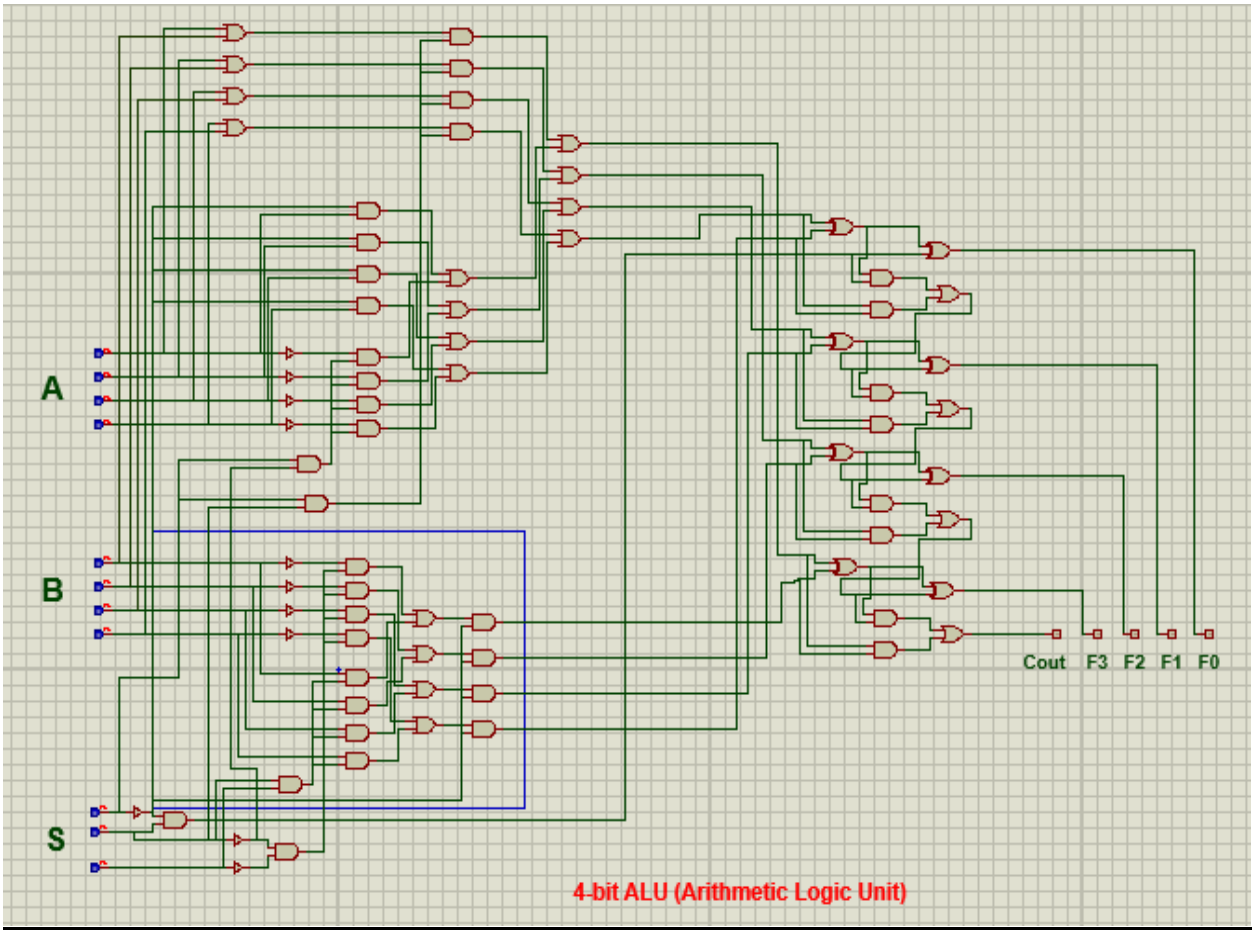
S1S0 / S2	$\overline{S1}\ \overline{S0}$	$\overline{S1}\ S0$	S1 S0	S1 $\overline{S0}$
$\overline{S2}$	0	0	(1)	(1)
S2	0	0	0	0

$Z = \overline{S2}\ S1\ \overline{S0} + \overline{S2}\ S1\ S0$
$= \overline{S2}\ S1(\overline{S0} + S0)$
$= \overline{S2}\ S1$

Equipment and Budget:

IC Name	IC Number	Amount	Price per IC (Tk)	Price (Tk)
AND Gate	7408	10	25	250
OR Gate	7432	5	28	140
NOT Gate	7404	2	20	40
XOR Gate	7486	2	25	50
			Total:	480 Tk

Simulation:



Result:

For A=1110 and B=0101, these results can be observed:

S2	S1	S0	Output	Function	Cout	F3	F2	F2	F0
0	0	0	Ai-Bi-1	Subtract with Borrow	1	1	0	0	0
0	0	1	Ai	Transfer A	0	1	1	1	0
0	1	0	Ai + 1	Increment A	0	1	1	1	1
0	1	1	Ai + Bi + 1	Add with Carry	1	0	1	0	0
1	0	X	Ai’	Complement A	0	0	0	0	1
1	1	X	Ai | Bi	OR	0	1	1	1	1

Conclusion:

There were some errors while working with Dual carry save full adder (IC 74LS183). While working with IC74LS183 the proteus software was showing some errors such as (No model specified, Simulation Failed due to partition analysis error). But even after fixing these errors the circuit was not showing any output. After that, we built a 4-bit Binary full adder. After using that, the circuit worked perfectly and there was no error during simulation. All operations worked without generating any error.