AIM:TO IMPLEMENT DECODERS

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity decoder is

Port ( I : in STD\_LOGIC\_VECTOR (1 downto 0);

Y : out STD\_LOGIC\_VECTOR (3 downto 0));

end decoder;

architecture Behavioral of decoder is

begin

process (I)

begin

case I is

when "00" => Y <= "0001" ;

when "01" => Y <= "0010" ;

when "10" => Y <= "0100" ;

when others => Y <= "1000" ;

end case;

end process;

end Behavioral;

**DECODER \_TB CODE:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity decoder\_tb is

end entity;

architecture tb of decoder\_tb is

component decoder is

Port ( I : in STD\_LOGIC\_VECTOR (1 downto 0);

Y : out STD\_LOGIC\_VECTOR (3 downto 0));

end component;

signal I: STD\_LOGIC\_VECTOR(1 downto 0);

signal Y: STD\_LOGIC\_VECTOR(3 downto 0);

begin

uut: decoder port map(

I => I, Y => Y);

stim: process

begin

I <= "00";

wait for 20 ns;

I <= "01";

wait for 20 ns;

I <= "10";

wait for 20 ns;

I <= "11";

wait for 20 ns;

wait;

end process;

end tb;