**AIM: TO IMPLEMENT BINARY TO GRAY CONVERTER**

library ieee;

use ieee.std\_logic\_1164.all;

entity b2g is

port (bin : in std\_logic\_vector(3 downto 0);

g : out std\_logic\_vector(3 downto 0));

end b2g;

architecture b2g\_arch of b2g is

begin

g(3) <= bin(3);

g(2) <= bin(3) xor bin(2);

g(1) <= bin(2) xor bin(1);

g(0) <= bin(1) xor bin(0);

end b2g\_arch;

**BINTOGREY TESTBENCH CODE**

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY bin2grey IS

END bin2grey;

ARCHITECTURE behavior OF bin2grey IS

component b2g is

port( bin : in std\_logic\_vector(3 downto 0);

g : out std\_logic\_vector(3 downto 0)

);

end component;

signal bin,g,b\_out : std\_logic\_vector(3 downto 0) := (others => '0');

BEGIN

uut1: b2g port map (

bin => bin,

g=> g

);

stim\_proc: process

begin

bin <= "0000"; wait for 10 ns;

bin <= "0001"; wait for 10 ns;

bin <= "0010"; wait for 10 ns;

bin <= "0011"; wait for 10 ns;

bin <= "0100"; wait for 10 ns;

bin <= "0101"; wait for 10 ns;

bin <= "0110"; wait for 10 ns;

bin <= "0111"; wait for 10 ns;

bin <= "1000"; wait for 10 ns;

bin <= "1001"; wait for 10 ns;

bin <= "1010"; wait for 10 ns;

bin <= "1011"; wait for 10 ns;

bin <= "1100"; wait for 10 ns;

bin <= "1101"; wait for 10 ns;

bin <= "1110"; wait for 10 ns;

bin <= "1111"; wait for 10 ns;

wait;

end process;

end;