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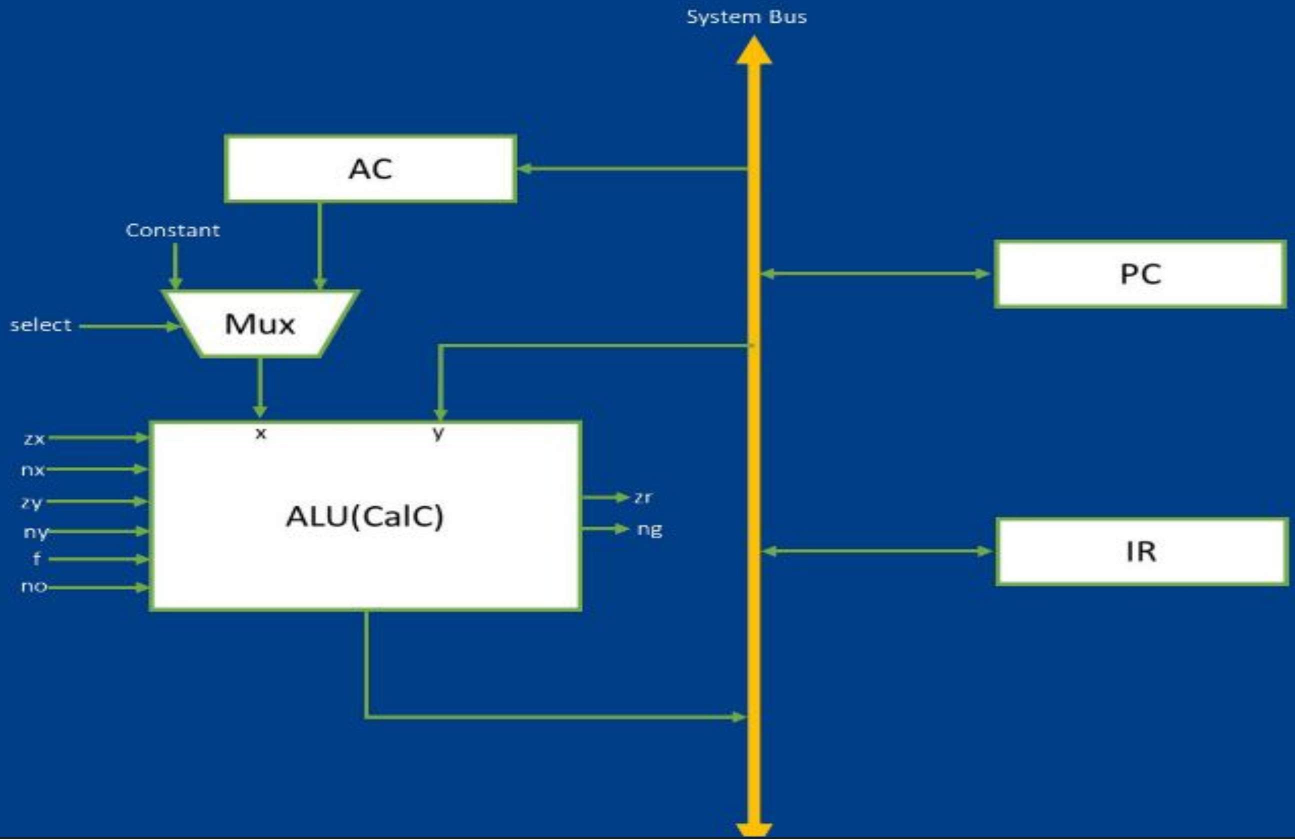
BACKGROUND and AREA OF INTEREST

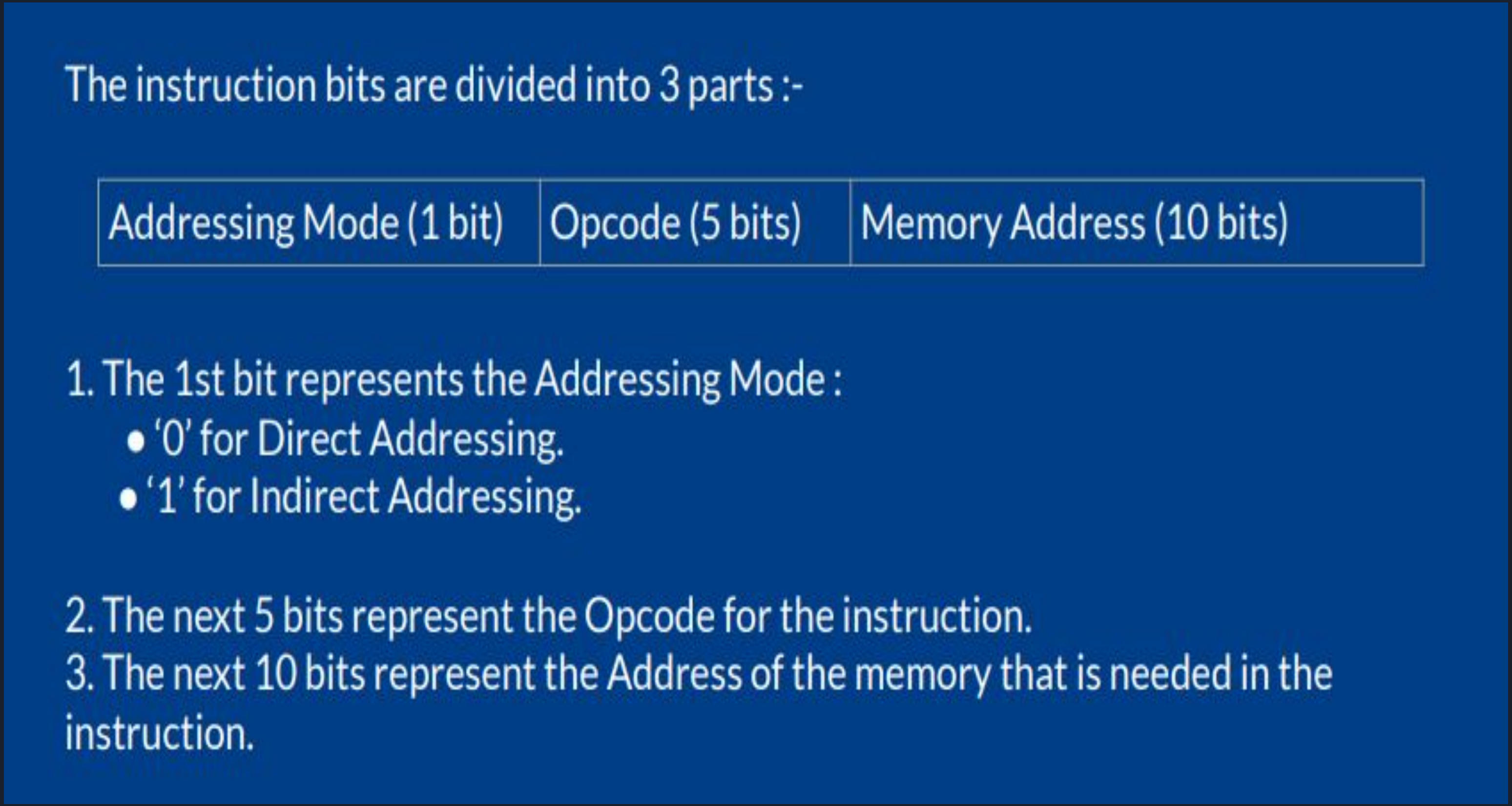
- Digital/Integrated Circuit Design
- Verilog
- Computer Architecture
- Microprocessor Design
- Static Time Analysis(STA)
- Power Electronics

PROJECT 1:
MICROPROCESSOR PROTOTYPE

- Designed a prototype of a complete Von Neumann accumulator-based microprocessor in HDL and tested it on a given set of instructions and data.
- It is a 16-bit CPU which uses an 2KB (1K x 16) memory and address for code segment and data segment of memory is 0-0x190 and 0x191-0x3FF respectively.

The CPU architecture is shown below :





The instruction bits are divided into 3 parts :-

Addressing Mode (1 bit)	Opcode (5 bits)	Memory Address (10 bits)

1. The 1st bit represents the Addressing Mode :
   - '0' for Direct Addressing.
   - '1' for Indirect Addressing.

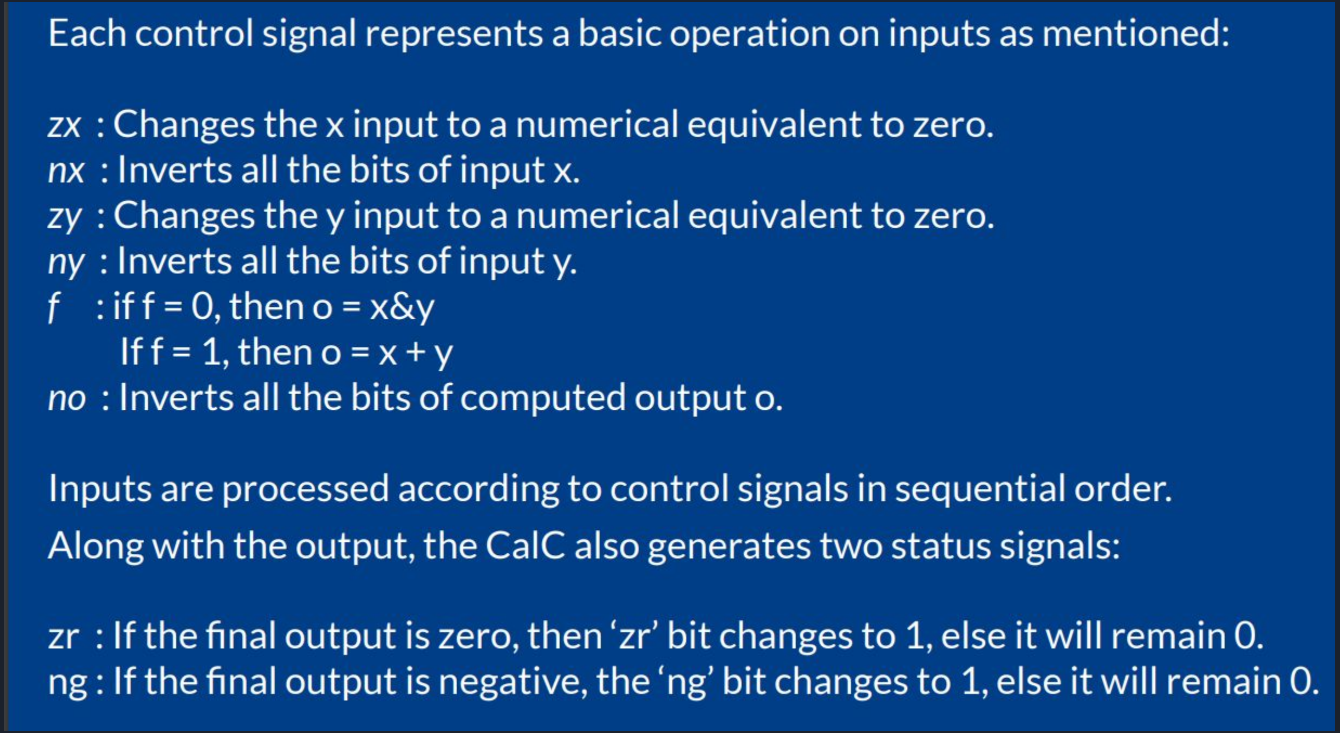
2. The next 5 bits represent the Opcode for the instruction.
3. The next 10 bits represent the Address of the memory that is needed in the instruction.

The CPU takes 4 high levels of the clock to complete one single instruction.

- State 00: The address of the instruction is equated to the counter (PC) and the next state is set to 01.
- State 01: The instruction is fetched from external memory and the bits of the instruction are decoded. The next state is set to 10.
- State 10: The mode of the instruction is checked. If the mode is indirect, then the effective address is calculated. The next state is set to 11.
- State 11: The opcode of the instruction is decoded and the appropriate ALU operation is performed. The output of the ALU is stored in the AC register. The next state is set to 00.

ALU(CalC) Designing:

ALU is performing logical and arithmetic operations on two 16 bit digital inputs(‘X’ and ‘Y’) and returning an 16 bit output (‘o’)



Each control signal represents a basic operation on inputs as mentioned:

zx : Changes the x input to a numerical equivalent to zero.
nx : Inverts all the bits of input x.
zy : Changes the y input to a numerical equivalent to zero.
ny : Inverts all the bits of input y.
f : if f = 0, then o = x&y
If f = 1, then o = x + y
no : Inverts all the bits of computed output o.

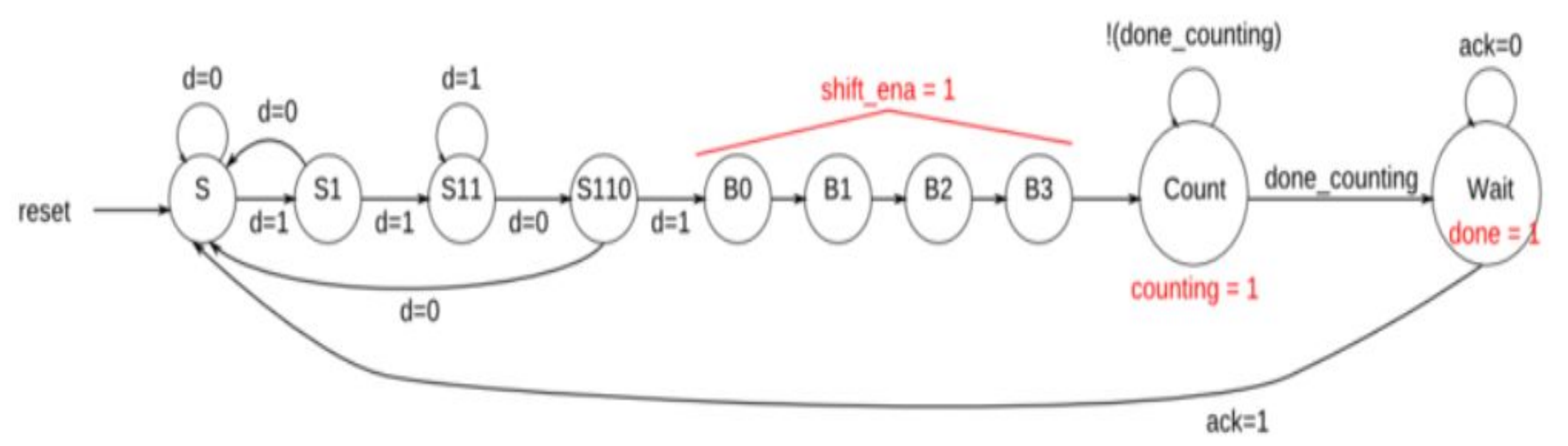
Inputs are processed according to control signals in sequential order.

Along with the output, the CalC also generates two status signals:

zr : If the final output is zero, then ‘zr’ bit changes to 1, else it will remain 0.
ng : If the final output is negative, the ‘ng’ bit changes to 1, else it will remain 0.

PROJECT 2: FSM TIMER

- Timer is started when a particular input pattern (1101) is detected,
- It shifts in 4 more bits to determine the duration to delay,
- waits for the counters to finish counting, and
- notifies the user and waits for the user to acknowledge the timer



PROJECT 3:
FIBONACCI SERIES FSM

- Implemented a Fibonacci series generator using Finite State Machine (FSM) in Verilog .
- Fibonacci sequence : `F(n) = F(n - 1) + F(n - 2)`
- The first two numbers in the sequence are 0 and 1.
- `0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233`.........
- Designed 4 state FSM.
- The first state is ideal and next two are for the two initial terms, and the fourth last does the the calculation.

PROJECT 4:
Photovoltaic Three-Phase DC to AC Grid synchronization Simulation

- It is my Exploratory project under the supervision of Prof. Santosh Kumar Singh .
- First generated solar voltage at a constant power rating using a solar panel box in MATLAB.
- Built DC to DC Boost converter using MPPT to boost the solar voltage.
- Simulated a 3-phase 120-degree notation Inverter using the SPWM technique.

THANK YOU