1. **Course Code:**
2. **Course Title:**
3. **Credit Hours:**
4. **Contact Hours:**
5. **Type: Core, Engineering**
6. **Prerequisite:**
7. **Instructor’s Information:**

*Instructor*:

*Designation*:

*Office Location*:

*Email*:

1. **Course Rationale / Summary:**

(Demo) The purpose of this course is to provide an overview of the architecture and organization of a computer hardware system and how it is built. Initially necessary preliminaries required for analyzing and measuring the computer performance are taught. This course familiarizes students with CPU, memory, I/O organization, peripheral and also the contemporary design and implementation of microprocessors.

1. **Course Objective:** (Demo)The objectives of this course are to
   * 1. To introduce the student with CPU, memory, I/O organization and peripherals.
     2. To introduce students to the contemporary design and implementation of microprocessors.
     3. To help the student to demonstrate an understanding of micro architecture concepts and features employed by contemporary microprocessors, such as pipelining, data forwarding, superscalar, branch predictors and also competence of basic skills in optimizing assembly programs.

1. **Course Outcomes (COs):**

(Demo) Upon successful completion of this course, students will be able to:

|  |  |  |
| --- | --- | --- |
| **#** | **CLO Description** | **Weightage (%)** |
| 1. | **Understand** the basic organization of computer and different instruction formats and addressing modes. Various modes of data transfer between CPU and I/O devices | 25 |
| 2. | **Analyze** the performance of computer systems using metrics, various issues related to memory hierarchy, various modes of data transfer between CPU and I/O devices, the impact of memory hierarchy on performance. Analyze techniques like interrupts, direct memory access (DMA), and I/O channeling. | 45 |
| 3. | **Illustrate** the working of the CPU, datapath, and control signals during  instruction execution through clear diagrams and examples. Use visual  aids to explain complex processes like pipelining, memory management,  and I/O operations effectively. | 30 |

1. **Mapping of CO-PO:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **CLOs** |  | **PLOs** | **DL** | **KP** | **EP** | **EA** | **Teaching**  **Learning**  **Strategy (TLS)** | **Assessment**  **Strategy (AS)** |
| CLO1 | **Understand** the basic organization of computer and different instruction formats and addressing modes. Various modes of data transfer between CPU and I/O devices. | PLO1 | C2 | K3,  K4 | EP1,  EP3,  EP4 | - | Lecture, Class discussion, Note | Exam, Quiz,  Assignment |
| CLO2 | **Analyze** the performance of computer systems using metrics, various issues related to memory hierarchy, various modes of data transfer between CPU and I/O devices, the impact of memory hierarchy on performance. Analyze techniques like interrupts, direct memory access (DMA), and I/O channeling. | PLO2 | C3 | K3,  K4 | EP1,  EP3,  EP4 | - | Discussion, Assignment | Assignment, Quiz, Exam |
| CLO3 | **Illustrate** the working of the CPU, datapath, and control signals during  instruction execution through clear diagrams and examples. Use visual  aids to explain complex processes like pipelining, memory management,  and I/O operations effectively. | PLO2 | C3 | K2,  K4 | EP1,  EP3,  EP4 | - | Lecture, Assignment, Quiz | CT, Assignment |
| **Note: DL:** Domain/level of learning taxonomy, **KP:** Knowledge Profile, **EP:** Attribute of Complex Engineering Problems, **EA:** Attribute of Complex Engineering Activities, **Learning Domains** (C: Cognitive, A: Affective, P: Psychomotor) | | | | | | | | |

1. **Resources:**

**Text Books:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **#** | **Name of Authors** | **Title of Book** | **Edition** | **Publisher’s Name** | **Year** | **ISBN** |
| **1.** | John Hennesy,  David  Patterson, | Computer  Organization | 3rd  Edition | Morgan Kaufman  publisher | 2005 | ISBN: 1-  55860-604-1 |

1. **Course Assessment Pattern:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | **CIE (70 marks)** |  | **SEE**  **(30marks)** |
| **Cognitive learning** | **Affective learning** | **Attendance Marks (10)** | **Continuous**  **Evaluation (60)** | **Final Exam**  **(30)** |
| Remember |  |  |  |  |
| Understand |  |  | 5 | 5 |
| Apply |  |  | 20 | 10 |
| Analyze |  |  | 25 | 10 |
| Evaluation |  |  | 10 | 5 |
| Create |  |  |  |  |
|  | Responding | 10 |  |  |
| **Total allocated marks** | 10 | 60 |  | 40 |

1. **Grading Policy:**

As per IIUC grading policy: <https://www.iiuc.ac.bd/academic/asystem>

1. **Course Content:**

**Section-A (Mid-term: 30 Marks)**

* 1. Computer architecture Basic, History, Different terminologies of computing device, Types of Computer Architecture
  2. Understanding Program Performance, Defining Performance, Measuring Performance, CPU Performance and its factor, Evaluating performance, MIPS as a performance Measure
  3. Instruction and data access methods, Instruction Set, Stored-Program Concept, Operations of the computer Hardware, Operands of the computer Hardware (Design Principles of Computer Hardware )
  4. Representation of Instructions in the Computer, Logical Operations, Instructions for decision making, MIPS Addressing for 32-Bit Immediate and Addresses
  5. Arithmetic and logical operations, floating point operations, ALU design, Signed and Unsigned numbers, Number Conversion and representation, Arithmetic Operations and Representation
  6. Matrix-chain multiplication and longest common subsequence problems as examples, Complexity analysis of the algorithms. Multiplication, Division and

Floating point Hardwar

# Section-B (Final Exam: 50 Marks) Group-A (20 Marks)

1. The control unit (Single cycle Data path) : hardwired and micro programmed, Logic Design Convention, Clocking Methodology, Data path Basic, State Element of Data path Building a single Data path (R-Type, I-Type and J-type Instructions) Designing the main control unit (with control signals effect), Operation of the data path
2. The control unit (Multiple cycle Data path): Hardwired and micro programmed, Multi-cycle implementation Basic. Necessity of multi-cycle implementation, Details of Control Signal Breaking the Instruction Execution into Clock Cycles,

Exceptions

# Group-B (30 Marks)

1. Pipelining: Overview of Pipelining, Pipelining Hazard, Pipeline Data Path (R-Type, I-Type and J-type Instructions) Pipeline Control, Exception, Exception Handling

1. Memory organization: Introduction to memory, memory Hierarchy, Basic on Cache, Accessing a cache, Handling cache miss and writes, Flexible placement of cache block

1. Introduction to virtual Memory, Virtual to physical, Handling page Fault TLB, Integrating Virtual Memory, TLBs and Caches

1. I/O systems, channels, interrupts, DMA, I/O Devices basic, Disk Storage and dependability, RAID, Buses and other connections between processors, Memory and I/O Devices, Interfacing I/O devices with processors.

*Please Make Necessary Changes*