AURIX™ TC2xx Data Sheet Addendum

About this document

Scope and purpose

This is an addendum to the TC2xx Data Sheet listing all intended product variants, key parameters such as memory size, and optional features.

Prefix naming conventions

- SAK: $T_{ambient}$ Temperature Range from -40 °C up to +125 °C
- SAL: $T_{ambient}$ Temperature Range from -40 °C up to +150 °C (packaged device)

Feature package naming conventions

- T – Standard type without HSM
- TP – Standard type with HSM enabled
- TA – ADAS feature package – HSM enabled
- TX – Truck / SRAM extension – HSM enabled

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Addendum

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DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		ADC CHAN.	FlexRay (#/ch.)	ETH	HSM	LOCK-STEP	CAN FD	CAN FD
									DSPR (KB)	PSPR (KB)							ISO 11898-1
SAK-TC214L-8F133N AC	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	0146 1142 H	133	0.5	64@125k	56	48	8	24	No	No	No	Yes	Yes	Yes
SAK-TC213L-8F133N AC	STANDARD	PG-TQFP-100-23	-40°C - +125 °C	0146 1042 H	133	0.5	64@125k	56	48	8	24	No	No	No	Yes	Yes	Yes
SAK-TC213L-8F133F AC	STANDARD	PG-TQFP-100-23	-40°C - +125 °C	0146 1042 H	133	0.5	64@125k	56	48	8	24	No	No	No	Yes	Yes	No
SAK-TC212L-8F133F AC	STANDARD	PG-TQFP-80-7	-40°C - +125 °C	0146 1242 H	133	0.5	64@125k	56	48	8	14	No	No	No	Yes	Yes	No
SAK-TC212L-8F133N AC	STANDARD	PG-TQFP-80-7	-40°C - +125 °C	0146 1242 H	133	0.5	64@125k	56	48	8	14	No	No	No	Yes	Yes	Yes

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DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		ADC Chan.	FlexRay (#/ch.)	ETH	HSM	LOCK STEP	CAN FD	CAN FD
									DSPR (KB)	PSPR (KB)							ISO 11898-1
SAK-TC224L-16F133N AC	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	0246 2142 H	133	1	96@ 125k	96	88	8	24	No	No	No	Yes	Yes	Yes
SAK-TC223L-16F133N AC	STANDARD	PG-TQFP-100-23	-40°C - +125 °C	0246 2042 H	133	1	96@125k	96	88	8	24	No	No	No	Yes	Yes	Yes
SAK-TC222L-16F133N AC	STANDARD	PG-TQFP-80-7	-40°C - +125 °C	0246 2242 H	133	1	96@125k	96	88	8	14	No	No	No	Yes	Yes	Yes

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TC23x

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3.1 Standard variants TC23x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		ADC Chan.	FlexRay (#/ch.)	ETH	HSM	CAN FD
									DSPR (KB)	PSPR (KB)					ISO 11898-1
SAK-TC237LP-32F200N AC	STANDARD	PG-LFBGA-292-6	-40°C - +125 °C	4446 3242 $_H$	200	2	128@125k	192	184	8	24	1 / 2	No	Yes	Yes
SAK-TC234LP-32F200N AC	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	4446 3142 $_H$	200	2	128@125k	192	184	8	24	1 / 2	No	Yes	Yes
SAK-TC233LP-32F200N AC	STANDARD	PG-TQFP-100-23	-40°C - +125 °C	4446 3042 $_H$	200	2	128@125k	192	184	8	24	1 / 2	No	Yes	Yes

3.2 ADAS type TC23x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		LMU (KB)	EMEM (KB)	ADC Chan.	FlexRay (#/ch.)	ETH	HSM	FFT
									DSPR (KB)	PSPR (KB)							
SAK-TC234LA-32F200F AB	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	4443 3941 $_H$ 4447 3941 $_H$	200	2	128@125k	736	184	8	32	512	24	1 / 2	Yes	Yes	Yes

3.3 Extended type TC23x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		LMU (KB)	EMEM (KB)	ADC Chan.	FlexRay (#/ch.)	ETH	HSM	FFT
									DSPR (KB)	PSPR (KB)							
SAK-TC234LX-32F200F AB	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	4443 3941 $_H$ 4447 3941 $_H$	200	2	128@125k	736	184	8	32	512	24	1 / 2	Yes	Yes	No

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4.1   Standard variants TC26x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 TC16P		CORE 0 TC16E		LMU (KB)	ADC CHAN.	ETH	CAN FD	CAN FD
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)					ISO frame
SAK-TC267D-40F200N BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	0546 6652$_H$	200	2.5	16 @500k	240	120	32	72	16	0	50	Yes	Yes	Yes
SAK-TC267D-40F200S BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	0544 6651$_H$	200	2.5	16 @500k	240	120	32	72	16	0	50	Yes	Yes	No
SAK-TC265D-40F200N BC	STANDARD	PG-LQFP-176-22	-40°C – +125°C	0546 6152$_H$	200	2.5	16 @500k	240	120	32	72	16	0	50	Yes	Yes	Yes
SAK-TC264D-40F200N BC	STANDARD	PG-LQFP-144-22	-40°C – +125°C	0546 6052$_H$	200	2.5	16 @500k	240	120	32	72	16	0	40	Yes	Yes	Yes
SAL-TC267D-40F200N BC	STANDARD	PG-LFBGA-292-6	-40°C – +150°C	0546 6652$_H$	200	2.5	16 @500k	240	120	32	72	16	0	50	Yes	Yes	Yes

4.2   ADAS type TC26x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 TC16P		CORE 0 TC16E		LMU (KB)	EMEM (KB)	ADC CHAN.	ETH	CIF	FFT	CAN FD	CAN FD
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)								ISO frame
SAK-TC264DA-40F200N BC	STANDARD	PG-LQFP-144-22	-40°C – +125°C	0547 6852$_H$	200	2.5	16 @500k	752	120	32	72	16	0	512	40	Yes	Yes	Yes	Yes	Yes

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DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 AND 2 TC16P		CORE 0 TC16E		LMU (KB)	ADC CHAN.	FlexRay (#/ch.)	ETH	HSM	CAN FD	CAN FD ISO frame
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)							
SAK-TC277TP-64F200N DC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4746 7172$_H$	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	Yes
SAK-TC277TP-64F200S DC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4746 7172$_H$	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	No
SAK-TC275TP-64F200N DC	STANDARD	PG-LQFP-176-22	-40°C – +125°C	4746 7072$_H$	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	Yes

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6.1 Standard variants TC29x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 AND 2 TC16P		CORE 0 TC16P		LMU (KB)	ADC CHAN.	FlexRay (#/ch.)	ETH	HSM	CAN FD	CAN FD
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)							ISO frame
SAL-TC299TP-128F300N BC	STANDARD	PG-LFBGA-516-5	-40°C – +150°C	4B46 9252ₕ	300	8	128@500k	728	240	32	120	32	32	84	2 / 4	Yes	Yes	Yes	Yes
SAL-TC298TP-128F300N BC	STANDARD	PG-LBGA-416-26	-40°C – +150°C	4B46 9152ₕ	300	8	128@500k	728	240	32	120	32	32	60	2 / 4	Yes	Yes	Yes	Yes
SAK-TC297TP-128F300N BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4B46 9052ₕ	300	8	128@500k	728	240	32	120	32	32	60	2 / 4	Yes	Yes	Yes	Yes

6.2 Extended type TC29x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMP. RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 AND 2 TC16P		CORE 0 TC16P		LMU (KB)	EMEM (KB)	ADC CHAN.	FlexRay (#/ch.)	ETH	CIF	FFT	HSM	CAN FD	CAN FD	AGBT
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)										ISO frame	
SAK-TC299TX-128F300N BC	STANDARD	PG-LFBGA-516-5	-40°C – +125°C	4B47 9A52ₕ	300	8	128 @500k	2776	240	32	120	32	32	2048	84	2 / 4	Yes	No	No	Yes	Yes	Yes	No
SAK-TC297TX-128F300N BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4B47 9852ₕ	300	8	128 @500k	2776	240	32	120	32	32	2048	60	2 / 4	Yes	No	No	Yes	Yes	Yes	No

6.3 ADAS Type TC29x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMP. RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 AND 2 TC16P		CORE 0 TC16P		LMU (KB)	EMEM (KB)	ADC Chan	Flex Ray (#/ch.)	ETH	CIF	FFT	HSM	CAN FD	CAN FD	AGBT
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)										ISO frame	
SAK-TC297TA-128F300N BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4B47 9052ₕ	300	8	128 @500k	2776	240	32	120	32	32	2048	60	2 / 4	Yes	Yes	Yes	Yes	Yes	Yes	No

7   Memory map of variants

This section shows the influence of the feature variants on the memory map.

7.1   TC21x
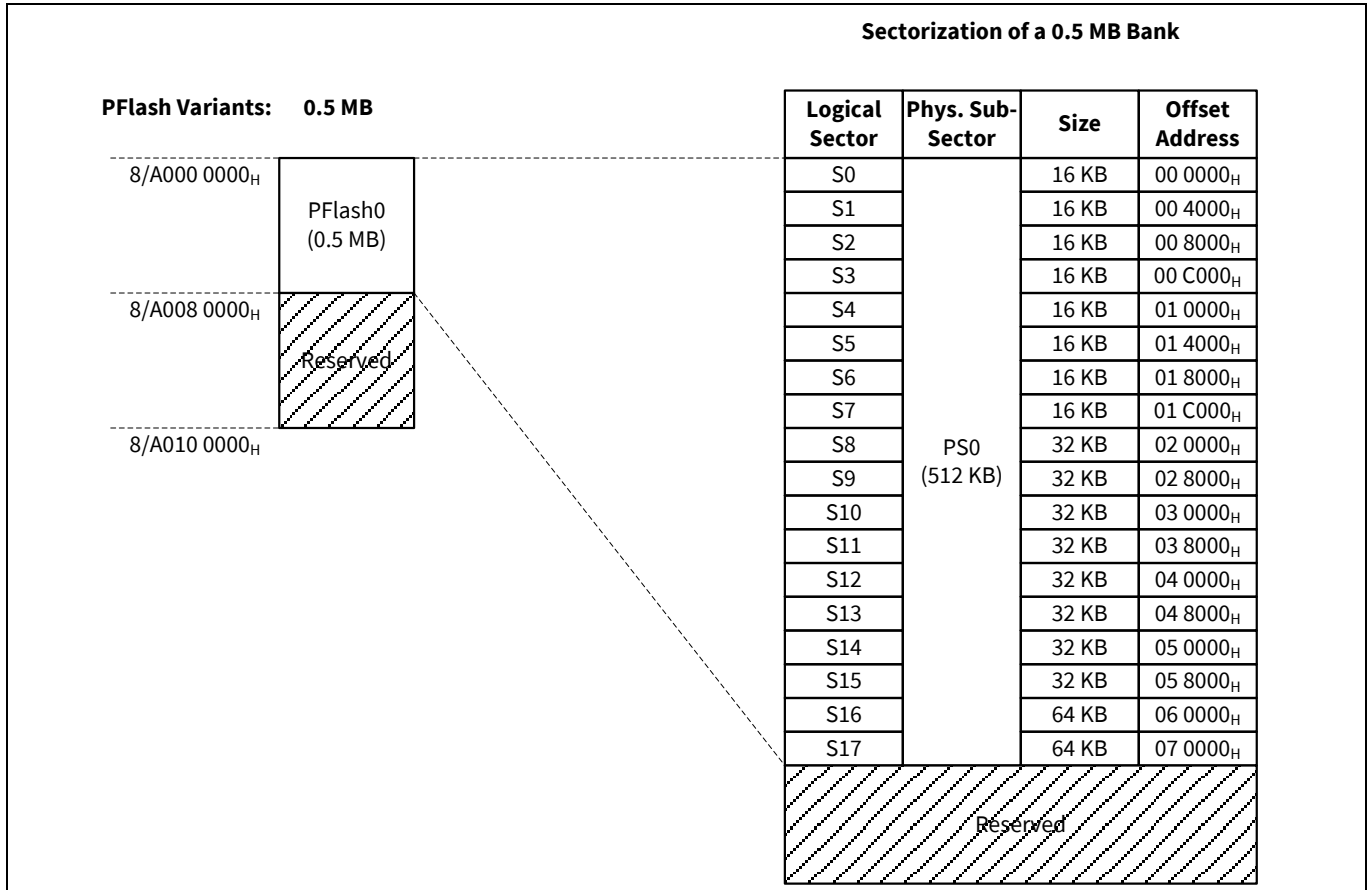
Sectorization of a 0.5 MB Bank			
Logical Sector	**Phys. Sub-Sector**	**Size**	**Offset Address**
S0		16 KB	00 0000$_H$
S1		16 KB	00 4000$_H$
S2		16 KB	00 8000$_H$
S3		16 KB	00 C000$_H$
S4		16 KB	01 0000$_H$
S5		16 KB	01 4000$_H$
S6		16 KB	01 8000$_H$
S7		16 KB	01 C000$_H$
S8	PS0 (512 KB)	32 KB	02 0000$_H$
S9		32 KB	02 8000$_H$
S10		32 KB	03 0000$_H$
S11		32 KB	03 8000$_H$
S12		32 KB	04 0000$_H$
S13		32 KB	04 8000$_H$
S14		32 KB	05 0000$_H$
S15		32 KB	05 8000$_H$
S16		64 KB	06 0000$_H$
S17		64 KB	07 0000$_H$

PFlash Variants: 0.5 MB

8/A000 0000$_H$ PFlash0 (0.5 MB)

8/A008 0000$_H$ Reserved

8/A010 0000$_H$

Reserved

Figure 1   TC21x PFlash variants

Core0 DSPR: 48 KB

7000 0000$_H$ CPU0.DSPR (48 KB)

7000 C000$_H$ Reserved

7001 6000$_H$
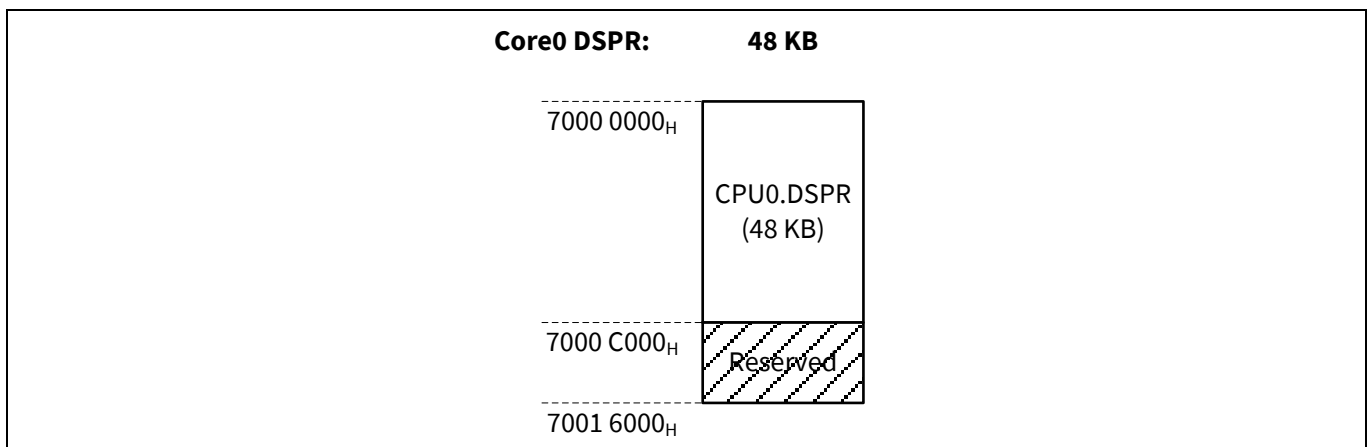
Figure 2   TC21x Coar0 DSPR

Lockstep Variants

No influence on memory ap.

Lockstep = "No" variants: In the Boot Mode Header the BMI.LCL0LSEN must be configured to 0_B.

Memory map of variants

7.2 TC22X

Sectorization of a 1 MB Bank				Sectors available in 0.75 MB Bank

PFlash Variants: 1 MB · 0.75 MB

Logical Sector	Phys. Sub-Sector	Size	Offset Address	Logical Sector
S0		16 KB	00 0000$_H$	S0
S1		16 KB	00 4000$_H$	S1
S2		16 KB	00 8000$_H$	S2
S3		16 KB	00 C000$_H$	S3
S4		16 KB	01 0000$_H$	S4
S5		16 KB	01 4000$_H$	S5
S6		16 KB	01 8000$_H$	S6
S7		16 KB	01 C000$_H$	S7
S8	PS0 (512 KB)	32 KB	02 0000$_H$	S8
S9		32 KB	02 8000$_H$	S9
S10		32 KB	03 0000$_H$	S10
S11		32 KB	03 8000$_H$	S11
S12		32 KB	04 0000$_H$	S12
S13		32 KB	04 8000$_H$	S13
S14		32 KB	05 0000$_H$	S14
S15		32 KB	05 8000$_H$	S15
S16		64 KB	06 0000$_H$	S16
S17		64 KB	07 0000$_H$	S17
S18	PS1 (512 KB)	64 KB	08 0000$_H$	S18
S19		64 KB	09 0000$_H$	S19
S20		128 KB	0A 0000$_H$	S20
S21		128 KB	0C 0000$_H$	Reserved
S22		128 KB	0E 0000$_H$	

PFlash0 (1 MB): 8/A000 0000$_H$ to 8/A010 0000$_H$

PFlash0 (0.75 MB) — Reserved

Figure 3   TC22x PFlash variants

DF_EEPROM Variants: **96 KB** — **64 KB**

Exemplary EEPROM size: 24 KB @ 500k — 16 KB @ 500k

Logical Sector	Size	Offset Address	Logical Sector	Size	Offset Address
EEPROM0	8 KB	00 0000$_H$	EEPROM0	8 KB	00 0000$_H$
EEPROM1	8 KB	00 2000$_H$	EEPROM1	8 KB	00 2000$_H$
EEPROM2	8 KB	00 4000$_H$	EEPROM2	8 KB	00 4000$_H$
...	...	...	...	...	...
			EEPROM7	8 KB	00 E000$_H$
			Reserved		
EEPROM11	8 KB	01 6000$_H$			

AF00 0000$_H$ / AF01 8000$_H$ (96 KB)

AF00 0000$_H$ / AF01 0000$_H$ / AF01 8000$_H$ (64 KB)

Figure 4   TC22x DF_EEPROM variants

Memory map of variants
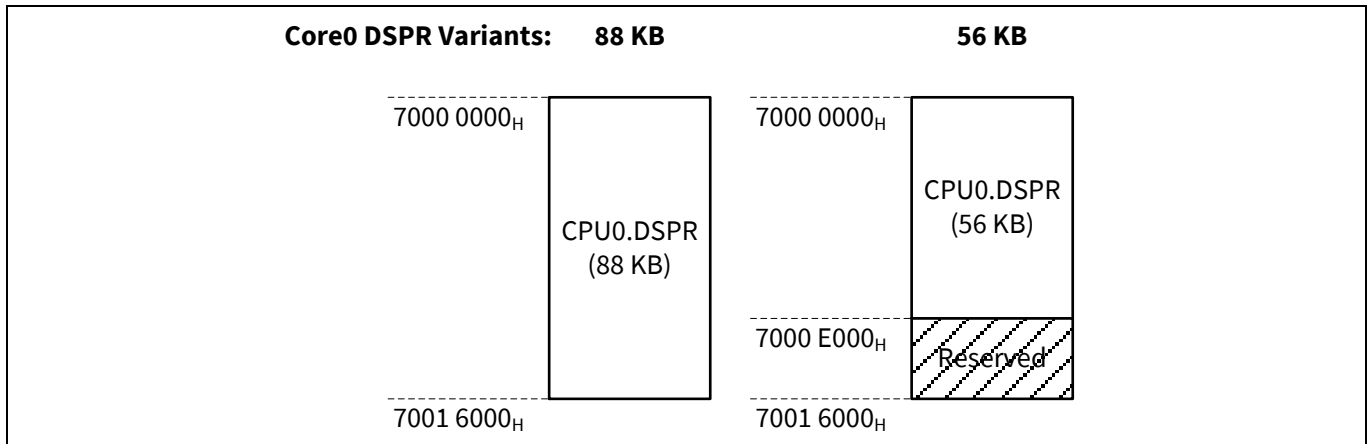
Figure 5   **TC22x Core0 DSPR variants**

7.3   TC23x
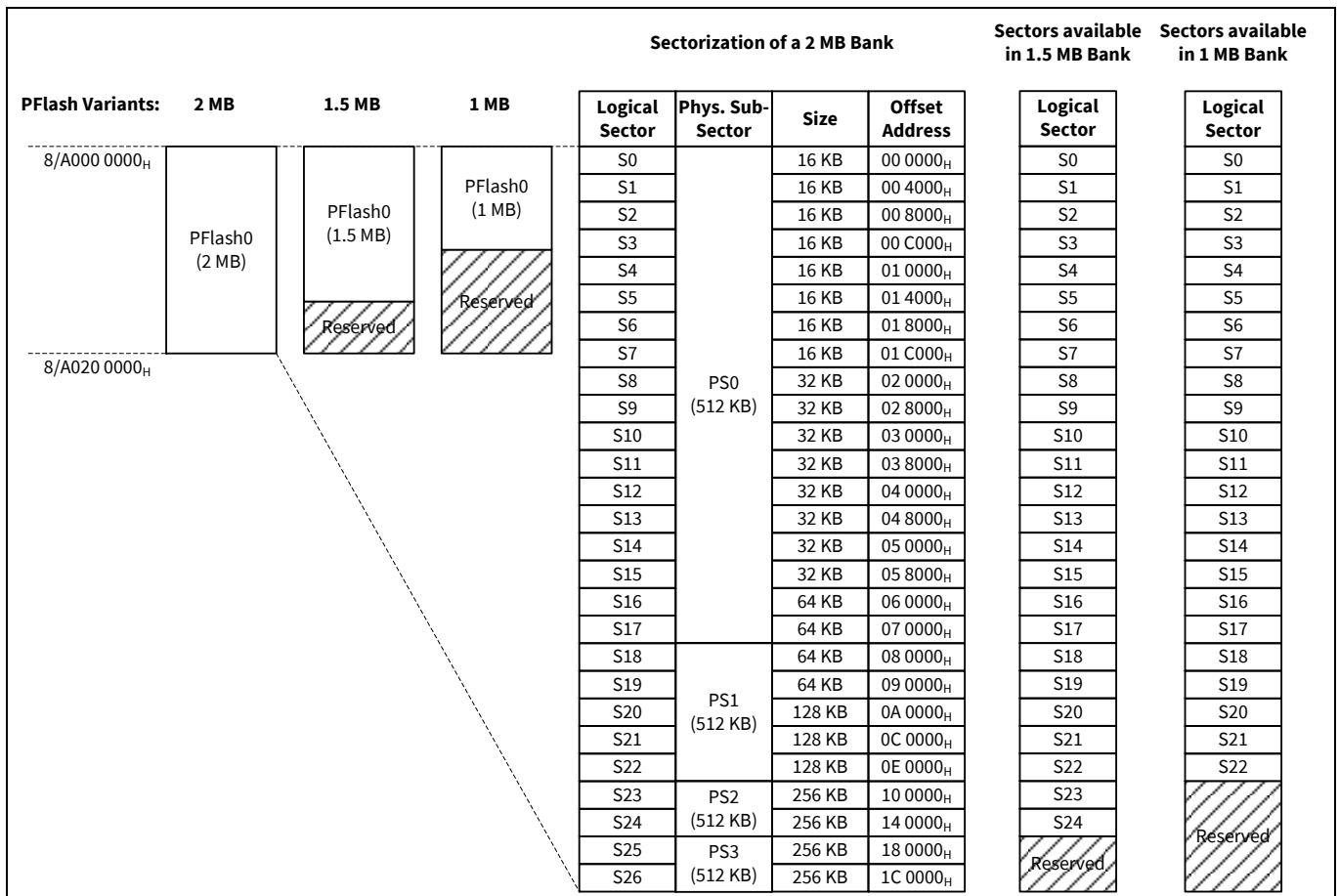
Figure 6   **TC23x PFlash variants**

Memory map of variants

Core0 DSPR Variants: 184 KB   120 KB   88 KB
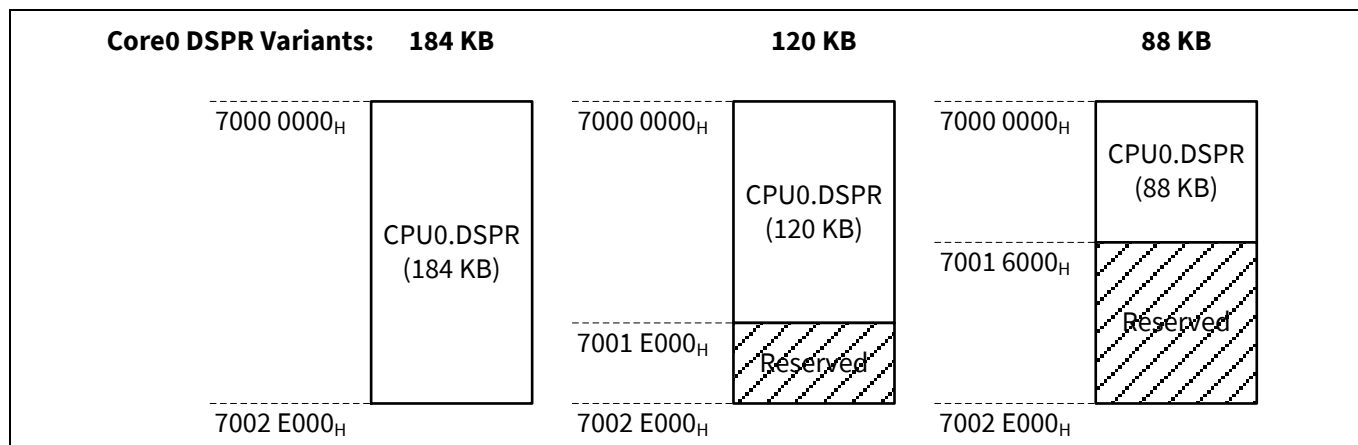
Figure 7   TC23x Core0 DSPR variants

LMU Variants: 32 KB   0 KB
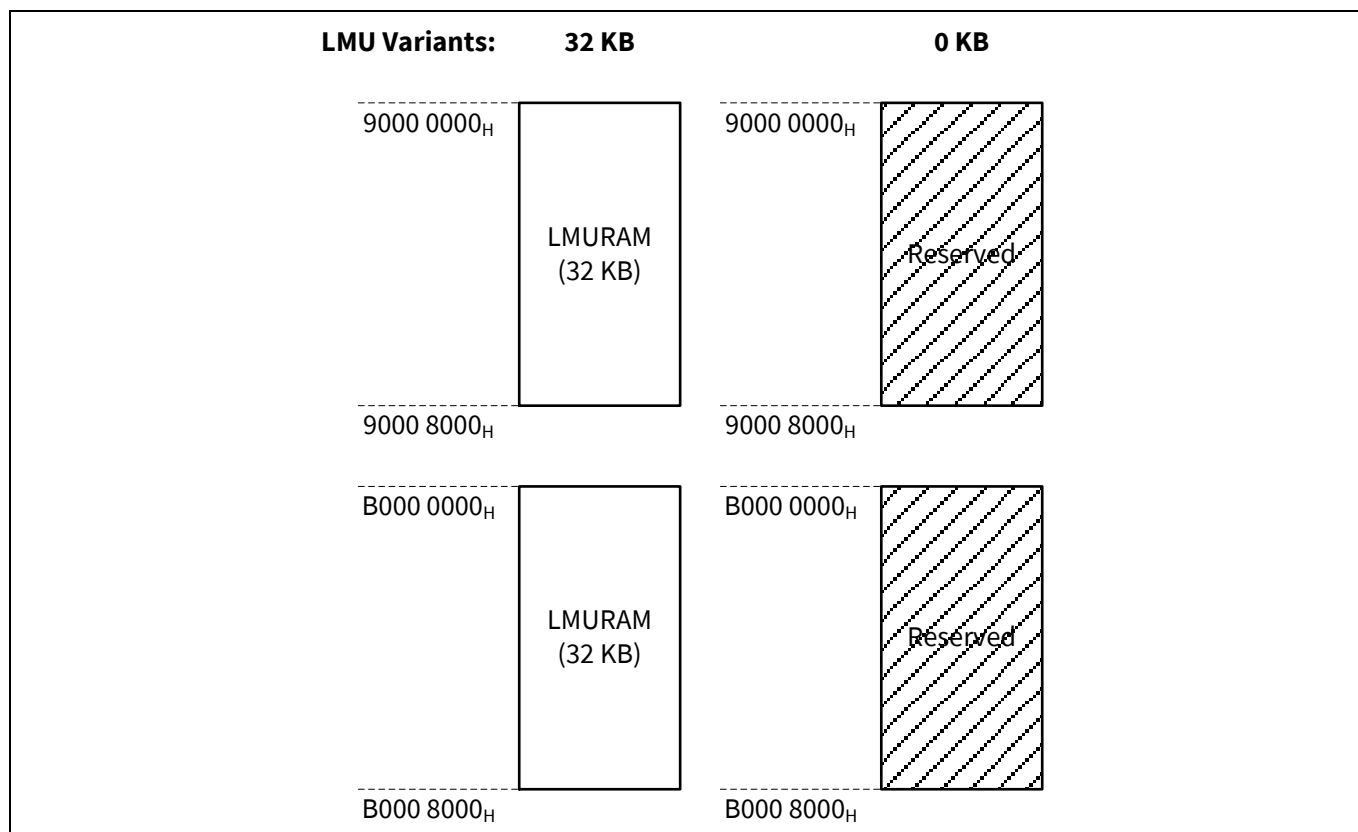
Figure 8   TC23x LMU variants

Memory map of variants
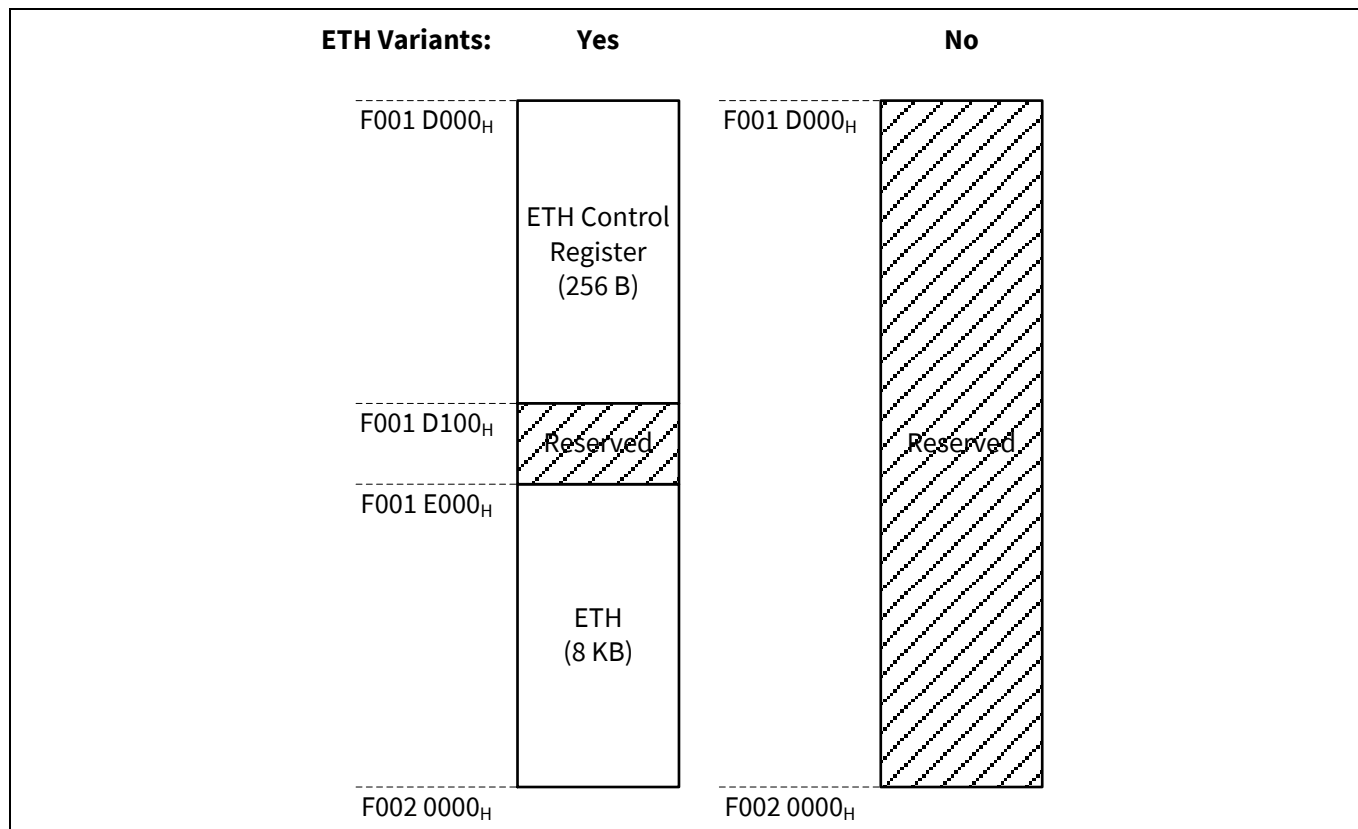
Figure 9   TC23x ETH variants
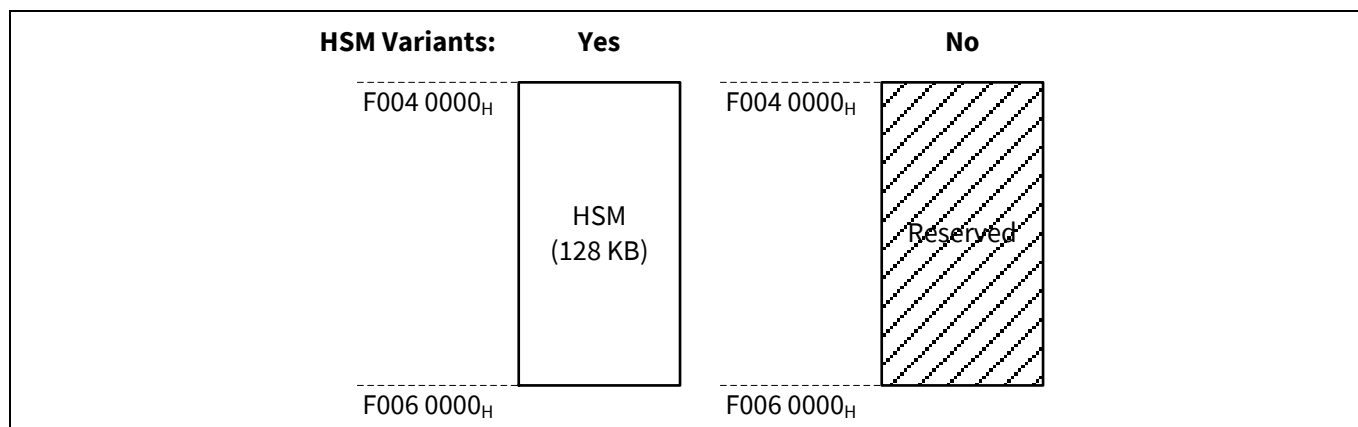
Figure 10   TC23x HSM variants

Memory map of variants
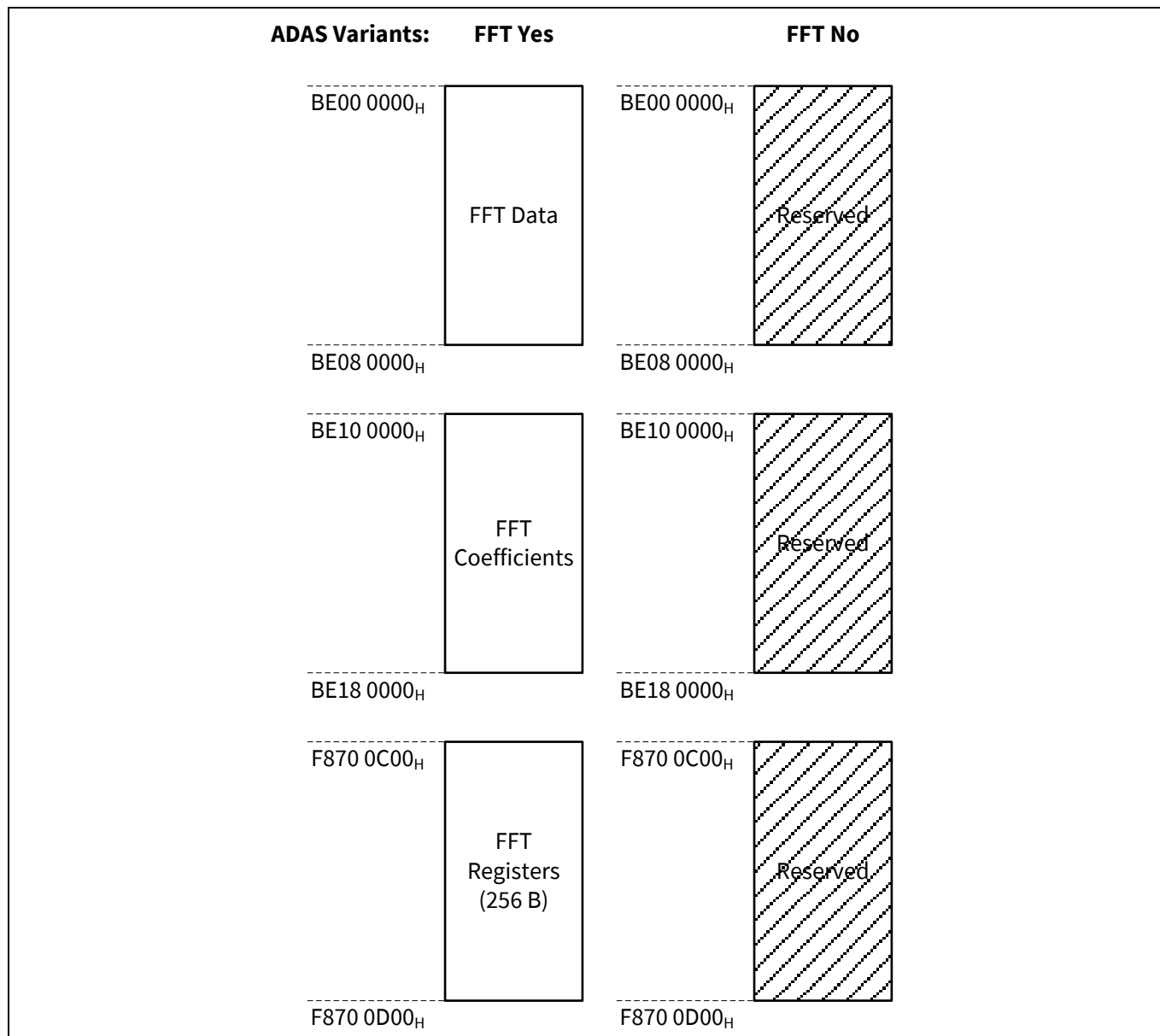
Figure 11   TC23x ADAS variants

ADAS variants

ADAS = "Yes" variants:

The VADC kernels ADC02 and ADC03 are available, offering the Converter Groups G02 and G03. Because of that, the group related registers with x = 2 and x = 3 are implemented.

7.4 TC26x

DF_EEPROM Variants:	96 KB				72 KB		
Exemplary EEPROM size:	16 KB @ 500k				12 KB @ 500k		

96 KB

	Logical Sector	Size	Offset Address
AF00 0000$_H$	EEPROM0	8 KB	00 0000$_H$
	EEPROM1	8 KB	00 2000$_H$
	EEPROM2	8 KB	00 4000$_H$
	...	...	...
	EEPROM11	8 KB	01 6000$_H$
AF01 8000$_H$			

72 KB

	Logical Sector	Size	Offset Address
AF00 0000$_H$	EEPROM0	8 KB	00 0000$_H$
	EEPROM1	8 KB	00 2000$_H$
	EEPROM2	8 KB	00 4000$_H$
	...	...	...
	EEPROM8	8 KB	01 0000$_H$
AF01 2000$_H$	Reserved		
AF01 8000$_H$			
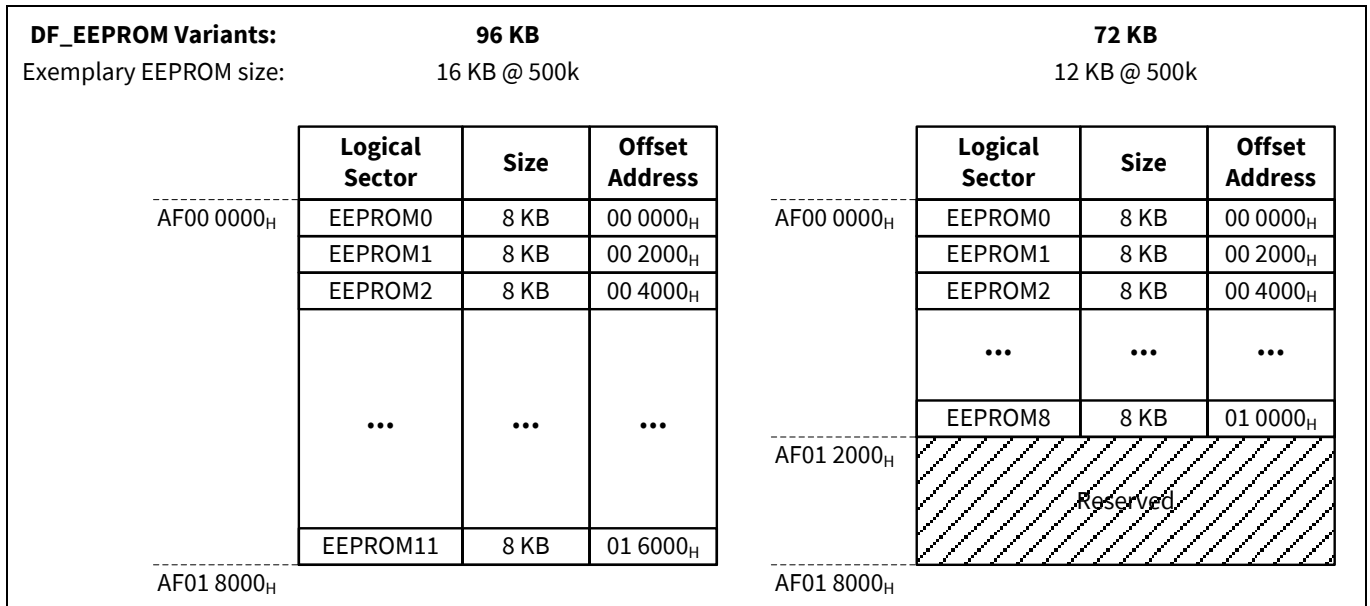
Figure 12 TC26x DF_EEPROM variants

Core1 PSPR Variants: 32 KB 24 KB

6010 0000$_H$ CPU1.PSPR (32 KB) 6010 8000$_H$

6010 0000$_H$ CPU1.PSPR (24 KB) 6010 6000$_H$ Reserved 6010 8000$_H$
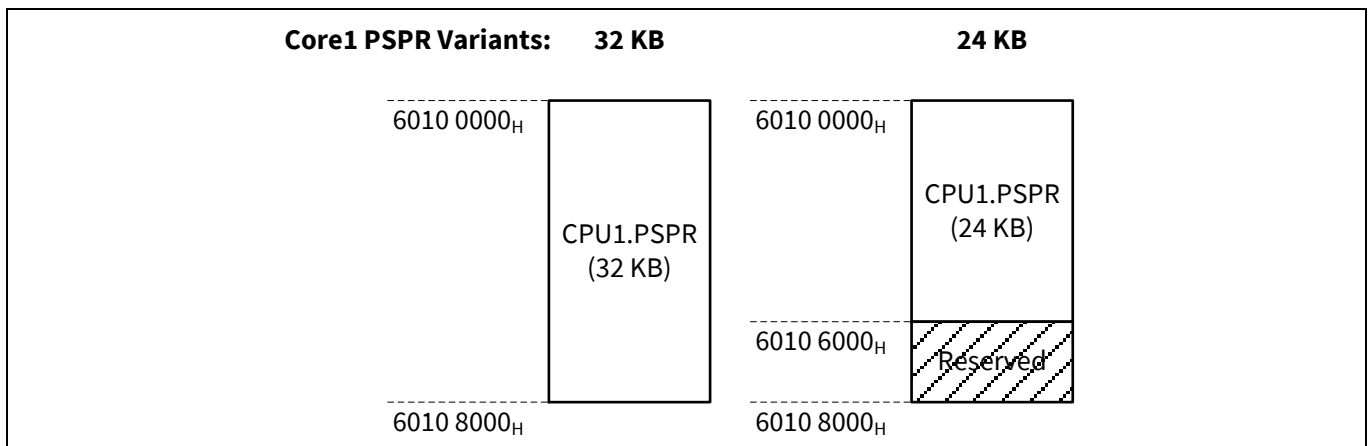
Figure 13 TC26x Core1 PSPR variants

Memory map of variants
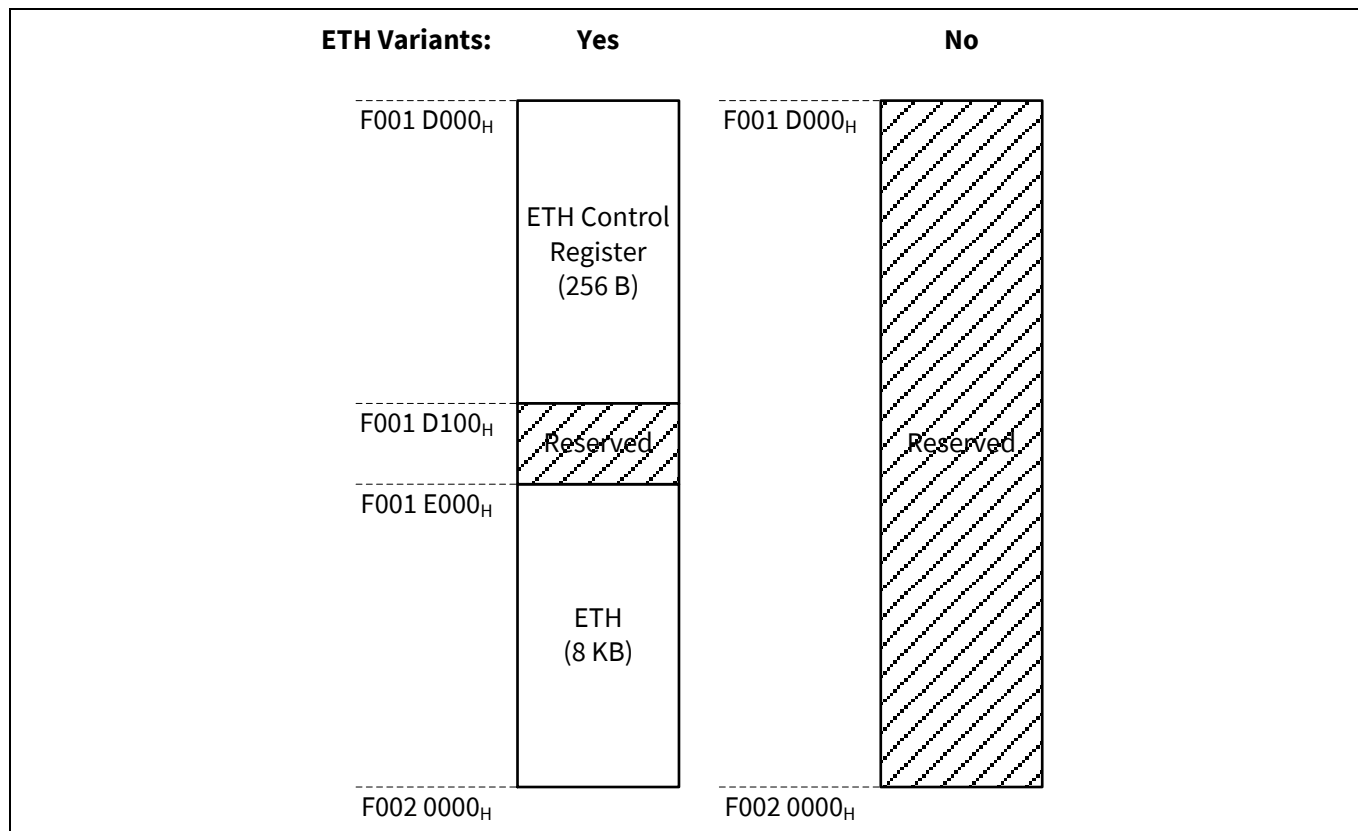
Figure 14   TC26x ETH variants

Memory map of variants

Extended SRAM / ADAS:	Yes	No
9/BF00 0000$_H$	ADM (512 KB)	9/BF00 0000$_H$
9/BF08 0000$_H$	Reserved	Reserved
A/C000 0000$_H$		A/C000 0000$_H$
F90E 6000$_H$	EMEM Registers (256 B)	F90E 6000$_H$ Reserved
F90E 6100$_H$		F90E 6100$_H$
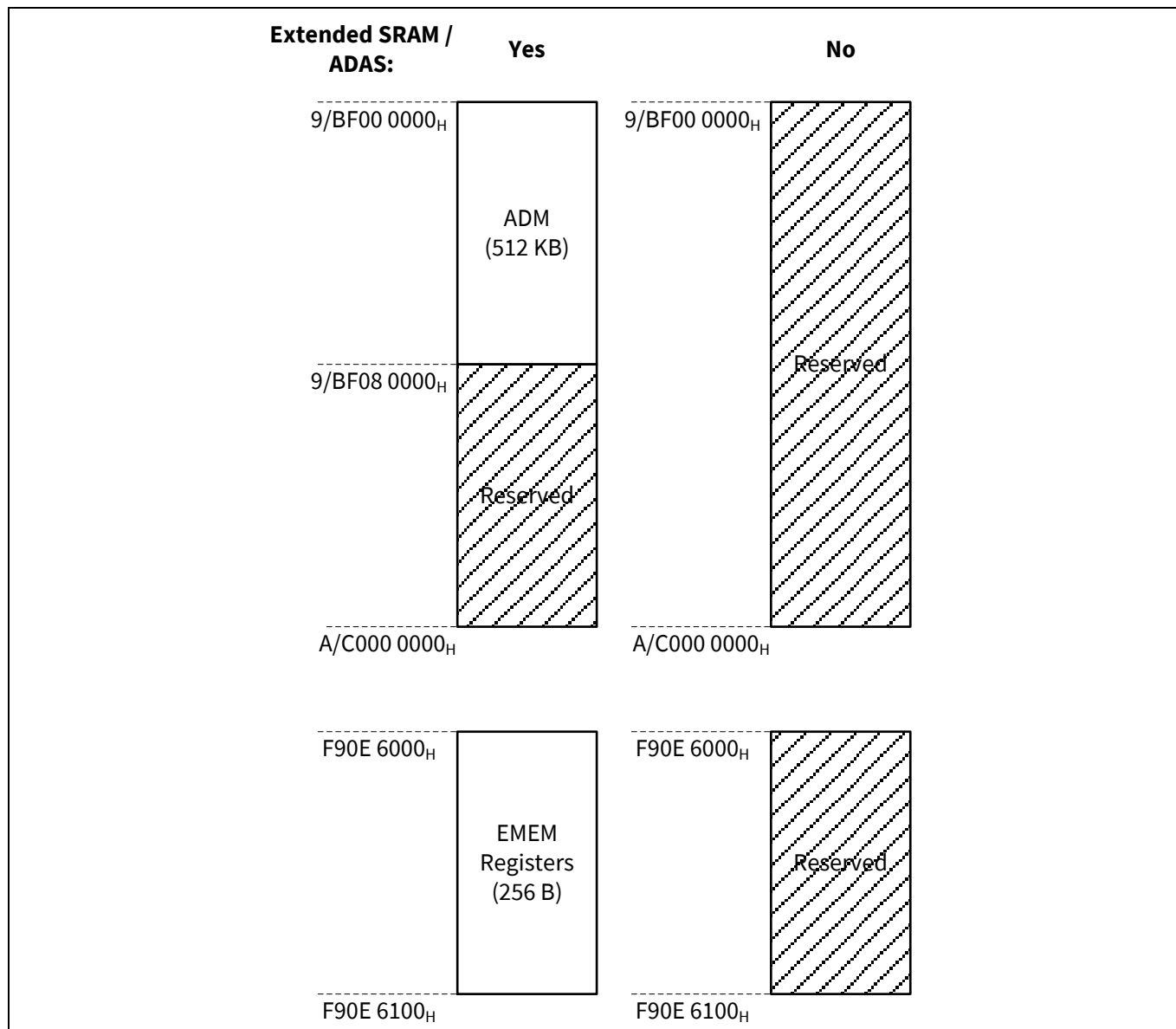
Figure 15   TC26x Extended SRAM / ADAS

Memory map of variants

ADAS Variants:	Yes	No
BE00 0000$_H$	FFT Data	BE00 0000$_H$ Reserved
BE08 0000$_H$		BE08 0000$_H$
BE10 0000$_H$	FFT Coefficients	BE10 0000$_H$ Reserved
BE18 0000$_H$		BE18 0000$_H$
F870 0C00$_H$	FFT Registers (256 B)	F870 0C00$_H$ Reserved
F870 0D00$_H$		F870 0D00$_H$
F90E 1F00$_H$	CIF	F90E 1F00$_H$ Reserved
F90E 5FFF$_H$		F90E 5FFF$_H$
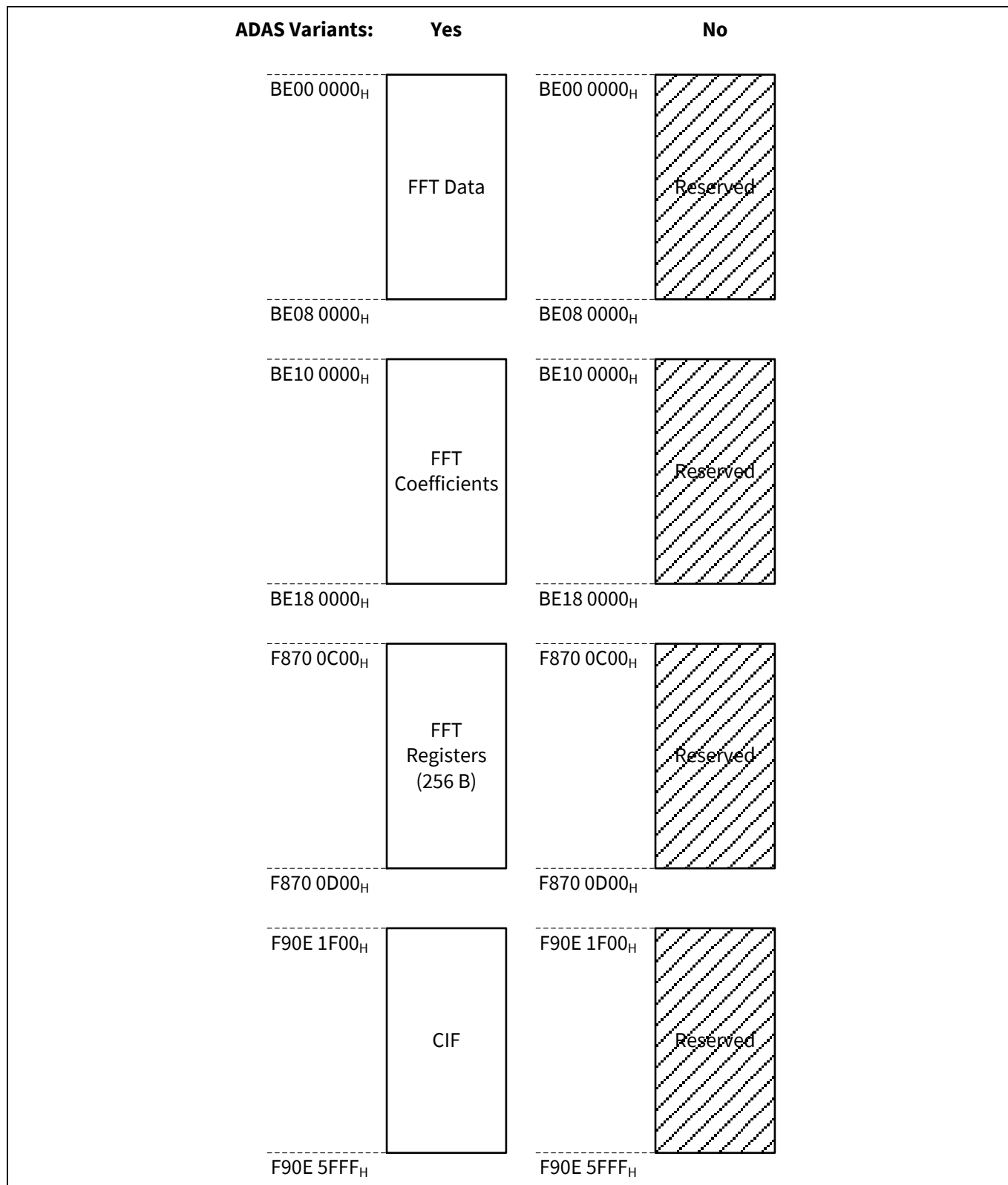
Figure 16   TC26x ADAS variants

CAN FD variants

No influence on Memory Map.

CAN FD = "No" variants: all CAN register fields NCRx.FDEN have to be kept at 0$_B$.

Memory map of variants

7.5   TC27x

DF_EEPROM Variants:	384 KB				144 KB		
Exemplary EEPROM size:	64 KB @ 500k				24 KB @ 500k		

TC27x DF_EEPROM table (384 KB):

	Logical Sector	Size	Offset Address
AF00 0000$_H$	EEPROM0	8 KB	00 0000$_H$
	EEPROM1	8 KB	00 2000$_H$
	EEPROM2	8 KB	00 4000$_H$
	...	...	...
	EEPROM47	8 KB	05 E000$_H$
AF06 0000$_H$			

TC27x DF_EEPROM table (144 KB):

	Logical Sector	Size	Offset Address
AF00 0000$_H$	EEPROM0	8 KB	00 0000$_H$
	EEPROM1	8 KB	00 2000$_H$
	EEPROM2	8 KB	00 4000$_H$
	...	...	...
	EEPROM17	8 KB	02 2000$_H$
AF02 4000$_H$	Reserved		
AF06 0000$_H$			

Figure 17   TC27x DF_EEPROM variants

Core1/2 PSPR Variants: 32 KB   24 KB

5010 0000$_H$ CPU2.PSPR (32 KB) 5010 8000$_H$
5010 0000$_H$ CPU2.PSPR (24 KB) 5010 6000$_H$ Reserved 5010 8000$_H$
6010 0000$_H$ CPU1.PSPR (32 KB) 6010 8000$_H$
6010 0000$_H$ CPU1.PSPR (24 KB) 6010 6000$_H$ Reserved 6010 8000$_H$
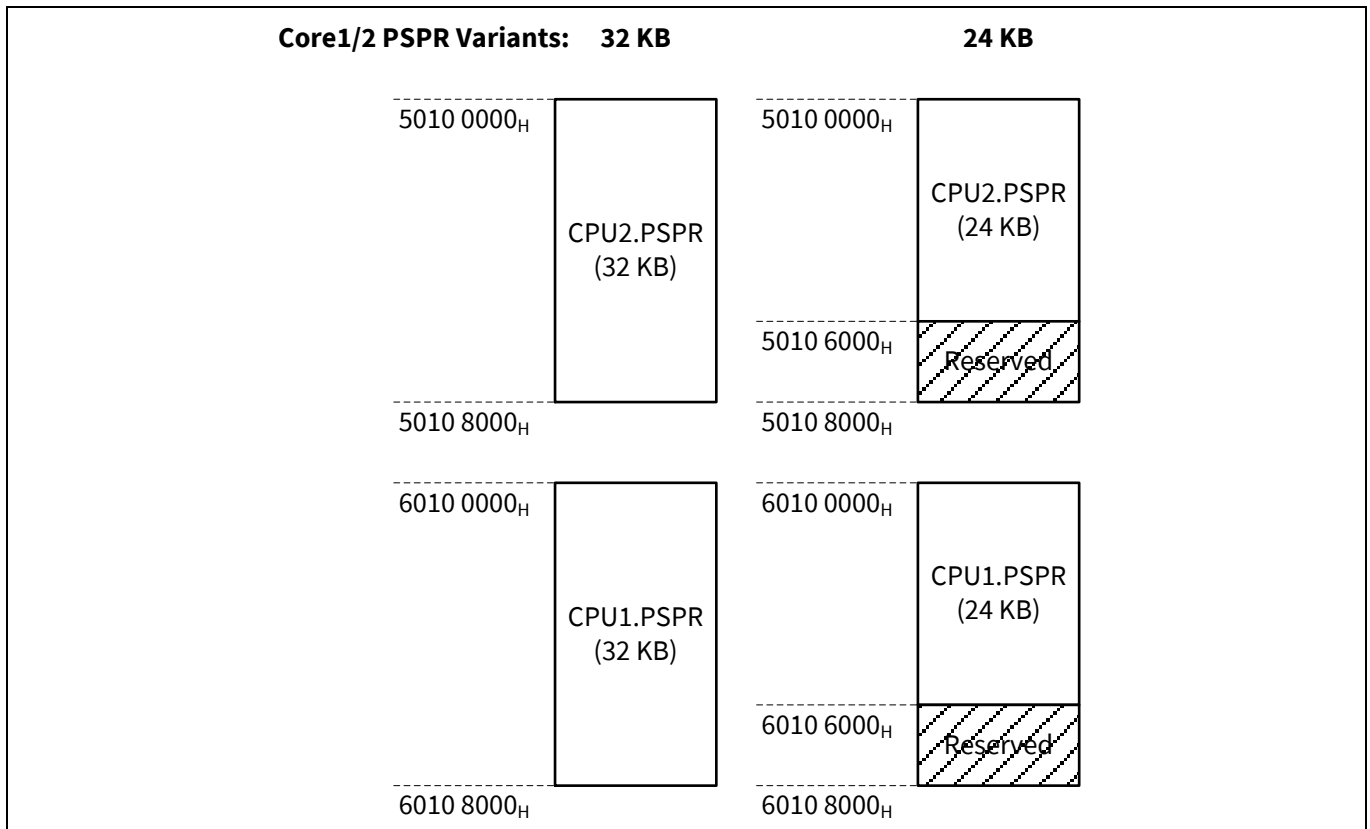
Figure 18   TC27x Core1/2 PSPR variants

Memory map of variants
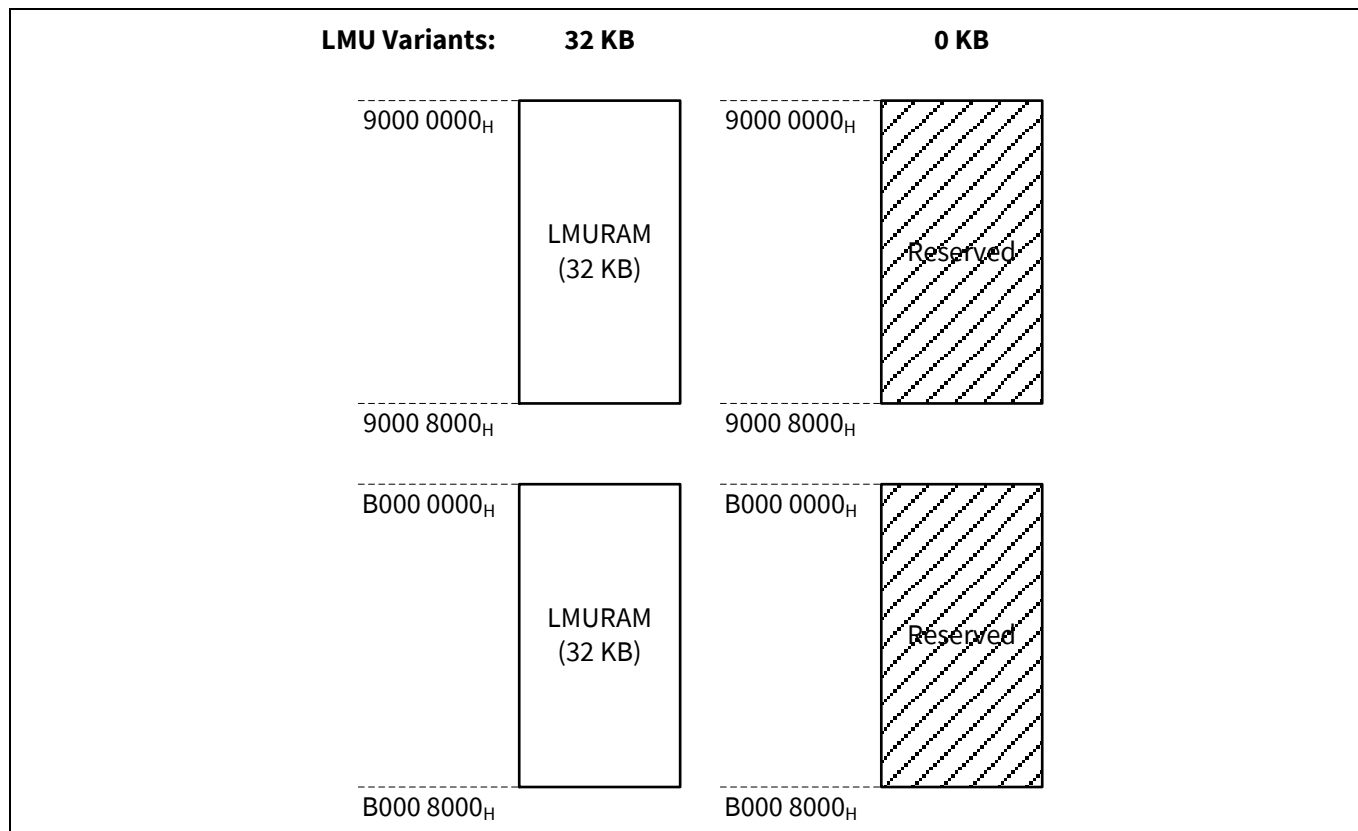
Figure 19   TC27x LMU variants
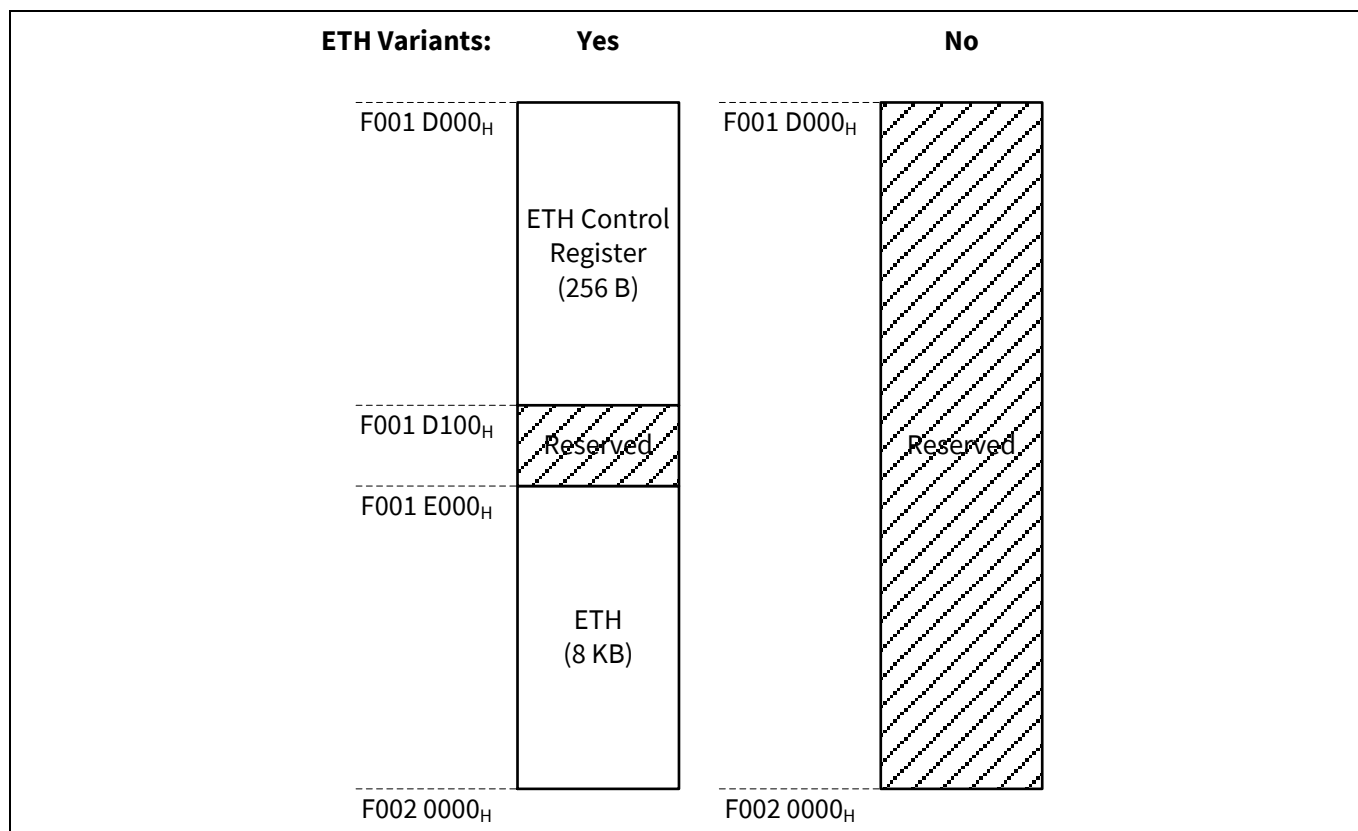
**Figure 20   TC27x ETH variants**

Memory map of variants

HSM Variants:	Yes	No

AF11 0000$_H$ — DF_HSM (DF1) (64 KB) — AF12 0000$_H$

AF11 0000$_H$ — Reserved — AF12 0000$_H$

F004 0000$_H$ — HSM (128 KB) — F006 0000$_H$

F004 0000$_H$ — Reserved — F006 0000$_H$

FF11 0000$_H$ — DF_HSM (DF1) (64 KB) — FF12 0000$_H$

FF11 0000$_H$ — Reserved — FF12 0000$_H$
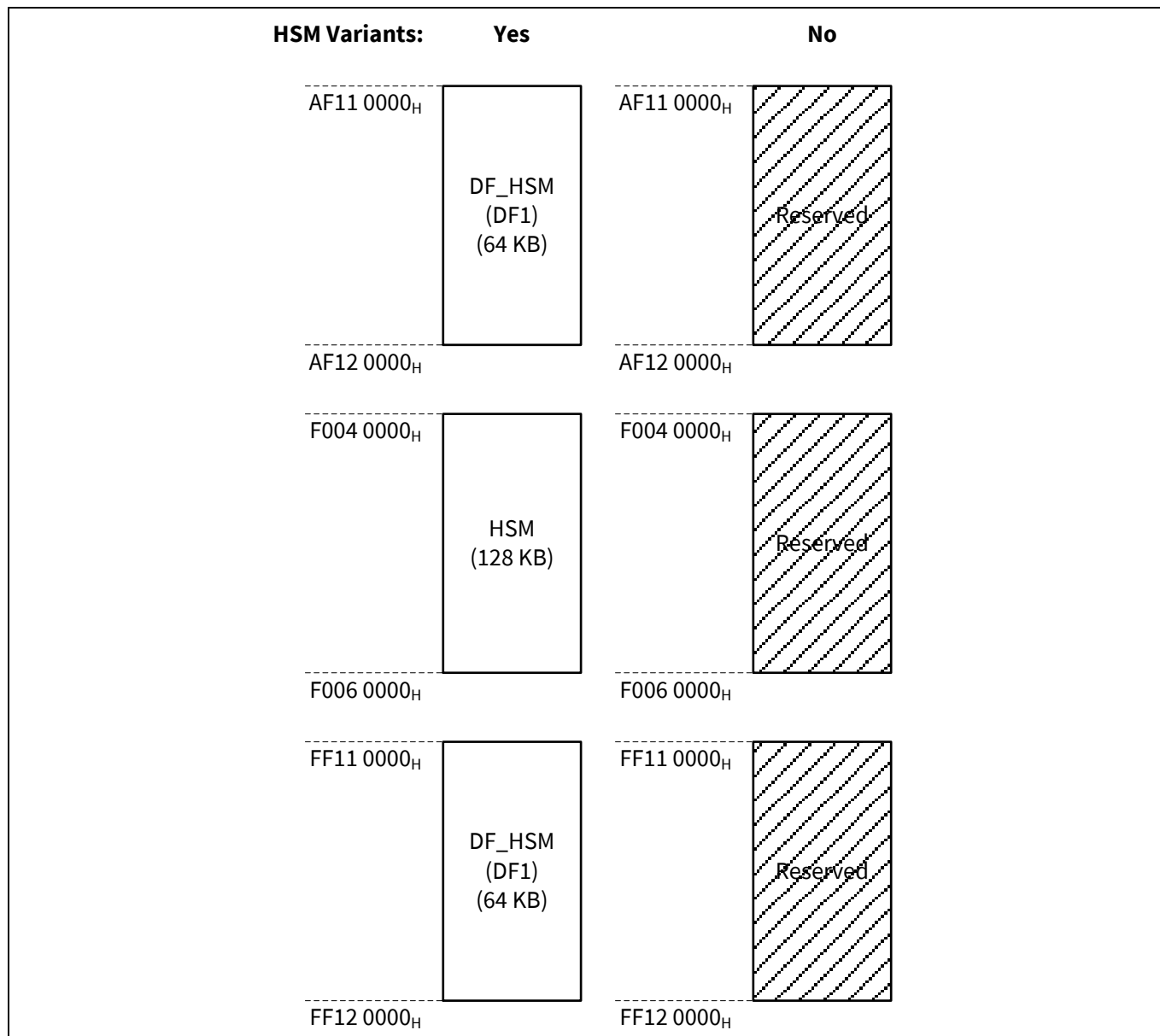
Figure 21   TC27x HSM variants

CAN FD variants

No influence on Memory Map.

CAN FD = "No" variants: all CAN register fields NCRx.FDEN have to be kept at 0_B

Memory map of variants

7.6 TC29x
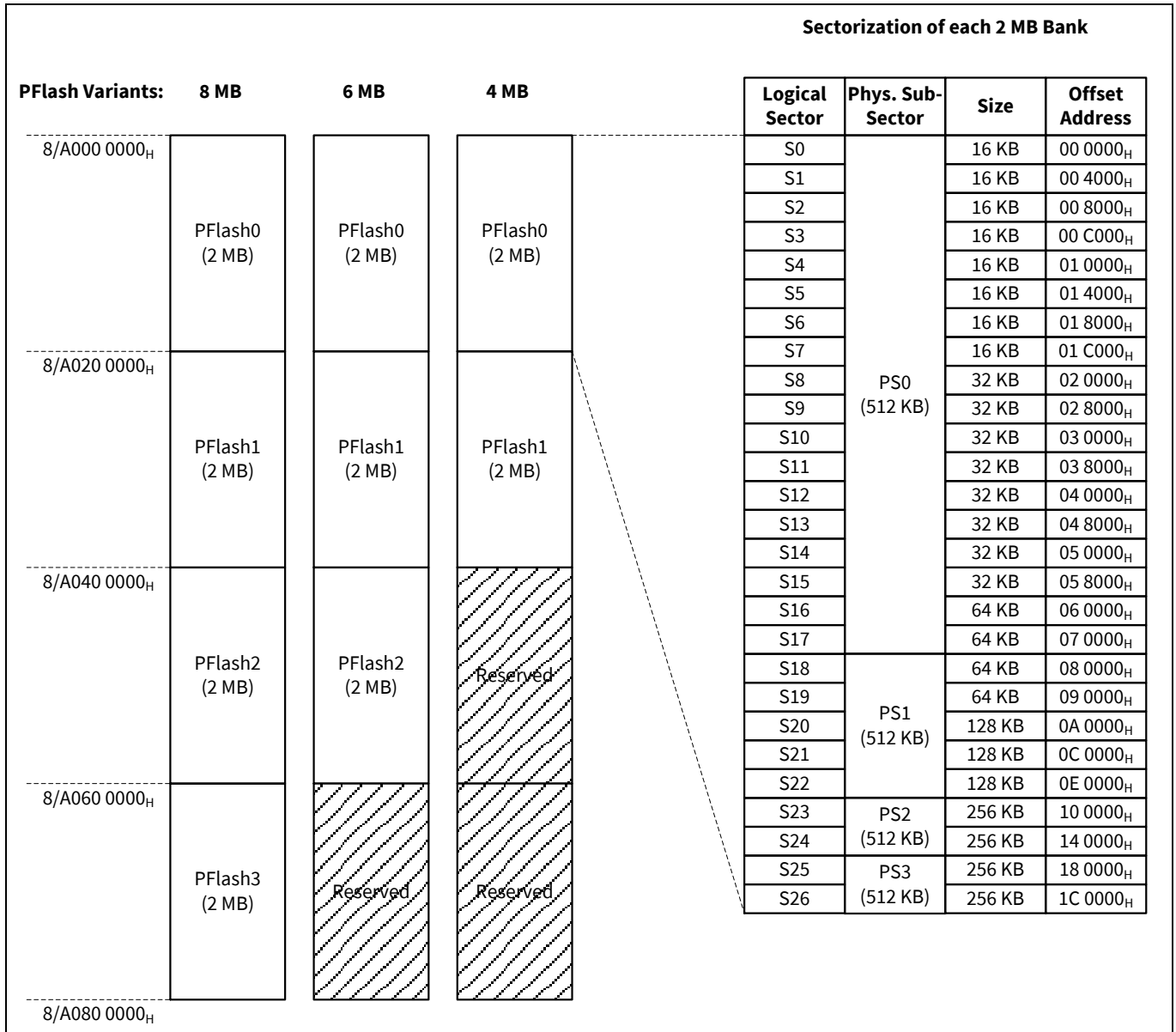
Figure 22   TC29x PFlash variants

Memory map of variants

DF_EEPROM Variants:		**768 KB**					**192 KB**	
Exemplary EEPROM size:		128 KB @ 500k					32 KB @ 500k	

	Logical Sector	**Size**	**Offset Address**			**Logical Sector**	**Size**	**Offset Address**
AF00 0000H	EEPROM0	8 KB	00 0000H		AF00 0000H	EEPROM0	8 KB	00 0000H
	EEPROM1	8 KB	00 2000H			EEPROM1	8 KB	00 2000H
	EEPROM2	8 KB	00 4000H			EEPROM2	8 KB	00 4000H
	...	...	...			...	...	...
						EEPROM23	8 KB	02 E000H
	EEPROM95	8 KB	0B E000H		AF03 0000H	Reserved		
AF0C 0000H					AF0C 0000H			
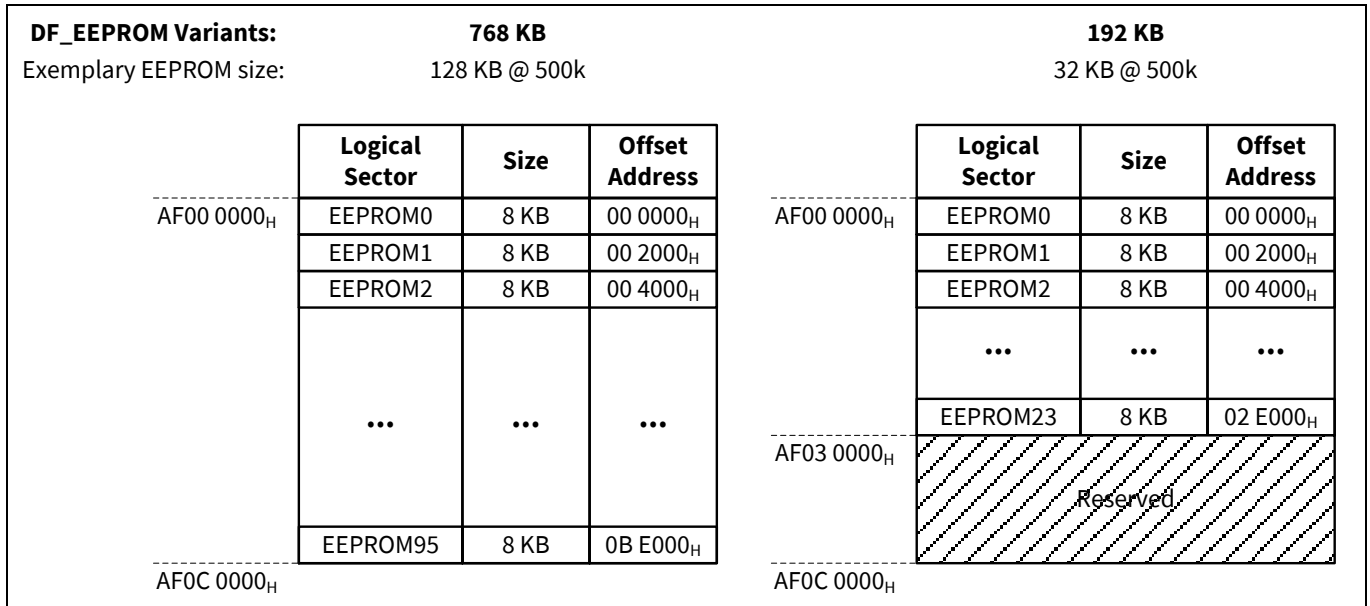
Figure 23   TC29x DF_EEPROM variants

Core1/2 DSPR Variants: 240 KB   120 KB

5000 0000H — CPU2.DSPR (240 KB) — 5003 C000H

5000 0000H — CPU2.DSPR (120 KB) — 5001 E000H — Reserved — 5003 C000H

6000 0000H — CPU1.DSPR (240 KB) — 6003 C000H

6000 0000H — CPU1.DSPR (120 KB) — 6001 E000H — Reserved — 6003 C000H
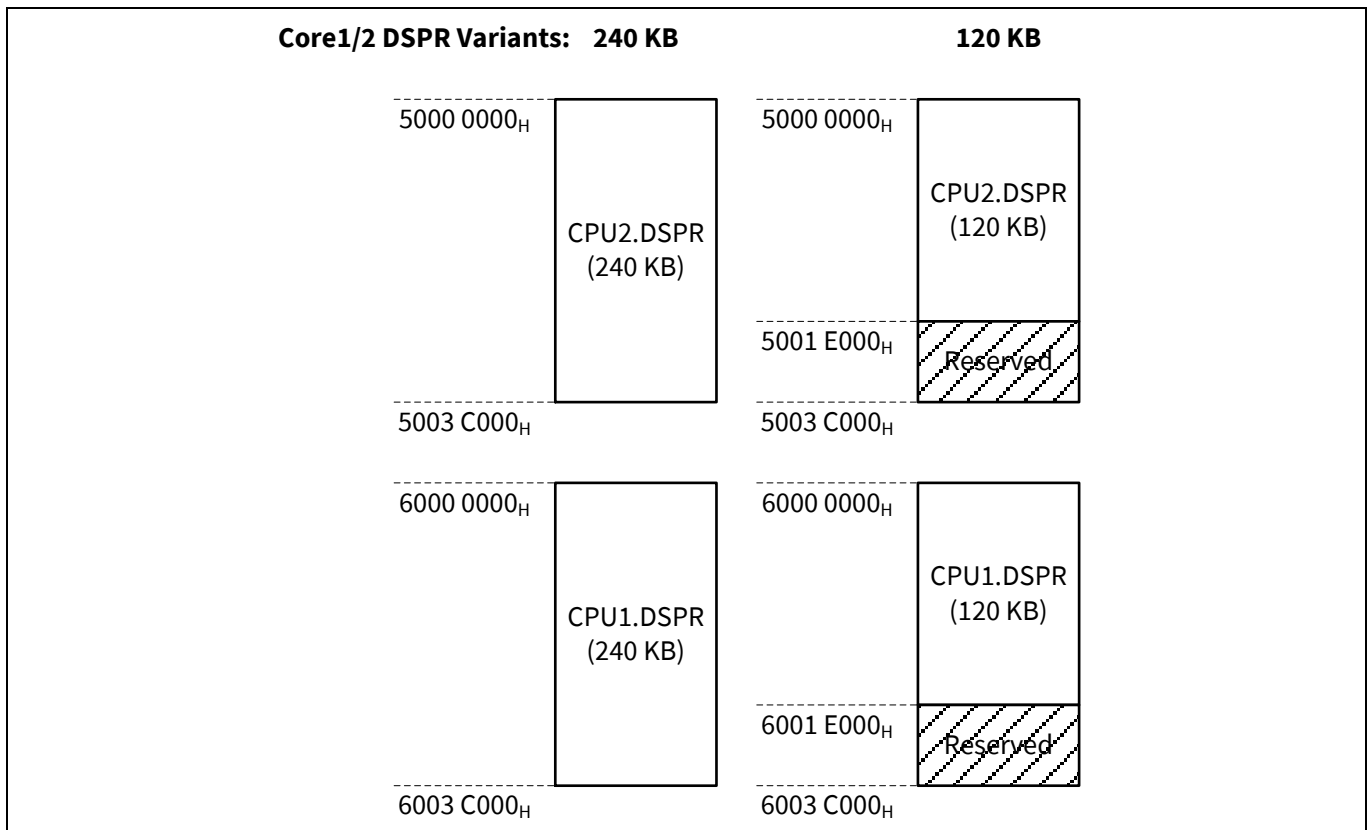
Figure 24   TC29x Core1/2 DSPR variants

Memory map of variants
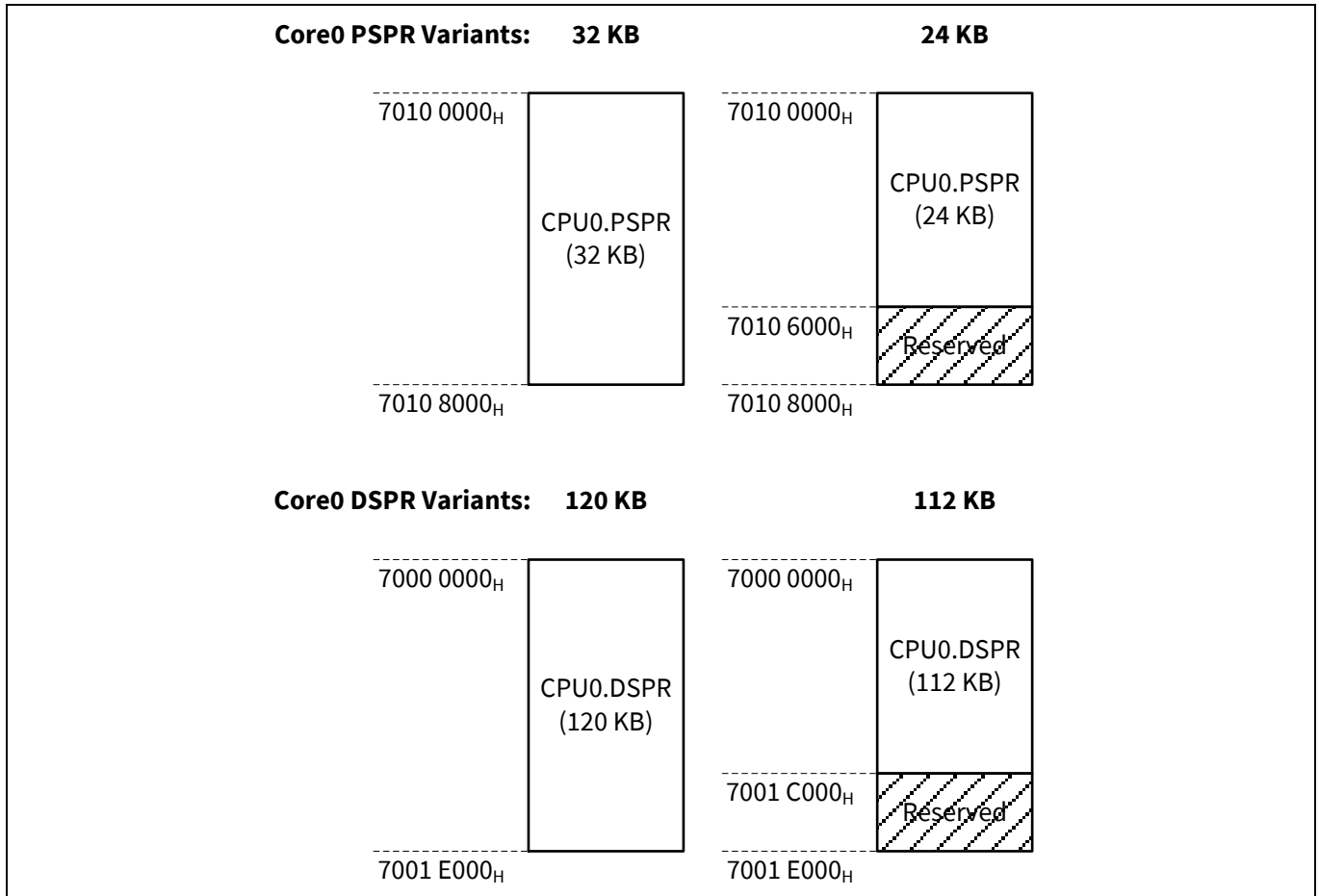
Figure 25   **TC29x Core0 PSPR / DSPR variants**
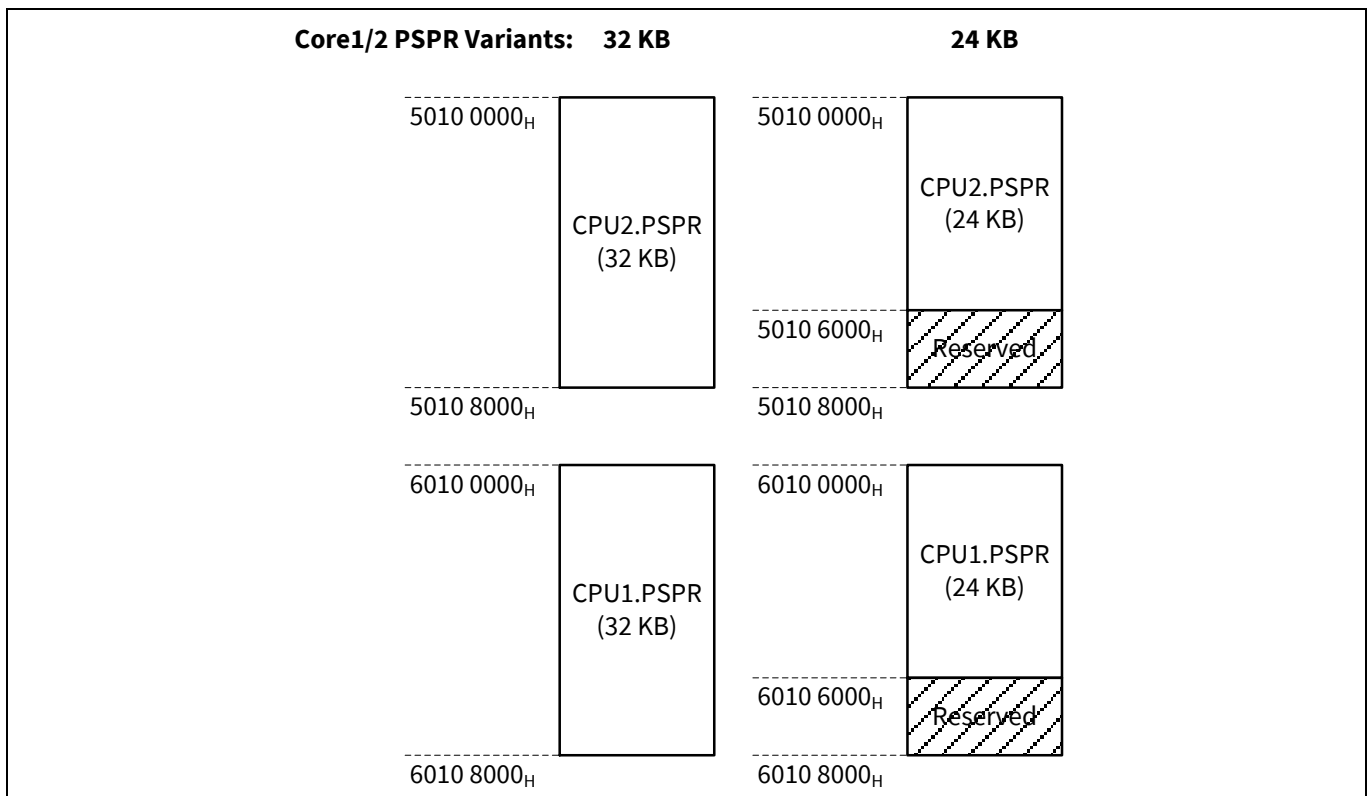
Figure 26   **TC29x Core1/2 PSPR variants**

Memory map of variants
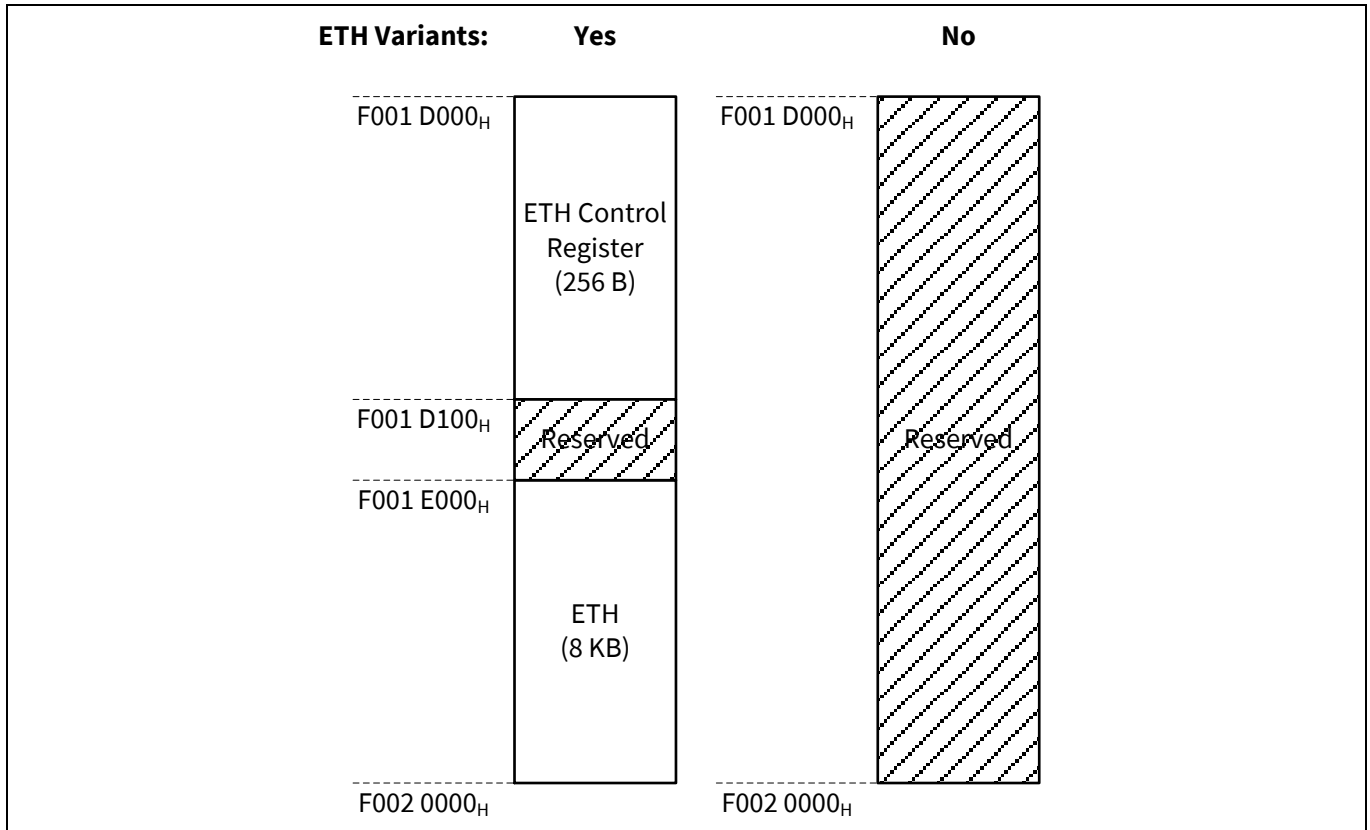
Figure 27　TC29x ETH variants
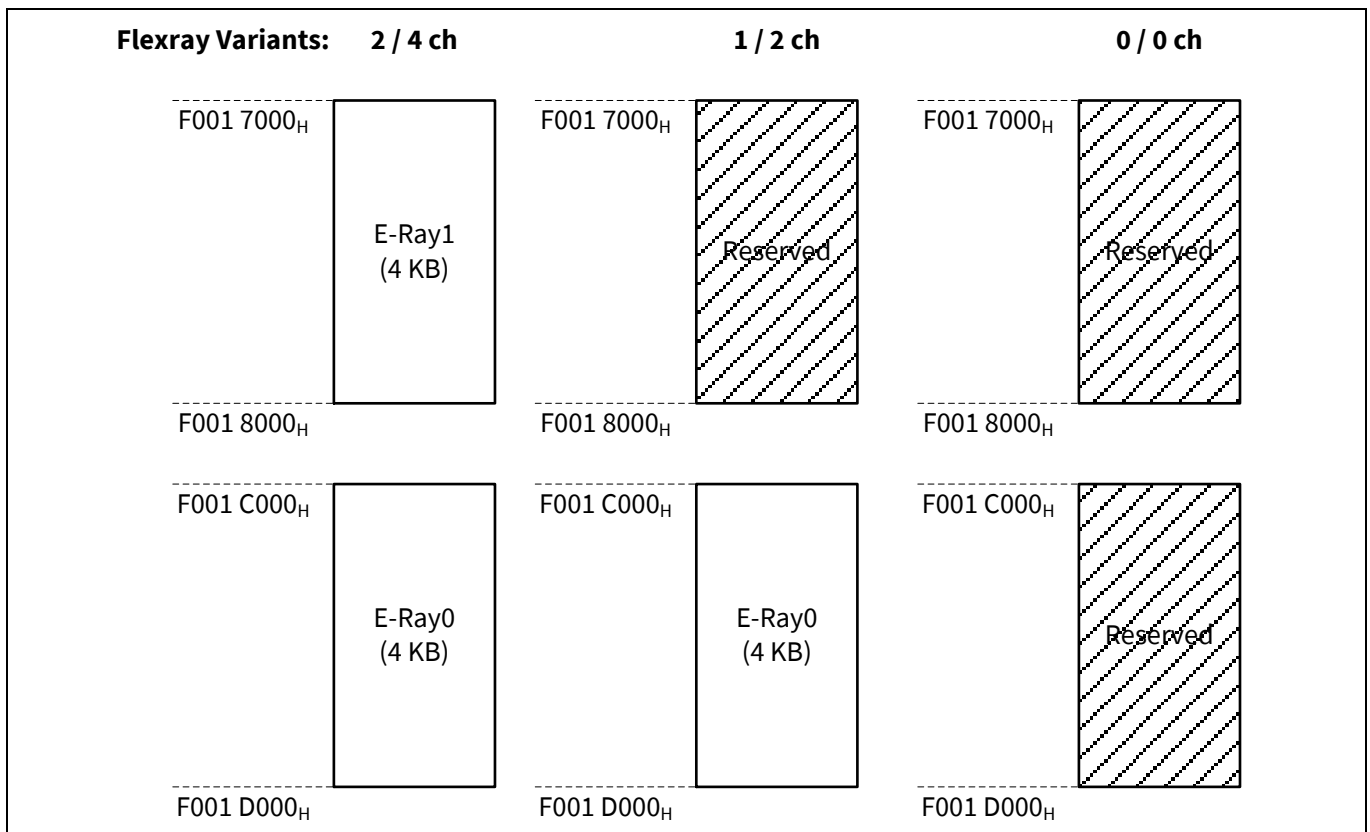
Figure 28　TC29x FlexRay variants

Memory map of variants
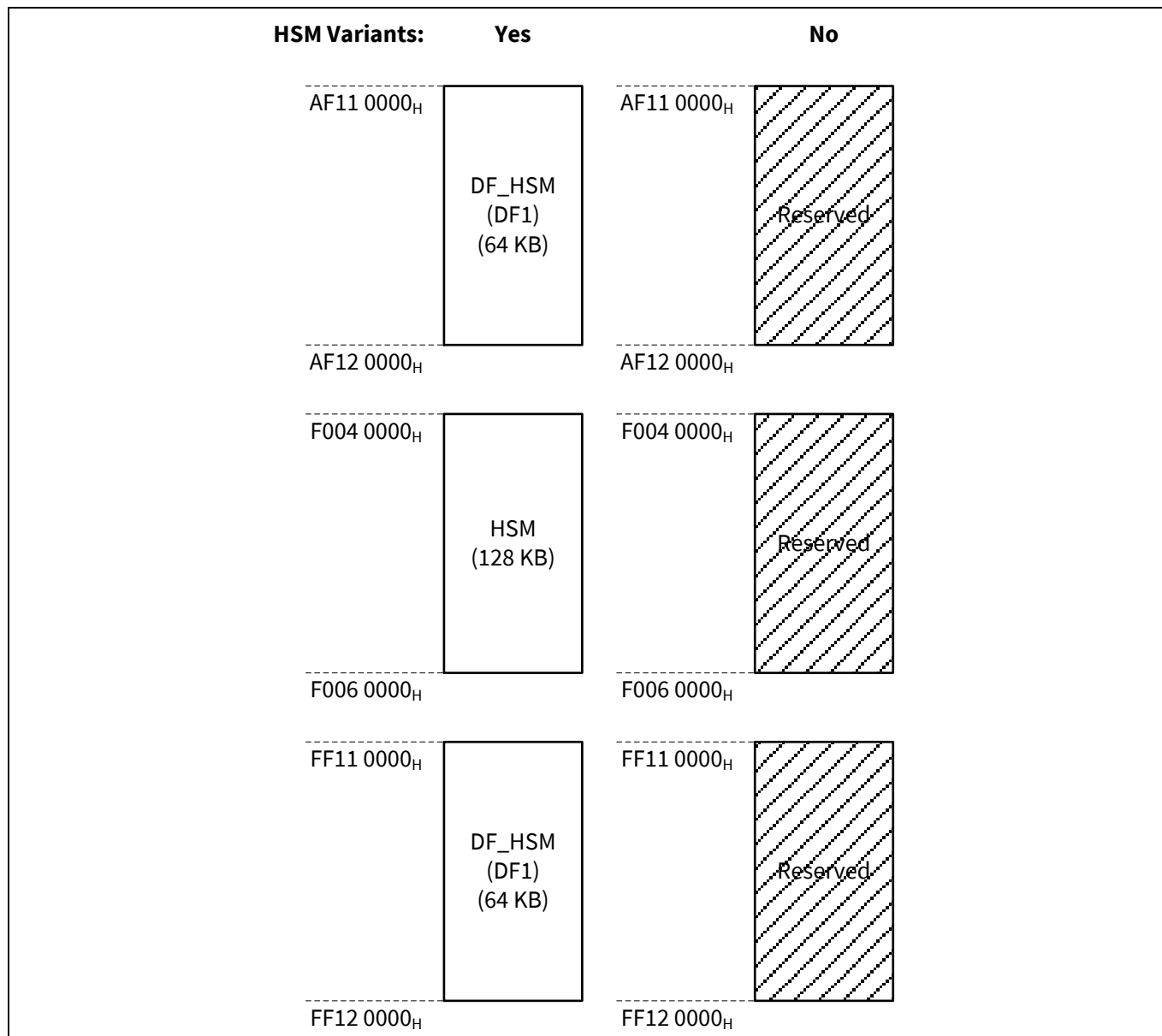
Figure 29   TC29x HSM variants

Memory map of variants
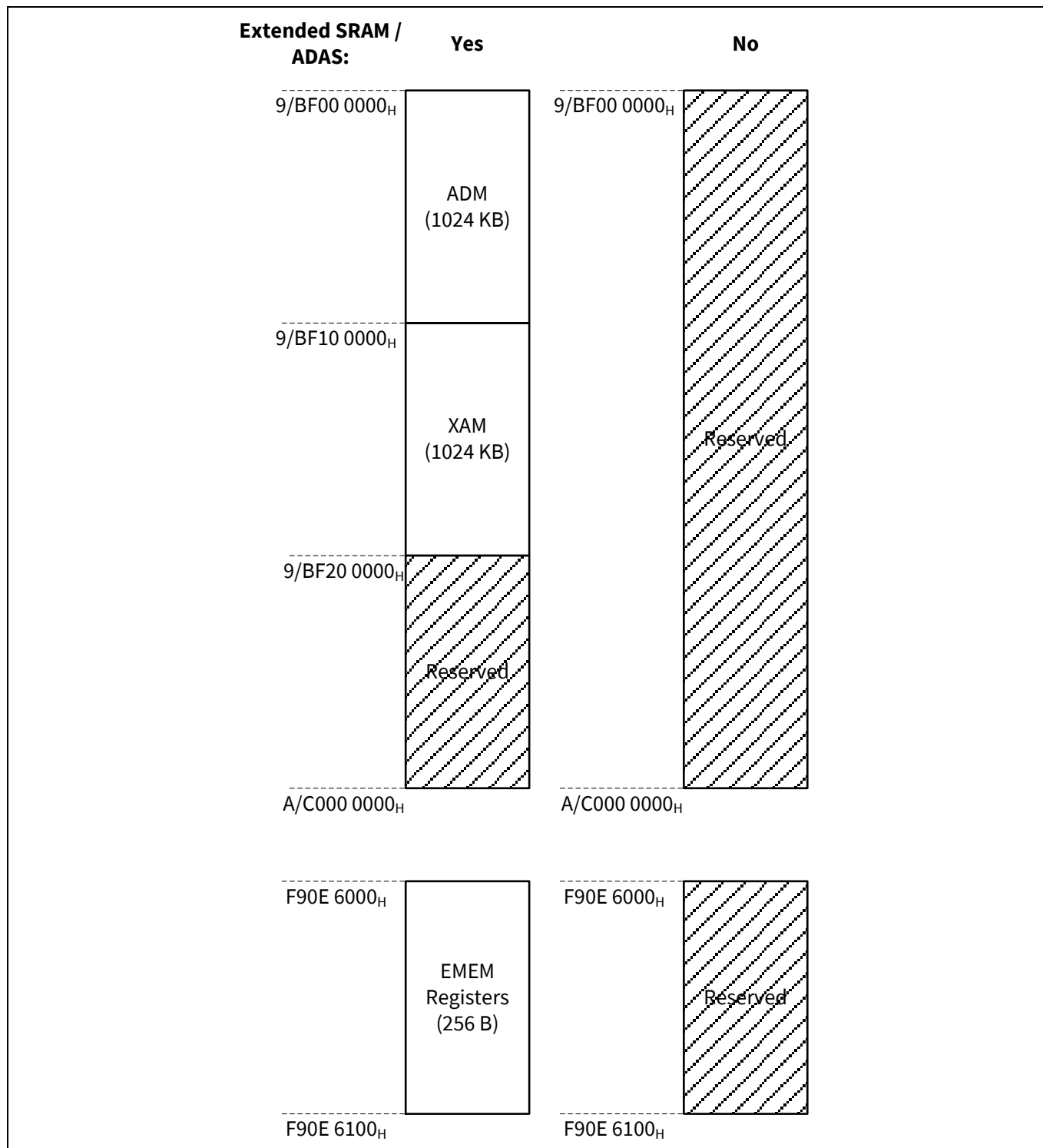
Figure 30   TC29x extended SRAM / ADAS

Memory map of variants
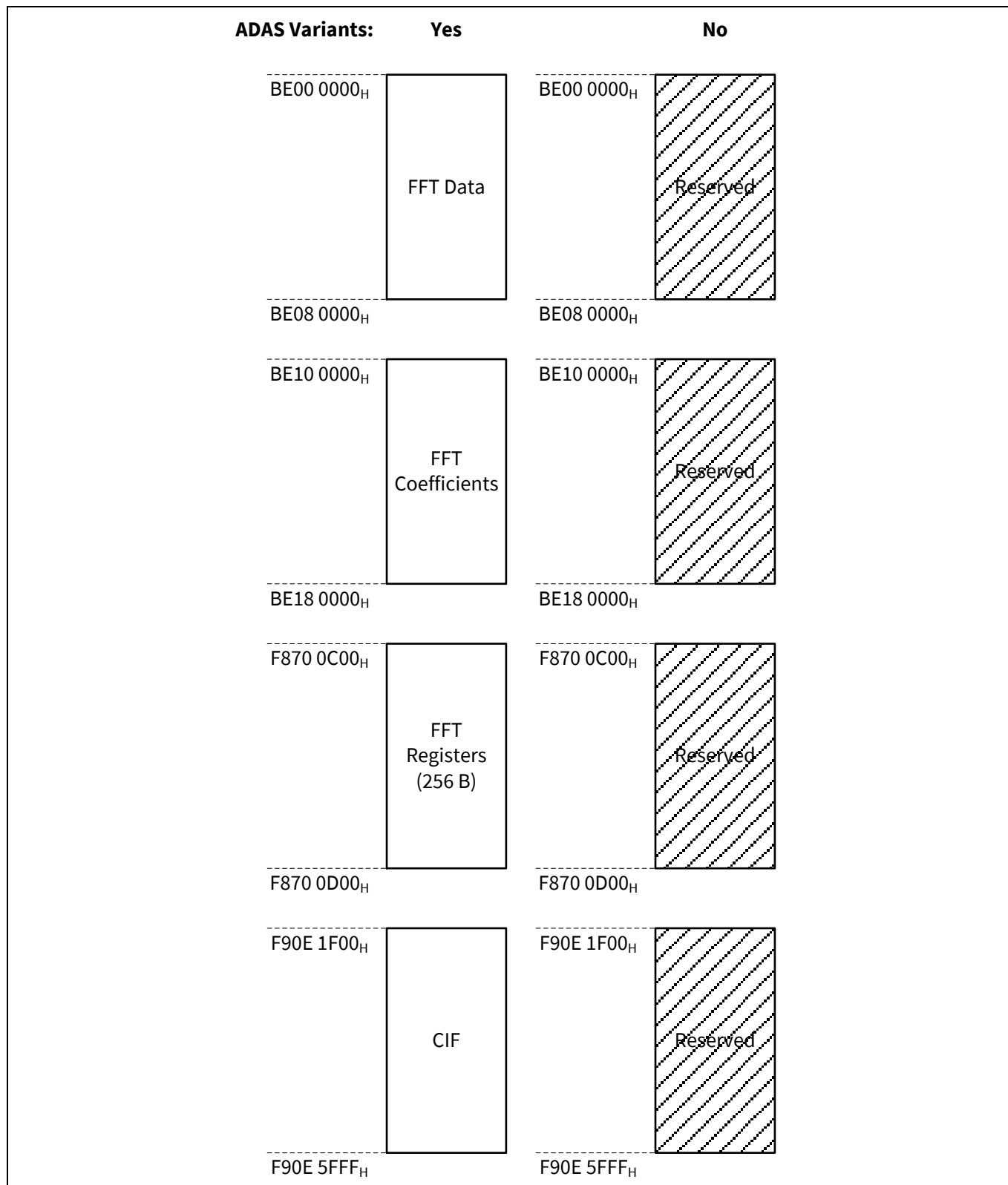
Figure 31   TC29x ADAS variants

CAN FD Variants

No influence on Memory Map.

CAN FD = "No" variants: all CAN register fields NCRx.FDEN have to be kept at 0_B

Revision history

Major changes since the last revision

Page or reference	Description of change
V1.0	First release

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