ARM Microcontroller Based Programming

Lecture 1

Introduction to ARM Processor

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Advanced RISC Machine

History

1990

ARM was formed in as Advanced RISC Machines Ltd., a joint venture of Apple Computer, Acorn Computer Group, and VLSI Technology.

1991

ARM introduced the ARM6 processor family to meet Apple requirement for its product “Personal Digital Assistant” called Newton.

Unfortunately, the Newton was not a great success and so ***Robin Saxby***, ARM’s CEO, decided to grow the business by pursuing what we now call intellectual property “IP” business model.

The ARM processor was licensed to many semiconductor companies for an upfront license fee and then royalties on production silicon. This effectively incentivized ARM to help its partner get to high volume shipments as quickly as possible.

History

1993

Nokia approached ***TI*** to produce a chipset for an upcoming GSM mobile phone and TI proposed an ARM7 based system to meet Nokia's performance and power requirements. Unfortunately Nokia rejected the proposal !

ARM came up with a radical idea to create a subset of the ARM instruction set that required just 16 bits per instruction. This improved the code density by about 35% and brought the memory footprint down to a size comparable with 16 bit microcontrollers.

The first ARM-powered GSM phone was the hugely popular ***Nokia6110*** and the ***ARM7TDMI***.

History

1997

ARM had grown to become a £27m business with a net income of £3m !
ARM then decided to build software-based systems on a single chip, the so-called system-on-chip, or SoC.

2001

ARM9 was announced. It was fully synthesizable with a 5 stage pipeline and a proper MMU, as well as hardware support for Java acceleration and some DSP extension.

2002

ARM11 families had extended the capability of the ARM architecture in the direction of higher performance with the introduction of multi-processing, SIMD multimedia instructions, DSP capability, Java acceleration etc

Advanced RISC Machine

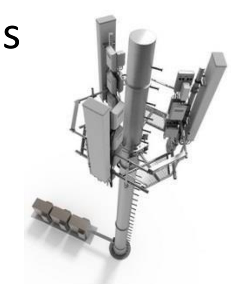
History

ARM® CORTEX®
Processor Technology

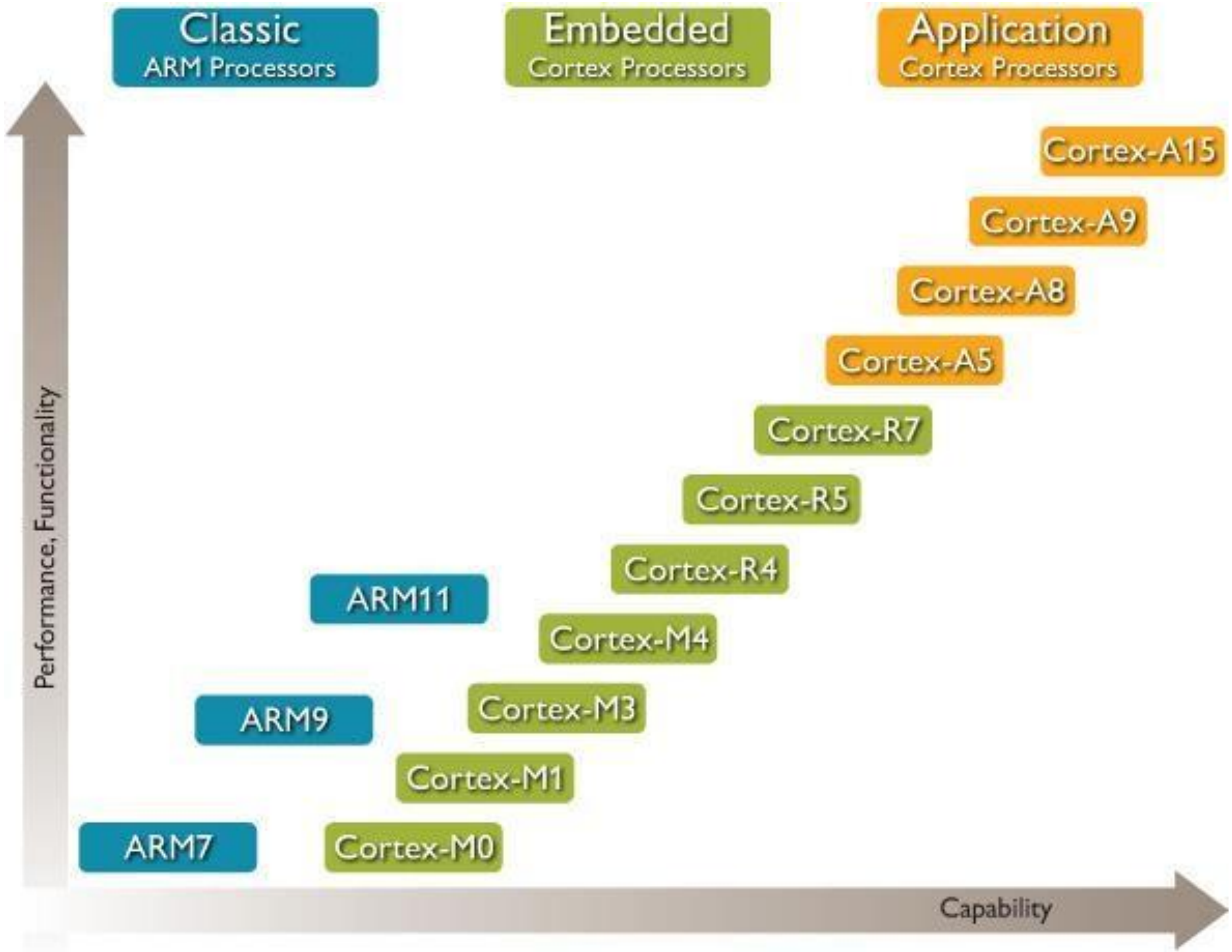
2005

The ARM Cortex … !

Cortex - A	Cortex - R	Cortex - M
Application Processors for full OS and Open Application Platforms	Embedded Processors for real time signal processing and control applications	Microcontroller Oriented Processors



ARM Processor Roadmap



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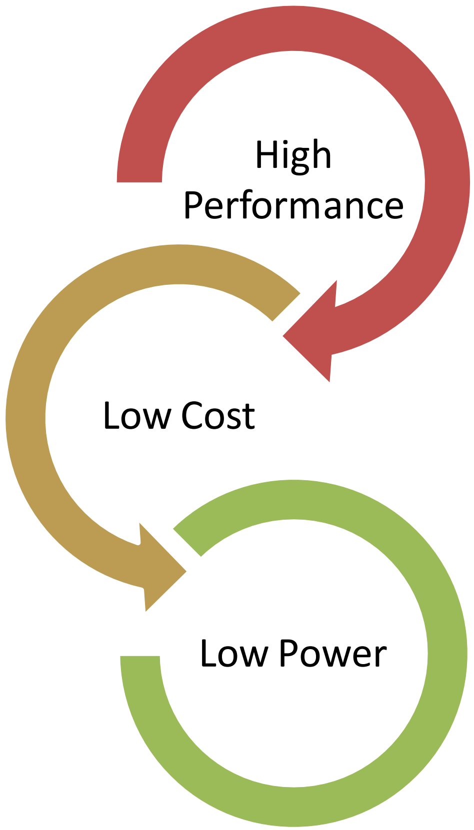
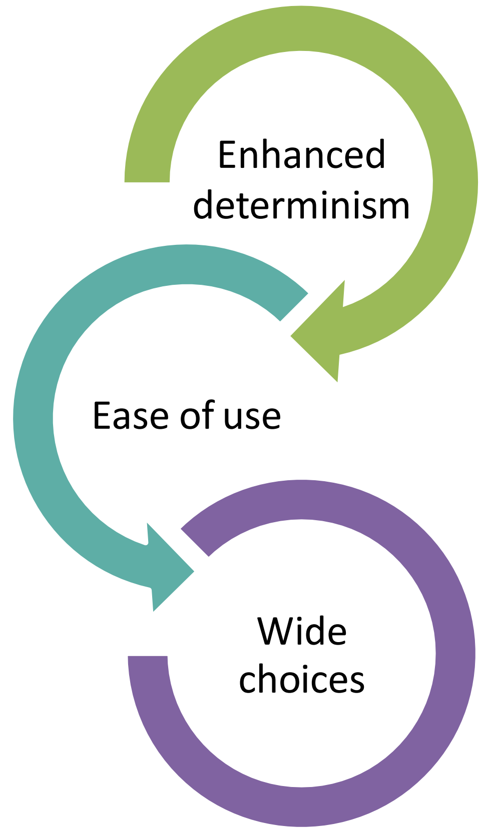
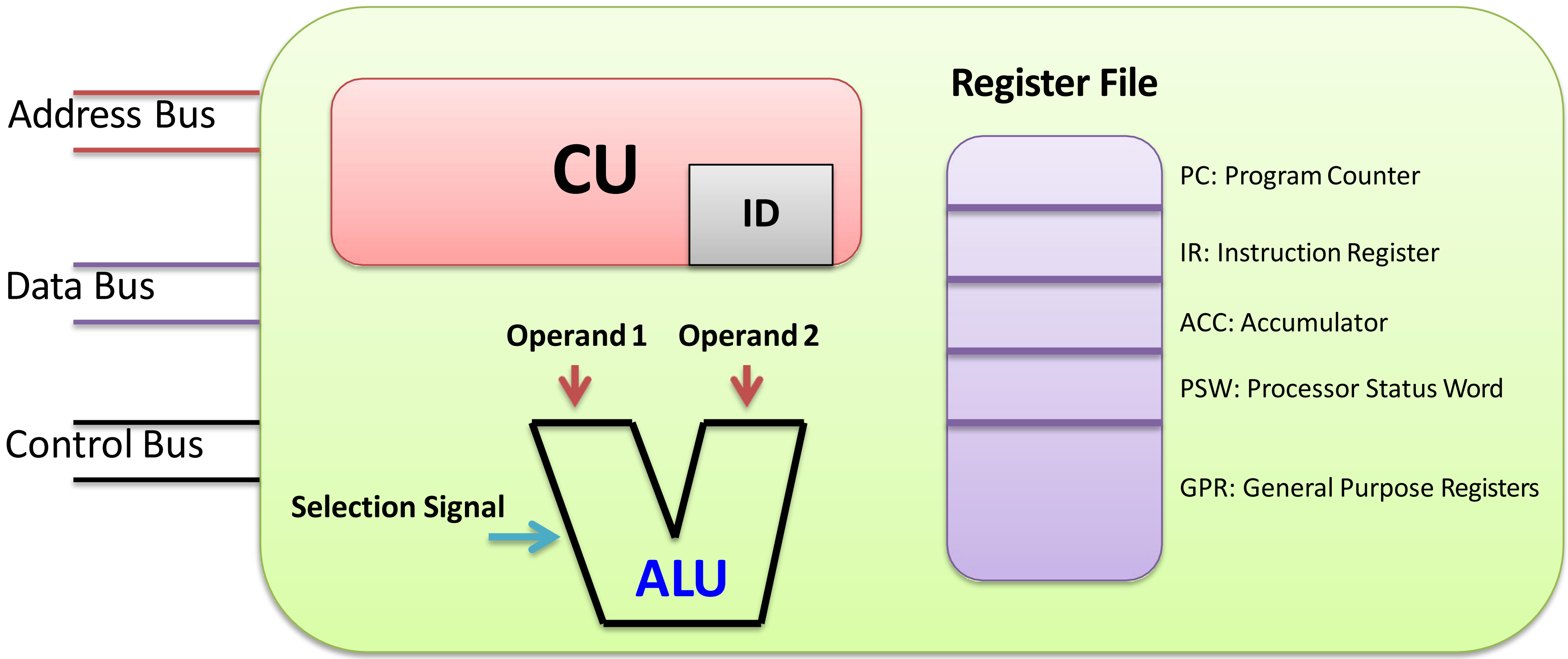
ARM Silicon Partners

ARM Major Characteristics





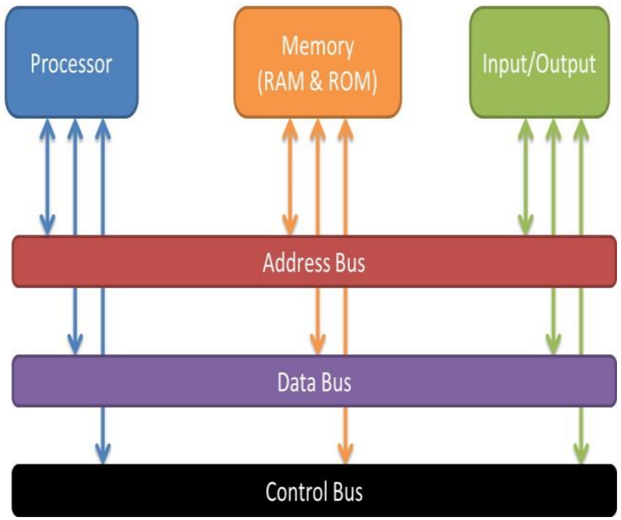
General Processor Architecture



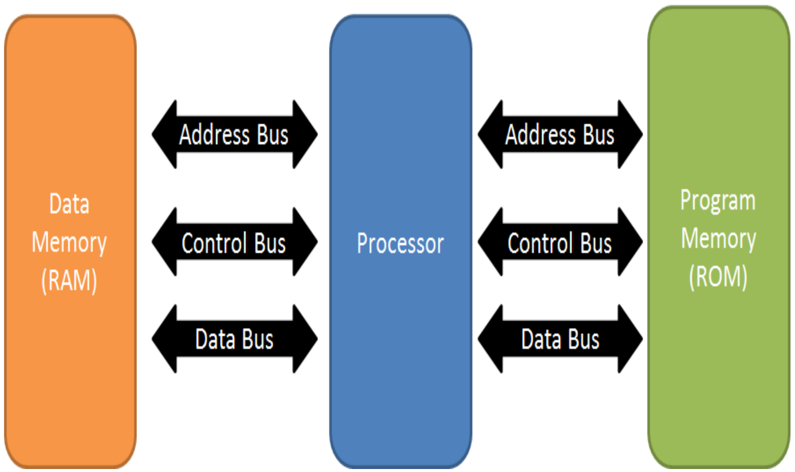
CU : Control Unit
ID : Instruction Decoder
ALU: Arithmetic Logic Unit

Von Neumann Vs Harvard Architecture

1- Von Numann



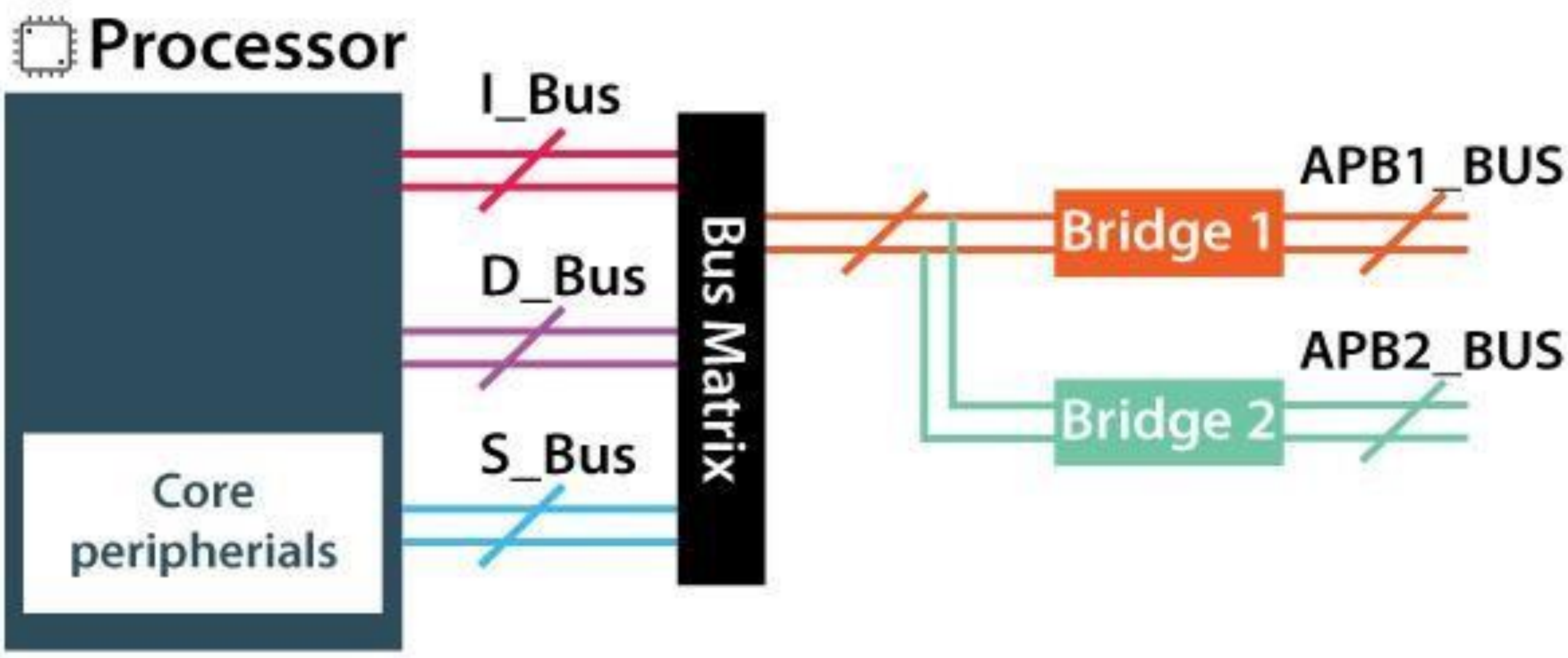
2- Harvard Architecture



- Simple in Design
- The code is executed serially

- Complex in design
- The code is executed in parallel

ARM Hybrid Architecture

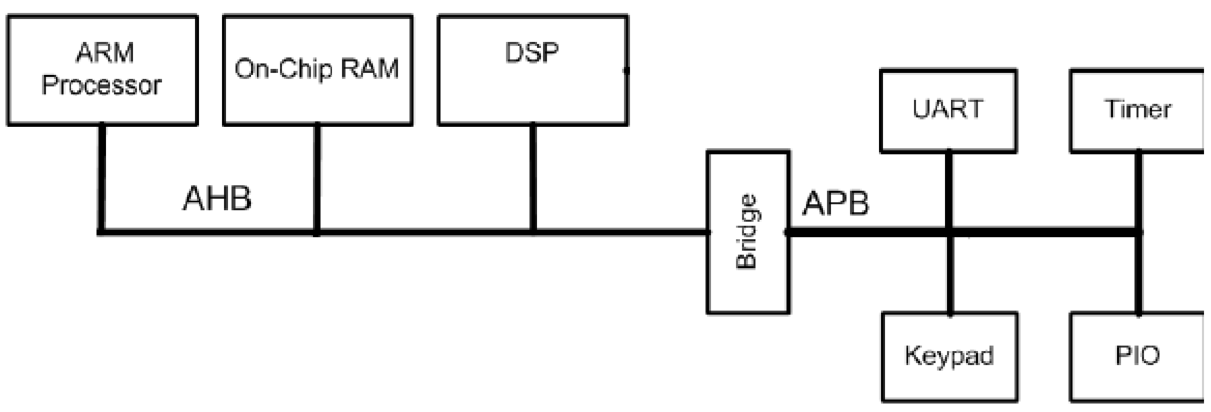


ARM Hybrid Architecture

AMBA Bus

Advanced Microcontroller Bus Architecture

AMBA is a description or a documentation of how to connect the external peripherals. Because of success of AMBA documentation, the other microcontroller companies use it into their microcontroller products.



AHB Vs APB

AHB

stands for *Advanced High Performance Bus*

- High Performance
- Full Duplex
- Support Pipelining
- MultiMaster operation
- Complex in design
- Max speed is 72 MHz .

APB

stands for *Advanced Peripheral Bus*

- Low Power
- No Pipelining
- Simple in design
- Used for connecting peripherals
- Max speed is 36 MHz .

Operation Modes

Access Level:

Privileged Level:

At this mode, Processor can access any thing at microcontroller.

User Level:

At this mode, Processor is prohibited from accessing somethings at microcontroller like MPU “Memory Protection Unit”.

Processor Mode:

Thread Mode:

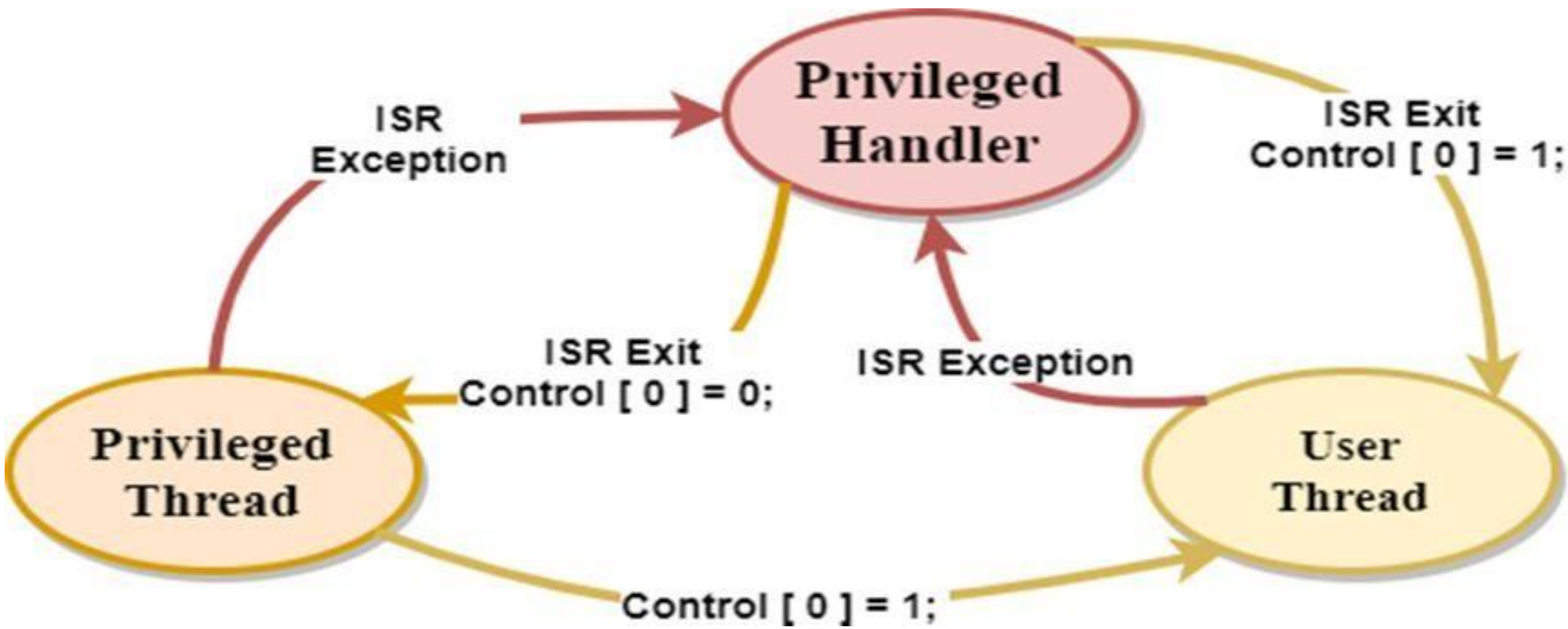
At this mode, program runs at normal code.
Processor can be Privileged or user at this mode.

Handler Mode:

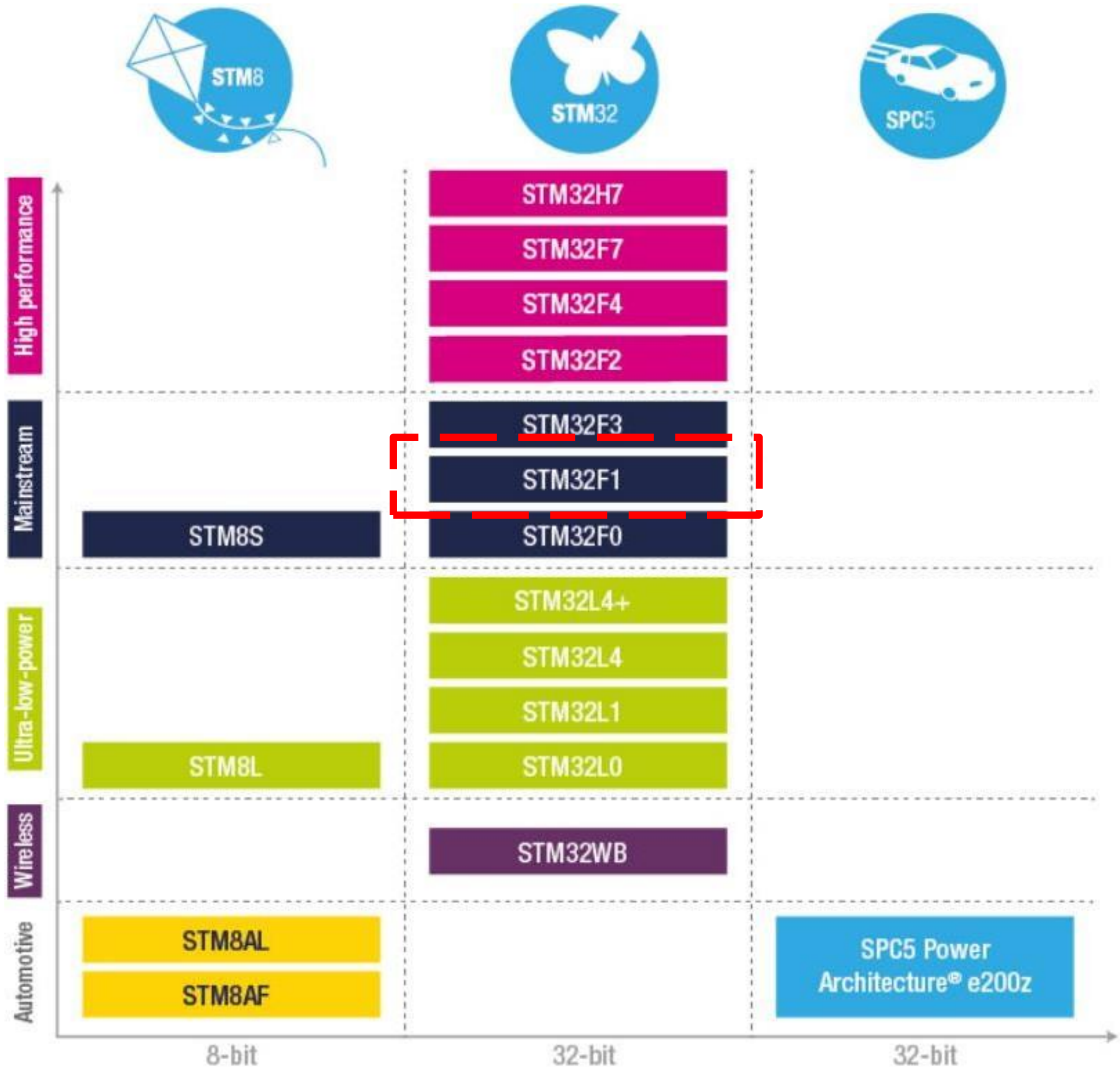
At this mode, program runs at interrupt level.
Processor can be Privileged only.

Operation Modes

Conversion from Privileged to User and vice versa:

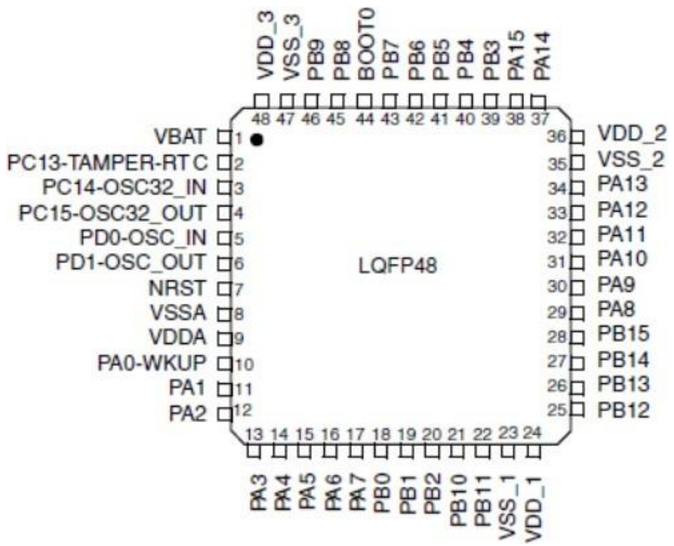


ST Product lines

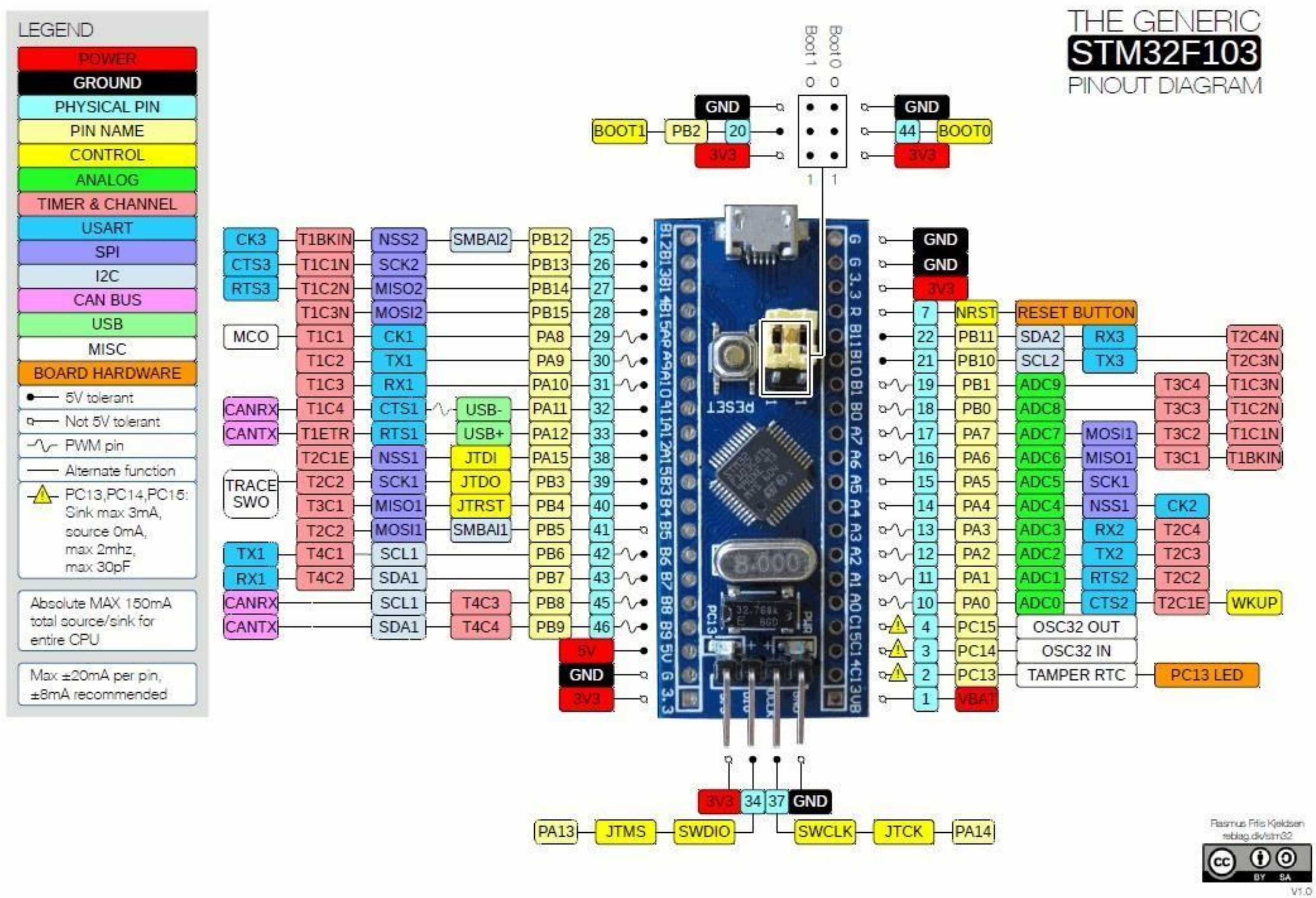


STM32F103C8 Specifications

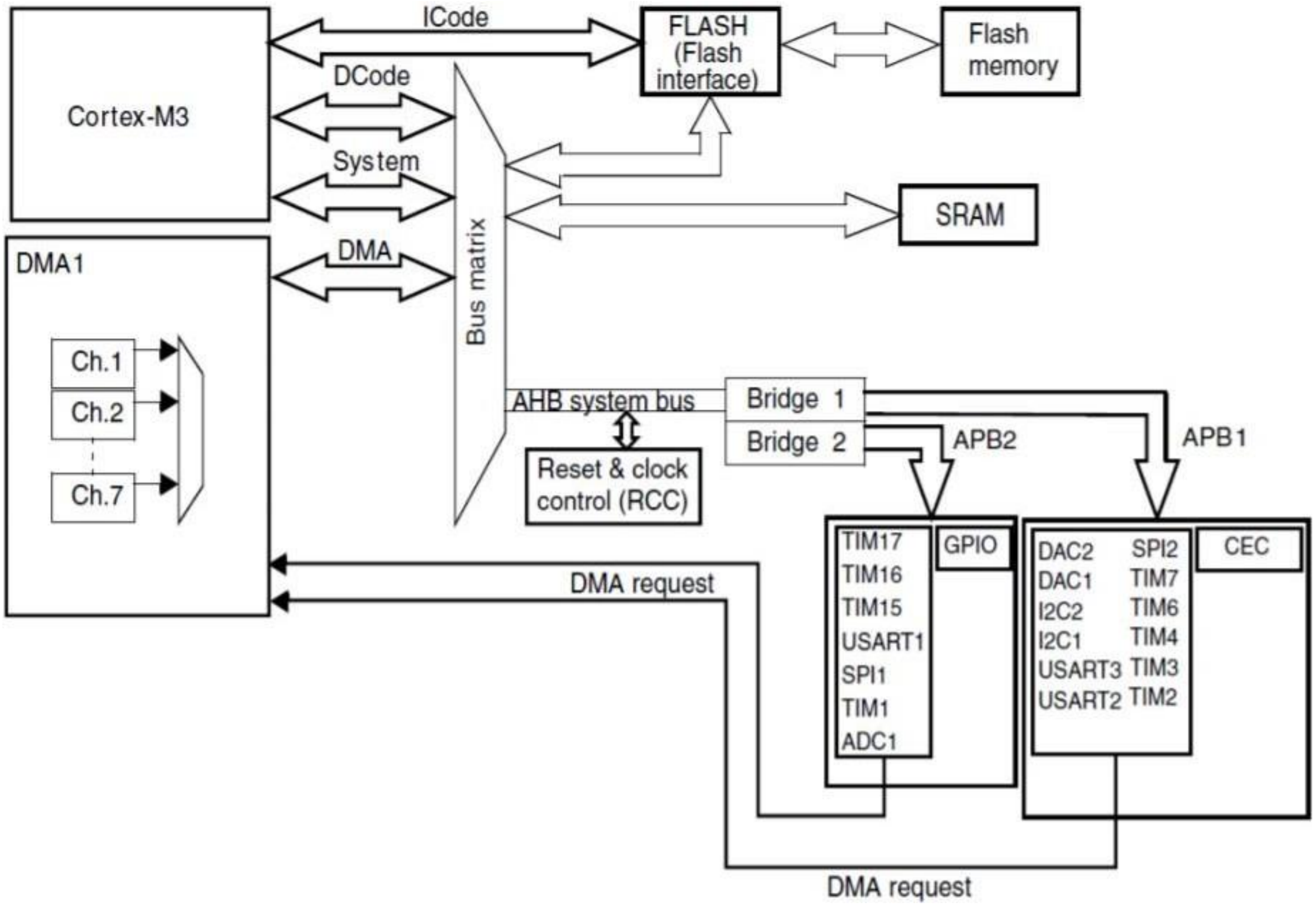
Core	ARM Cortex-M3
Max Operating Frequency	72 MHz
Flash Memory Size	64 KB
RAM Size	20 KB
Timers	4 x 16 Bit Timers 2 x WDT 24-Bit Down Counter RTC
ADC Converter	10 x 12 Bit Channels
GPIO	32 High Current + 3 low current
I2C Bus	2 Channels
SPI Bus	2 Channels
USART Bus	3 Channels
CAN Bus	1 Channel
Operating Voltage	2 to 3.6 Voltage
Operating Temperature	- 40 to 105 Degree C



Development Kit



Processor Architecture



Bus Connections

Boundary address	Peripheral	Bus
0x4002 3000 - 0x4002 33FF	CRC	AHB
0x4002 2400 - 0x4002 2FFF	Reserved	
0x4002 2000 - 0x4002 23FF	Flash memory interface	
0x4002 1400 - 0x4002 1FFF	Reserved	
0x4002 1000 - 0x4002 13FF	Reset and clock control RCC	
0x4002 0400 - 0x4002 0FFF	Reserved	
0x4002 0000 - 0x4002 03FF	DMA1	
0x4001 4C00 - 0x4001 FFFF	Reserved	APB2
0x4001 4800 - 0x4001 4BFF	TIM17 timer	
0x4001 4400 - 0x4001 47FF	TIM16 timer	
0x4001 4000 - 0x4001 43FF	TIM15 timer	
0x4001 3C00 - 0x4001 3FFF	Reserved	
0x4001 3800 - 0x4001 3BFF	USART1	
0x4001 3400 - 0x4001 37FF	Reserved	
0x4001 3000 - 0x4001 33FF	SPI1	
0x4001 2C00 - 0x4001 2FFF	TIM1 timer	
0x4001 2800 - 0x4001 2BFF	Reserved	
0x4001 2400 - 0x4001 27FF	ADC1	
0x4001 1C00 - 0x4001 23FF	Reserved	
0x4001 1800 - 0x4001 1BFF	GPIO Port E	
0x4001 1400 - 0x4001 17FF	GPIO Port D	
0x4001 1000 - 0x4001 13FF	GPIO Port C	
0x4001 0C00 - 0x4001 0FFF	GPIO Port B	
0x4001 0800 - 0x4001 0BFF	GPIO Port A	
0x4001 0400 - 0x4001 07FF	EXTI	
0x4001 0000 - 0x4001 03FF	AFIO	

Boundary address	Peripheral	Bus
0x4000 7C00 - 0x4000 FFFF	Reserved	APB1
0x4000 7800 - 0x4000 7BFF	CEC	
0x4000 7400 - 0x4000 77FF	DAC	
0x4000 7000 - 0x4000 73FF	Power control PWR	
0x4000 6C00 - 0x4000 6FFF	Backup registers (BKP)	
0x4000 5C00 - 0x4000 6BFF	Reserved	
0x4000 5800 - 0x4000 5BFF	I2C2	
0x4000 5400 - 0x4000 57FF	I2C1	
0x4000 4C00 - 0x4000 53FF	Reserved	
0x4000 4800 - 0x4000 4BFF	USART3	
0x4000 4400 - 0x4000 47FF	USART2	
0x4000 3C00 - 0x4000 3FFF	Reserved	
0x4000 3800 - 0x4000 3BFF	SPI2	
0x4000 3400 - 0x4000 37FF	Reserved	
0x4000 3000 - 0x4000 33FF	Independent watchdog (IWDG)	
0x4000 2C00 - 0x4000 2FFF	Window watchdog (WWDG)	
0x4000 2800 - 0x4000 2BFF	RTC	
0x4000 1800 - 0x4000 27FF	Reserved	
0x4000 1400 - 0x4000 17FF	TIM7 timer	
0x4000 1000 - 0x4000 13FF	TIM6 timer	
0x4000 0C00 - 0x4000 0FFF	Reserved	
0x4000 0800 - 0x4000 0BFF	TIM4 timer	
0x4000 0400 - 0x4000 07FF	TIM3 timer	
0x4000 0000 - 0x4000 03FF	TIM2 timer	

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