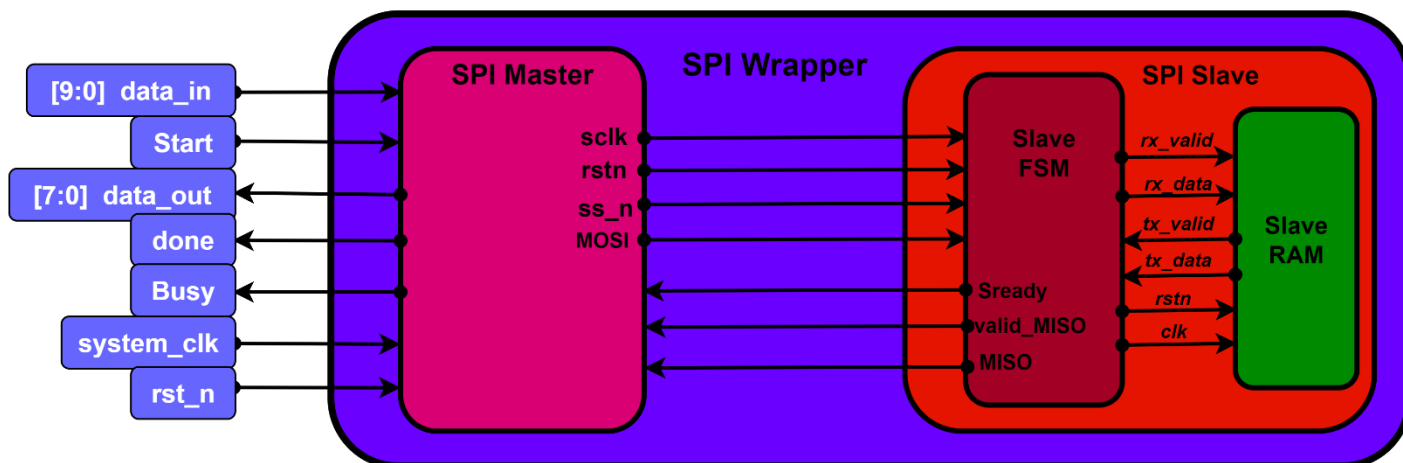
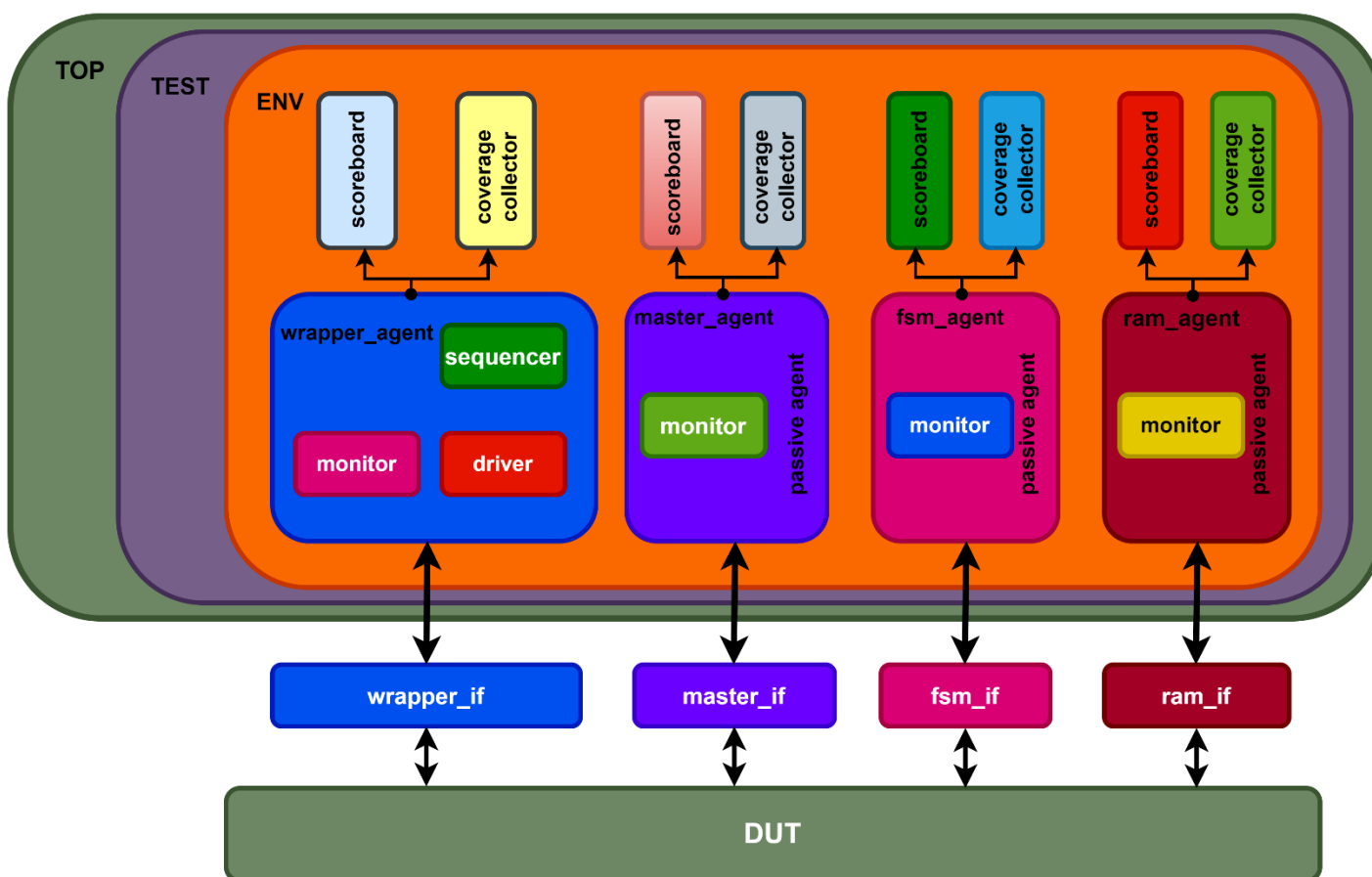


Simple SPI Master-Slave Interface

RTL Design and Verification with SVA, UVM, and COCOTB



--- Top-level design Wrapper ---



--- UVM Testbench Architecture ---

Design Specifications

1.Master Specs

Port	Direction	Function
<i>data_in</i>	input	Parallel input vector from the wrapper representing a read/write transaction. This data is serialized and transmitted to the slave via the MOSI line.
<i>start</i>	input	Initiates an SPI transaction when asserted.
<i>busy</i>	output	Indicates an ongoing SPI transfer. When busy is high, new transactions via start are ignored until the current transfer completes.
<i>data_out</i>	output	Parallel output data received via MISO, valid after transfer completes.
<i>done</i>	output	Asserted for one cycle when the current SPI transaction (read/write) finishes.
<i>ss_n</i>	output	Active-low signal used to select the slave device. When asserted, the master initiates transmission by sending the <i>data_in</i> starting with the MSB on the next clock cycle on MOSI
<i>MOSI</i>	output	Serial data line for transmitting bits to the slave, sending the <i>data_in</i> vector serially starting from the most significant bit (MSB)
<i>sready</i>	input	Indicates the slave is ready to receive the next transaction. The master waits until this signal is asserted, which occurs after the slave completes the current transaction.
<i>valid_MISO</i>	input	Indicates valid data is present on the MISO line.
<i>MISO</i>	input	Serial data line to receive bits from the slave.

2.Slave Specs

2.1.Slave FSM Specs

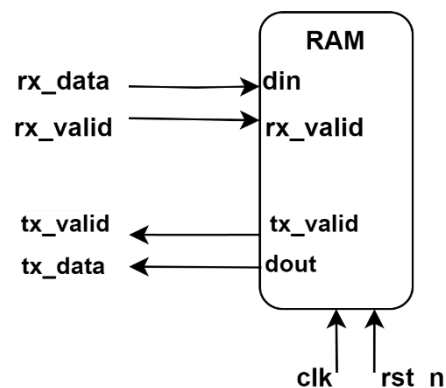
Port	Direction	Function
<i>sclk</i>	input	Serial clock signal driven by the master. The slave uses this clock to sample incoming data on MOSI and shift out data on MISO.
<i>ss_n</i>	input	Active-low slave select. When asserted low by the master, the slave is activated and starts data reception/transmission on the next <i>sclk</i> edge.
<i>MOSI</i>	input	Serial data line carrying bits from the master to the slave. Data is typically shifted in MSB first.
<i>sready</i>	output	Indicates the slave is ready to accept a new transaction. Asserted after completing the current read/write operation.
<i>valid_MISO</i>	output	Asserted when the slave has valid data available on the MISO line for the master to read.
<i>MISO</i>	output	Serial data line carrying bits from the slave to the master, shifted out in sync with <i>sclk</i> .

2.2.Slave RAM Specs

Port	Direction	Function
<i>rx_valid</i>	input	Asserted by the FSM when a complete 10-bit command has been received via MOSI. Indicates valid data for processing.
<i>rx_data</i>	input	The 10-bit vector received from MOSI, containing the command (e.g., read/write) and address/data
<i>tx_valid</i>	output	Asserted by the FSM during a read transaction to indicate valid <i>tx_data</i> is available for transmission.
<i>tx_data</i>	output	The 8-bit data read from memory, which will be serialized and sent to the master via MISO

2.2.1.Slave RAM operations

din[9:8]	command	description
00	Write	hold din[7:0] as write address
01	write	Write din[7:0] in the memory with the write address held previously
10	read	Hold din[7:0] as read address
11	read	Read the memory with the read address held previously.



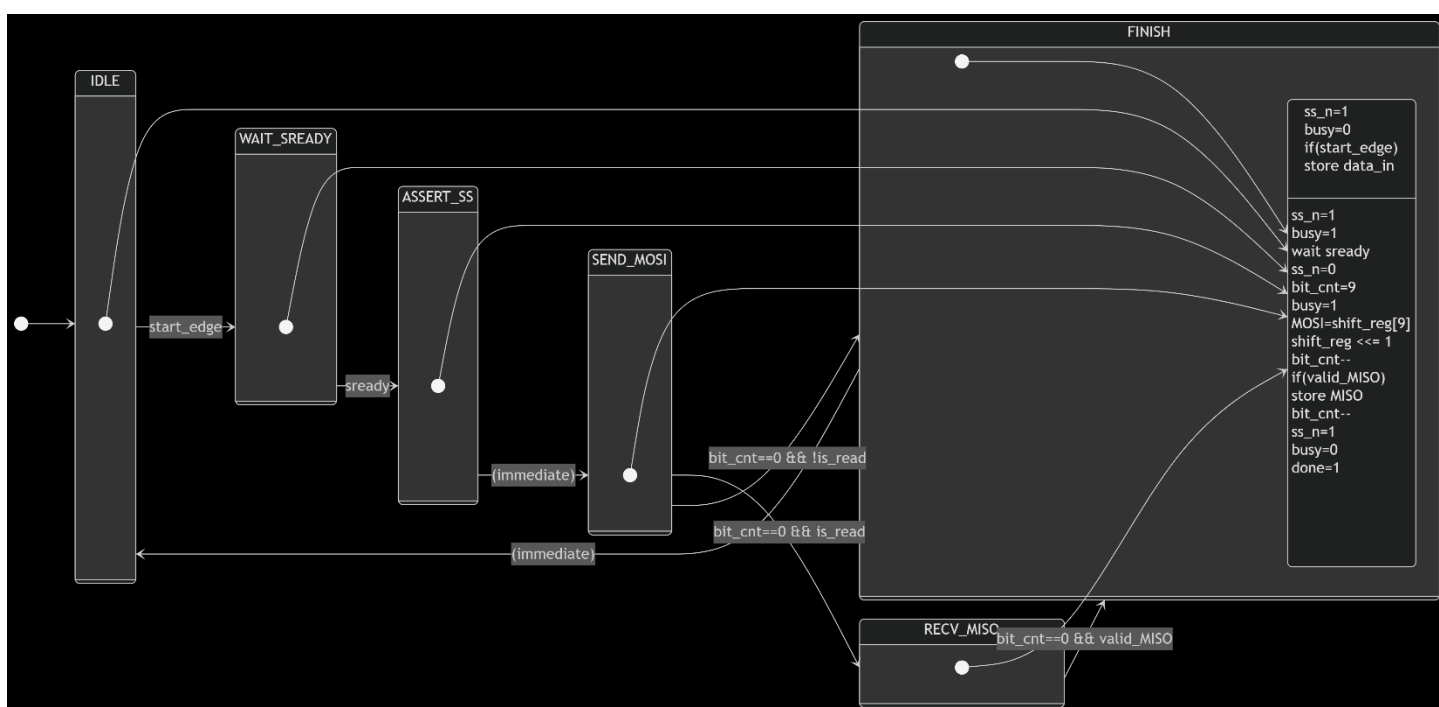
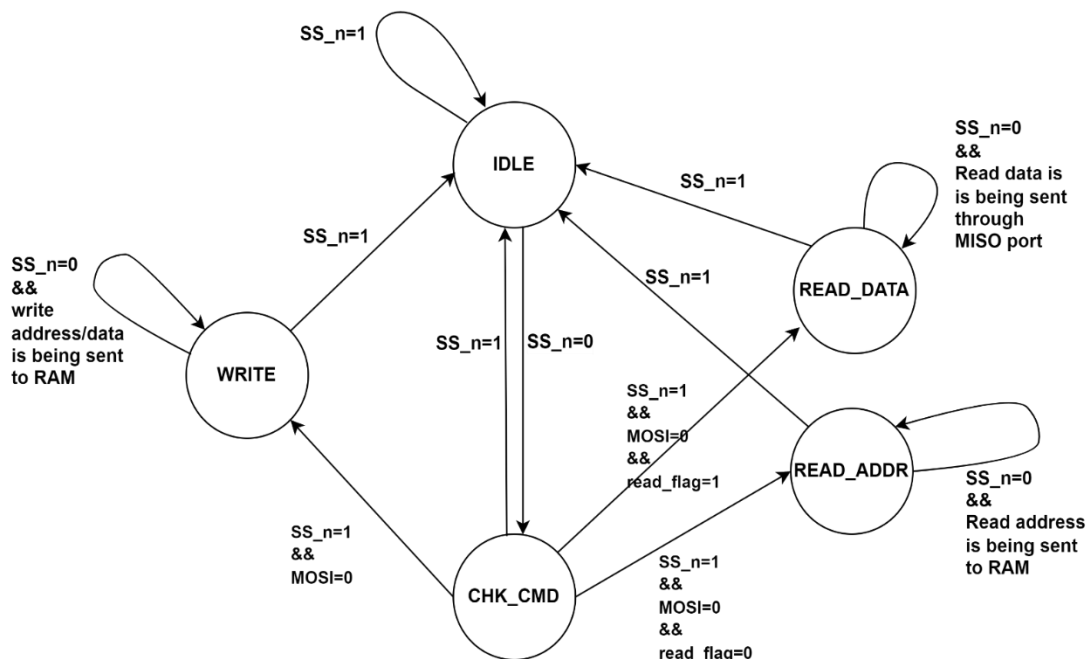
Slave Operations Summary

When the SPI slave is selected, it receives and assembles a 10-bit serial input from MOSI, starting with the MSB first. These 10 bits are then combined into a 10-bit vector and sent to the RAM unit. The RAM interprets the two most significant bits (MSBs) as control bits to determine whether to store or retrieve data:

- 2'b00: Stores the remaining 8 bits as a write address.
- 2'b01: Stores the remaining 8 bits as data at the previously stored write address.
- 2'b10: Stores the remaining 8 bits as a read address.
- 2'b11: Retrieves the data from the previously stored read address.

Once data is retrieved, the FSM (Finite State Machine) processes the 8-bit output, serializes it on MISO, and asserts the MISO valid signal. This cycle continues accordingly.

SLAVE FSM



Master FSM

***** TESTING & VERIFYING *****

1.Cocotb Results

```

mahmoud_abdo_001@DESKTOP-877H80L: /mnt/d/DDVPs/SPI/Python_testing
0.00ns INFO cocotb Running tests with cocotb v1.9.2 from /home/mahmoud_abdo_001/myenv/lib/python3.12/site-pac
kages/cocotb
0.00ns INFO cocotb Seeding Python random module with 1749986432
0.00ns INFO cocotb.regression Found test wrapper_tb.test_spi_write
0.00ns INFO cocotb.regression Found test wrapper_tb.test_spi_read
0.00ns INFO cocotb.regression Found test wrapper_tb.test_spi_read_write
0.00ns INFO cocotb.regression running test_spi_write (1/3)
Test 1000 randomized write operations
test_spi_write passed
640120.00ns INFO cocotb.regression running test_spi_read (2/3)
640120.00ns INFO cocotb.regression Test 1000 randomized write+read operations with verification
test_spi_read passed
2160240.00ns INFO cocotb.regression running test_spi_read_write (3/3)
2160240.00ns INFO cocotb.regression Test 500 write followed immediately by read
test_spi_read_write passed
2920360.00ns INFO cocotb.regression
2920360.00ns INFO cocotb.regression
*****
** TEST STATUS SIM TIME (ns) REAL TIME (s) RATIO (ns/s) **
*****
** wrapper_tb.test_spi_write PASS 640120.00 17.36 36878.25 **
** wrapper_tb.test_spi_read PASS 1520120.00 25.45 59728.29 **
** wrapper_tb.test_spi_read_write PASS 760120.00 17.24 44095.77 **
*****
** TESTS=3 PASS=3 FAIL=0 SKIP=0 2920360.00 60.66 48141.00 **
*****

```

Test Report : results.xml

```

wrapper_tb
├── test_spi_write
├── test_spi_read
└── test_spi_read_write

```

Test Suite: all

Package: all

Results

Duration	0.0 sec
Tests	3
Failures	0

Tests

wrapper_tb

Test case:	test_spi_write
Outcome:	Passed
Duration:	17.358 sec
Test case:	test_spi_read
Outcome:	Passed
Duration:	25.451 sec
Test case:	test_spi_read_write
Outcome:	Passed
Duration:	17.238 sec

2- SVA Results

Assertions							
File Edit View Add Bookmarks Window Help							
Assertions							
Name	Included	Assertion Type	Language	Enable	Failure Count	P.	
/wrapper_pkg::rand_sequence::body/#anonblk#112914279#74#4#/#ublk#112914279#74/immed__77	✓	Immediate	SVA	on	0		
/wrapper_pkg::rand_sequence::body/#anonblk#112914279#90#4#/#ublk#112914279#90/immed__93	✓	Immediate	SVA	on	0		
/top/DUT/MASTER/assert_inst/assert__p_reset_behavior	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/assert__p_start_initiates_busy_ss	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/assert__p_busy_ends_with_done	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/assert__p_no_start_while_busy	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/assert__p_busy_high_low_sready	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/assert__p_ss_active_low_when_busy	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/assert__p_uvalid_MISO	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[0]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[1]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[2]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[3]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[4]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[5]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[6]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[7]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[8]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/gen_mosi_assert[9]/assert__p_mosi_assert	✓	Concurrent	SVA	on	0		
/top/DUT/MASTER/assert_inst/#ublk#139340017#141/assert__p_miso_data_match	✓	Concurrent	SVA	on	0		
/top/DUT/SLAVE/spi_fsm/slave_fsm_sva/assert__p_reset_behavior	✓	Concurrent	SVA	on	0		
/top/DUT/SLAVE/spi_fsm/slave_fsm_sva/assert__p_ss_fall_then_sready_fall	✓	Concurrent	SVA	on	0		
/top/DUT/SLAVE/spi_fsm/slave_fsm_sva/assert__p_tx_valid_then_validMISO	✓	Concurrent	SVA	on	0		
/top/DUT/SLAVE/spi_fsm/slave_fsm_sva/assert__p_mosi_match	✓	Concurrent	SVA	on	0		
/top/DUT/SLAVE/spi_fsm/slave_fsm_sva/assert__p_rx_valid_after_8bits	✓	Concurrent	SVA	on	0		
/top/DUT/SLAVE/mem_inst/ram_assert/reset_check	✓	Concurrent	SVA	on	0		
/top/DUT/SLAVE/mem_inst/ram_assert/tx_valid_read_cmd	✓	Concurrent	SVA	on	0		
/top/DUT/SLAVE/mem_inst/ram_assert/tx_valid_other_cmds	✓	Concurrent	SVA	on	0		
/top/DUT/SLAVE/mem_inst/ram_assert/dout_stability	✓	Concurrent	SVA	on	0		

Assertions Filter: NoFilter

Cover Directives							
File Edit View Add Bookmarks Window Help							
Cover Directives							
Name	Language	Enabled	Cmplt %	Cmplt graph	Log	Count	Included
/top/DUT/MASTER/assert_inst/cove_p_reset_behavior	SVA	✓	100%		Off	5	✓
/top/DUT/MASTER/assert_inst/cove_p_start_initiates_busy_ss	SVA	✓	100%		Off	50000	✓
/top/DUT/MASTER/assert_inst/cove_p_busy_ends_with_done	SVA	✓	100%		Off	49999	✓
/top/DUT/MASTER/assert_inst/cove_p_no_start_while_busy	SVA	✓	100%		Off	720000	✓
/top/DUT/MASTER/assert_inst/cove_p_busy_high_low_sready	SVA	✓	100%		Off	50000	✓
/top/DUT/MASTER/assert_inst/cove_p_ss_active_low_when_busy	SVA	✓	100%		Off	50000	✓
/top/DUT/MASTER/assert_inst/cove_p_uvalid_MISO	SVA	✓	100%		Off	840000	✓
/top/DUT/MASTER/assert_inst/cove_p_miso_data_match	SVA	✓	100%		Off	49999	✓
/top/DUT/SLAVE/spi_fsm/slave_fsm_sva/cove_p_ss_fall_then_sready_fall	SVA	✓	100%		Off	50000	✓
/top/DUT/SLAVE/spi_fsm/slave_fsm_sva/cove_p_tx_valid_then_validMISO	SVA	✓	100%		Off	10000	✓
/top/DUT/SLAVE/spi_fsm/slave_fsm_sva/cove_p_mosi_match	SVA	✓	100%		Off	50000	✓
/top/DUT/SLAVE/spi_fsm/slave_fsm_sva/cove_p_rx_valid_after_8bits	SVA	✓	100%		Off	50000	✓
/top/DUT/SLAVE/mem_inst/ram_assert/cover__dout_resets_if_not_receiving	SVA	✓	100%		Off	869999	✓
/top/DUT/SLAVE/mem_inst/ram_assert/cover__tx_valid_on_read_data	SVA	✓	100%		Off	10000	✓
/top/DUT/SLAVE/mem_inst/ram_assert/cover__tx_valid_on_other_cmds	SVA	✓	100%		Off	40000	✓
/top/DUT/SLAVE/mem_inst/ram_assert/cover__reset_behavior	SVA	✓	100%		Off	5	✓

Recursive Mode

Coverage Summary By Instance (100%)

Instance ↑	Assertions	Directives	Total
Total	100%	100%	100%
slave_fsm_sva	100%	100%	100%

Coverage Summary By Instance (100%)			
Instance ↑	Assertions	Directives	Total
Total	100%	100%	100%
ram_assert	100%	100%	100%

Coverage Summary By Instance (97.22%)			
Instance ↑	Assertions	Directives	Total
Total	94.44%	100%	97.22%
assert_inst	94.44%	100%	97.22%

Master assertions

3- agents coverage collectors Results

3.1. Wrapper Coverage Collector & coverage summary

Name	Coverage	Goal	% of Goal	Status	Included	Class Type
/master_pkg/master_coverage_collector	100.00%					
/fsm_pkg/fsm_coverage_collector	100.00%					
/wrapper_pkg/wrapper_coverage_collector	100.00%					
TYPE WRAPPER_CG	100.00%	100	100.00%			
CVP WRAPPER_CG::opcode_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::start_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::done_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::busy_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::data_val_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::dout_cp	100.00%	100	100.00%			
CROSS WRAPPER_CG::opcode_start_cross	100.00%	100	100.00%			
bin <rd_data,inactive>	269999	1	100.00%			
bin <rd_addr,inactive>	150000	1	100.00%			
bin <wr_data,inactive>	225000	1	100.00%			
bin <wr_addr,inactive>	225007	1	100.00%			
bin <rd_data,active>	10000	1	100.00%			
bin <rd_addr,active>	10000	1	100.00%			
bin <wr_data,active>	15000	1	100.00%			
bin <wr_addr,active>	15000	1	100.00%			
CROSS WRAPPER_CG::dout_done_cross	100.00%	100	100.00%			
bin <max,not_done>	1806	1	100.00%			
bin <zero,not_done>	459455	1	100.00%			
bin <max,done>	86	1	100.00%			
bin <zero,done>	30449	1	100.00%			
INST \wrapper_pkg::wrapper_coverage_collector::WRAPPER_CG	100.00%	100	100.00%			

```

uvm_test_top.env.w_cov [COV_REPORT] ***** WRAPPER Coverage Summary
uvm_test_top.env.w_cov [COV_REPORT] ***** Opcode Commands: 100.00%
uvm_test_top.env.w_cov [COV_REPORT] ***** Start Signal: 100.00%
uvm_test_top.env.w_cov [COV_REPORT] ***** Done Signal: 100.00%
uvm_test_top.env.w_cov [COV_REPORT] ***** Busy Signal: 100.00%
uvm_test_top.env.w_cov [COV_REPORT] ***** Input Data Patterns: 100.00%
uvm_test_top.env.w_cov [COV_REPORT] ***** Output Data Patterns: 100.00%
uvm_test_top.env.w_cov [COV_REPORT] ***** Opcode/Start Cross: 100.00%
uvm_test_top.env.w_cov [COV_REPORT] ***** Dout/Done Cross: 100.00%

```


3.2.Master Coverage Collector & coverage summary

Name	Coverage	Goal	% of Goal	Status	Included	Class Type	Merc
/ram_pkg/ram_coverage_collector	100.00%						
/master_pkg/master_coverage_collector	100.00%						
TYPE SPI_Master_CG	100.00%	100	100.00%				
CVP SPI_Master_CG::data_in_cp	100.00%	100	100.00%				
bin zero	966	1	100.00%				
bin max	816	1	100.00%				
default bin others	918224	-	-				
CVP SPI_Master_CG::data_out_cp	100.00%	100	100.00%				
bin zero	489903	1	100.00%				
bin max	1892	1	100.00%				
default bin others	428211	-	-				
CVP SPI_Master_CG::cp_cmd_type	100.00%	100	100.00%				
bin write_addr	240006	1	100.00%				
bin write_data	240000	1	100.00%				
bin read_addr	160000	1	100.00%				
bin read_data	279999	1	100.00%				
CVP SPI_Master_CG::cp_busy	100.00%	100	100.00%				
CVP SPI_Master_CG::cp_done	100.00%	100	100.00%				
CVP SPI_Master_CG::cp_ss_n	100.00%	100	100.00%				
CVP SPI_Master_CG::cp_sready	100.00%	100	100.00%				
CVP SPI_Master_CG::cp_valid_MISO	100.00%	100	100.00%				
/fsm_pkg/fsm_coverage_collector	100.00%						
/wrapper_pkg/wrapper_coverage_collector	100.00%						

Covergroups Filter: NoFilter

```

uvm_test_top.env.master_cov [COV_REPORT] ***** SPI Master Coverage Summary
uvm_test_top.env.master_cov [COV_REPORT] ***** Command Types: 100.00%
uvm_test_top.env.master_cov [COV_REPORT] ***** Busy Signal: 100.00%

```

3.3.Slave FSM Coverage Collector & coverage summary

Name	Coverage	Goal	% of Goal	Status	Included	Class Type	Merc
/fsm_pkg/fsm_coverage_collector	100.00%						
TYPE FSM_CG	100.00%	100	100.00%				
CVP FSM_CG::cp_cmd_type	100.00%	100	100.00%				
CVP FSM_CG::cp_ss_n	100.00%	100	100.00%				
CVP FSM_CG::cp_rx_valid	100.00%	100	100.00%				
CVP FSM_CG::cp_tx_valid	100.00%	100	100.00%				
CVP FSM_CG::cp_valid_MISO	100.00%	100	100.00%				
CVP FSM_CG::cp_rx_data	100.00%	100	100.00%				
CVP FSM_CG::cp_tx_data	100.00%	100	100.00%				
CROSS FSM_CG::cmd_x_ss_n	100.00%	100	100.00%				
bin <read_cmd,low>	329183	1	100.00%				
bin <write_cmd,low>	340817	1	100.00%				
bin <read_cmd,high>	124201	1	100.00%				
bin <write_cmd,high>	125799	1	100.00%				
CROSS FSM_CG::cmd_x_rx_valid	100.00%	100	100.00%				
bin <read_cmd,idle>	428543	1	100.00%				
bin <write_cmd,idle>	441457	1	100.00%				
bin <read_cmd,active>	24841	1	100.00%				
bin <write_cmd,active>	25159	1	100.00%				
CROSS FSM_CG::cmd_x_valid_MISO	100.00%	100	100.00%				
bin <read_cmd,idle>	413720	1	100.00%				
bin <write_cmd,idle>	426280	1	100.00%				
bin <read_cmd,active>	39664	1	100.00%				
bin <write_cmd,active>	40336	1	100.00%				
/wrapper_pkg/wrapper_coverage_collector	100.00%						

Covergroups Filter: NoFilter

```

uvm_test_top.env.fsm_cov [COV_REPORT] ***** FSM Coverage Summary
uvm_test_top.env.fsm_cov [COV_REPORT] ***** Command Types: 100.00%
uvm_test_top.env.fsm_cov [COV_REPORT] ***** RX Data: 100.00%
uvm_test_top.env.fsm_cov [COV_REPORT] ***** TX Data: 100.00%

```

3.4.Slave RAM Coverage Collector & coverage summery

Name	Coverage	Goal	% of Goal	Status	Included
/ram_pkg/ram_coverage_collector	100.00%	100	100.00%		
TYPE RAM_CG	100.00%	100	100.00%		✓
CVP RAM_CG::cp_cmd	100.00%	100	100.00%		✓
CVP RAM_CG::cp_addr	100.00%	100	100.00%		✓
CVP RAM_CG::cp_wr_data	100.00%	100	100.00%		✓
CVP RAM_CG::cp_rd_data	100.00%	100	100.00%		✓
CVP RAM_CG::cp_rx_valid_trans	100.00%	100	100.00%		✓
CVP RAM_CG::cp_tx_valid_trans	100.00%	100	100.00%		✓
CVP RAM_CG::wr_sequence	100.00%	100	100.00%		✓
CVP RAM_CG::rd_sequence	100.00%	100	100.00%		✓
INST \ram_pkg::ram_coverage_collector::RAM_CG	100.00%	100	100.00%		✓
/master_pkg/master_coverage_collector	100.00%				
/fsm_pkg/fsm_coverage_collector	100.00%				
/wrapper_pkg/wrapper_coverage_collector	100.00%				

Covergroups Filter: NoFilter

```

uvm_test_top.env.ram_cov [COV_REPORT] ***** RAM Coverage Summary
uvm_test_top.env.ram_cov [COV_REPORT] ***** Command Types: 100.00%
uvm_test_top.env.ram_cov [COV_REPORT] ***** Address Ranges: 100.00%
uvm_test_top.env.ram_cov [COV_REPORT] ***** Write Data Patterns: 100.00%
uvm_test_top.env.ram_cov [COV_REPORT] ***** Read Data Patterns: 100.00%

```

4.Scoreboard Results

4.1.Wrapper Scoreboard Results

```

uvm_test_top.env.w_sb [report_phase] ***** SPI WRAPPER RESULTS
uvm_test_top.env.w_sb [report_phase] ***** Total successful write transactions : 15000
uvm_test_top.env.w_sb [report_phase] ***** Total successful read transactions : 10000
uvm_test_top.env.w_sb [report_phase] ***** Total failed read transactions : 0

```

4.2.Master Scoreboard Results

```

uvm_test_top.env.master_sb [SB_REPORT] ***** SPI Master Scoreboard Results
uvm_test_top.env.master_sb [SB_REPORT] ***** Total Transactions: 920006
uvm_test_top.env.master_sb [SB_REPORT] ***** Write Transactions: 480006
uvm_test_top.env.master_sb [SB_REPORT] ***** Read Transactions: 439999
uvm_test_top.env.master_sb [SB_REPORT] ***** Errors Detected: 0
uvm_test_top.env.master_sb [SB_REPORT] ***** SPI Master Scoreboard: ALL TESTS PASSED

```

4.3.Slave FSM Scoreboard Results

```

uvm_test_top.env.fsm_sb [SB_REPORT] ***** SPI Slave FSM Scoreboard Results
uvm_test_top.env.fsm_sb [SB_REPORT] ***** Total Transactions: 920000
uvm_test_top.env.fsm_sb [SB_REPORT] ***** Write Operations: 30000
uvm_test_top.env.fsm_sb [SB_REPORT] ***** Read Operations: 20000
uvm_test_top.env.fsm_sb [SB_REPORT] ***** Protocol Errors: 0
uvm_test_top.env.fsm_sb [SB_REPORT] ***** FSM PROTOCOL: ALL CHECKS PASSED

```

4.4.Slave RAM Scoreboard Results

```

uvm_test_top.env.ram_sb [report_phase] ***** SLAVE RAM RESULTS
uvm_test_top.env.ram_sb [report_phase] ***** total write address transactions: 15000
uvm_test_top.env.ram_sb [report_phase] ***** total write data transactions: 15000
uvm_test_top.env.ram_sb [report_phase] ***** total read address transactions: 10000
uvm_test_top.env.ram_sb [report_phase] ***** total read data transactions: 10000
uvm_test_top.env.ram_sb [report_phase] ***** total successful ram transactions: 10000
uvm_test_top.env.ram_sb [report_phase] ***** total failed ram transactions: 0

```


Questa Covergroups Coverage Report

Covergroups Coverage

Covergroups	Bins	Hits	Misses	Goal	Coverage
Search...	Search...	Search...	Search...	Search...	Search...
/fsm_pkg/fsm_coverage_collector/FSM_CG	28	28	0	100	100%
/master_pkg/master_coverage_collector/SPI_Master_CG	18	18	0	100	100%
* /ram_pkg/ram_coverage_collector/RAM_CG	34	34	0	100	100%
* /wrapper_pkg/wrapper_coverage_collector/WRAPPER_CG	26	26	0	100	100%

Questa Design Units Coverage

Total Coverage (98.85%)

Overall Design Unit Coverage Summary:

Assertions	Directives	Covergroups
96.55%	100%	100%

Coverage Summary by Design Unit:

Design Unit ↑	Assertions	Directives	Covergroups	Total
Search...	Search...	Search...	Search...	Search...
work.SPIMSVA	94.44%	100%	-	97.22%
work.SPI_SFM_SVA	100%	100%	-	100%
work.fsm_pkg	-	-	100%	100%
work.master_pkg	-	-	100%	100%
work.ram_pkg	-	-	100%	100%
work.ram_sva	100%	100%	-	100%
work.wrapper_pkg	100%	-	100%	100%