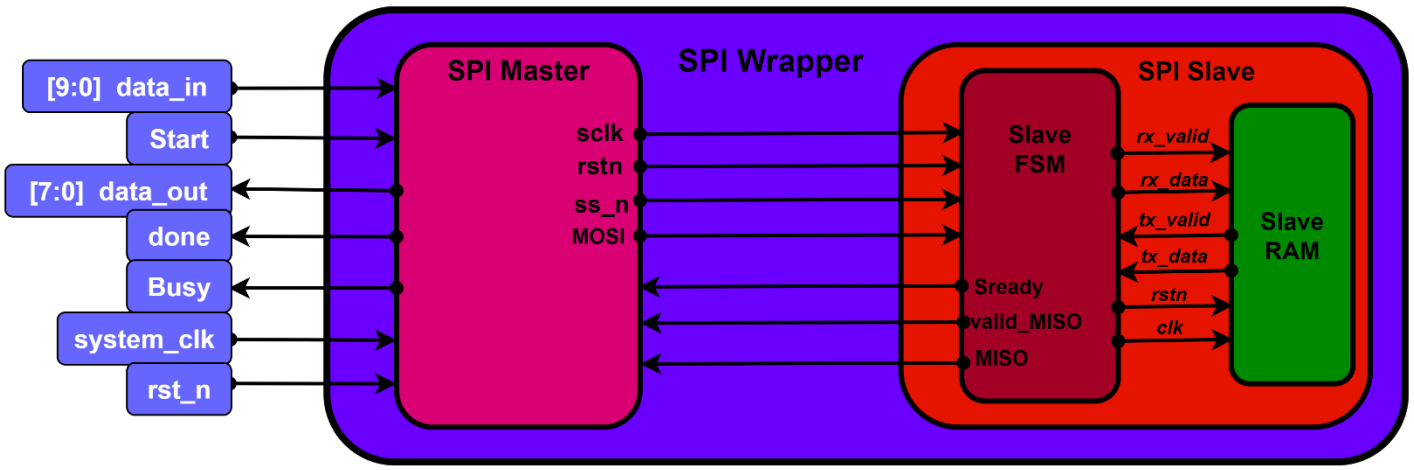
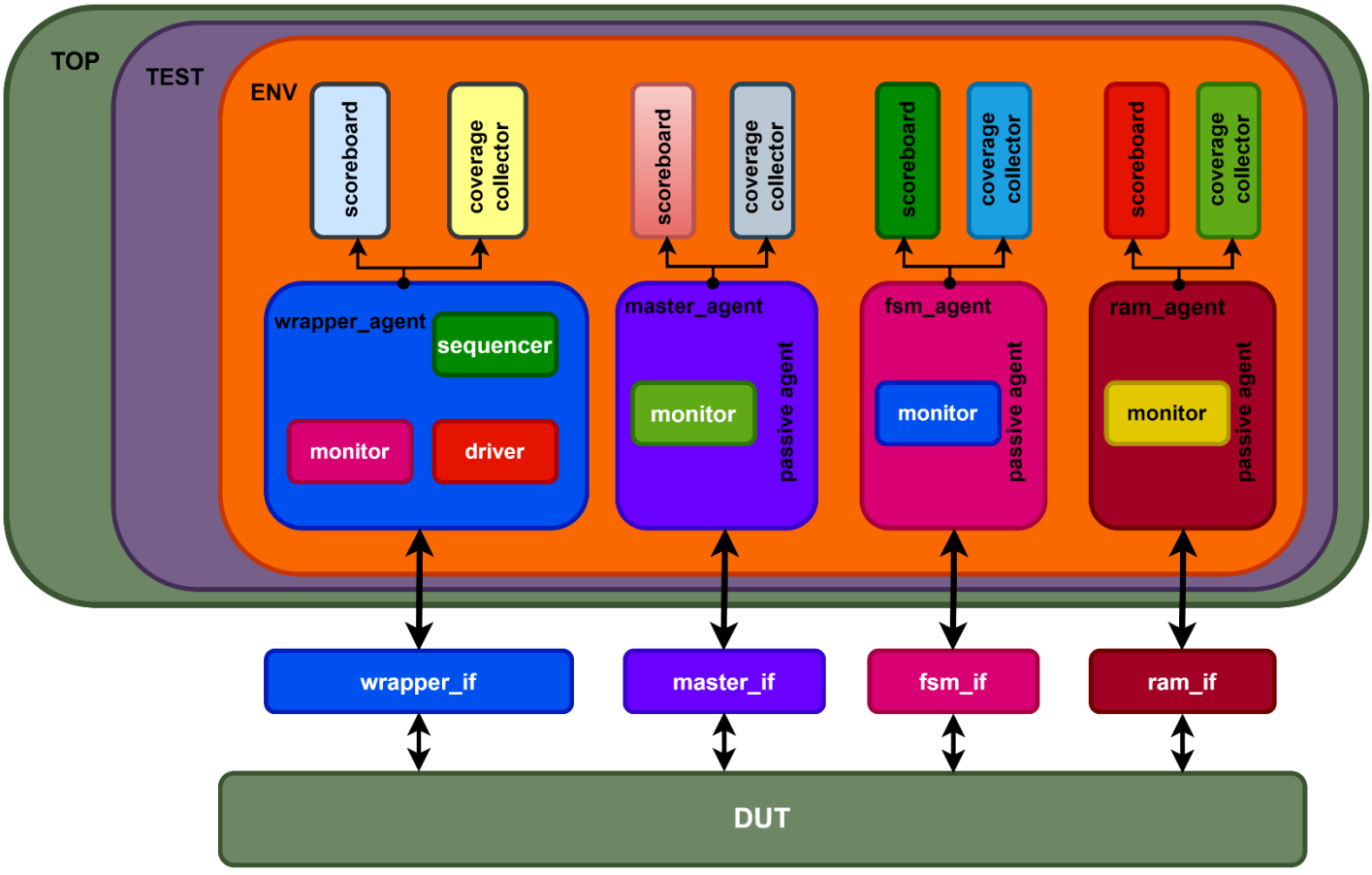
Simple SPI Master–Slave Interface

RTL Design and Verification with SVA, UVM, and COCOTB



--- Top-level design Wrapper ---



--- UVM Testbench Architecture ---

Design Specifications

1.Master Specs

Port	Direction	Function
data_in	input	Parallel input vector from the wrapper representing a read/write transaction. This data is serialized and transmitted to the slave via the MOSI line.
start	input	Initiates an SPI transaction when asserted.
busy	output	Indicates an ongoing SPI transfer. When busy is high, new transactions via start are ignored until the current transfer completes.
data_out	output	Parallel output data received via MISO, valid after transfer completes.
done	output	Asserted for one cycle when the current SPI transaction (read/write) finishes.
ss_n	output	Active-low signal used to select the slave device. When asserted, the master initiates transmission by sending the data_in starting with the MSB on the next clock cycle on MOSI
MOSI	output	Serial data line for transmitting bits to the slave, sending the data_in vector serially starting from the most significant bit (MSB)
sready	input	Indicates the slave is ready to receive the next transaction. The master waits until this signal is asserted, which occurs after the slave completes the current transaction.
valid_MISO	input	Indicates valid data is present on the MISO line.
MISO	input	Serial data line to receive bits from the slave.

2.Slave Specs

2.1.Slave FSM Specs

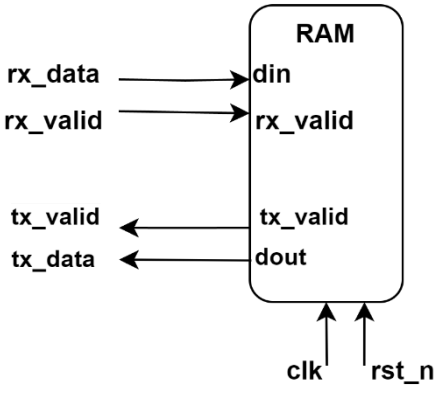
Port	Direction	Function
sclk	input	Serial clock signal driven by the master. The slave uses this clock to sample incoming data on MOSI and shift out data on MISO.
ss_n	input	Active-low slave select. When asserted low by the master, the slave is activated and starts data reception/transmission on the next sclk edge.
MOSI	input	Serial data line carrying bits from the master to the slave. Data is typically shifted in MSB first.
sready	output	Indicates the slave is ready to accept a new transaction. Asserted after completing the current read/write operation.
valid_MISO	output	Asserted when the slave has valid data available on the MISO line for the master to read.
MISO	output	Serial data line carrying bits from the slave to the master, shifted out in sync with sclk.

2.2.Slave RAM Specs

Port	Direction	Function
rx_valid	input	Asserted by the FSM when a complete 10-bit command has been received via MOSI. Indicates valid data for processing.
rx_data	input	The 10-bit vector received from MOSI, containing the command (e.g., read/write) and address/data
tx_valid	output	Asserted by the FSM during a read transaction to indicate valid tx_data is available for transmission.
tx_data	output	The 8-bit data read from memory, which will be serialized and sent to the master via MISO

2.2.1.Slave RAM operations

din[9:8]	command	description
00	Write	hold din[7:0] as write address
01	write	Write din[7:0] in the memory with the write address held previously
10	read	Hold din[7:0] as read address
11	read	Read the memory with the read address held previously.



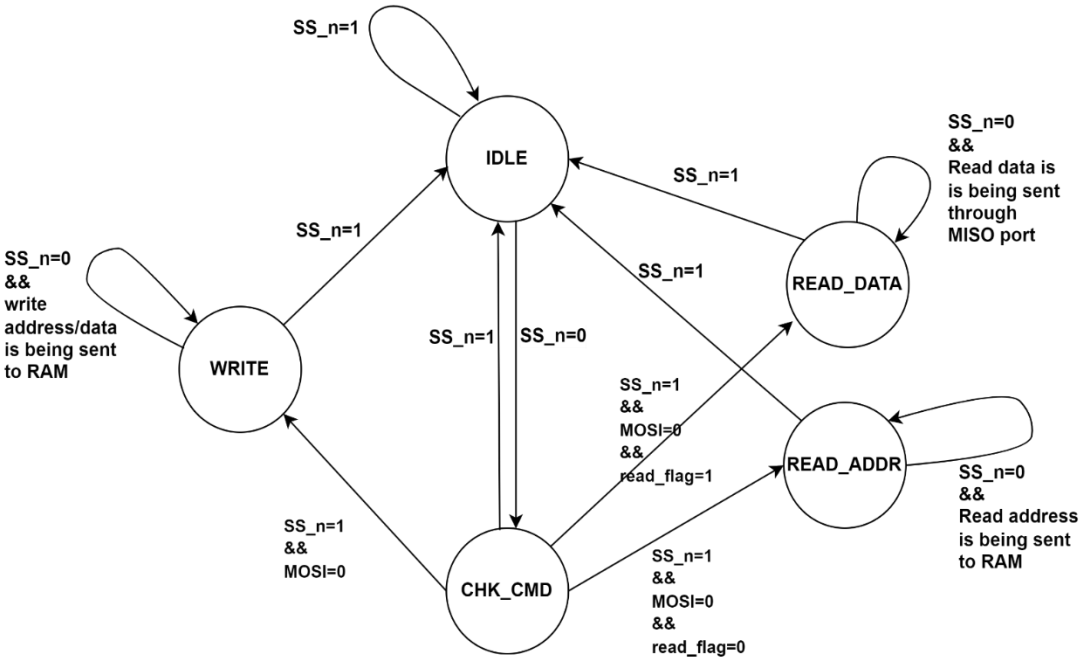
Slave Operations Summary

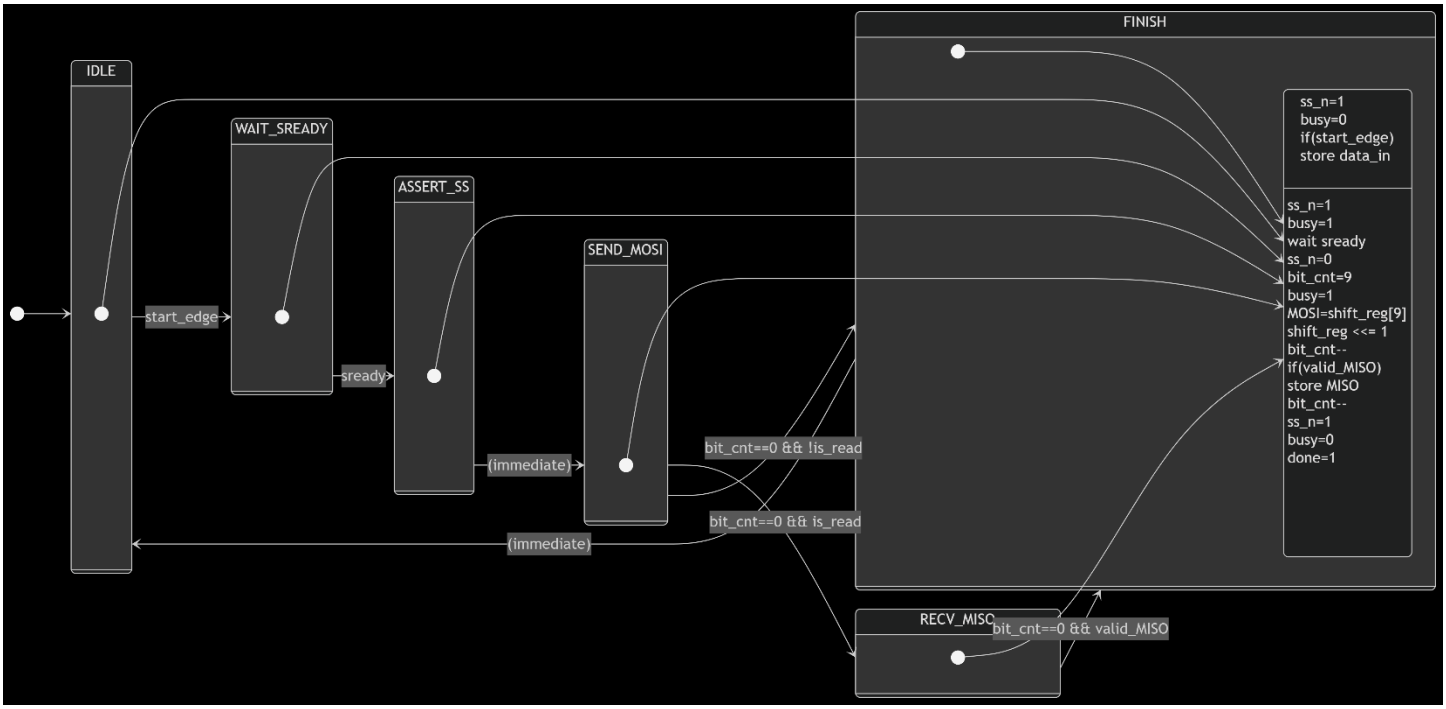
When the SPI slave is selected, it receives and assembles a 10-bit serial input from MOSI, starting with the MSB first. These 10 bits are then combined into a 10-bit vector and sent to the RAM unit. The RAM interprets the two most significant bits (MSBs) as control bits to determine whether to store or retrieve data:

- 2'b00: Stores the remaining 8 bits as a write address.
- 2'b01: Stores the remaining 8 bits as data at the previously stored write address.
- 2'b10: Stores the remaining 8 bits as a read address.
- 2'b11: Retrieves the data from the previously stored read address.

Once data is retrieved, the FSM (Finite State Machine) processes the 8-bit output, serializes it on MISO, and asserts the MISO valid signal. This cycle continues accordingly.

SLAVE FSM





Master FSM

********** TESTING & VERIFYING **********

1.Cocotb Results

```
mahmoud_abdo_001@DESKTOP-877H80L: /mnt/d/DDVPs/SPI/Python_testing
     0.00ns INFO     cocotb                          Running tests with cocotb v1.9.2 from /home/mahmoud_abdo_001/myenv/lib/python3.12/site-pac
kages/cocotb
     0.00ns INFO     cocotb                          Seeding Python random module with 1749986432
     0.00ns INFO     cocotb.regression               Found test wrapper_tb.test_spi_write
     0.00ns INFO     cocotb.regression               Found test wrapper_tb.test_spi_read
     0.00ns INFO     cocotb.regression               Found test wrapper_tb.test_spi_read_write
     0.00ns INFO     cocotb.regression               running test_spi_write (1/3)
                                                       Test 1000 randomized write operations
640120.00ns INFO     cocotb.regression               test_spi_write passed
640120.00ns INFO     cocotb.regression               running test_spi_read (2/3)
                                                       Test 1000 randomized write+read operations with verification
2160240.00ns INFO     cocotb.regression               test_spi_read passed
2160240.00ns INFO     cocotb.regression               running test_spi_read_write (3/3)
                                                       Test 500 write followed immediately by read
2920360.00ns INFO     cocotb.regression               test_spi_read_write passed
2920360.00ns INFO     cocotb.regression               ****************************************************************************************
                                                      ** TEST                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                      ****************************************************************************************
                                                      ** wrapper_tb.test_spi_write      PASS      640120.00          17.36      36878.25  **
                                                      ** wrapper_tb.test_spi_read       PASS     1520120.00          25.45      59728.29  **
                                                      ** wrapper_tb.test_spi_read_write PASS      760120.00          17.24      44095.77  **
                                                      ****************************************************************************************
                                                      ** TESTS=3 PASS=3 FAIL=0 SKIP=0             2920360.00          60.66      48141.00  **
                                                      ****************************************************************************************
```

Test Report : results.xml

wrapper_tb
- test_spi_write
- test_spi_read
- test_spi_read_write

Test Suite: all

Package: all

Results

Duration	0.0 sec
Tests	3
Failures	0

Tests

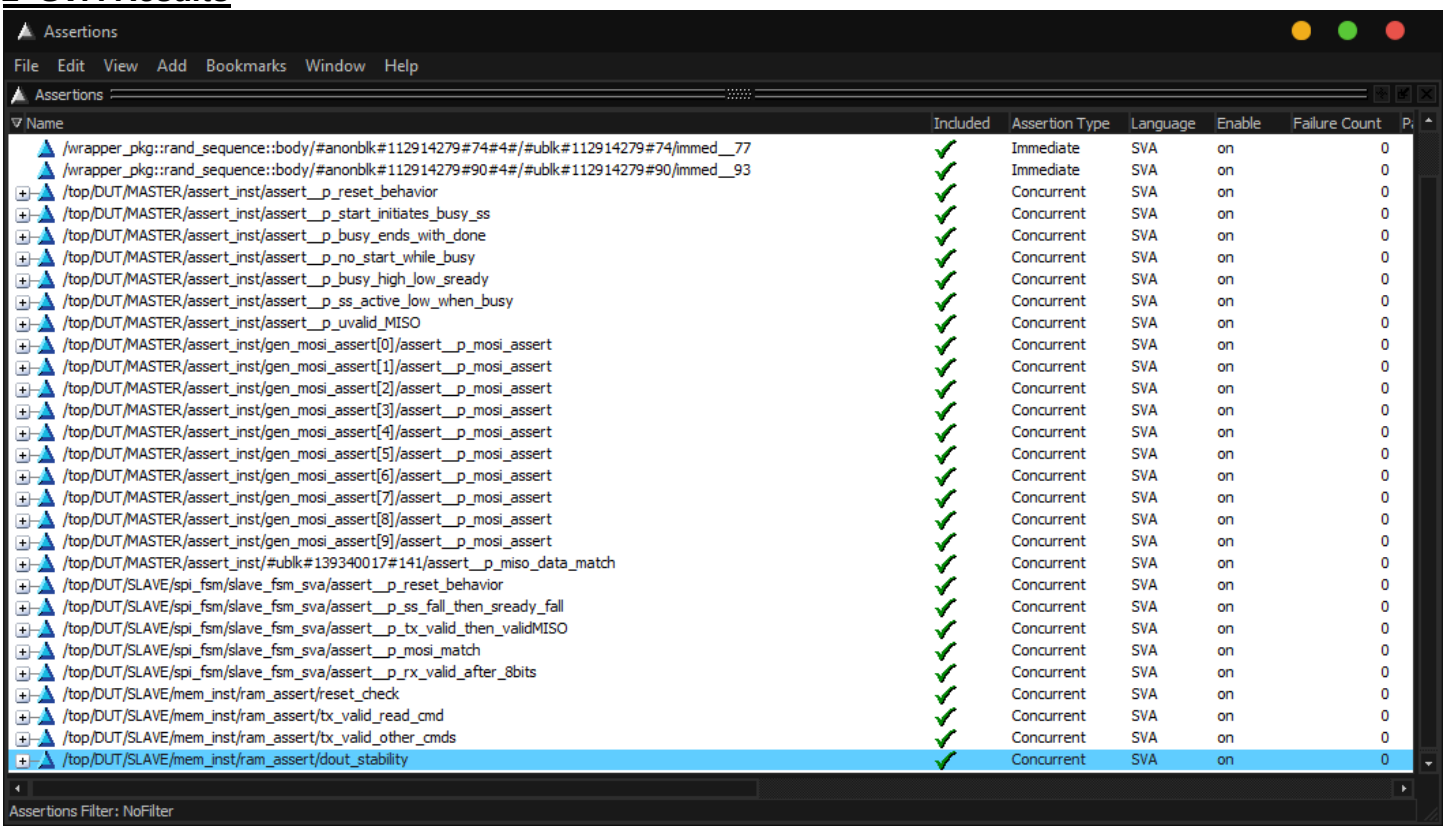
wrapper_tb

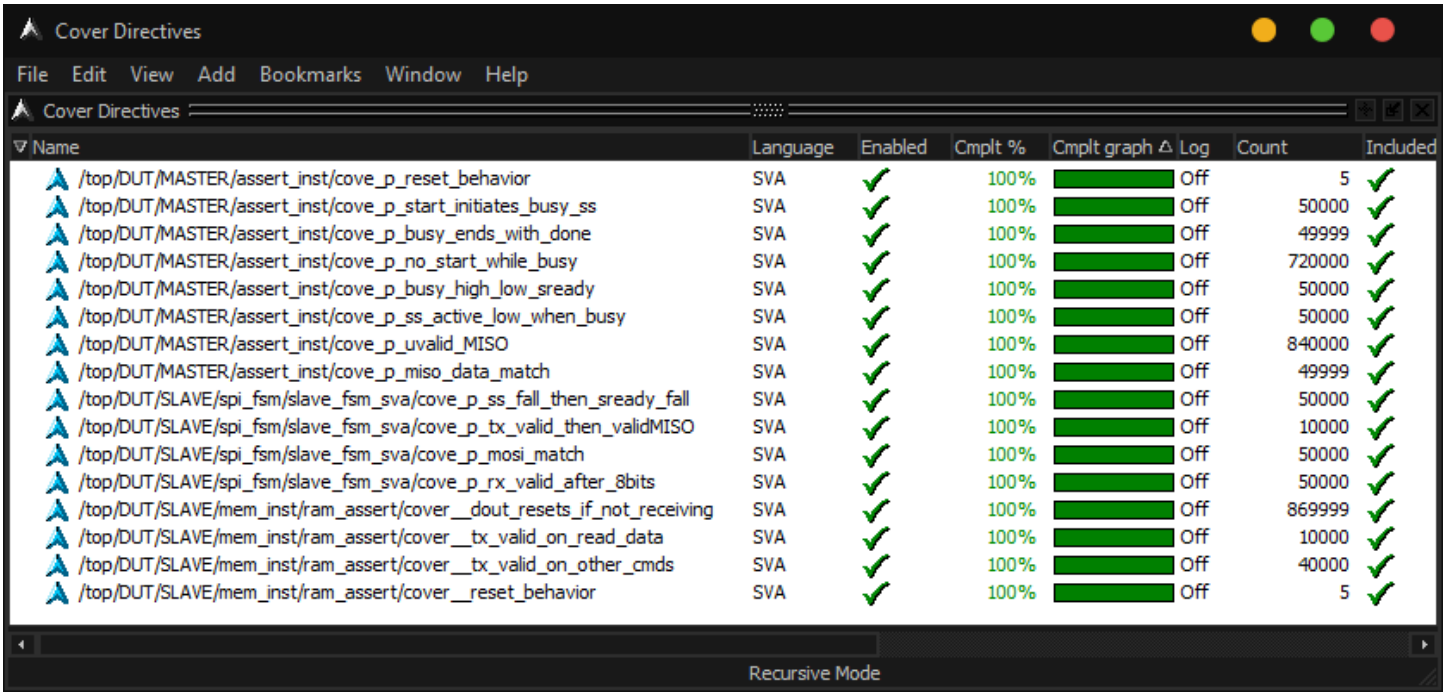
Test case:	**test_spi_write**
Outcome:	Passed
Duration:	17.358 sec

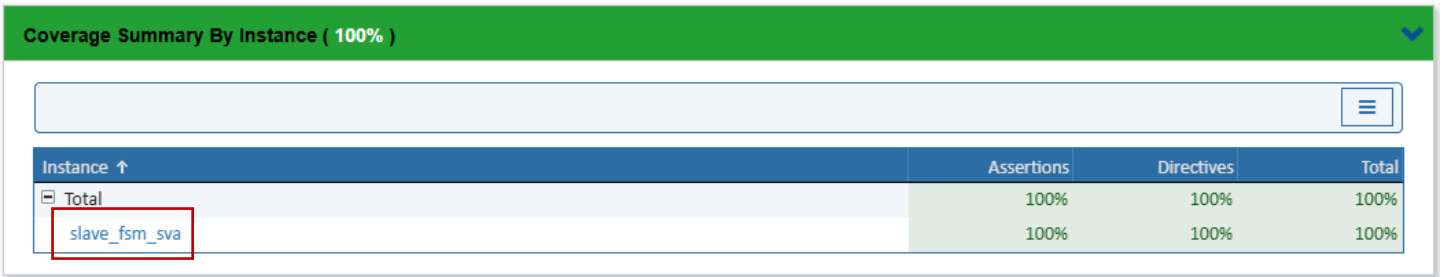
Test case:	**test_spi_read**
Outcome:	Passed
Duration:	25.451 sec

Test case:	**test_spi_read_write**
Outcome:	Passed
Duration:	17.238 sec

2- SVA Results







Coverage Summary By Instance (100%)

Instance ↑	Assertions	Directives	Total
Total	100%	100%	100%
ram_assert	100%	100%	100%

Coverage Summary By Instance (97.22%)

Instance ↑	Assertions	Directives	Total
Total	94.44%	100%	97.22%
assert_inst	94.44%	100%	97.22%

Master assertions

3- agents coverage collectors Results

3.1.Wrapper Coverage Collector & coverage summery

Covergroups

File Bookmarks Window Help

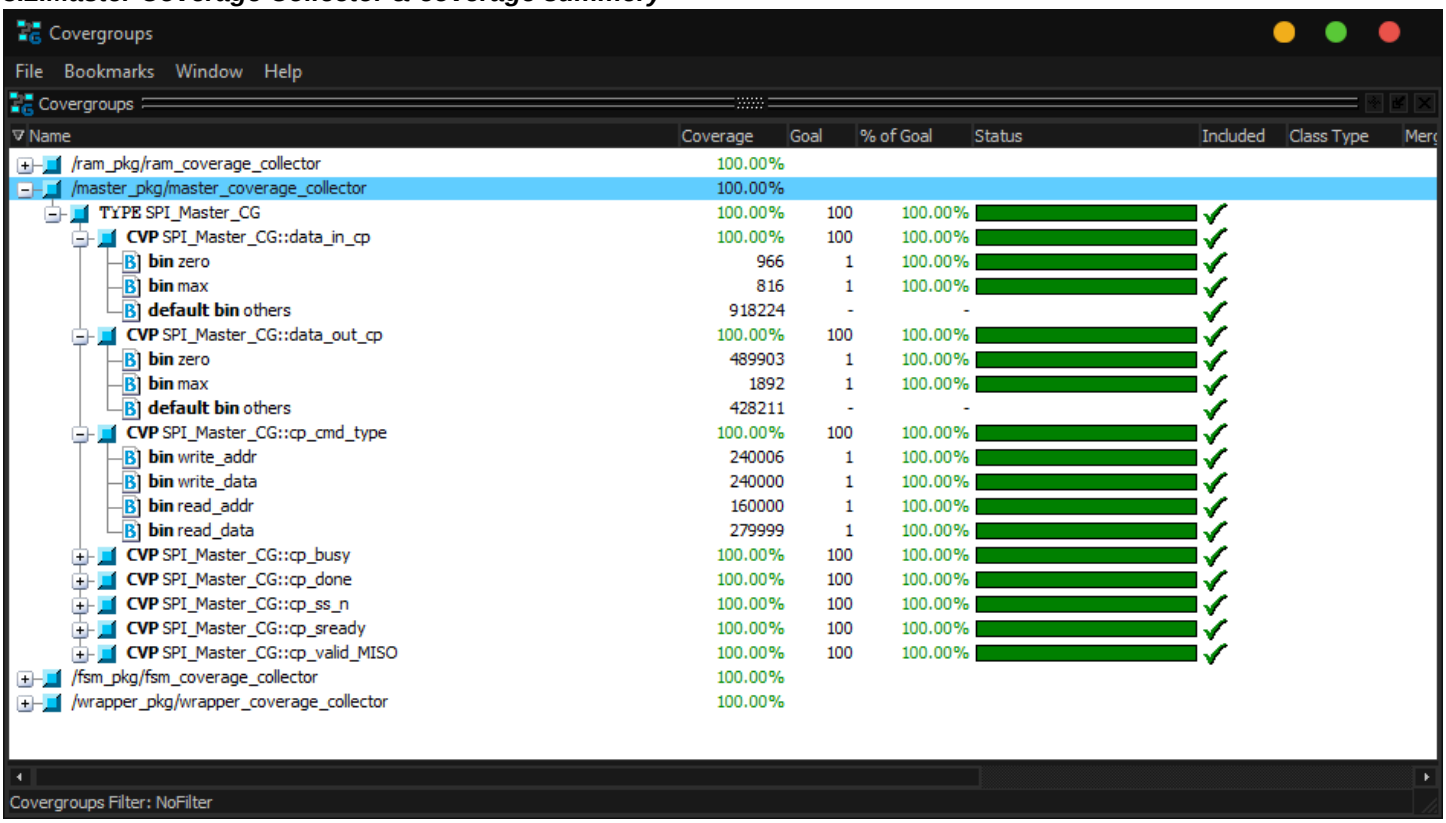
Covergroups

Name	Coverage	Goal	% of Goal	Status	Included	Class Type
/master_pkg/master_coverage_collector	100.00%					
/fsm_pkg/fsm_coverage_collector	100.00%					
/wrapper_pkg/wrapper_coverage_collector	100.00%					
TYPE WRAPPER_CG	100.00%	100	100.00%			
CVP WRAPPER_CG::opcode_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::start_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::done_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::busy_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::data_val_cp	100.00%	100	100.00%			
CVP WRAPPER_CG::dout_cp	100.00%	100	100.00%			
CROSS WRAPPER_CG::opcode_start_cross	100.00%	100	100.00%			
bin <rd_data,inactive>	269999	1	100.00%			
bin <rd_addr,inactive>	150000	1	100.00%			
bin <wr_data,inactive>	225000	1	100.00%			
bin <wr_addr,inactive>	225007	1	100.00%			
bin <rd_data,active>	10000	1	100.00%			
bin <rd_addr,active>	10000	1	100.00%			
bin <wr_data,active>	15000	1	100.00%			
bin <wr_addr,active>	15000	1	100.00%			
CROSS WRAPPER_CG::dout_done_cross	100.00%	100	100.00%			
bin <max,not_done>	1806	1	100.00%			
bin <zero,not_done>	459455	1	100.00%			
bin <max,done>	86	1	100.00%			
bin <zero,done>	30449	1	100.00%			
INST \/wrapper_pkg::wrapper_coverage_collector::WRAPPER_CG	100.00%	100	100.00%			

Covergroups Filter: NoFilter

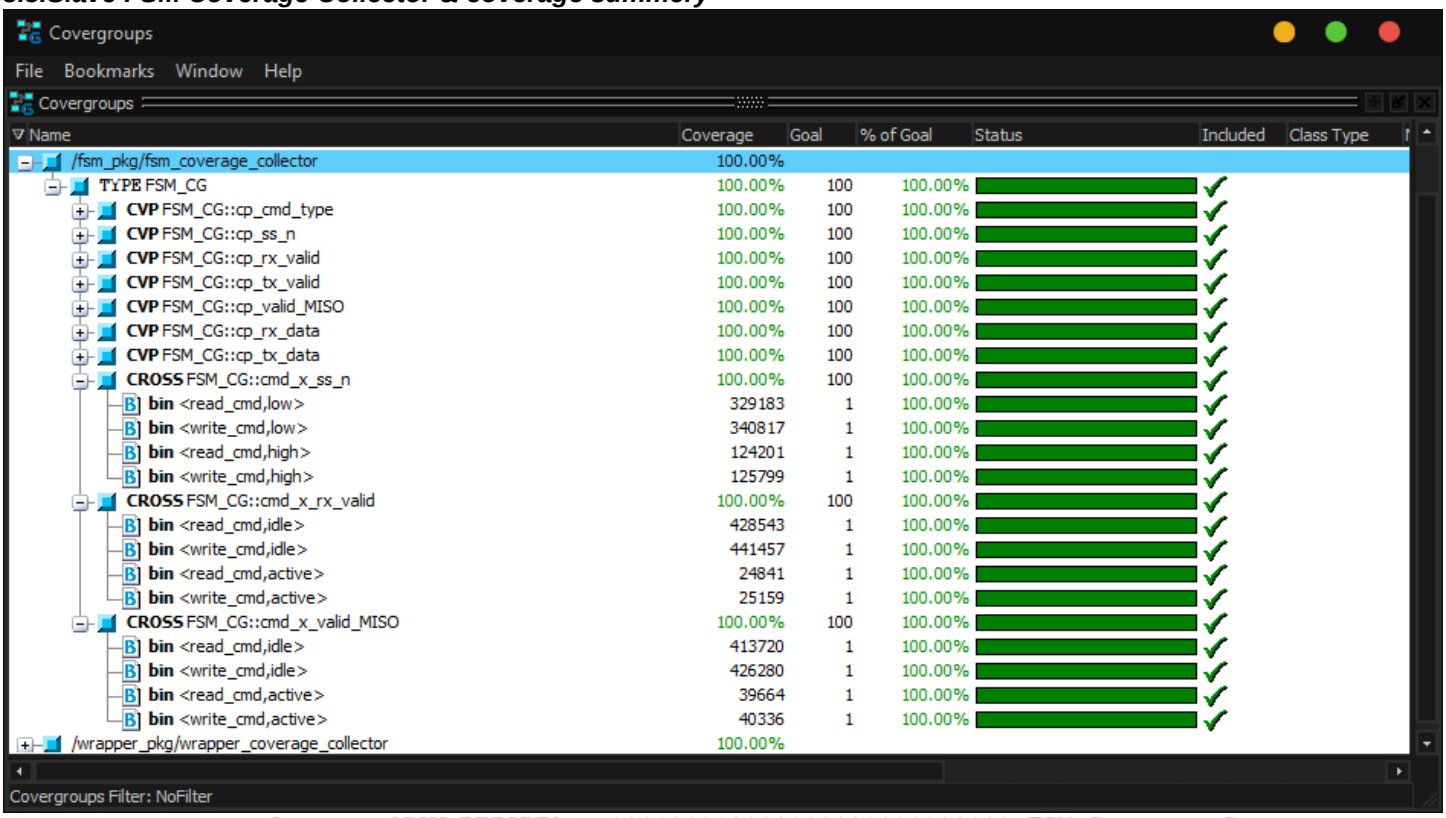
```
uvm_test_top.env.w_cov [COV_REPORT]    ***************************** WRAPPER Coverage Summary
uvm_test_top.env.w_cov [COV_REPORT]    ******   Opcode Commands: 100.00%
uvm_test_top.env.w_cov [COV_REPORT]    ******   Start Signal: 100.00%
uvm_test_top.env.w_cov [COV_REPORT]    ******   Done Signal: 100.00%
uvm_test_top.env.w_cov [COV_REPORT]    ******   Busy Signal: 100.00%
uvm_test_top.env.w_cov [COV_REPORT]    ******   Input Data Patterns: 100.00%
uvm_test_top.env.w_cov [COV_REPORT]    ******   Output Data Patterns: 100.00%
uvm_test_top.env.w_cov [COV_REPORT]    ******   Opcode/Start Cross: 100.00%
uvm_test_top.env.w_cov [COV_REPORT]    ******   Dout/Done Cross: 100.00%
```

3.2.Master Coverage Collector & coverage summery



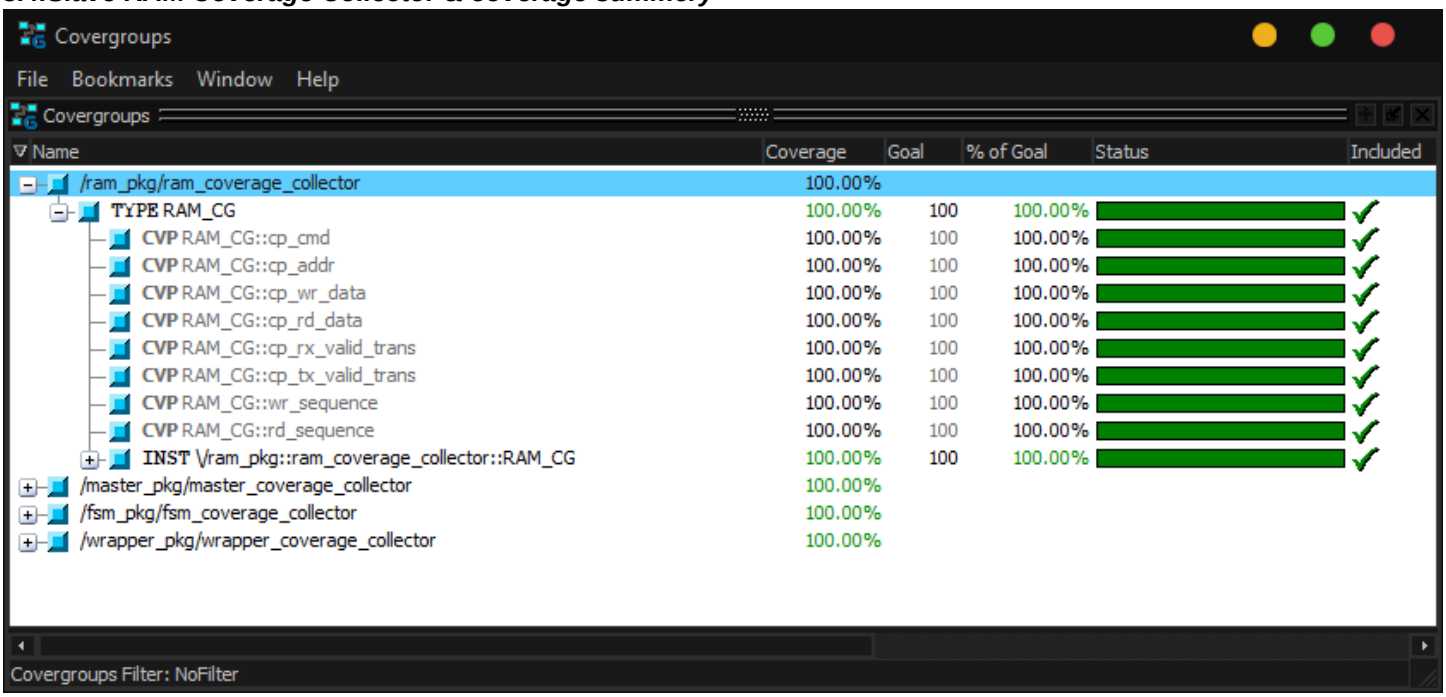

```
uvm_test_top.env.master_cov [COV_REPORT]    ***************************** SPI Master Coverage Summary
uvm_test_top.env.master_cov [COV_REPORT]    *****   Command Types: 100.00%
uvm_test_top.env.master_cov [COV_REPORT]    *****   Busy Signal: 100.00%
```

3.3.Slave FSM Coverage Collector & coverage summery




```
uvm_test_top.env.fsm_cov [COV_REPORT]    ***************************** FSM Coverage Summary
uvm_test_top.env.fsm_cov [COV_REPORT]    ******   Command Types: 100.00%
uvm_test_top.env.fsm_cov [COV_REPORT]    ******   RX Data: 100.00%
uvm_test_top.env.fsm_cov [COV_REPORT]    ******  TX Data: 100.00%
```

3.4.Slave RAM Coverage Collector & coverage summery




```
uvm_test_top.env.ram_cov [COV_REPORT]   ************************** RAM Coverage Summary
uvm_test_top.env.ram_cov [COV_REPORT]   ******   Command Types: 100.00%
uvm_test_top.env.ram_cov [COV_REPORT]   ******   Address Ranges: 100.00%
uvm_test_top.env.ram_cov [COV_REPORT]   ******   Write Data Patterns: 100.00%
uvm_test_top.env.ram_cov [COV_REPORT]   ******   Read Data Patterns: 100.00%
```

4.Scoreboard Results

4.1.Wrapper Scoreboard Results

```
uvm_test_top.env.w_sb [report_phase]    ***************************  SPI WRAPPER RESULTS
uvm_test_top.env.w_sb [report_phase]    *****   Total successful write transactions : 15000
uvm_test_top.env.w_sb [report_phase]    *****   Total successful read transactions : 10000
uvm_test_top.env.w_sb [report_phase]    *****   Total failed read transactions     : 0
```

4.2.Master Scoreboard Results

```
uvm_test_top.env.master_sb [SB_REPORT]     ************************** SPI Master Scoreboard Results
uvm_test_top.env.master_sb [SB_REPORT]     *****   Total Transactions: 920006
uvm_test_top.env.master_sb [SB_REPORT]     *****   Write Transactions: 480006
uvm_test_top.env.master_sb [SB_REPORT]     *****   Read Transactions: 439999
uvm_test_top.env.master_sb [SB_REPORT]     *****   Errors Detected: 0
uvm_test_top.env.master_sb [SB_REPORT]     *****   SPI Master Scoreboard: ALL TESTS PASSED
```

4.3.Slave FSM Scoreboard Results

```
uvm_test_top.env.fsm_sb [SB_REPORT]   ************************** SPI Slave FSM Scoreboard Results
uvm_test_top.env.fsm_sb [SB_REPORT]   *****   Total Transactions: 920000
uvm_test_top.env.fsm_sb [SB_REPORT]   *****   Write Operations: 30000
uvm_test_top.env.fsm_sb [SB_REPORT]   *****   Read Operations: 20000
uvm_test_top.env.fsm_sb [SB_REPORT]   *****   Protocol Errors: 0
uvm_test_top.env.fsm_sb [SB_REPORT]   *****   FSM PROTOCOL: ALL CHECKS PASSED
```

4.4.Slave RAM Scoreboard Results

```
uvm_test_top.env.ram_sb [report_phase]    **************************  SLAVE RAM RESULTS
uvm_test_top.env.ram_sb [report_phase]    *****   total write address transactions: 15000
uvm_test_top.env.ram_sb [report_phase]    *****   total write data transactions: 15000
uvm_test_top.env.ram_sb [report_phase]    *****   total read address transactions: 10000
uvm_test_top.env.ram_sb [report_phase]    *****   total read data transactions: 10000
uvm_test_top.env.ram_sb [report_phase]    *****   total successful ram transactions: 10000
uvm_test_top.env.ram_sb [report_phase]    *****   total failed ram transactions: 0
```

Questa Covergroups Coverage Report

Covergroups Coverage

Covergroups	Bins	Hits	Misses	Goal	Coverage
/fsm_pkg/fsm_coverage_collector/FSM_CG	28	28	0	100	100%
/master_pkg/master_coverage_collector/SPI_Master_CG	18	18	0	100	100%
/ram_pkg/ram_coverage_collector/RAM_CG	34	34	0	100	100%
/wrapper_pkg/wrapper_coverage_collector/WRAPPER_CG	26	26	0	100	100%

Questa Design Units Coverage

Total Coverage (98.85%)

Overall Design Unit Coverage Summary:

Assertions	Directives	Covergroups
96.55%	100%	100%

Coverage Summary by Design Unit:

Design Unit	Assertions	Directives	Covergroups	Total
work.SPIMSVA	94.44%	100%	-	97.22%
work.SPIS_FSM_SVA	100%	100%	-	100%
work.fsm_pkg	-	-	100%	100%
work.master_pkg	-	-	100%	100%
work.ram_pkg	-	-	100%	100%
work.ram_sva	100%	100%	-	100%
work.wrapper_pkg	100%	-	100%	100%