A hypothetical computer has a 256-byte memory that is byte-addressable, and a processor with 2 general-purpose registers (R0 and R1), a stack pointer (SP), and a program counter (PC). The processor supports a variable-length instruction set. Instructions with no operands are 8-bit long. Instructions with one or two operands are 16-bit long. The instruction formats, the opcodes and the addressing modes are described by the following three tables respectively. Notice that any 16-bit instruction would require two successive locations in memory to be stored. In this case, the most-significant byte of the instruction would be assigned the location with the lower address.

Type	Assembly Format	Binary Format
2-operand	Mnemonic Op1, Op2	4-bit Opcode | 6-bit Op1 | 6-bit Op2 Where Op1 and Op2 fields are formatted as follows: 2-bit addressing mode (AM) | 4-bit value/address (VA)
1-operand	Mnemonic Op1	6-bit Opcode | 10-bit Op1 Where Op1 field is formatted as follows: 2-bit AM | 8-bit VA
0-operand	Mnemonic	8-bit Opcode

Assembly Instruction	Binary Opcode	Meaning
MOV Op1, Op2	0000	Copy Op2 to Op1.
ADD Op1, Op2	0010	Add Op2 to Op1 and store the result to Op1.
SUB Op1, Op2	0011	Subtract Op2 from Op1 and store the result to Op1.
XOR Op1, Op2	1000	XOR Op2 with Op1 and store the result to Op1.
LSL Op1	110000	Shift Op1 logically one-bit position to the left.
ASL Op1	110001	Shift Op1 arithmetically one-bit position to the left.
PUSH Op1	110100	Decrement SP, and then put Op1 on top of the stack.
POP Op1	110101	Copy the top element of the stack to Op1, and then increment SP.
JUMP Op1	111000	Branch to an address specified by the VA field of Op1.
DJNZ Op1	111001	Decrement R0, and check its new value. If it is not zero, branch to the address specified by the VA field of Op1.
CALL Op1	111011	Call a subroutine whose address is specified by the VA field of Op1. The return address is saved to the stack.
RETURN	11110010	Return from a subroutine call. The return address is restored from the stack.
INITSP	11110100	Load SP with a binary value of 11111111.
NOP	11111110	No operation.
HALT	11111111	Stop execution.

Addressing mode	Binary code	Notes
Immediate	00	The immediate value is stored in the VA field of the instruction.
Register	01	Register number is encoded by the least-significant bit (LSB) of the VA field.
Register Indirect	10	Register number is encoded by the LSB of the VA field.
Displacement (Base-Register)	11	Base-register number is encoded by the LSB of the VA field. Displacement is encoded by the rest of the VA field.

Suppose the memory contains the following program:

Address (hexadecimal)	Contents (hexadecimal)	Address (hexadecimal)	Contents (hexadecimal)
10	F4	18	11
11	04	19	FF
12	02	1A	C5
13	04	1B	01
14	60	1C	E4
15	EC	1D	1A
16	1A	1E	F2
17	2D	1F	FE

```
      INITSP
      MOV     R0, #2
      MOV     R1, (R0)
L1:   CALL    L1
      ADD     R0(2), R1
      HALT
L1:   ASL     R1
      DJNZ    L1
      RETURN
      NOP
```

Instruction	PC	SP	R0	R1	Memory Locations	
					02	FE
Initially	10	B3	BE	EF	03	5F
F4	11	FF	BE	EF	03	5F
0402	13	FF	02	EF	03	5F
0460	15	FF	02	03	03	5F
EC1A	1A	FE	02	03	03	17
C501	1C	FE	02	06	03	17
E41A	1A	FE	01	06	03	17
C501	1C	FE	01	0C	03	17
E41A	1E	FE	00	0C	03	17
F2	17	FF	00	0C	03	17
2D11	19	FF	00	0C	0F	17
FF	1A	FF	00	0C	0F	17