Faculty of Engineering

EECE Engineering Department

ELC2060 Project

Electronics Project

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Task #1:

The circuit is a **simple NMOS current source characterization setup**, commonly used in analog and digital integrated circuit design. Its main purpose is to analyze key MOSFET parameters under controlled biasing conditions to support device modeling and performance evaluation, particularly for analog applications like **amplifiers** and **current mirrors**.

Question 1:

N_12_HS_L130E **N_LV_12_HS_L13**

Figures for V_{th}

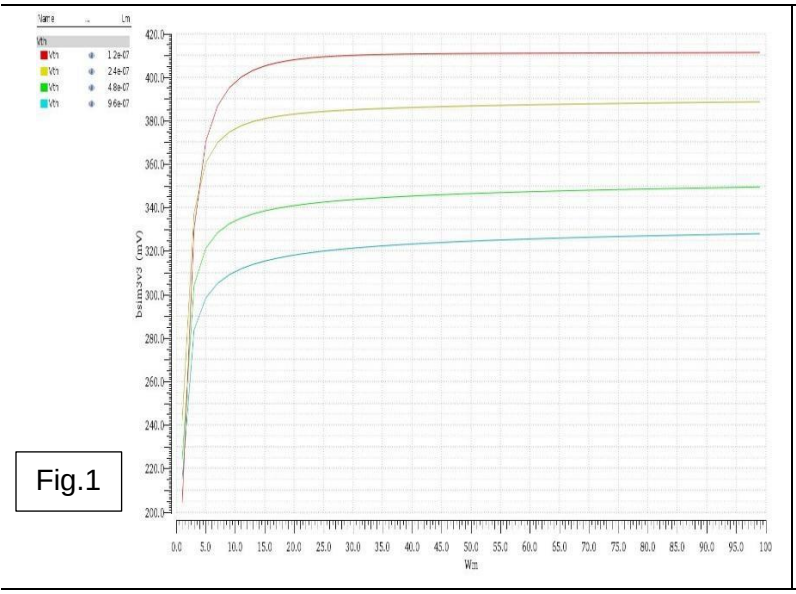


Fig.1

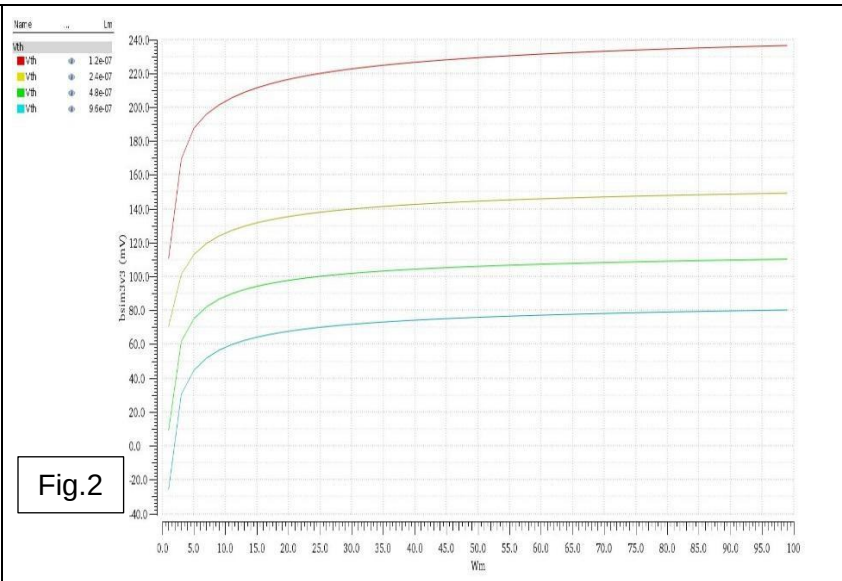


Fig.2

Figures for V_{ov}

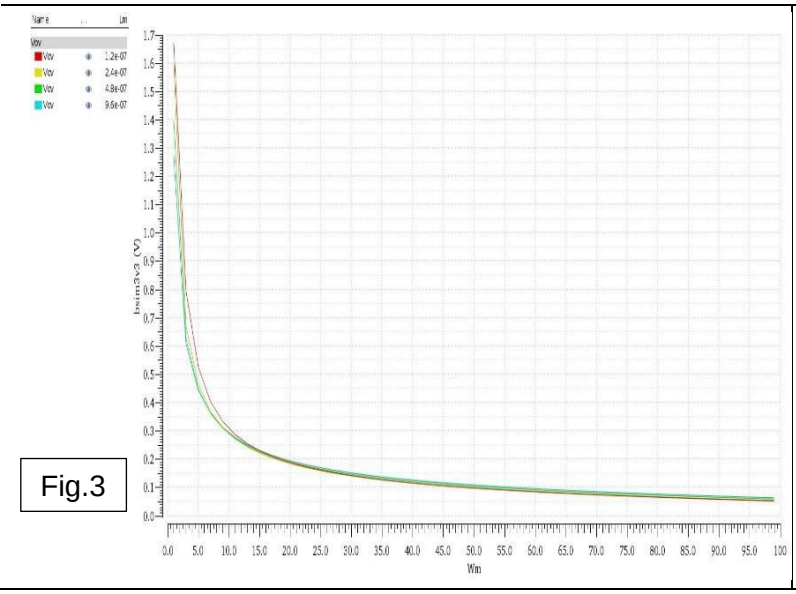


Fig.3

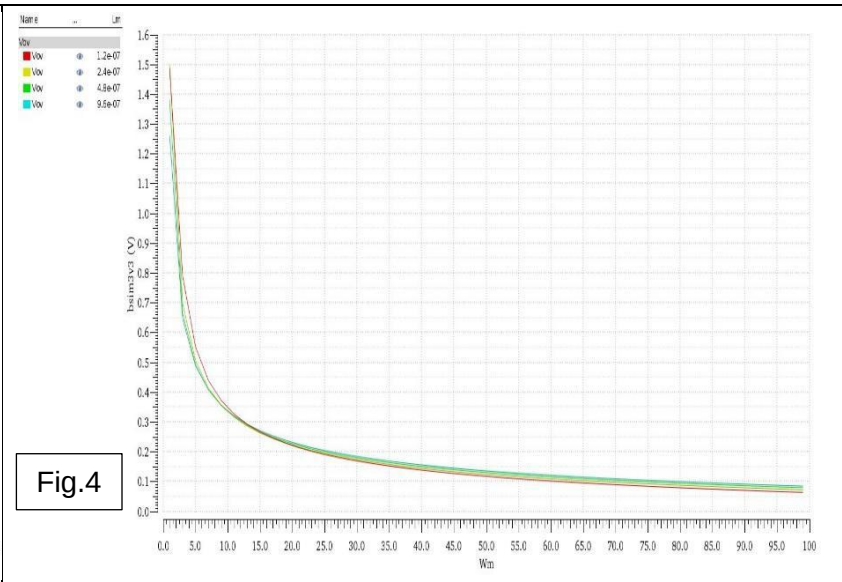


Fig.4

Figures for V_{DSAT}

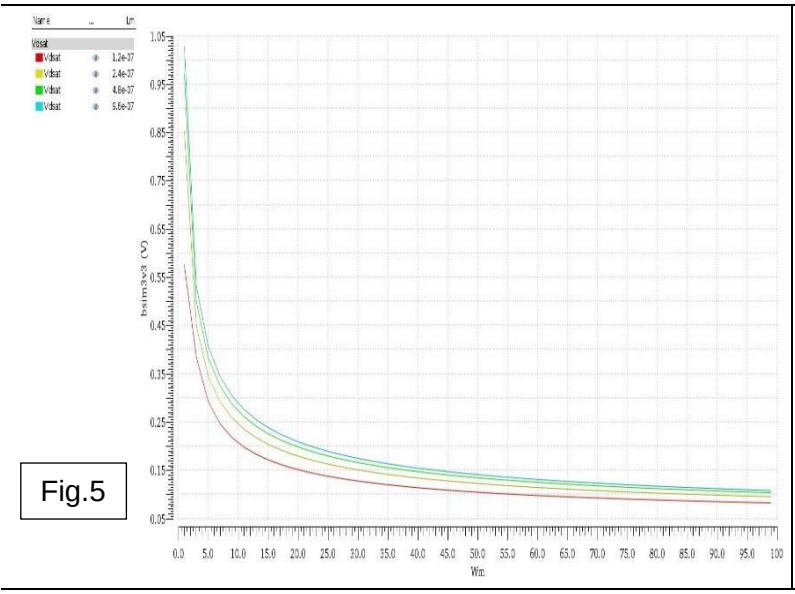


Fig.5

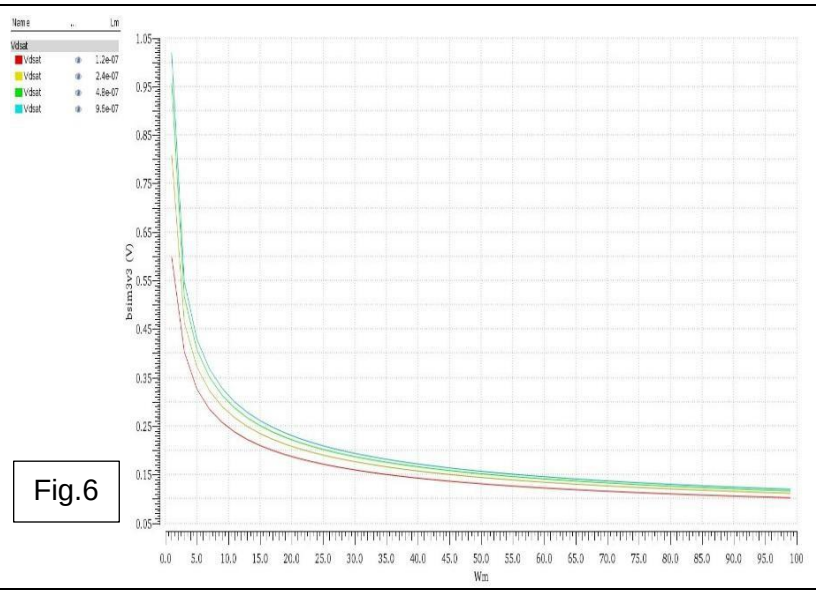


Fig.6

Figures for $g_m r_o$

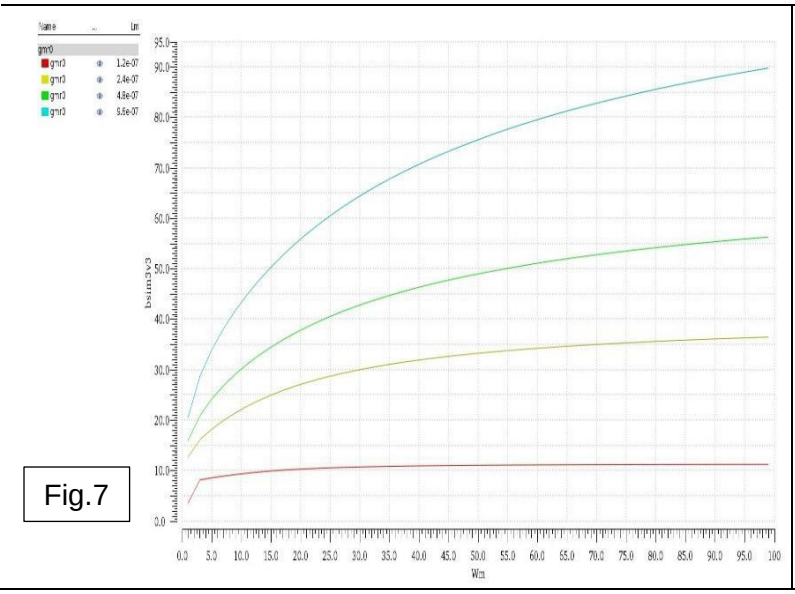


Fig.7

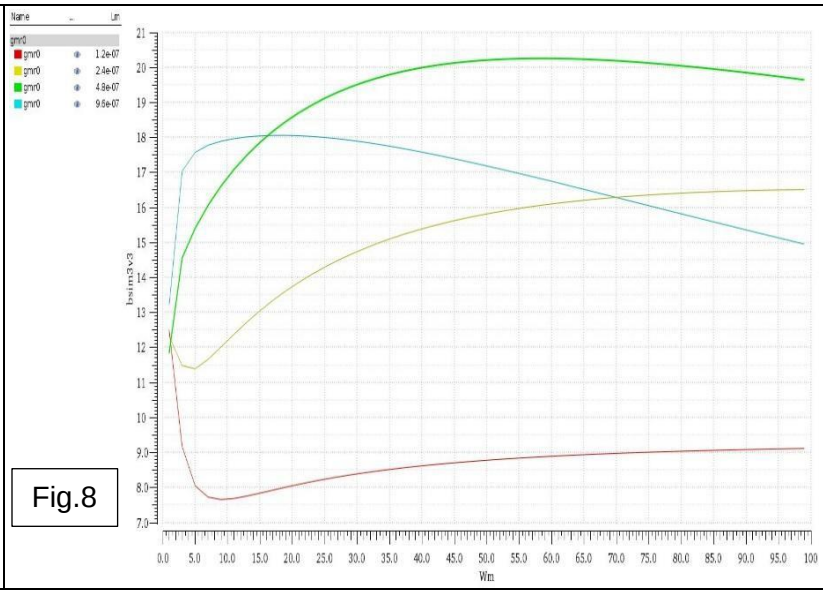


Fig.8

Question 2:

Yes, the simulation trends are generally similar to the theoretical long-channel equations.

For Vth:

At small aspect ratios (low $\frac{w}{l}$), V_{th} increases slightly due to edge effects. As $\frac{w}{l}$ increases, these edge effects become negligible, and V_{th} stabilizes and becomes nearly constant as expected in long-channel devices.

$$I = \frac{\mu C_{ox} w}{2l} (V_{GS} - V_{th})^2 (1 + \lambda Vds)(Square\ law)$$

For Vov and Vdsat :

Both parameters show an inverse relationship with the aspect ratio.

This aligns with the equation:

$$Vov = \sqrt{\frac{2I}{\frac{w}{l}\mu C_{ox}}}$$

As $\frac{w}{l}$ increases, **Vov** and **Vdsat** decrease accordingly.

For gm * ro:

The gain initially increases because gm grows proportionally with $\frac{w}{l}$, while ro decreases more gradually as it is mainly dependent on the current and channel length modulation. Eventually, the product gm * ro a saturation point and becomes relatively constant with higher aspect ratios. This matches the expected behavior from:

$$gm * ro = \frac{w}{l}\mu C_{ox} Vov * \frac{1}{\lambda I}$$

Question 3:

Advantages of N_LV_12_HS_L130E:

Lower Threshold Voltage (Vth):

Since it has a lower threshold voltage, the N_LV_12_HS_L130E can **turn on at lower gate voltages,** allowing for:

- **Higher transconductance gm** at the same bias current

  (because $gm = \frac{2ID}{Vov}$, and Vov tends to be lower)
- **Better performance at lower supply voltages**, which is useful in low-power or scaled technologies.

Disadvantage of N_LV_12_HS_L130E:

Higher Subthreshold Leakage and Lower Output Resistance ro :

The lower threshold voltage can lead to:

- **Higher leakage current** in subthreshold operation (increases static power consumption).
- **Lower intrinsic gain $gm\,ro$** , because ro tends to be smaller due to increased channel length modulation (lambda effect).
- **Worse noise performance**, which can impact analog signal fidelity.

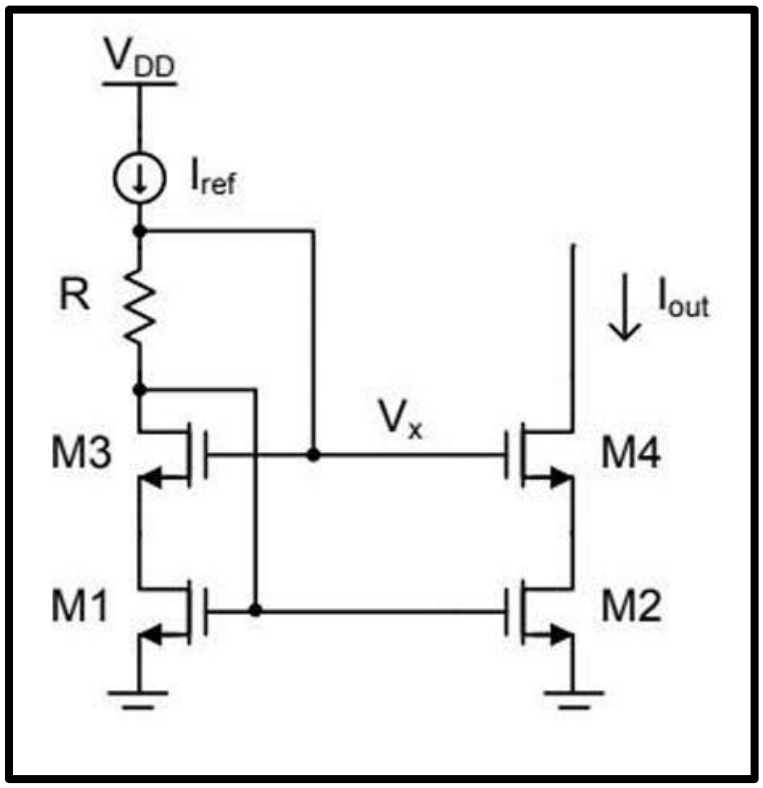
Recommendation for a High-Gain Amplifier:

I recommend using **N_12_HS_L130E** as a high-gain amplifier, because it generally provides **higher intrinsic gain**, **better linearity**, and **lower leakage**, which are essential for analog precision and signal integrity.

Task #2:

In analog integrated circuit design, **current mirrors** are fundamental building blocks used to replicate a reference current across multiple branches of a circuit. They're essential in biasing networks, active loads, and analog signal processing applications. However, conventional current mirrors often suffer from limited output voltage swing due to the requirement of keeping transistors in saturation to maintain accuracy and high output impedance.

To address this, **high-swing current mirrors** have been developed. These designs enhance the available output voltage range while still ensuring that all transistors operate within their desired regions. The **high-swing current mirror** architecture typically adds cascode devices or auxiliary transistors to improve output resistance (Rout) and reduce the minimum voltage required at the output node (Vcomp) for proper operation.



1-Schematic diagram with dimensions and component values annotated.

- The schematic diagram in **Fig.9**:
  - For M1&M3: Width=W & Length=L
  - For M4&M2: Width=2W & Length=L
  - VD4= VOUT & let R0= 2K **(we will explain it in Hand Analysis)**

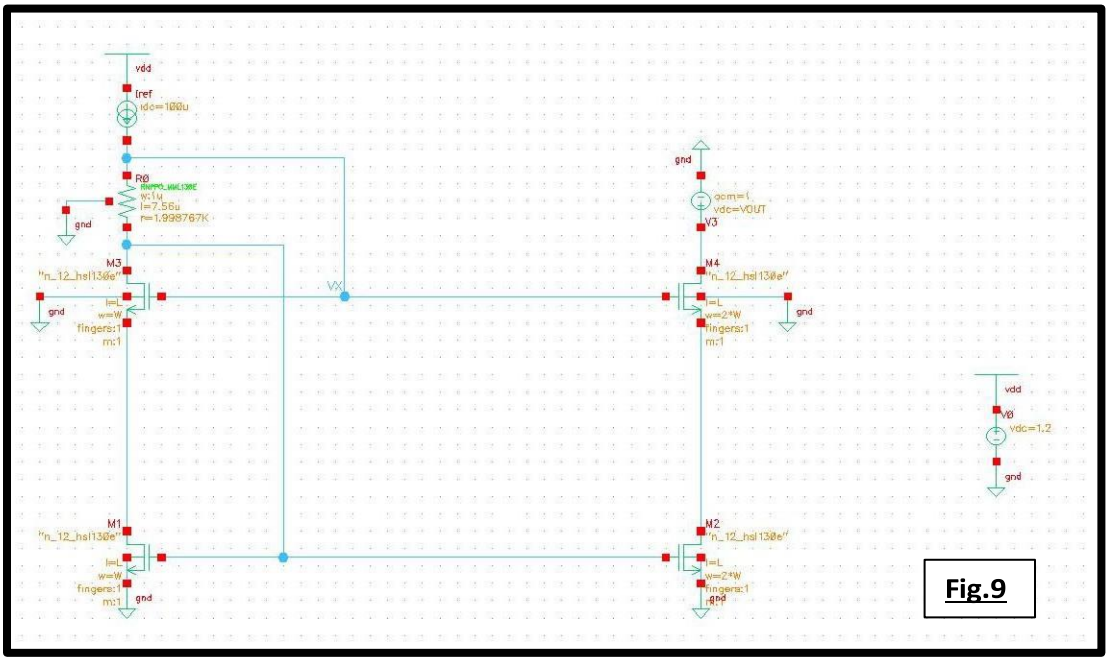


Fig.9

- We launch our schematic in ADE XL with global variables as shown in **Fig.10**
- From results in **Fig.11,** we took W=55u m & L=3u m this also achieve current mirror = 201.8u A, with error < 1%

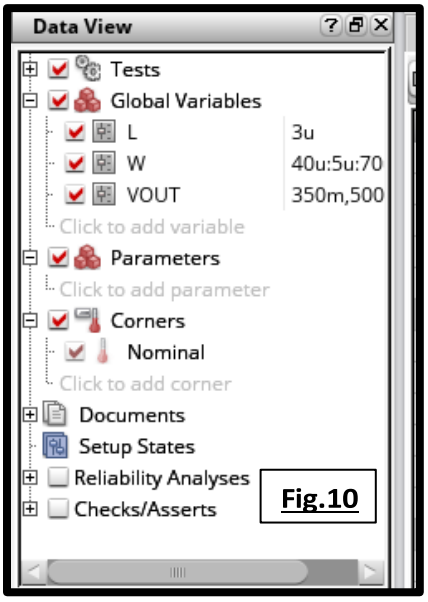


Fig.10

Parameters: W=55u, VOUT=350m			
7	Task#2:Taskk2:1	OP("/M3" "region")	2
7	Task#2:Taskk2:1	OP("/M1" "region")	2
7	Task#2:Taskk2:1	OP("/M2" "region")	2
7	Task#2:Taskk2:1	OP("/M4" "region")	2
7	Task#2:Taskk2:1	IDC("/M4/D")	201.2u
7	Task#2:Taskk2:1	/M4/D	
Parameters: W=55u, VOUT=500m			
8	Task#2:Taskk2:1	OP("/M3" "region")	2
8	Task#2:Taskk2:1	OP("/M1" "region")	2
8	Task#2:Taskk2:1	OP("/M2" "region")	2
8	Task#2:Taskk2:1	OP("/M4" "region")	2
8	Task#2:Taskk2:1	IDC("/M4/D")	201.8u
8	Task#2:Taskk2:1	/M4/D	

Fig.11

- **Hand Analysis:**
  - To get $R0$:

$$R0 = \frac{Vgs3 - Vds3}{Iref}, \because Vds3 \geq Vgs3 - Vth$$

$$\therefore R0 = \frac{Vgs3 - Vgs3 + Vth}{Iref} = \frac{Vth}{Iref}, \text{ assume } Vth = 0.2\,V$$

$$\boxed{\therefore R0 \geq 2K\ \Omega}$$

$$\because R0 = \frac{Vgs4 + Vds2 - Vgs2}{Iref}, \because Vds2 \geq Vgs2 - Vth$$

$$\therefore R0 = \frac{Vgs4 + Vgs2 - Vth - Vgs2}{Iref} = \frac{Vgs4 - Vth}{Iref} = \frac{Vcomp}{Iref}$$

$$\because Vcomp \leq 350mV$$

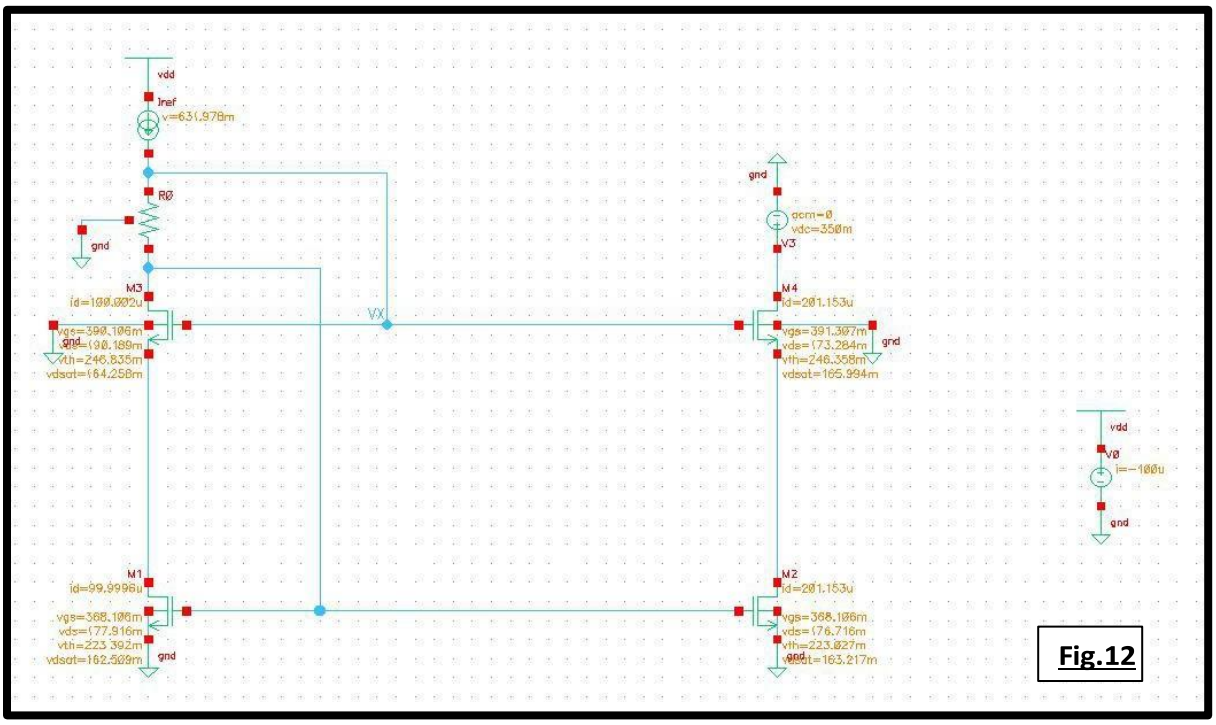
$$\boxed{\therefore R0 \leq 3.5K\ \Omega}$$

$$\boxed{\therefore 3.5K \geq R0 \geq 2K}$$

2. Schematic diagram with DC operating point annotated at Vout=350mV to verify the Vcomp specification.

- The schematic of DC operating point in **Fig.12** @$Vout$ = 350mV
  - For M4: $Vgs4$ = 391.307mV
    $Vds4$ = 173.284mV
    $Ids4$ = 201.153$u\ A$
  - For M2: $Vgs2$ = 368.106mV
    $Vds2$ = 176.716mV
    $Ids2$ = 201.153mV

- Note: we found from DC operating point that Vth = 223.02$mV \simeq 0.2V$
  And this verifies our assumption in **Hand Analysis**



3. Simulation results to verify Iout and $Rout$ specifications.

- To get $Rout$:
  - First, we put $Vout, ac$ = $1V$
  - Second, from ADE L we have done an analysis as shown in **Fig.13**.
  - Third, from output we choose setup (from design) and then we take this equation $\mathbf{1/mag(i("/M4/D" ? result "ac"))}$
  - Fourth, we get the graph of $Rout$ as shown in **Fig.14**
  - $\boldsymbol{Rout}$ = $\mathbf{725.6742K\Omega}$

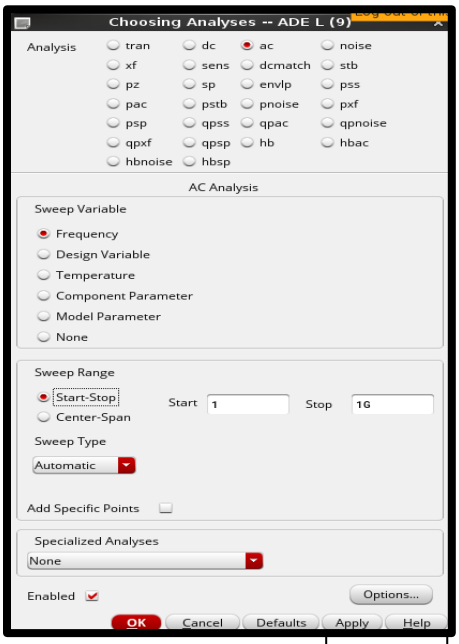


Fig.13

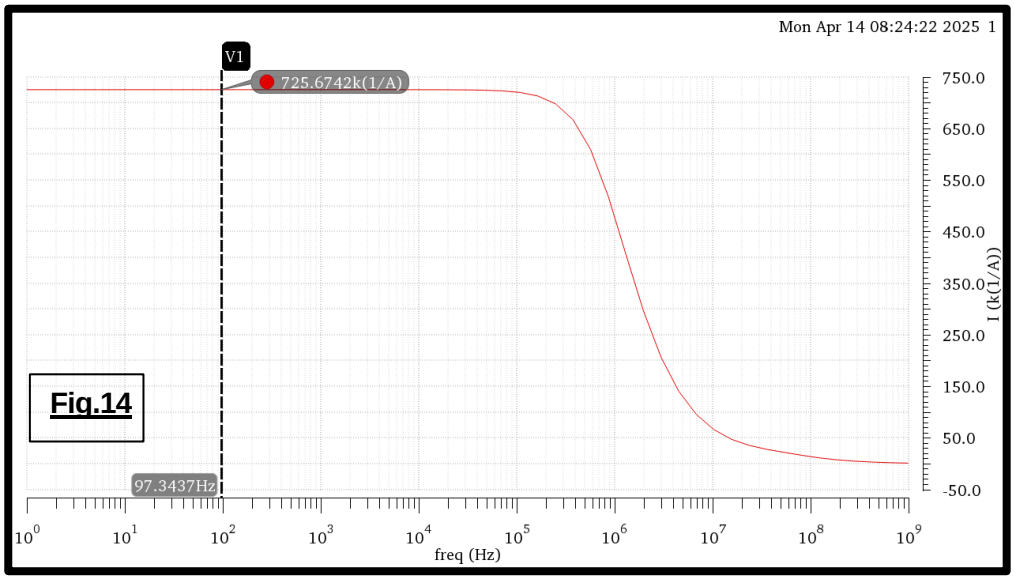


Fig.14

- To get $Iout$:
  - First, we take the results from ADE XL in **Fig.11**
  - Second, we plot $Iout$ versus W as shown in **Fig.15**

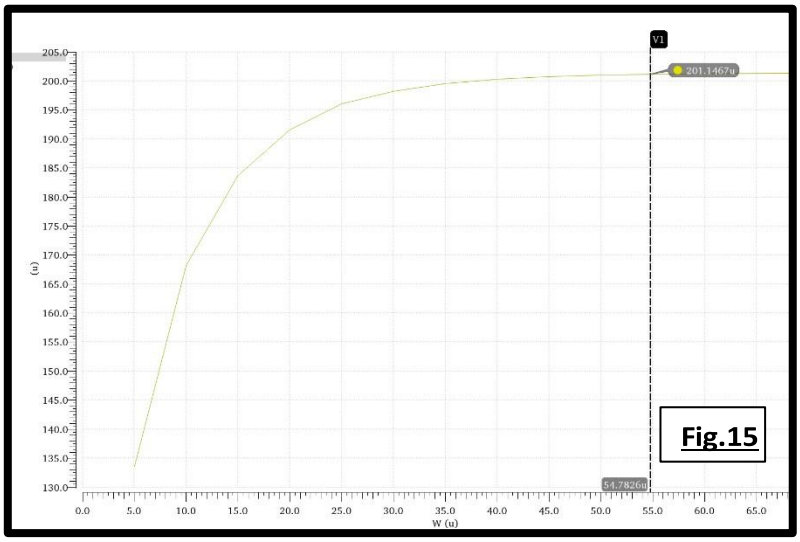


Fig.15

4. An estimate of this mirror's area.

- Area = Area of NMOS Transistors + Area of R0

  $= 6 * W_N * L_N + W_R * L_R$

  $= 6 * 55u * 3u + 1u * 7.56u$

  $= 0.997nm^2$

5. If the area you ended up with is too large and you need to sacrifice one of the specs to have reasonable area, suggest a modification and comment on what you will gain and lose from it.

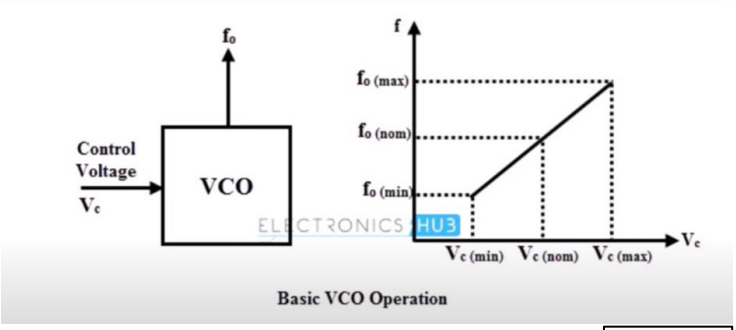
- If the designed current mirror occupies a large layout area, one effective modification is to relax the output resistance specification from $Rout \geq 500K$ to a slightly lower value, such as $300 - 400K\Omega$. This can be achieved by using shorter channel lengths for the output transistors, which significantly reduces the area.
  Impact of the Modification:
  - **Advantage:** Reduced area and parasitic capacitance, leading to a more compact and potentially faster design.
  - **Disadvantage:** Lower output resistance may reduce the accuracy and gain when the mirror is used in analog circuits, especially in high-gain stages.

Task #3:

In this task, we deal with a **Voltage Controlled Oscillator (VCO),** it works such that the oscillation frequency is controlled by an input voltage, but how?

- The control voltage Vcont sets the tail current IB through the transistor M1.
- MOSFETs M1 and M4 act as current sources for the inverter.
- This current determines the charging and discharging rate of the capacitive nodes between inverters in the ring oscillator.
- In a ring oscillator the delay of each inverter stage directly affects the total oscillation period.
- Since the delay is a function of the current, and the current is a function of Vcont then the oscillation frequency becomes a function of Vcont. [6]

An ideal VCO is a circuit whose output frequency is a linear function of its control voltage.



[7]

Fig.16

Schematic

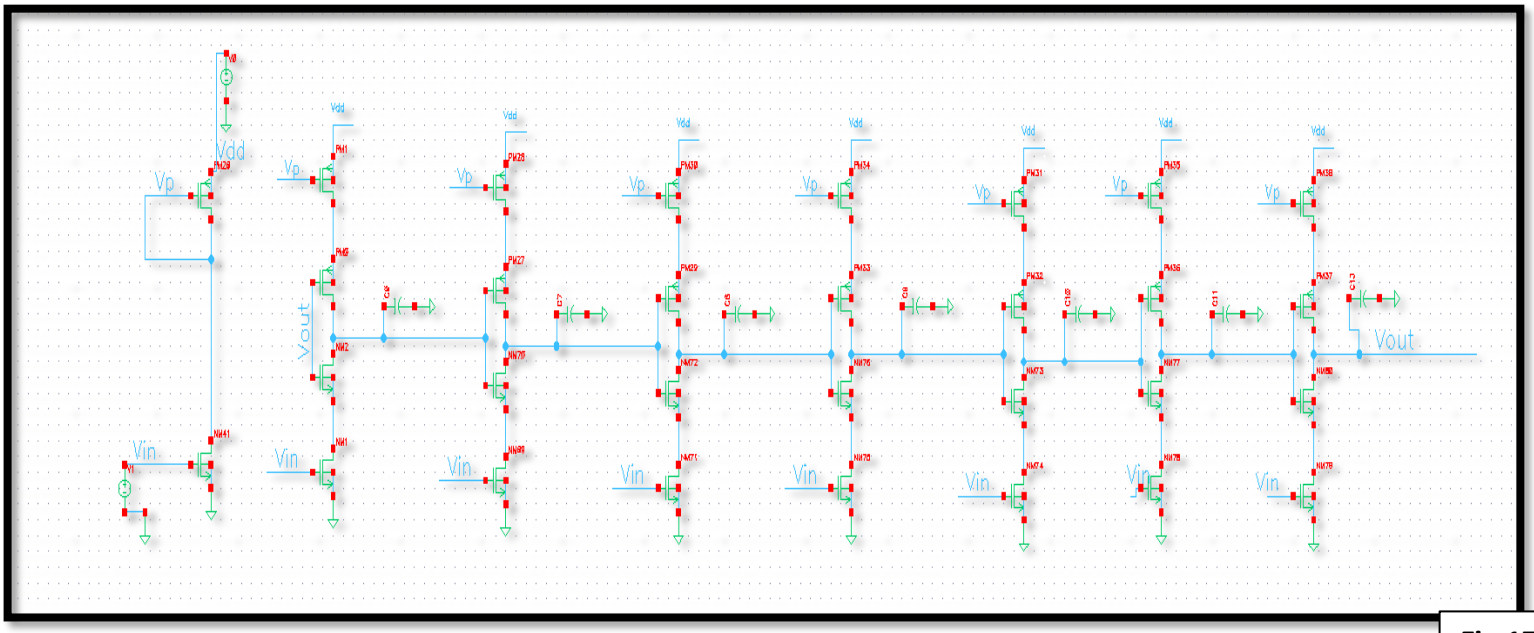


Fig.17

Simulation;

Question 1:

1. We first built the circuit's schematic, then we chose that M4 width "W3" to be double the width of M1 "W1" or more for proper biasing to ensure that all transistors operate in sat. We chose W3=1000n and W1=500n to achieve this while also keeping the areas of M1 and M4 as small as possible without diversifying the dimensions of all transistors. We also kept in mind that increasing the width results in reducing the required voltage to reach saturation. We chose minimum length 130n for all transistors to minimize parasitic capacitance and area.

Test	Output	Nominal	Spec
Project:task3:1	frequency(VT("/Vout"))	20.15M	
Project:task3:1	VT("/Vout")		
Project:task3:1	OP("/PM26" "region")	2	
Project:task3:1	OP("/NM41" "region")	2	
Project:task3:1	OP("/NM1" "region")	2	

Fig.18

2. We then launched the schematic in ADE XL to with global variables as shown in **Fig.19** to sweep the width of M2, M3 "W2 and W4" using the function "frequency" to find the width that corresponds to the required oscillation frequency 20MHz. we got W2=W4=30u which is very large, so we used capacitors between every stage to reduce the required widths, resulting in W2=W4=1.2u which are reasonable widths, in order to do that we sweeped the value of the capacitor to reach the oscillation frequency resulting in C=263femto F.

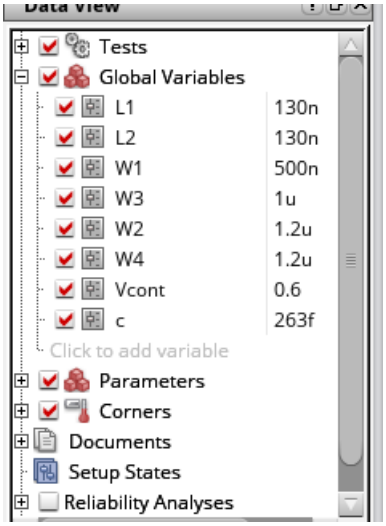


Fig.19

L1	**Length of N-Mos &P-Mos Current source**
L2	**Length of N-Mos &P-Mos Inverters**
W1	**Width of N-Mos Current source**
W2	**Width of N-Mos Inverters**
W3	**Width of P-Mos Current source**
W4	**Width of P-Mos Inverters**
Vcont	**V control**
c	**Value of the Cap**

3. We then got IB from DC Operating point as shown in **Fig.20**.

IB=52.965 uA

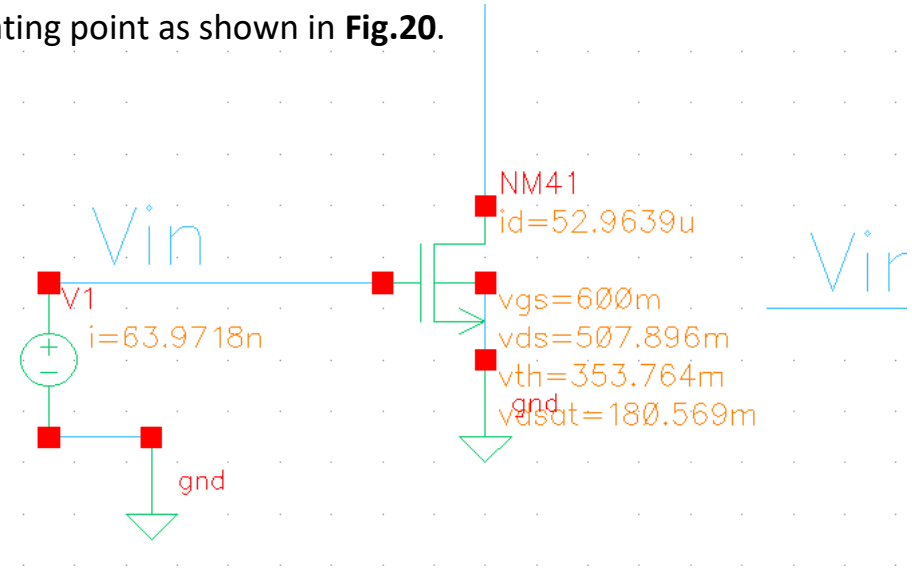


Fig.20

Question 2:

Vout

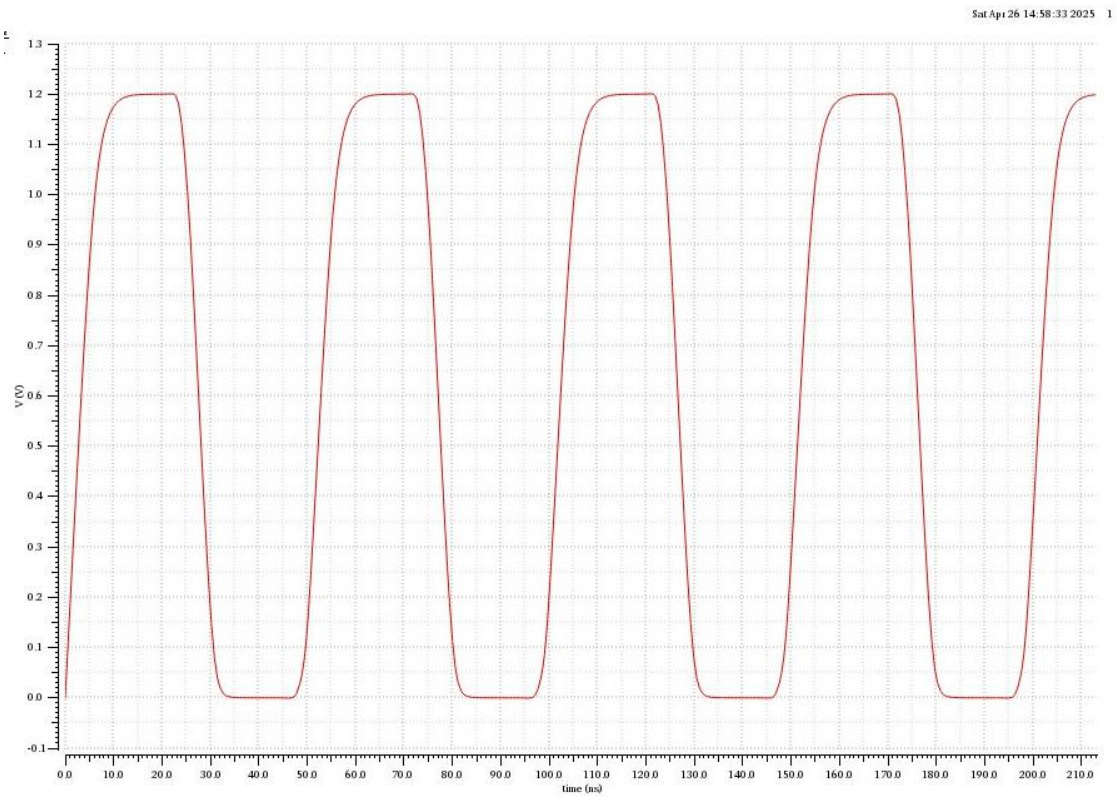


Fig.21

1st Stage

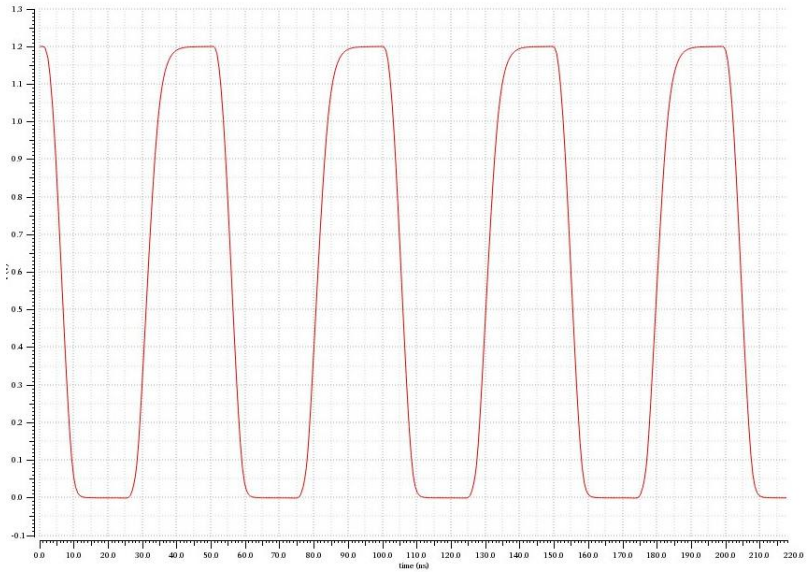


Fig.22

2nd Stage

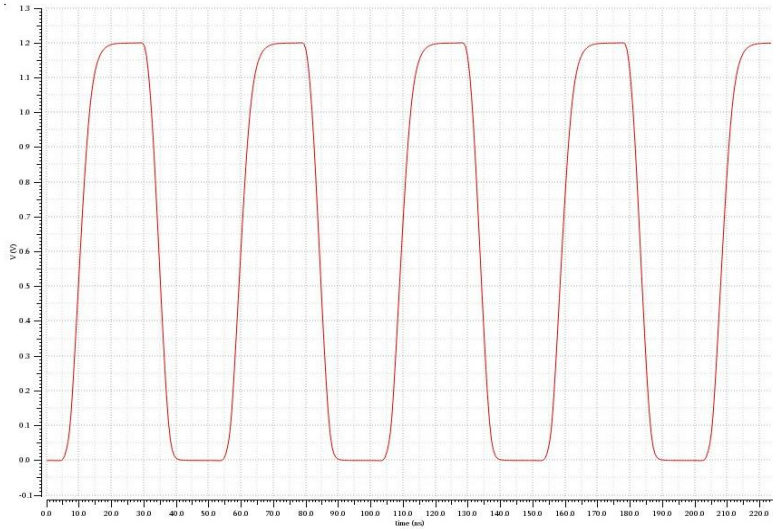


Fig.23

3rd Stage

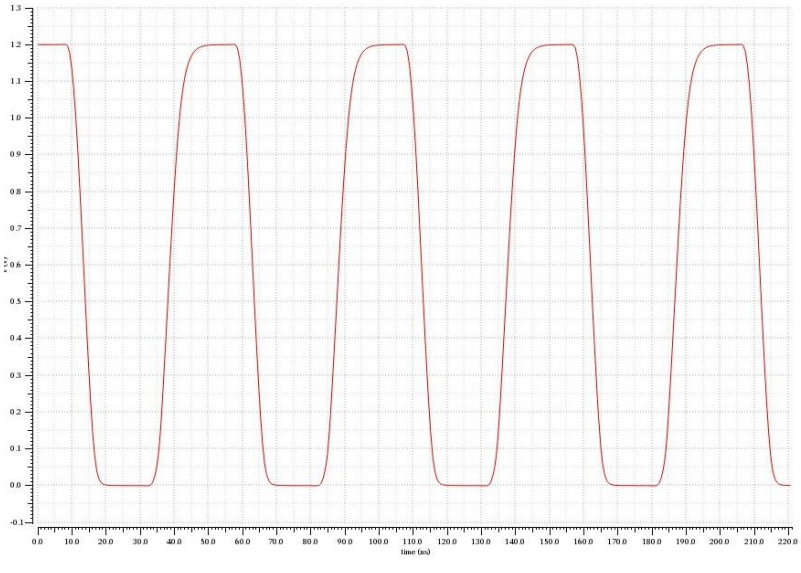


Fig.24

4th Stage

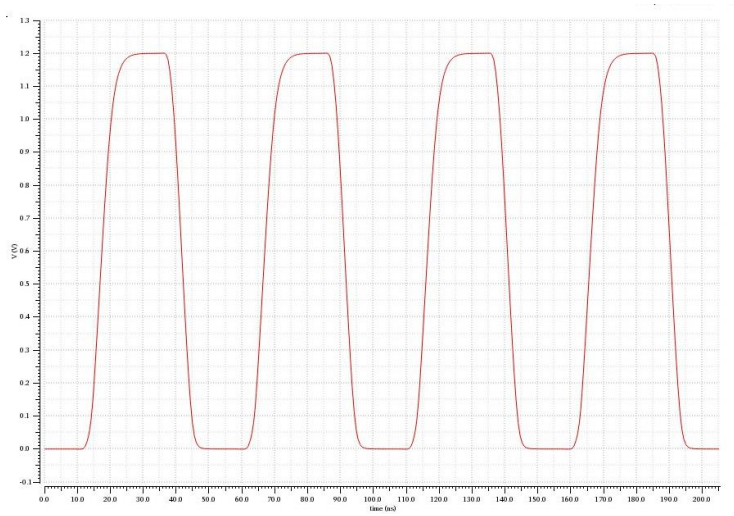


Fig.25

5th Stage

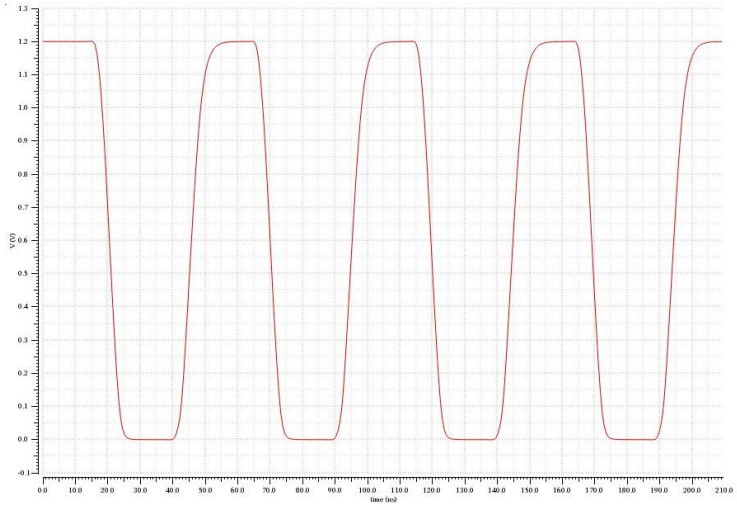


Fig.26

6th Stage

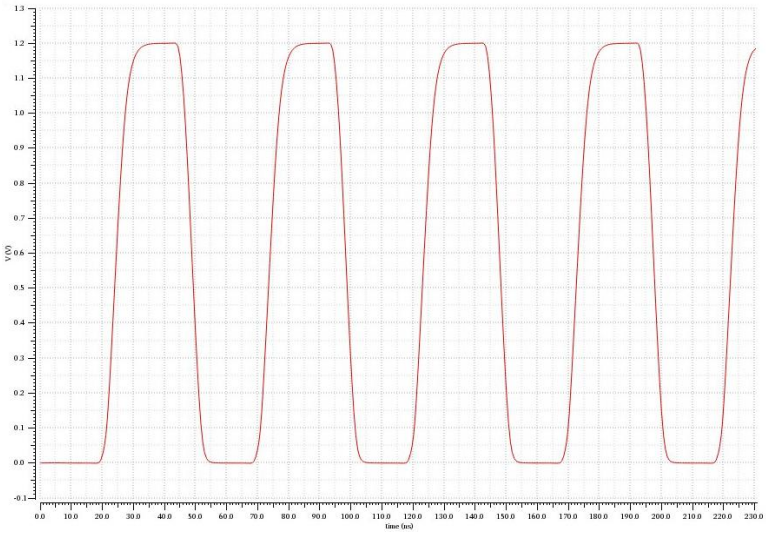


Fig.27

Question 3:

As we had mentioned earlier, increasing Vcont will result in increasing the output frequency due to their relationship as shown in **Fig.28** and **Fig.30**:

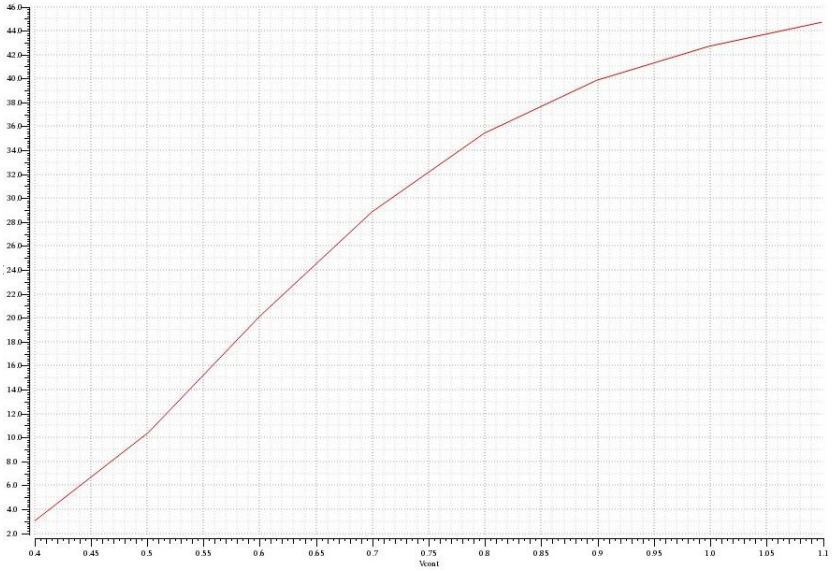


Fig.28

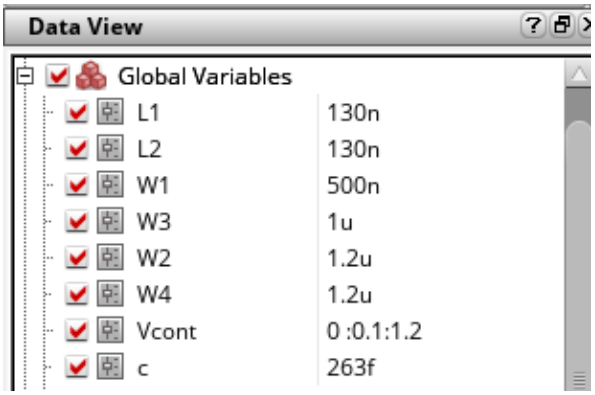


Fig.29

Parameters: Vcont=0						
1	Project:task3:1	frequency(VT("/Vout"))	eval err			
Parameters: Vcont=100m						
2	Project:task3:1	frequency(VT("/Vout"))	eval err			
Parameters: Vcont=200m						
3	Project:task3:1	frequency(VT("/Vout"))	eval err			
Parameters: Vcont=300m						
4	Project:task3:1	frequency(VT("/Vout"))	eval err			
Parameters: Vcont=400m						
5	Project:task3:1	frequency(VT("/Vout"))	3.034M			
Parameters: Vcont=500m						
6	Project:task3:1	frequency(VT("/Vout"))	10.34M			
Parameters: Vcont=600m						
7	Project:task3:1	frequency(VT("/Vout"))	20.15M			
Parameters: Vcont=700m						
8	Project:task3:1	frequency(VT("/Vout"))	28.88M			
Parameters: Vcont=800m						
9	Project:task3:1	frequency(VT("/Vout"))	35.46M			
Parameters: Vcont=900m						
10	Project:task3:1	frequency(VT("/Vout"))	39.88M			
Parameters: Vcont=1						
11	Project:task3:1	frequency(VT("/Vout"))	42.73M			
Parameters: Vcont=1.1						
12	Project:task3:1	frequency(VT("/Vout"))	44.73M			
Parameters: Vcont=1.2						
13	Project:task3:1	frequency(VT("/Vout"))	46.17M			

Fig.30

Vout at Vcont=0.4v

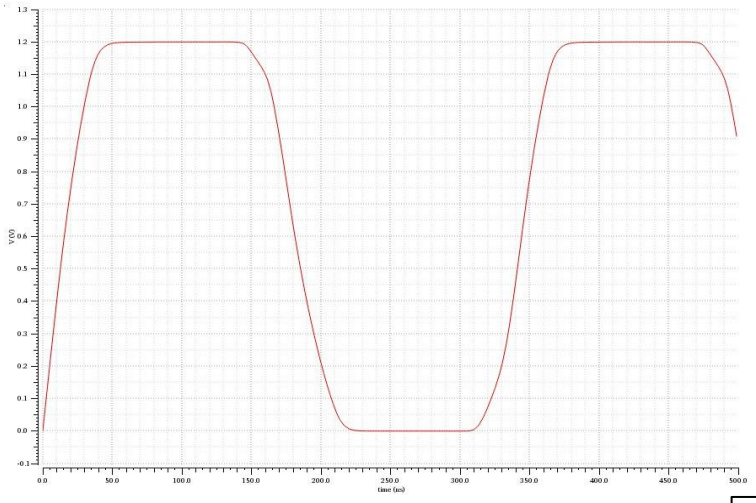


Fig.31

Vout at Vcont=0.8v

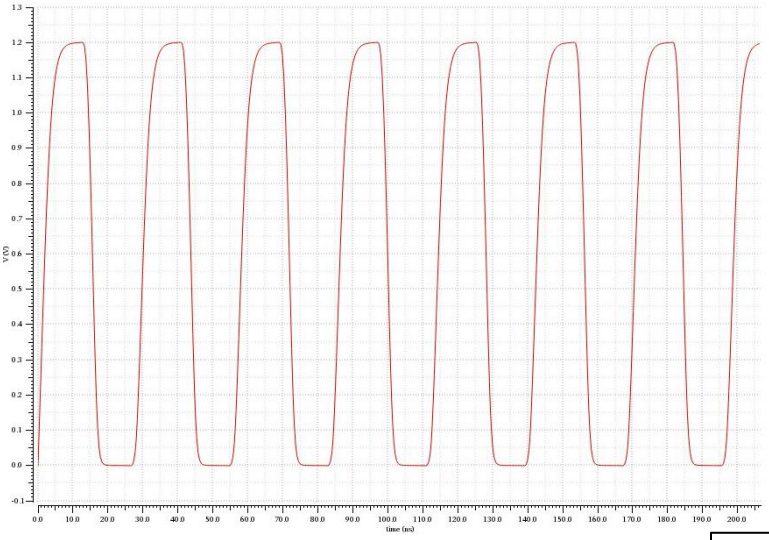


Fig.32

Vout at Vcont=1.1v

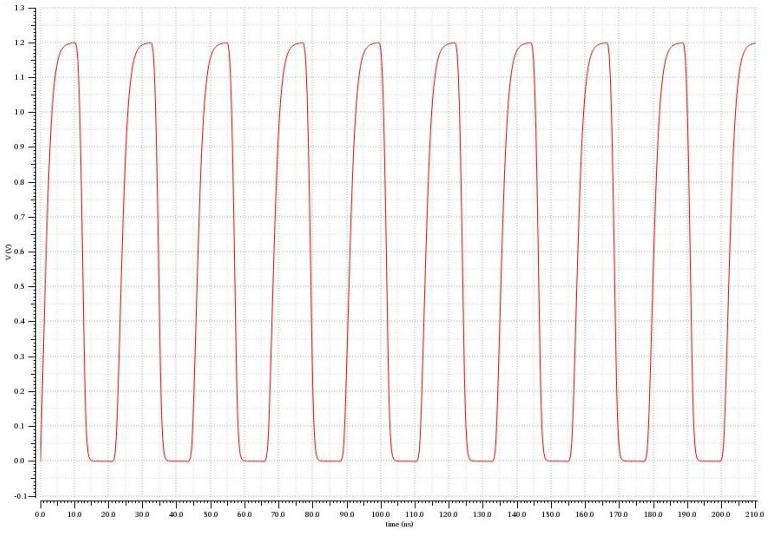


Fig.33

Question 4:

1. Observations

- The ring-oscillator VCO's output frequency relies on the control voltage that sets the bias current through M1, which in turn controls the charging/discharging rates of the inverter nodes.
- Ensuring all transistors remain in saturation requires careful sizing; M4 was chosen at twice the width of M1 to maintain proper biasing without overly diversifying device dimensions.
- Achieving a 20 MHz oscillation purely by widening M2/M3 demanded impractically large device sizes, but introducing capacitors between each stage restored the target frequency with more moderate transistor widths.

2. Conclusions

- **Voltage to Frequency Conversion**: By biasing M1 with Vcont, our ring-oscillator VCO directly translates a control voltage into a bias current, and hence into oscillation frequency, making it a straightforward, fully-integrated frequency tuning element.
- **Ease of Integration:** A CMOS ring-VCO requires only standard digital cells (inverters and small caps) plus two bias transistors, no inductors or large passive LC tanks, so it's ideal for on-chip PLLs, clock generation, and other voltage-controlled timing blocks.

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