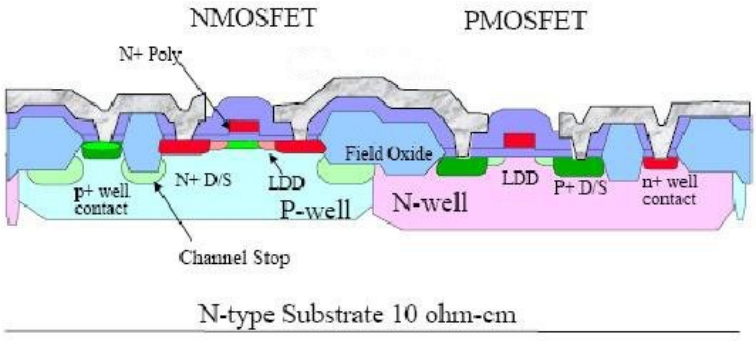
Integrated Circuits Lab

482 COURSE PROJECT 1 – FALL 2019: PLANAR CMOS TCAD SIMULATION

The project consists of two essential phases: Phase I, getting ready to the project and Phase II process simulation.

Phase I: Get Ready!
This is an orientation phase, to get you on the correct track to start the project. This phase has no deliverables. Before you start the project you need to:
1. Review the process integration lecture from the course.
2. Get a closer look on SILVACO tools.
3. Study and understand SILVACO ATHENA syntax and code organization.
4. Study the MOSFET examples included with ATHENA and try them by yourself.

Phase II: CMOS process simulation
At this point you are ready to start working on your own. The objective of this phase is to perform a simulation for the CMOS process integration. Your target is to simulate the processes one by one to get a cross section as in the figure below. The action for this phase can be summarized as follows:



1. Consider the main process parameters presented in the table below.
2. Assume reasonable values for all other parameters (dimensions and doping). Justify your choices using course data and charts.
3. Start building your ATHENA simulation code in an incremental way: Simulate the processes one by one till you get the complete structure. This will be your major effort.
4. Consider modeling the process in 2D only. Extra care should be taken with the initial mesh generation.

Table 1: CMOS process parameters

L	$0.35\mu m$	T_{ox}	7.9 nm
X_J	150 nm	L_D	$0.8\mu m$
$N_{subNMOS}$	$6.8 \times 10^{15} cm^{-3}$	$N_{subPMOS}$	$1.6 \times 10^{16} cm^{-3}$

-Deliverables:

It is required to deliver:

1. Cross section after each major process step.
2. Doping level contours after each major step.
3. ATHENA code for the process simulation.
4. ID-VGS curves for high and low VDS, plot ID in both linear and log scale (this will produce four curves)

5. Extracting the electrical parameters listed in table below from the log scale curves for both n and p-devices

Parameter	Unit
ON drain current (Ion)	µA
Off leakage current (Ioff)	µA
Threshold Voltage in both low and high VDS (Vthlin,Vthsat)	mV
Drain Induced Barrier Lowering (DIBL)	mV/V
Sub-threshold Swing (SS)	mV/dec
Current ratio (Ion/Ioff ratio)	unitless