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Research and Implementation of Channel Estimation Algorithm Based on Wideband Micro-power System

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Abstract. Channel estimation and equalization are the keys to realize wideband micro-power wireless communication system. In this paper, the channel estimation algorithm is improved according to the frame structure characteristics of wideband micro-power. Compared with the original algorithm, new algorithm is more suitable for this system and its performance is improved by 0.2dB. By establishing the system simulation model in MATLAB environment, the corresponding channel estimation algorithm is used to simulate and compare. The performance of the improved algorithm is verified and the improved algorithm is implemented on the FPGA platform. In the process of hardware implementation, formula transformation is used to reduce the use of multipliers in complex multiplication and reduce resource consumption. The results of ISE Design Suite 14.7 synthesis and Modelsim simulation show that the algorithm has low algorithm complexity, small hardware resources, and the estimation accuracy meets the expectations and meets the application requirements.

1. Introduction

With the new trend of power industry development, a development blueprint of smart grid [1] has been planned by state grid. As an important part in the smart grid, smart meters are responsible for collecting and managing the electricity consumption data of users, which is equivalent to the hub between the grid system and power users. The low-cost short-range wireless technology is used between the concentrator and the energy meter for networking. The wireless channel has a large randomness, which causes distortion of the amplitude, phase and frequency of the received signal, which seriously affects the performance of the wireless communication system. Therefore, the estimation and equalization of wireless channel are the keys to implement the wideband micro-power wireless communication system.

The wideband micropower wireless communication system is a chirp signal wideband communication system based on BOK modulation [2]. The mathematical expression of Chirp signal is

$$s(t)=\alpha(t)\cos(2\pi(f_0 t+\mu^{t^2}/2),-T/2\le t\le T/2 \tag{1}$$

Where, $\alpha(t)$ is the envelope of Chirp signal, which usually a rectangular pulse,when $t\le T/2$, $\alpha(t)=a$,otherwise $\alpha(t)=0$; T is pulse height, also known as frequency sweep time of signal; f_0 is the center frequency of Chirp signal, the expression of signal instantaneous frequency:

$$f(t)=\frac{1}{2\pi}\frac{\mathrm{d}}{\mathrm{dt}}s(t)=f_0+\mu t \tag{2}$$

Where, μ is the linear FM slope of Chirp signal. The instantaneous frequency is linear with time over a pulse width. $\mu < 0$ represents negative slope signal, whose instantaneous frequency decreases with time; $\mu > 0$ represents a positive slope signal whose instantaneous frequency increases with time. The frame structure of wideband micro-power AD hoc network system is shown in figure 1.

Preamble	Synchronization Code	Frame Control bit	Frame interval	Data

Figure 1. Frame structure of wideband micro-power AD hoc network system

In Figure 1, the preambles of the frame structure is fixed to 1, the length can be set, and the longest is 512 bits (up) for coarse synchronization and channel estimation; the synchronization code is fixed to 0, the length can be set and the maximum length is 64 bits (down)) for channel estimation. Next in the frame structure are frame control bits, frame intervals, and data.

It can be seen from the above frame structure analysis that we will use all 1 and all 0 training sequences for channel estimation in the wideband micro-power system. Since there is no need to consider the peak superposition problem in the Orthogonal Frequency Division Multiplex (OFDM) system, the whole 1 training sequence and the all-zero training sequence are used in this system, and the effect is not much different from the pseudo -random sequence, and it is useful to distinguish training sequences and data during data reception and implementation. This paper will mainly analyze and implement the channel estimation and equalization correlation algorithms based on training sequences.

2. Channel estimation algorithm

The channel estimation algorithms based on training sequences mainly include Least Squares (LS) and MMSE Minimum Mean Square Error (MMSE). The channel estimation algorithm can also be divided into time domain channel estimation algorithm and frequency domain channel estimation algorithm. Since time domain convolution can be converted into a simple multiplication operation in the frequency domain, only the frequency domain channel estimation algorithm is discussed herein.

2.1. The LS algorithm

LS algorithm [3] is the most basic and simple channel estimation algorithm. Suppose the information of the transmitter's reference signal is $\boldsymbol{X}_{\mathrm{p}}$, the information of the receiver's reference signal is $\boldsymbol{Y}_{\mathrm{p}}$, the channel impulse response matrix is $\boldsymbol{H}_{\mathrm{p}}$, and the noise is $\boldsymbol{N}$, then the relationship between them can be expressed as

$$\boldsymbol{Y}_{\mathrm{p}} = \boldsymbol{X}_{\mathrm{p}}\boldsymbol{H}_{\mathrm{p}} + \boldsymbol{N} \tag{3}$$

Let $\boldsymbol{Y} - \mathrm{diag}(\boldsymbol{X})\boldsymbol{H}$ be the minimum, the estimated value of channel response can be expressed as

$$\hat{\boldsymbol{H}} = \arg\min \left\| \boldsymbol{Y} - \mathrm{diag}(\boldsymbol{X})\boldsymbol{H} \right\|^2 \tag{4}$$

According to the least square criterion and partial derivative, we can get

$$\boldsymbol{H}_{\mathrm{p,LS}} = (\boldsymbol{X}_{\mathrm{p}}^{\mathrm{T}}\boldsymbol{X}_{\mathrm{p}})^{-1}\boldsymbol{X}_{\mathrm{p}}^{\mathrm{T}} = \boldsymbol{X}_{\mathrm{p}}^{-1}\boldsymbol{Y}_{\mathrm{p}} = \boldsymbol{H}_{\mathrm{p}} + \frac{\boldsymbol{N}_{\mathrm{p}}}{\boldsymbol{X}_{\mathrm{p}}} \tag{5}$$

Therefore, the channel estimation expression of LS algorithm is

$$\hat{\boldsymbol{H}}_{\mathrm{LS}} = \boldsymbol{X}_{\mathrm{p}}^{-1}\boldsymbol{Y}_{\mathrm{p}} \tag{6}$$

It can be obtained from the above equation that the LS channel estimation algorithm does not make use of prior information of the channel,and it only needs to know the training sequence information of the sender and receiver to estimate the channel. The algorithm has a simple structure and a small amount of computation.

2.2. The MMSE algorithm

MMSE channel estimation [4-6] eliminates the influence of noise. According to MMSE criterion, the channel frequency domain response of MMSE algorithm is

$$\hat{\boldsymbol{H}}_{\mathrm{MMSE}} = \boldsymbol{R}_{\mathrm{HH}}[\boldsymbol{R}_{\mathrm{HH}} + \sigma_{\mathrm{N}}^2(\boldsymbol{X}_{\mathrm{p}}^{\mathrm{H}}\boldsymbol{X}_{\mathrm{p}})^{-1}]^{-1}\hat{\boldsymbol{H}}_{\mathrm{LS}} \tag{7}$$

It can be seen from the above formula that the channel estimation based on the MMSE algorithm is actually based on the LS algorithm and the filtering process with the coefficient $\boldsymbol{R}_{\mathrm{HH}}[\boldsymbol{R}_{\mathrm{HH}} + \sigma_{\mathrm{N}}^2(\boldsymbol{X}_{\mathrm{p}}^{\mathrm{H}}\boldsymbol{X}_{\mathrm{p}})^{-1}]^{-1}$ is performed once again. The result of the LS estimation passes a Finite Impulse Response (FIR) filter with a coefficient of $\boldsymbol{R}_{\mathrm{HH}}[\boldsymbol{R}_{\mathrm{HH}} + \sigma_{\mathrm{N}}^2(\boldsymbol{X}_{\mathrm{p}}^{\mathrm{H}}\boldsymbol{X}_{\mathrm{p}})^{-1}]^{-1}$, which eliminates the influence of noise on the channel estimation. Therefore, the performance of the MMSE algorithm is better than that of the LS algorithm.

However, from the perspective of implementation, the MMSE algorithm needs to calculate the correlation function of the channel in the ideal mode, and also needs to invert the autocorrelation matrix of the channel to obtain the coefficients of the filter. Therefore, the amount of computation required is large, the complexity is also high, and the implementation is difficult.

3. algorithm simulation

The baseband system model and multipath channel model based on wideband micro-power system were built in MATLAB environment, and the performance simulation of LS and MMSE channel estimation algorithm was carried out. The simulation results of mean square error were shown in figure 2.

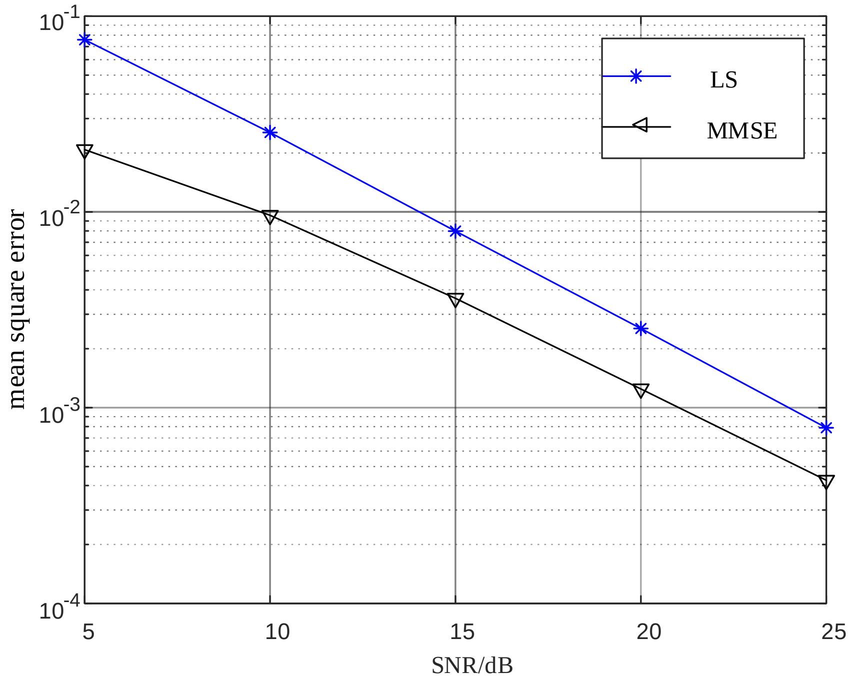

Figure 2. Comparison of mean square error between LS algorithm and MMSE algorithm

It can be seen from figure 2 that the performance of MMSE algorithm is better than LS algorithm, but the complexity of MMSE algorithm increases exponentially with the increase of sampling points, and the channel correlation value [7] is needed to know, which is difficult to get in actual hardware implementation. Therefore, this paper adopts the channel estimation algorithm based on LS algorithm.

In the OFDM system, there are two long training sequence with the same symbolic content, and the two long training sequences have the same symbol content, because the sum of two statistically independent noise samples divided by 2 is equivalent to half the variation of a single noise sample. Therefore, the average of the two can be taken to improve the quality of channel estimation, which is usually called the average-based LS algorithm (Ave-LS)[8]. In this paper, according to the characteristics of wideband micro-power system, the Ave-LS algorithm algorithm is improved, so that the improved algorithm is more applicable while improving the channel estimation performance. In this paper, the improved algorithm is called LS-A algorithm.

The LS-A algorithm utilizes the characteristics that the preamble is all 1 and the synchronization code is all 0. The 16-bit preamble and the synchronization code symbols are respectively taken, and then averaged and sent to the channel estimation module. The channel estimation values $\hat{\boldsymbol{H}}_{\mathrm{LS1}}$ and $\hat{\boldsymbol{H}}_{\mathrm{LS0}}$ are obtained through the preambles and synchronization codes after the channel estimation module, then the $\hat{\boldsymbol{H}}_{\mathrm{LS0}}$ and $\hat{\boldsymbol{H}}_{\mathrm{LS0}}$ are added together and averaged to further improve the quality of channel estimation. The calculation formula is:

$$R_{\mathrm{A1}} = \frac{R_{1,0} + R_{1,1} + \cdots + R_{1,14} + R_{1,15}}{16} \tag{8}$$

$$R_{\mathrm{A0}} = \frac{R_{0,0} + R_{0,1} + \cdots + R_{0,14} + R_{0,15}}{16} \tag{9}$$

$$\hat{\boldsymbol{H}}_{\mathrm{LS}} = \frac{\hat{\boldsymbol{H}}_{\mathrm{LS1}} + \hat{\boldsymbol{H}}_{\mathrm{LS0}}}{2} \tag{10}$$

Where $R_{0,i}, R_{1,i}, i \in \{0,1,\cdots 15\}$ is the received preambles and synchronization code, respectively. R_{A1} and R_{A1} respectively represent the average value of received preambles and synchronous codes, $\hat{\boldsymbol{H}}_{\mathrm{LS1}}$ and $\hat{\boldsymbol{H}}_{\mathrm{LS0}}$ respectively represent the estimated channel frequency response obtained by all 1 and all 0 sequences. The comparison results of the mean square error obtained by performance simulation of the LS channel estimation algorithm and the Ave-LS algorithm and the proposed LS-A algorithm are shown in Fig. 3. It can be seen from the figure that the performance of the LS-A algorithm is significantly better than that of the LS algorithm, and the performance is also improved relative to the Ave-LS algorithm (using only the preambles for channel estimation).

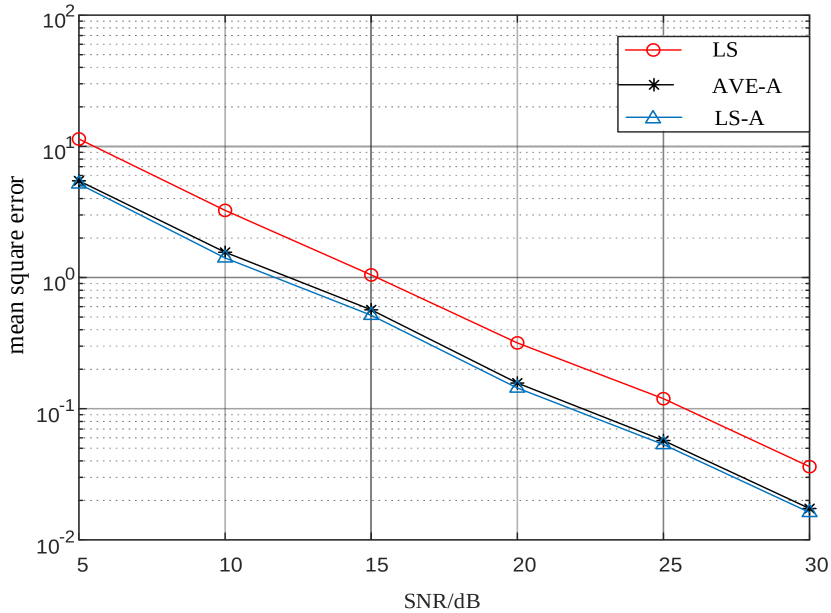

Figure 3. Comparison of mean square error between ls-a algorithm and other algorithms

4. FPGA design and implementation of channel estimation algorithm

4.1. Block diagram of system structure

Figure 4 shows the overall flow chart of the wideband micro-power system from the sender end to the receiver. The data flow is sent to the receiver through complex wireless channels after coding and other operations at the sender. The channel estimation at the receiver is the main content of this paper.

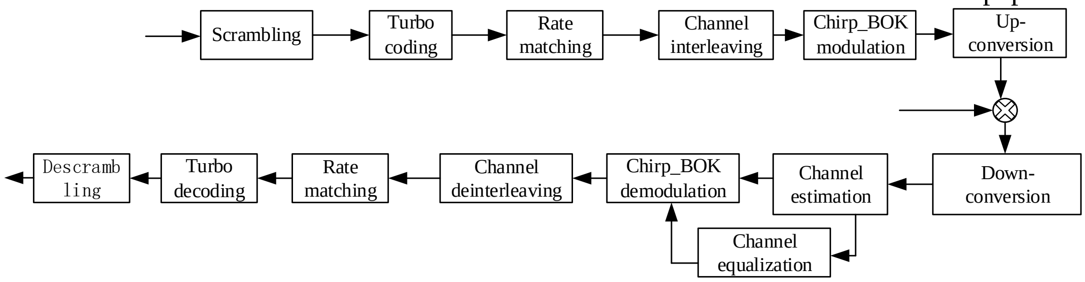

Figure 4. Overall flow chart of wideband micro-power system

4.2. block diagram of channel estimation implementation

The hardware implementation structure of channel estimation and equalization module in the frequency domain is shown in figure 5. It can be divided into four parts: training sequence extraction (here all 1 and all 0 sequences are collectively referred to as training sequences), energy calculation, channel estimation and channel equalization.

When the serial input data arrives, the two training sequences are extracted, and the average values of the two different training sequences are respectively obtained, and simultaneously sent to the energy calculation module and the channel estimation module. The energy calculation module is responsible for estimating the amount of amplitude change caused by the channel, while the channel estimation module performs correlation processing on the received training sequence and the locally sampled training sequence to obtain two channel estimation values, and averages the obtained two channel estimation values.

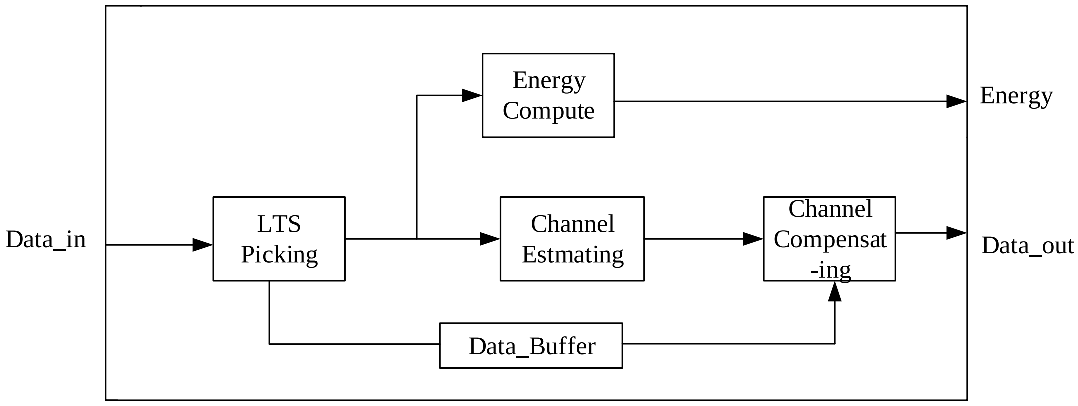

Figure 5. The hardware block diagram of channel estimation and equalization

4.3. The implementation of channel estimation module

The first part of channel estimation module is training sequence extraction, which is mainly responsible for the extraction and storage of two training sequences. When the preambles or synchronization codes is detected, the data is added to the data in the register and stored in the register. After 16 times of accumulation, the data is shifted to the right by 4 bits and sent to the energy calculation module and the channel estimation module. Because the number of preambles and synchronization codes is more than 16, a counter is used to determine the flag bit in the implementation process, and when the flag bit is high, the data will be output. When the data is detected, it is directly sent to the channel equalization module for compensation processing.

The FPGA hardware implementation scheme of LS-A channel estimation algorithm is selected by the simulation comparison of the previous channel estimation algorithm. Due to the algorithm requires division, which requires a complex division structure in the FPGA implementation process and it is too difficult to implement in the hardware circuit, so the algorithm is simplified as follows [9-10]

$$\hat{\boldsymbol{H}}_{\mathrm{LS}} = \frac{R_{\mathrm{A}}}{L_{\mathrm{LTS}}} = \frac{R_{\mathrm{A}} \times L^{*}_{\mathrm{LTS}}}{\left\| L_{\mathrm{LTS}} \right\|} \tag{11}$$

Where, R_A represents the received preambles or synchronization code, L_{LTS} represents a known preambles or synchronous code. Due to Chirp signal is a signal with constant amplitude, so the denominator of the above equation is a constant value. In the wideband micro-power system, the amplitude of Chirp signal is identical to 1, so

$$\hat{\boldsymbol{H}}_{\mathrm{LS}} = R_{\mathrm{A}} \times L^{*}_{\mathrm{LTS}} \tag{12}$$

Four multipliers are needed if the minimum delay parallel structure is adopted for channel estimation module calculation. In this paper, a method of calculating complex numbers is proposed by using formula transformation, which reduces the number of multipliers used.

The implementation of complex data multiplication can usually be expressed as

$$Z_{\mathrm{r}} + Z_{\mathrm{i}} j = (A_{\mathrm{r}} + A_{\mathrm{i}} j) \times (B_{\mathrm{r}} + B_{\mathrm{i}} j) \tag{13}$$

$$\Rightarrow Z_{\mathrm{r}} = A_{\mathrm{r}} B_{\mathrm{r}} - A_{\mathrm{i}} B_{\mathrm{i}}, Z_{\mathrm{i}} = A_{\mathrm{r}} B_{\mathrm{i}} - A_{\mathrm{i}} B_{\mathrm{r}} \tag{14}$$

Now transforming the above equation as follows

$$\begin{aligned} Z_{\mathrm{r}} &= A_{\mathrm{r}} B_{\mathrm{r}} - A_{\mathrm{i}} B_{\mathrm{i}} \\ &= A_{\mathrm{r}} (B_{\mathrm{r}} + B_{\mathrm{i}}) - B_{\mathrm{r}} (A_{\mathrm{r}} + A_{\mathrm{i}}) \end{aligned} \tag{15}$$

Where, A and B are the input of the multiplier, Z represents the output of the multiplier, and A_{r} and A_{i} represent the real and imaginary parts of A, B_{r} and B_{i}, Z_{r} and Z_{i} are the same . At this time, only three multipliers and some additional addition and subtraction operations are needed to realize the multiplication operation of complex data, reducing the use of resources. The improved structure is shown in figure 6.

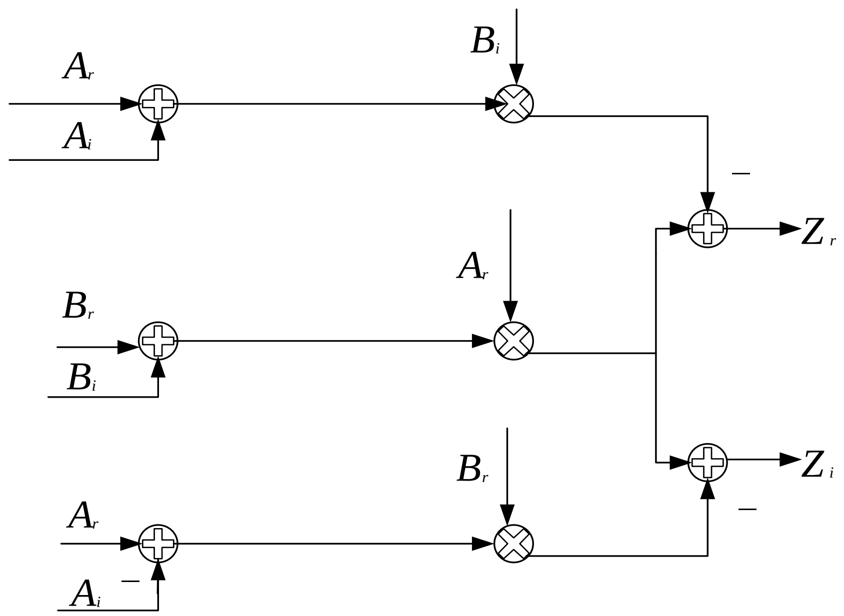

Figure 6. Block diagram of complex multiplication after formula transformation

The real and imaginary parts of the received training sequence data and the local conjugate signal are multiplied as shown in figure 6, the real and imaginary parts of the 32 bit width channel estimation results are obtained respectively, then 16 bits of valid data are intercepted and spliced into channel estimation results. Finally, the channel frequencies estimated by the all-one sequence and the all-zero sequence are averaged. After the average channel frequency response calculation is completed, the top layer module sends an output enable signal to the data buffer module.The channel equalization is performed by sending the data to be equalized and the conjugate of the channel frequency response to the channel equalization module, the concrete hardware implementation is completed by a complex multiplier. The energy calculation module is responsible for compensating the fading of signal amplitude caused by wireless channel.

5. System Simulation and Results Analysis

In this paper takes the virtex-5 series development board of Xilinx company as the hardware platform, and adopts Verilog HDL as the hardware description language under the development software of Xilinx ISE Design Suite 14.7. The module is simulated and verified under Mentor's modelsimse-64 10.4 software platform. After the whole module of the channel estimation is integrated, the logical resource comprehensive map shown in the following figure is obtained. As can be seen from the figure, the occupied resources in the implementation process are small and meets the the pre-design expectations.

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	534	12,480	4%	
Number used as Flip Flops	534			
Number of Slice LUTs	614	12,480	4%	
Number used as logic	614	12,480	4%	
Number using O6 output only	542			
Number using O5 and O6	72			
Number of route-thrus	27			
Number using O5 output only	27			
Number of occupied Slices	242	3,120	7%	
Number of LUT Flip Flop pairs used	783			
Number with an unused Flip Flop	249	783	31%	
Number with an unused LUT	169	783	21%	
Number of fully used LUT-FF pairs	365	783	46%	
Number of unique control sets	9			
Number of slice register sites lost to control set restrictions	18	12,480	1%	

Figure 7. Occupation of FPGA logic resources

The RTL diagram of the design module compiled by ISE Design Suite 14.7 is shown in Figure 8. This part is divided into three modules as sequence extraction, channel estimation and channel equalization modules.

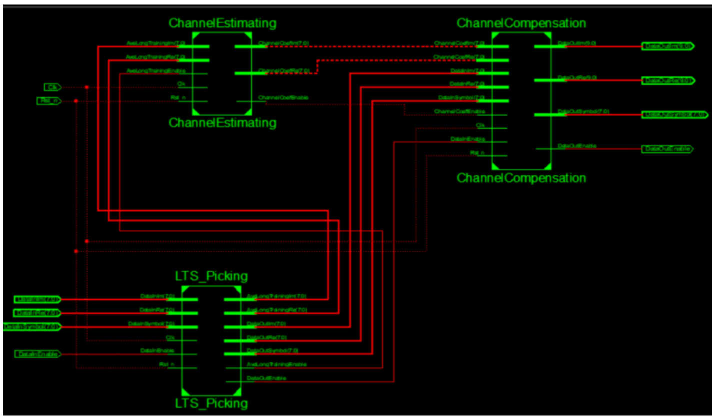

Figure 8.RTL diagram of the whole module

According to the idea of module Design, we compilte the ISE Design Suite 14.7 software with Verilog HDL language, and write testbench for the Design module and simulate it in modelsimse-64 10.4 software. The simulation results are shown in figure 9.

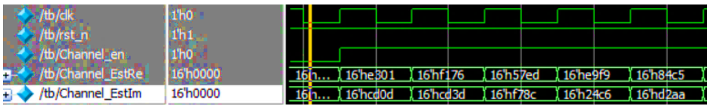

Figure 9. Modelsim simulation diagram

In Figure 9, Channel_EstRe and Channel_EstIm is the real and imaginary part of the estimated output value of the data after the channel estimation module, and Channel_en is the data output enable. The Channel_EstRe and Channel_EstIm outputs are valid only when Channel_en is 1. As shown in FIG. 9, when Channel_en is 0, the Channel_EstRe and Channel_EstIm outputs are 0.

6. Conclusion

Since the wireless channel has a great influence on the receiver, the channel estimation algorithm is the key to improving the communication quality in the wideband micropower wireless communication system. In this paper, under the wideband micropower system, the Ave-LS algorithm is improved according to the frame structure of the system. The improved algorithm improves the performance of the algorithm with a small amount of computation and is implemented on the FPGA. The results show that the channel estimation module is reasonable in design and has high performance, meeting the requirements of the system.

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