Timer Specs

Introduction

The timer module is a submodule under the LTSSM block, it is only connected to the state machine as shown in the figure below:

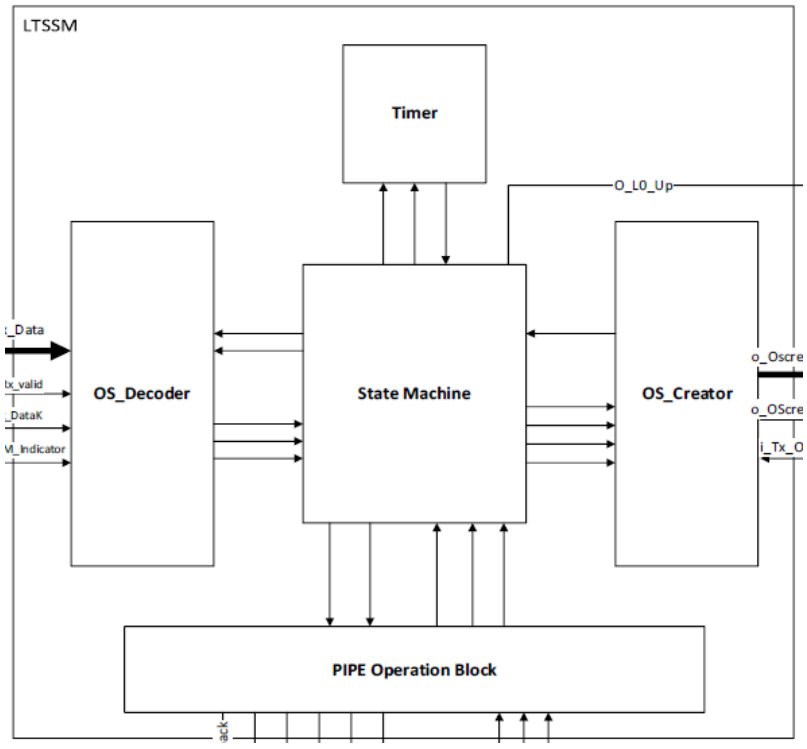

Figure 1: LTSSM Implementation

Signals

Name	Direction	Description
i_time_out_value [22:0]	Input	**Input from State machine:** Time, we need to reach
i_clk	Input	Clock
i_start	Input	**Input from State machine** To start count the time - Start = 1, Start count - Start = 0, Stop count and restart all the time data (when we start again, we will start from 0)
i_resetn	Input	Negative edge reset
o_time_out	Output	**Output to State machine** - Time Out = 1, when we reach the time needed - Time Out = 0, when we still count the time needed

Block Diagram

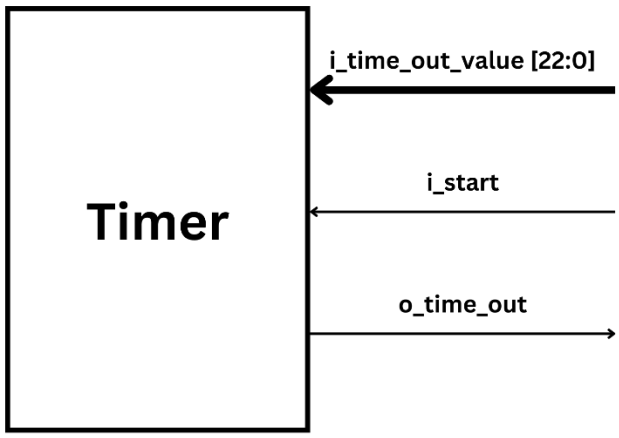

Figure 2: Timer Implementation

Functionality

The main function of timer is to provide the time out signal to the StateMachine according to the given timeout value. So basically, it takes timeout value from the StateMachine, and when the start signal is asserted, it starts counting with each clock period until the timeout value is reached then it asserts the timeout signal to the state machine.

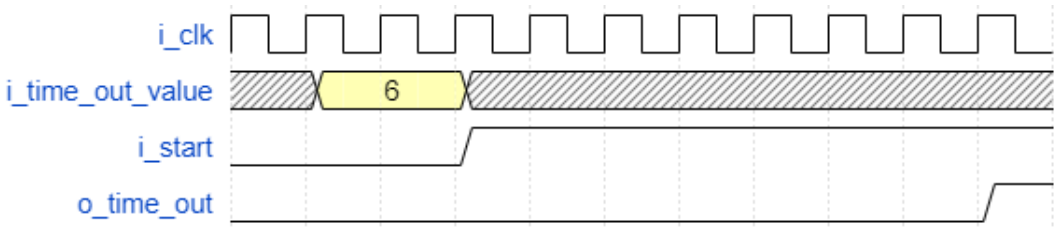

Figure 3: Wave Diagram Example