PIPE Operation Block Specs

Introduction

The PIPE Operation Block module is a submodule under the LTSSM block. It is the connection between the LTSSM and the PHY layer.

The upper signals are connected to the State Machine while the lower signals are connected to a PHY module given by Mentor Graphics which we don't have access to.

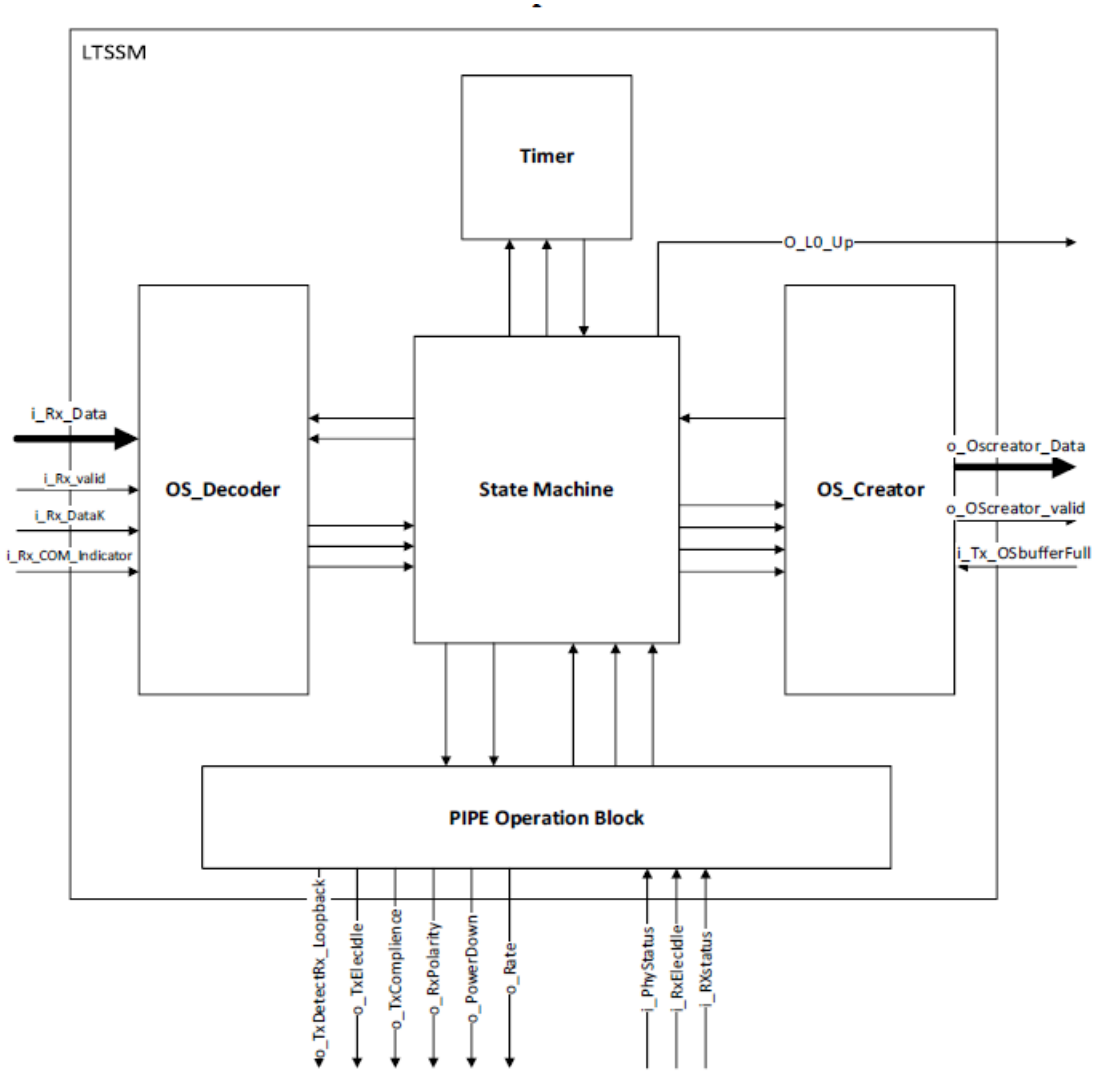


Figure 1: LTSSM Implementation

Signals

Note: (*) means that this signal comes from PIPE V3.0 standard.

<table>
<tr><th>Name</th><th>Direction</th><th>Source/ destinaion</th><th>Description</th></tr>
<tr><td>i_LTSSMState [4:0]</td><td>Input</td><td>State Machine</td><td>Inputs from State machine
Indicate the current state</td></tr>
<tr><td>i_PhyStatus*</td><td>Input</td><td>PHY Layer</td><td>Inputs from PHY
Used to communicate completion of several PHY functions including stable PCLK after Reset_n deassertion, power management state transitions, rate change, and receiver detection.</td></tr>
<tr><td>i_RxElecIdle*</td><td>Input</td><td>PHY Layer</td><td>Inputs from PHY
Indicates receiver detection of an electrical idle.</td></tr>
<tr><td>i_RxStatus* [2:0]</td><td>Input</td><td>PHY Layer</td><td>Inputs from PHY
Encodes receiver status and error codes for the received data stream when receiving data.

<table><tr><th>Value</th><th>Description</th></tr><tr><td>000</td><td>Received data OK</td></tr><tr><td>001</td><td>1 SKP added</td></tr><tr><td>010</td><td>A SKP removed</td></tr><tr><td>011</td><td>Receiver detected</td></tr><tr><td>100</td><td>Both 8B/10B decode error and receive disparity error</td></tr><tr><td>101</td><td>Elastic buffer overflow</td></tr><tr><td>110</td><td>Elastic buffer under flow</td></tr><tr><td>111</td><td>Receive disparity error</td></tr></table></td></tr>
<tr><td>o_TxDetectRx_loopback*</td><td>Output</td><td>PHY Layer</td><td>Output to PHY
Used to tell the PHY to begin a receiver detection operation or to begin loopback</td></tr>
<tr><td>o_TxElecIdle*</td><td>Output</td><td>PHY Layer</td><td>Output to PHY
Tells PHY that the transmitter is electrically idle</td></tr>
<tr><td>o_TxCompliance*</td><td>Output</td><td>PHY Layer</td><td>Output to PHY
Sets the running disparity to negative. Used when transmitting the PCI Express compliance pattern</td></tr>
<tr><td>o_RxPolarity*</td><td>Output</td><td>PHY Layer</td><td>Output to PHY
Tells PHY to do a polarity inversion on the received data.</td></tr>
<tr><td>o_PowerDown* [1:0]</td><td>Output</td><td>PHY Layer</td><td>Output to PHY
<table><tr><th>Value</th><th>Description</th></tr><tr><td>00</td><td>L0, normal operation</td></tr><tr><td>01</td><td>L0s, low recovery power saving state</td></tr><tr><td>10</td><td>L1, long recovery power saving state</td></tr><tr><td>11</td><td>L2, lowest power state</td></tr></table></td></tr>
<tr><td>o_Rate*</td><td>Output</td><td>PHY Layer</td><td>Output to PHY
Control the link signaling rate.</td></tr>
</table>

o_LTSSM_UpLink	Output	State Machine	**Output to LTSSM** Indicates bit and symbol lock, ready to L0 state
o_LTSSM_RxElecIdle	Output	State Machine	**Output to LTSSM** Mirror the i_RxElecIdle coming from PHY to LTSSM
o_LTSSM_LaneDetected	Output	State Machine	**Output to LTSSM** Indicate successful detection of a receiver to LTSSM

Block Diagram

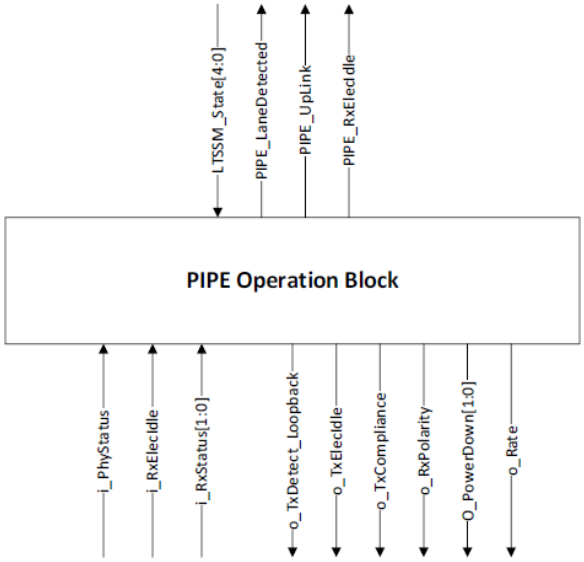
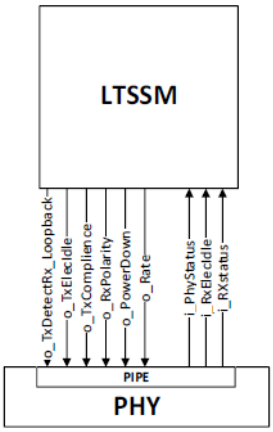


Figure 2: PIPE Operation block Implementation.

The upper signals are connected to the State Machine while the lower signals are connected to a PHY module given by Mentor Graphics which we don't have access to.

Functionality

- The main interface between the LTSSM and the PHY layer according to the PIPE standard.



- It is used to detect whether there's a receiver connected or not.

Theory of operation

It takes the state of LTSSM *i_LTSSM_State* as an input, when it is in the detect active, it checks the *i_PhyStatus* signal, if it is '1', it then checks the *i_RXstatus* signal and asserts the *o_LTSSM_LaneDetected* signal only if there's a receiver detected.

Otherwise, the *o_LTSSM_LaneDetected* signal is always '1' unless it is in the detect quite state.

Latency

It is a combinational block with no clock or reset signals; once any of the inputs change, the outputs change immediately.