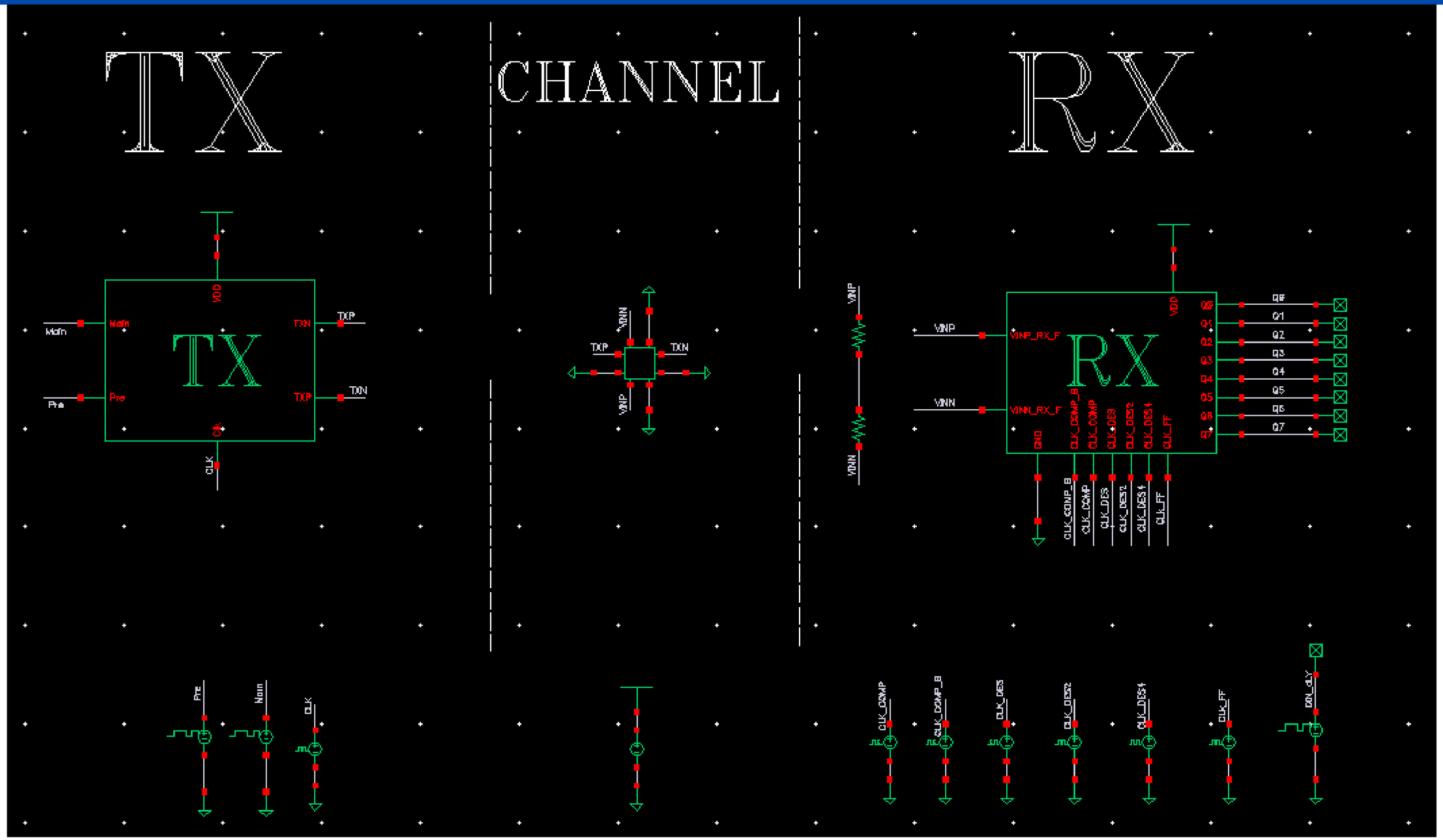
SerDes

TX-RX LINK SIGNALING

Design and Implementation of High-Speed Serial Link Transceiver
with Adaptive Terminatin and Equalization and Swing Control

TX-RX TOP LEVEL



TX LINK

OUR
TX BLOCKS

The TX consists of Serializer & Pre-driver, Voltage Mode Driver, and Feed-Forward Equalizer (FFE) to generate high-speed data with pre-distortion. Replica Driver and Verilog-A Controller are used for swing control, calibration, and programmability.

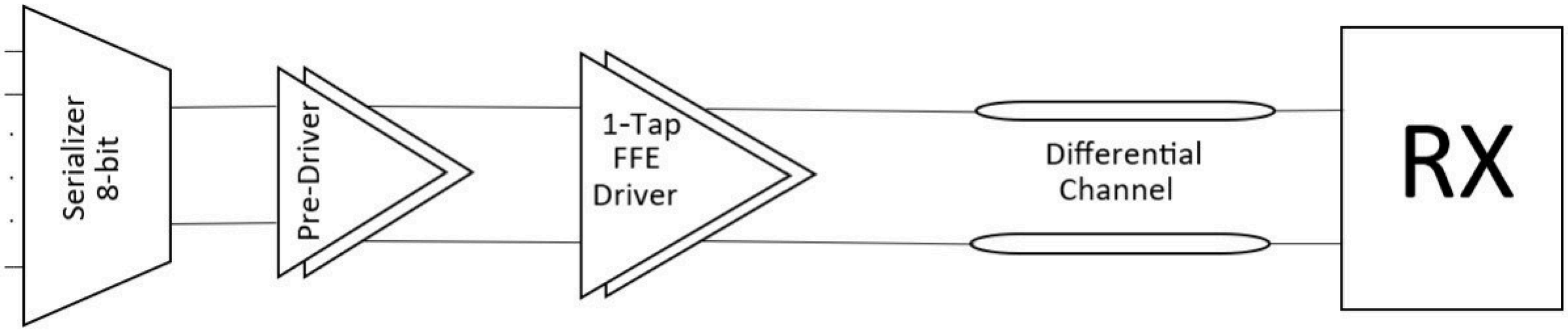
1. Parallel to Serial (Serializer)&Pre-Driver
2. Voltage Mode Driver (VM Driver)
3. Feed-Forward Equalizer (FFE)
4. Replica Driver
5. Verilog-A Controller

TX OVERVIEW

The Transmitter (TX) of the SerDes system converts parallel low-speed data into high-speed serial data and prepares it for transmission over the channel. It consists of three main stages:

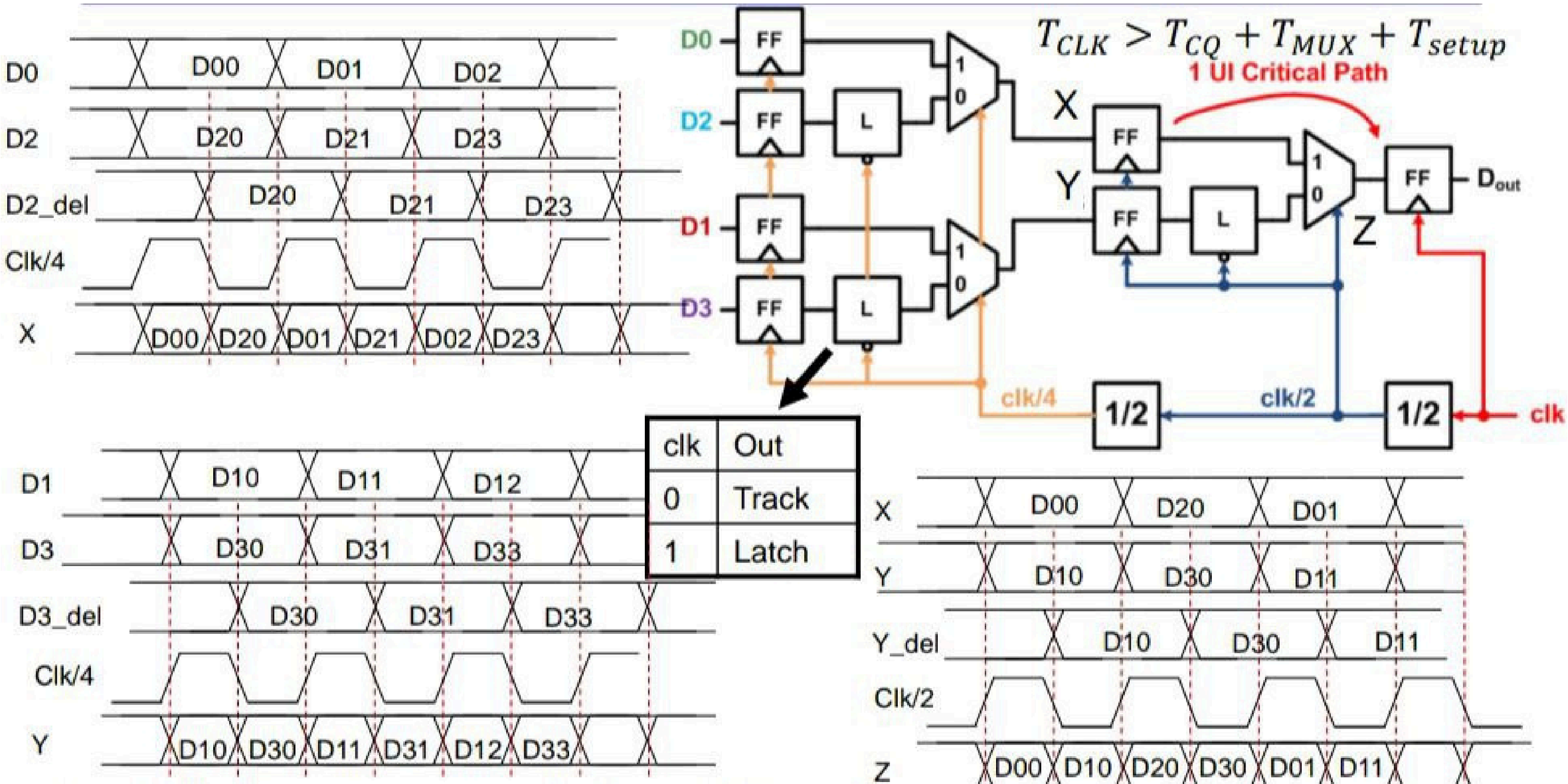
1. **Serializer – Converts 8-bit parallel input into 12 Gbps serial output.**
2. **Equalizer (FFE) – Pre-distorts the signal to cancel ISI and channel losses**
3. **Driver – A VM (Driver)-based driver with pre-driver stage and swing control to ensure strong, clean signaling with minimized EMI.**

TX LINE UP


Serializer
8-bit
Pre-Driver
1-Tap
FFE
Driver
Differential
Channel
RX

SERIALIZER

SERIALIZER OPERATION



clk	Out
0	Track
1	Latch

- Final Flip flop samples serial data at full rate → high speed sampler

TREE STRUCTURE

- The tree structure is the natural extension of the 2_1 Mux
- The idea is to group the input channels in pairs and multiplex
- each pair, reducing the number by a factor of two after each stage

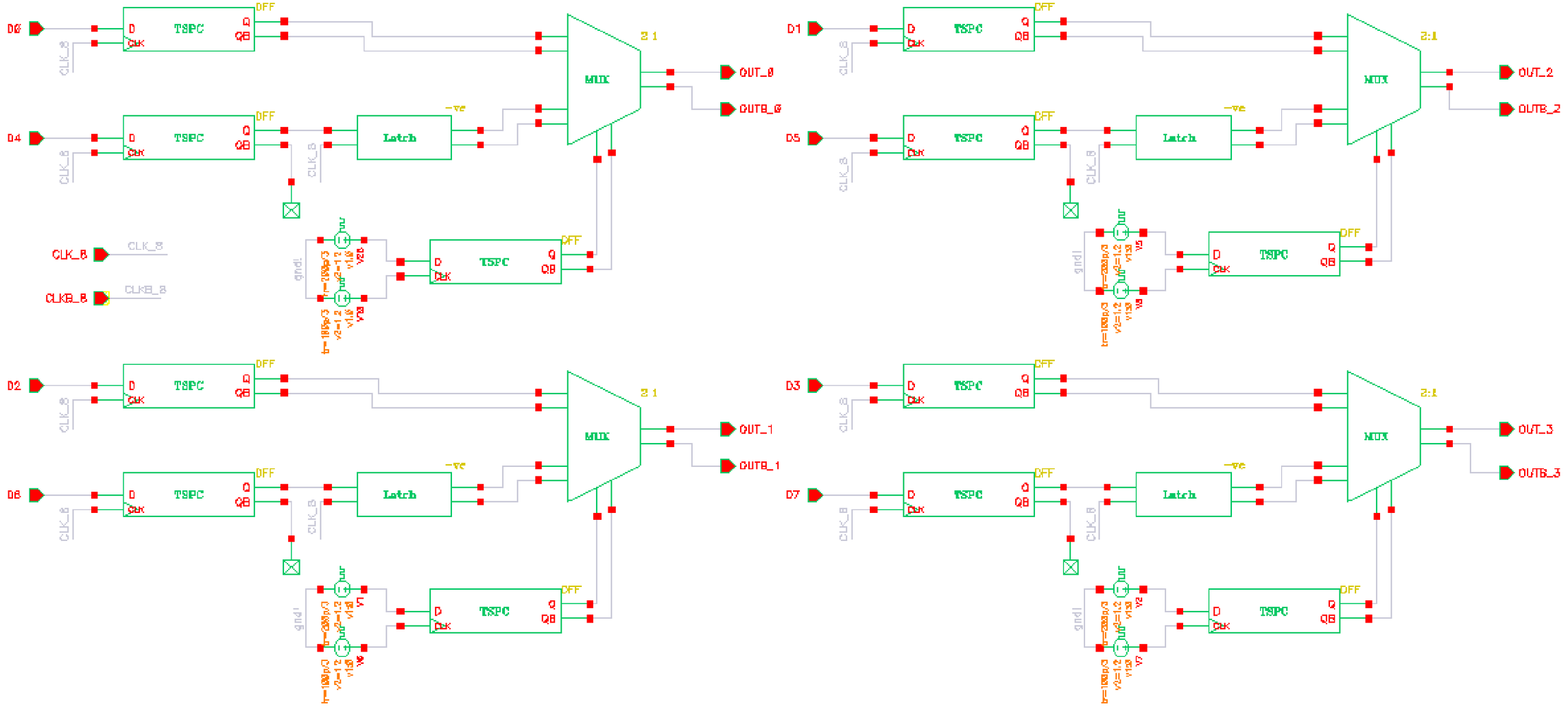
1 **Stage 1 is a 8:4 MUX driven by CLK/8**

2 **Stage 2 is a 4:2 MUX driven by CLK/4**

3 **Stage 3 is a 2:1 MUX driven by CLK/2**

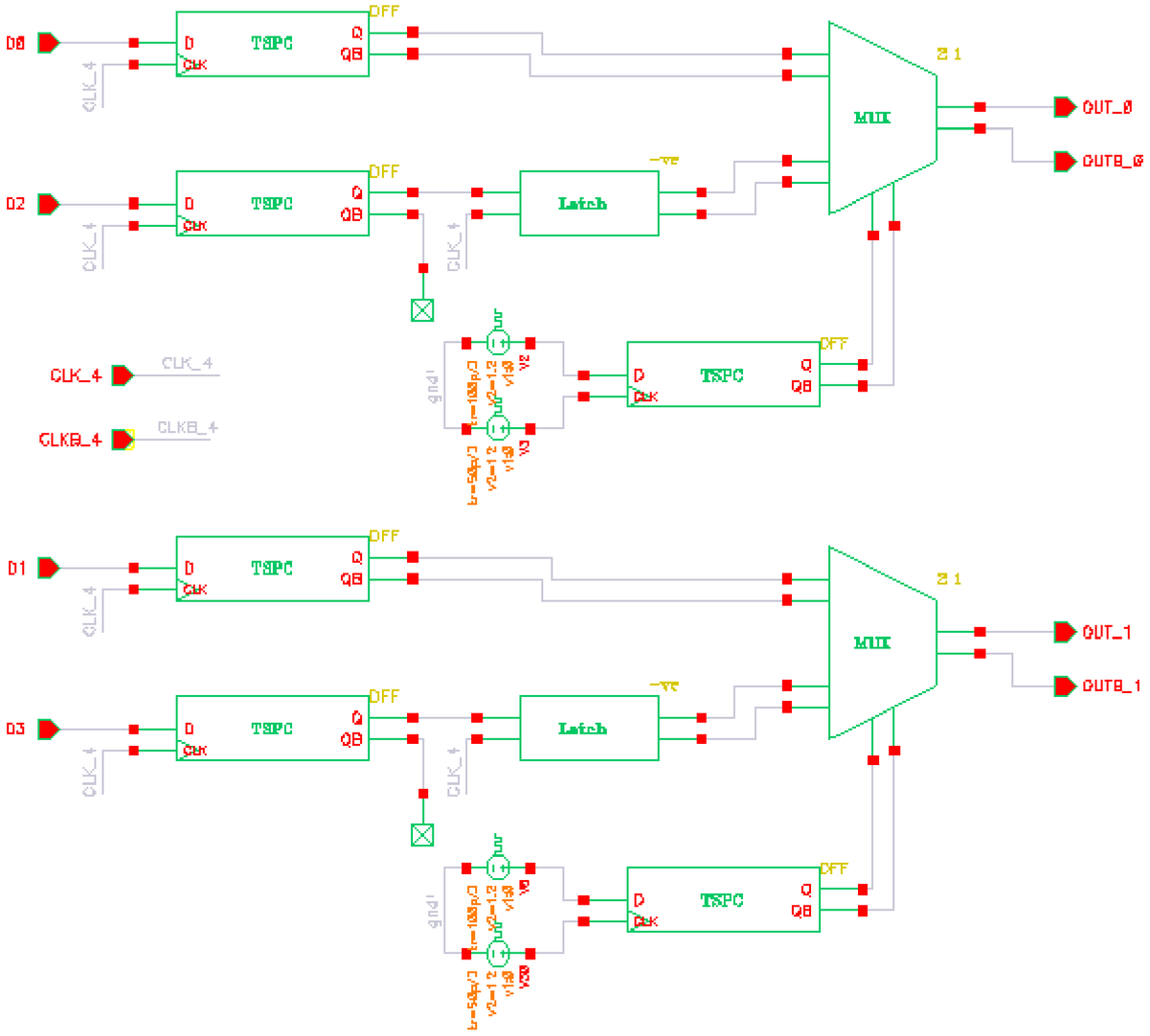
FIRST STAGE

MUX 8:4



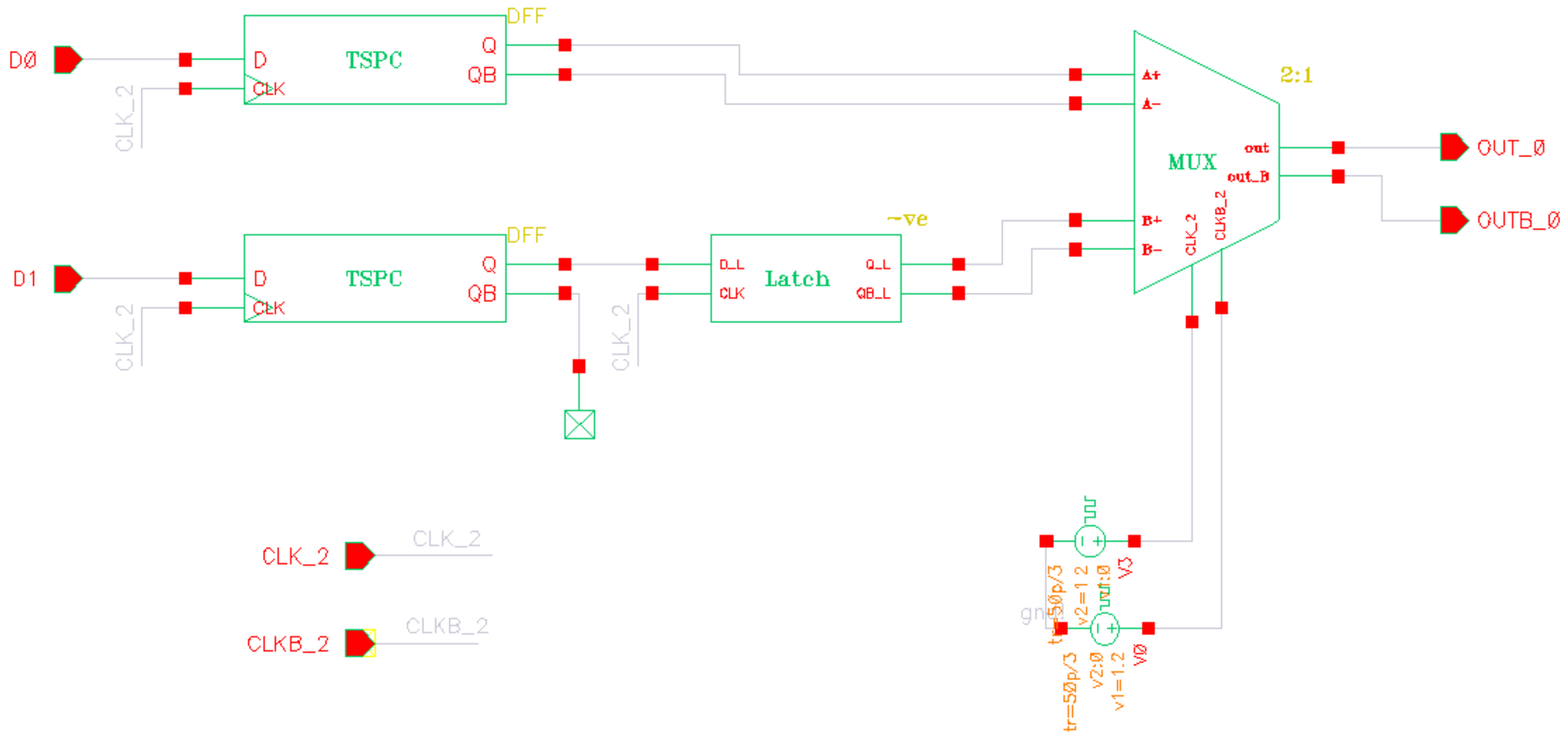
SECOND STAGE

MUX 4:2



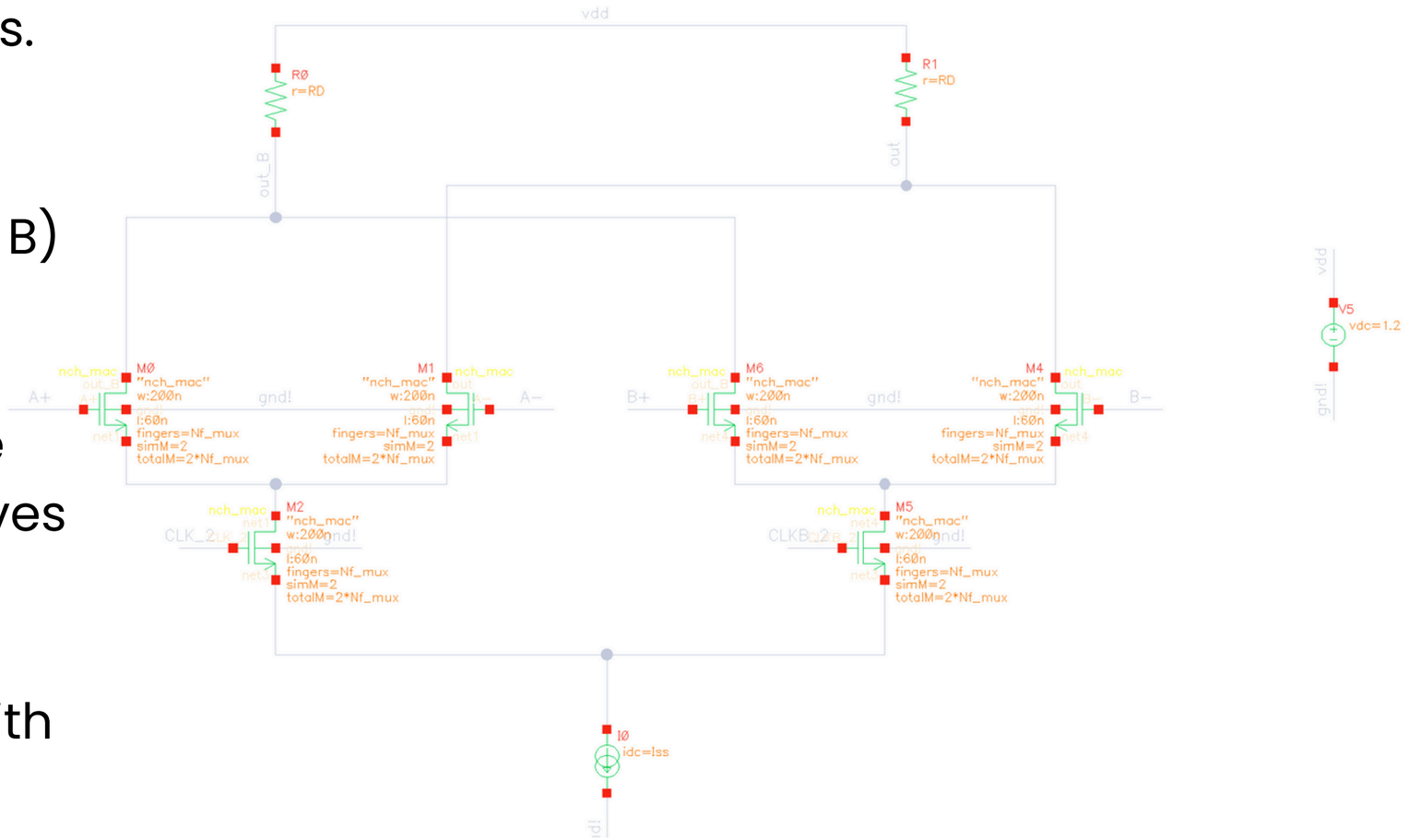
THERD STAGE

MUX 2:1



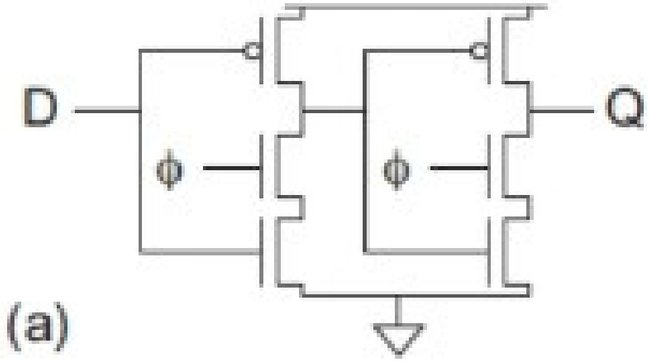
MUX 2:1

- CML circuits are commonly used in GHz-range high-speed multiplexers.
- Differential select signals (CLK and CLKB) determine which input (A or B) is connected to the output.
- When CLK = high, input A drives the output; when CLK = low, input B drives the output.
- CML offers high operating speed with constant power consumption, independent of frequency.

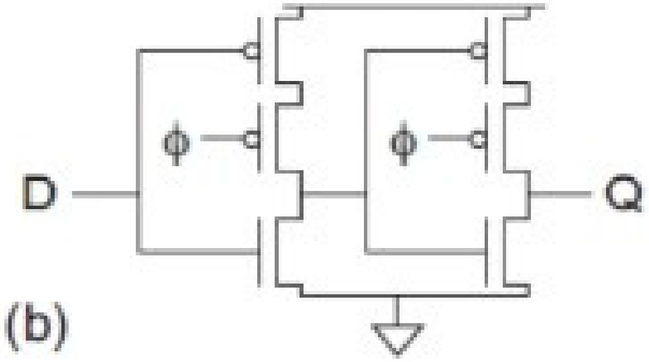


TSPC TOPOLOGY

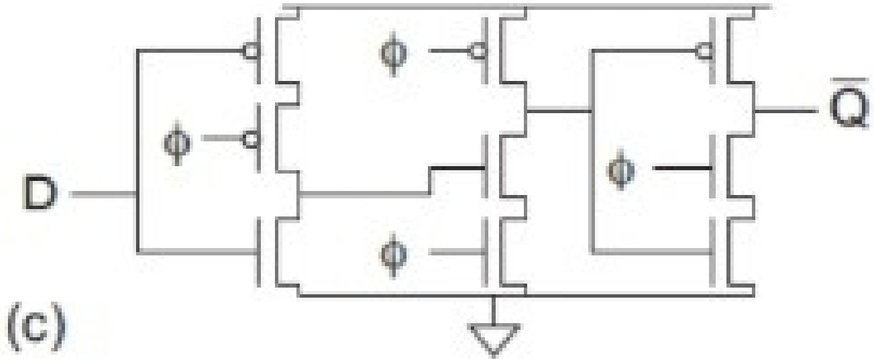
Positive Latch



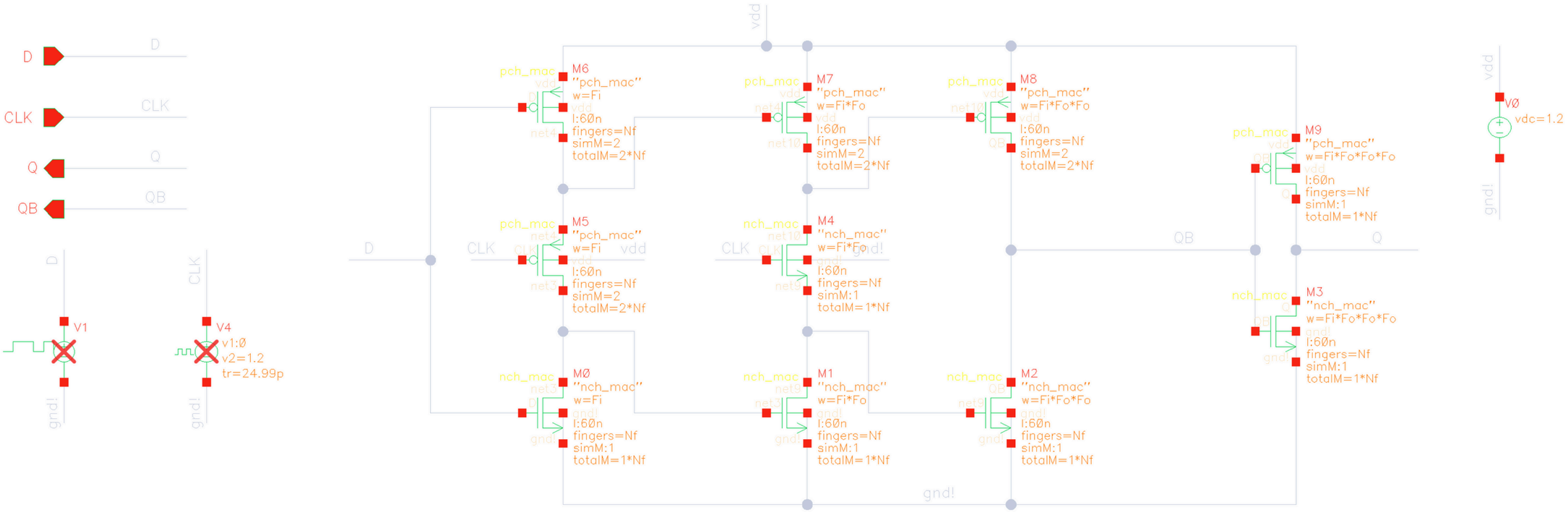
Negative Latch



D- flip flop

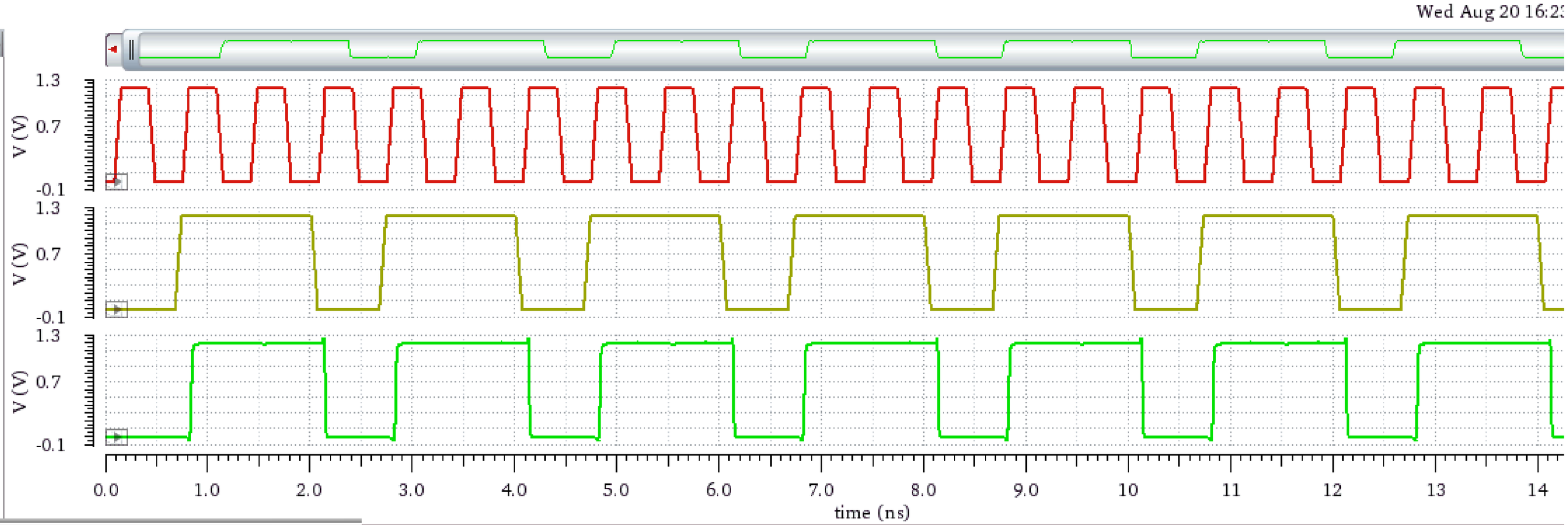


D-FF (TSPC)



- A True Single Phase Clocked (TSPC) can overcome the problem caused by clock overlap. as it only need one phase of CLK
- when the CLK is high, the latch is in the transparent mode, and corresponds to two cascaded inverters. When the CLK is low on the other hand, both inverters are off and the latch is in hold mode

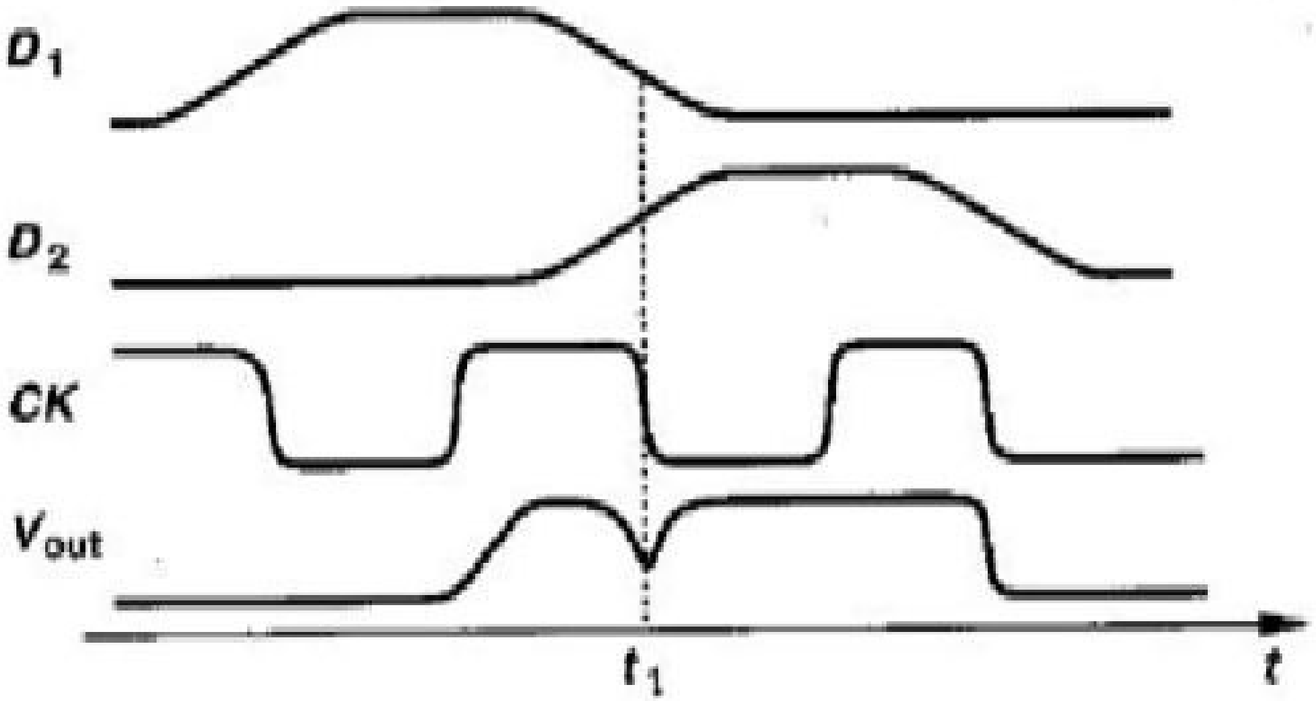
D-FF TEST



Output	Nominal
t_setup	73.33p
t_dq	127.7p
t_cq	54.35p

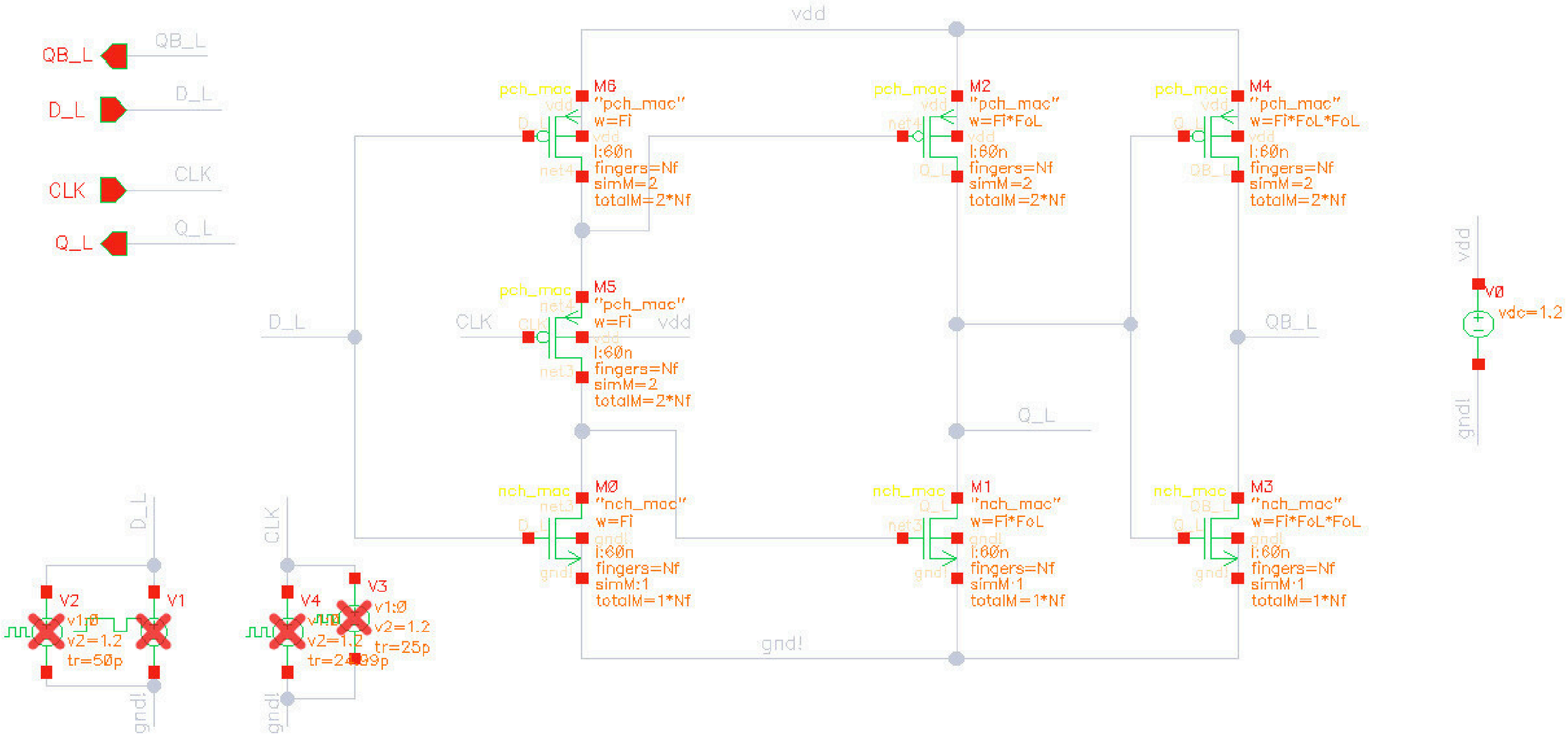
CLK D Q

LATCH

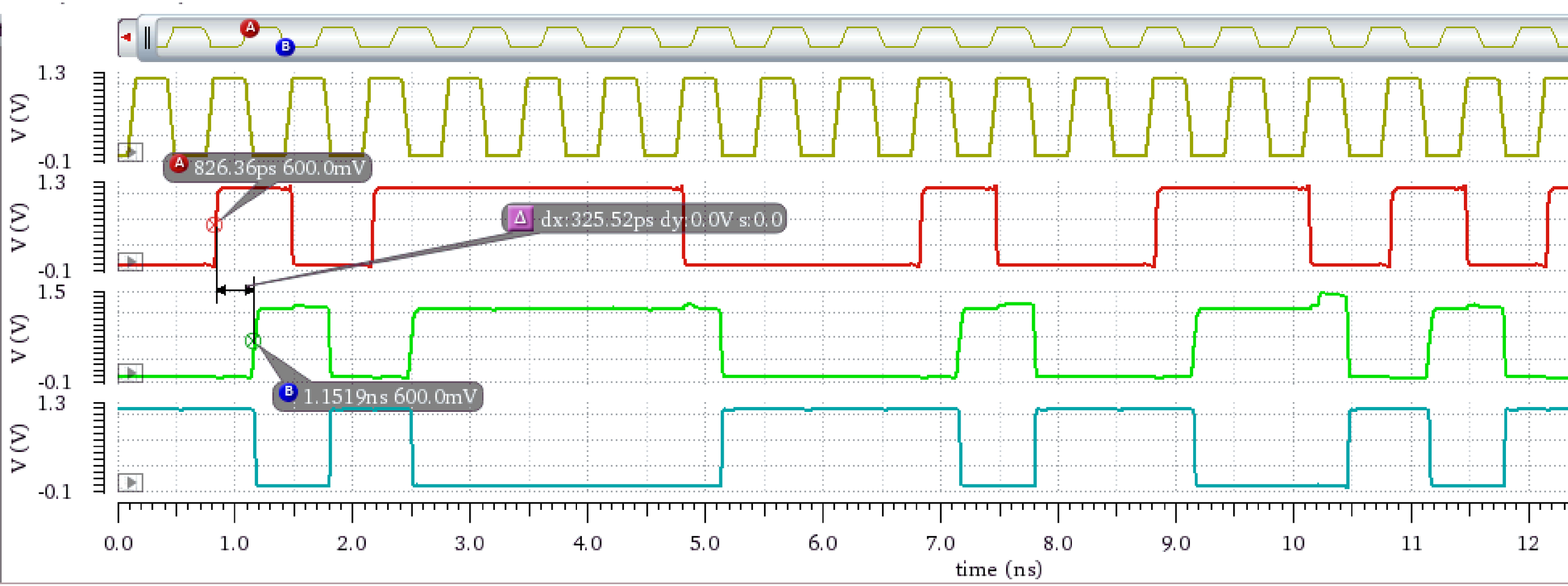


- The above analysis suggests that one of the input streams must be offset with respect to the other in the same domain so to avoid simultaneously transitions in both inputs in the MUX. The optimum value of the offset is half a clock period, obtained by introducing a latch in one of data paths

TSPC LATCH


QB_L
D_L
CLK
Q_L
vdd
gnd!
M6
"pch_mac"
w=Fi
l:60n
fingers=Nf
simM=2
totalM=2*Nf
M2
"pch_mac"
w=Fi*FoL
l:60n
fingers=Nf
simM=2
totalM=2*Nf
M4
"pch_mac"
w=Fi*FoL*FoL
l:60n
fingers=Nf
simM=2
totalM=2*Nf
M5
"pch_mac"
w=Fi
l:60n
fingers=Nf
simM=2
totalM=2*Nf
M0
"nch_mac"
w=Fi
l:60n
fingers=Nf
simM:1
totalM=1*Nf
M1
"nch_mac"
w=Fi*FoL
l:60n
fingers=Nf
simM:1
totalM=1*Nf
M3
"nch_mac"
w=Fi*FoL*FoL
l:60n
fingers=Nf
simM:1
totalM=1*Nf
V0
vdc=1.2
V1
V2
v1:0
v2=1.2
tr=50p
V3
v1:0
v2=1.2
tr=25p
V4
v1:0
v2=1.2
tr=24999p

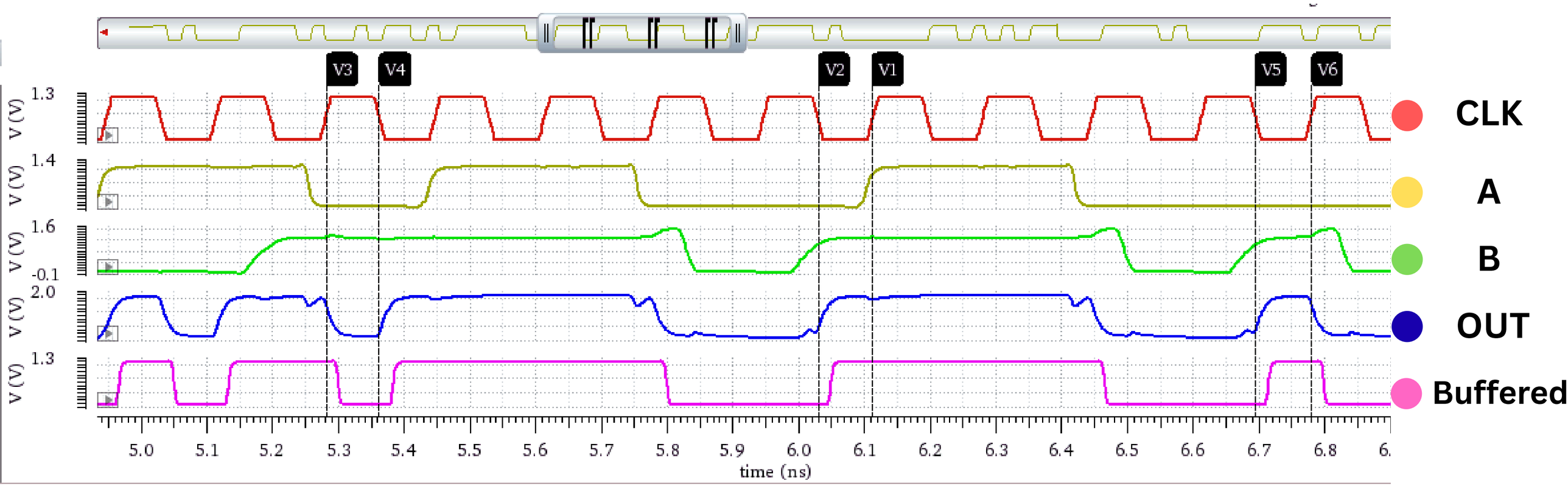
LATCH TEST



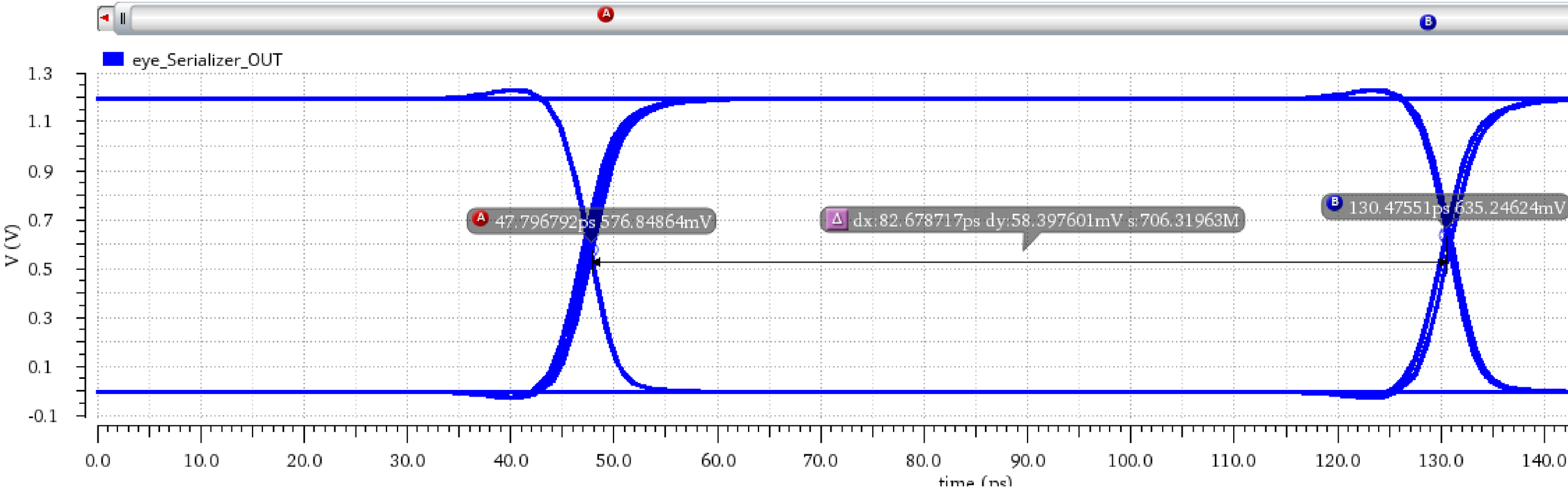
CLK D Q QB

"The output Q lags the input D by the CLK pulse width duration."

SER RESULT (MUX 2:1)



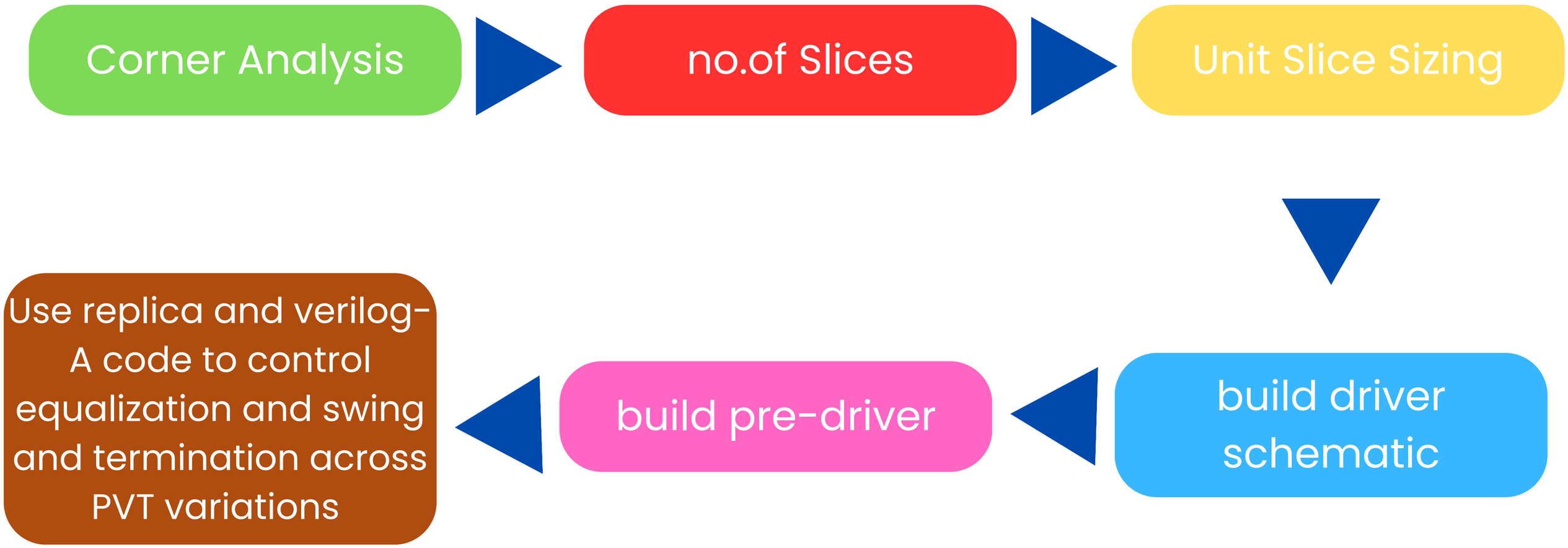
SER OUTPUT EYE



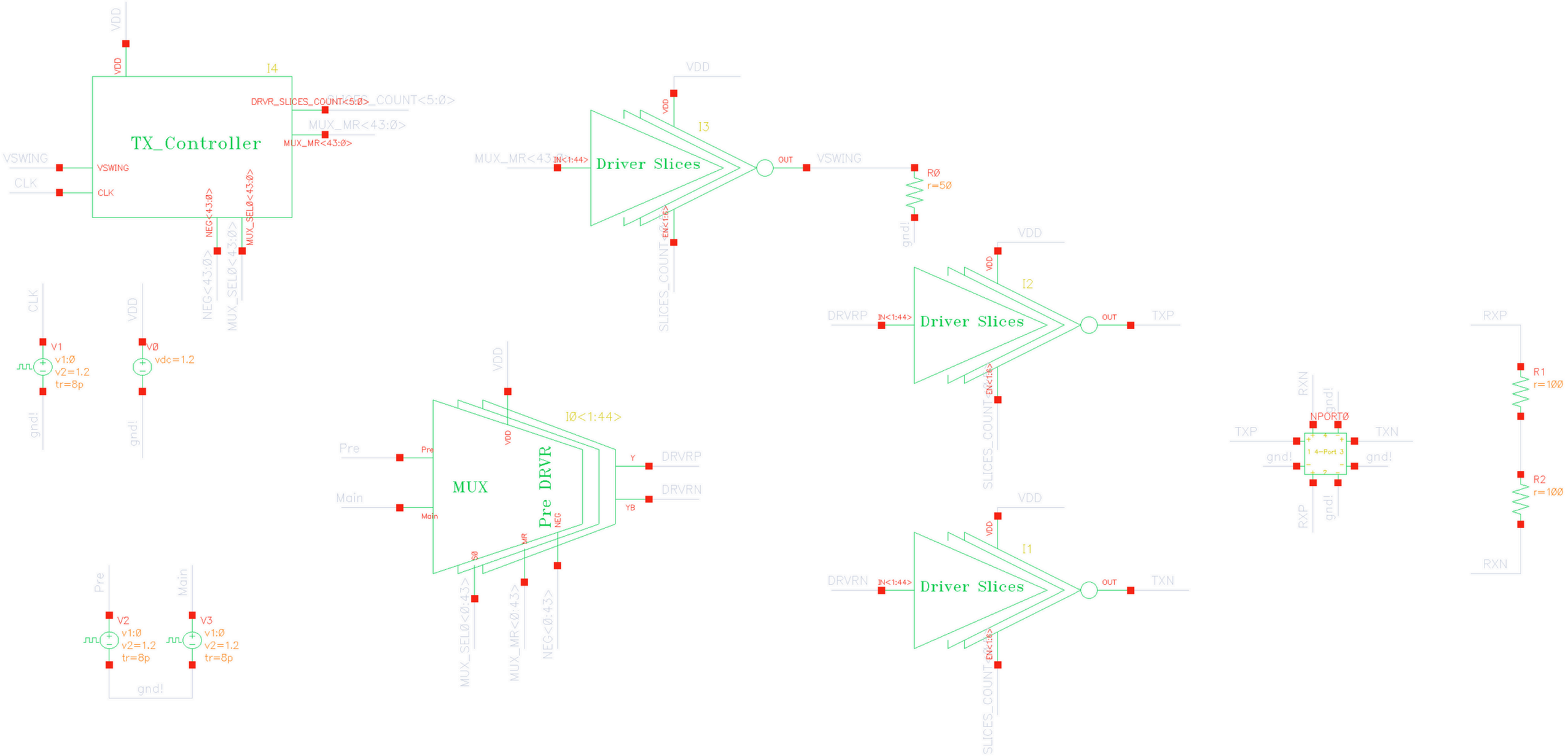
Horizontal Open Eye of 82.7psec

PRE DRVR &
DRIVER WITH 1-TAP FFE

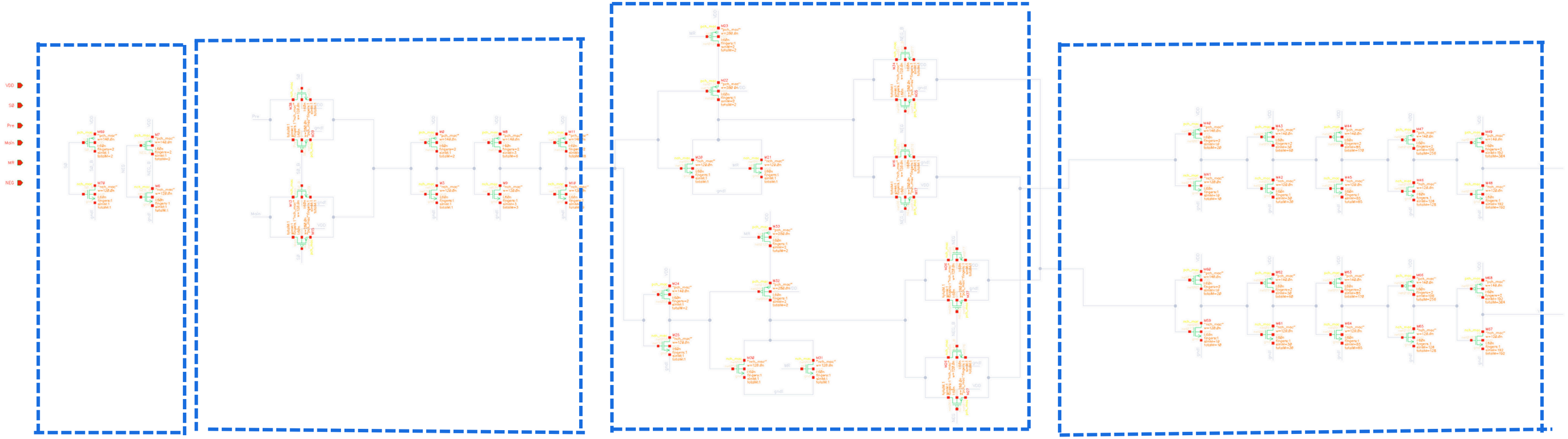
DESIGN FLOW


Corner Analysis
no.of Slices
Unit Slice Sizing
build driver schematic
build pre-driver
Use replica and verilog-A code to control equalization and swing and termination across PVT variations

DRVR TOP LEVEL



MUX & PRE_DRIVR



Internal signals gen

MUX

- MUX stage meant by choosing one out of two input using transmission gates followed by buffering (FO3)

Logic

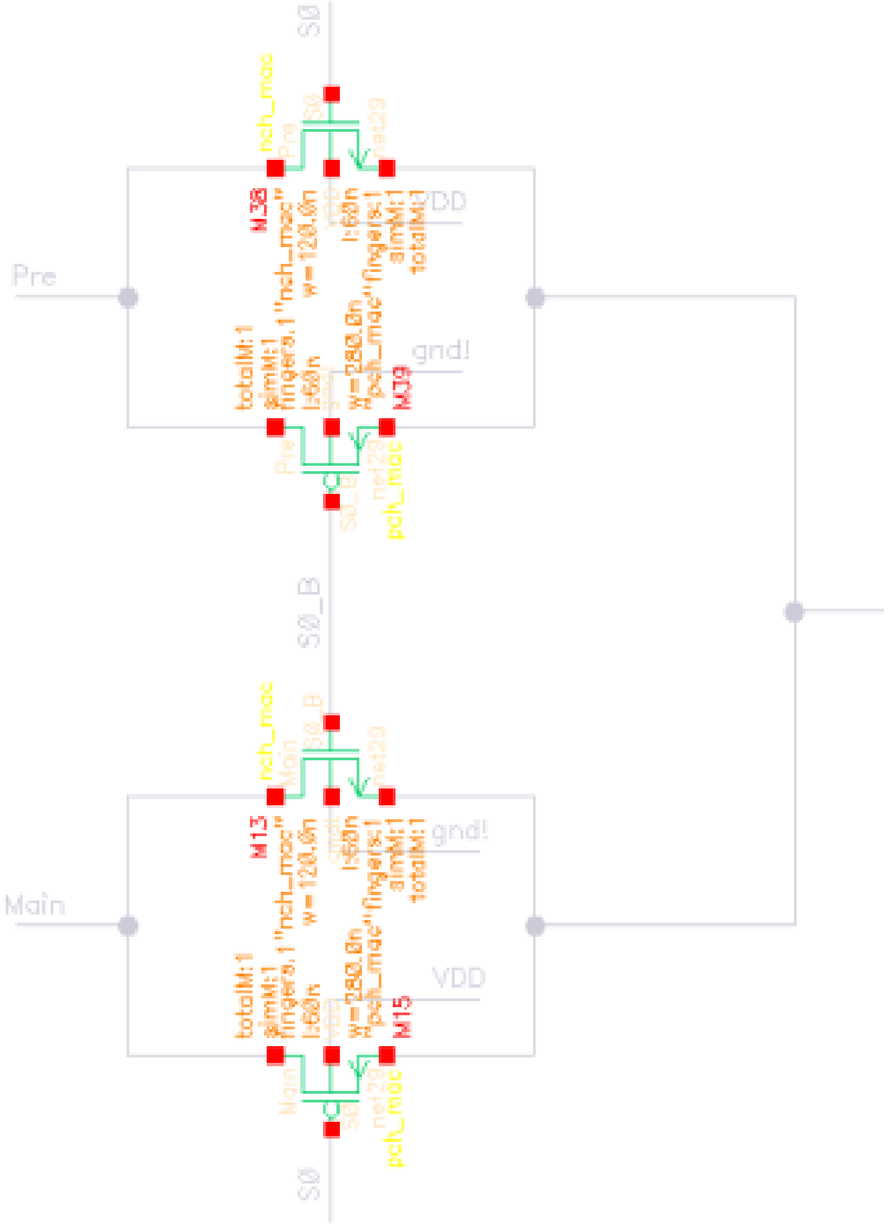
Buffering

MUX & PRE_DRIVR

MUX

- The MUX stage is designed to select one input from multiple available inputs using transmission gate switches. The selected signal is then buffered through FO3 (Fan-Out 3) stages to provide adequate drive strength, as illustrated in the truth table below:"

S0	Y
0	D0 (Pre)
1	D1 (Main)

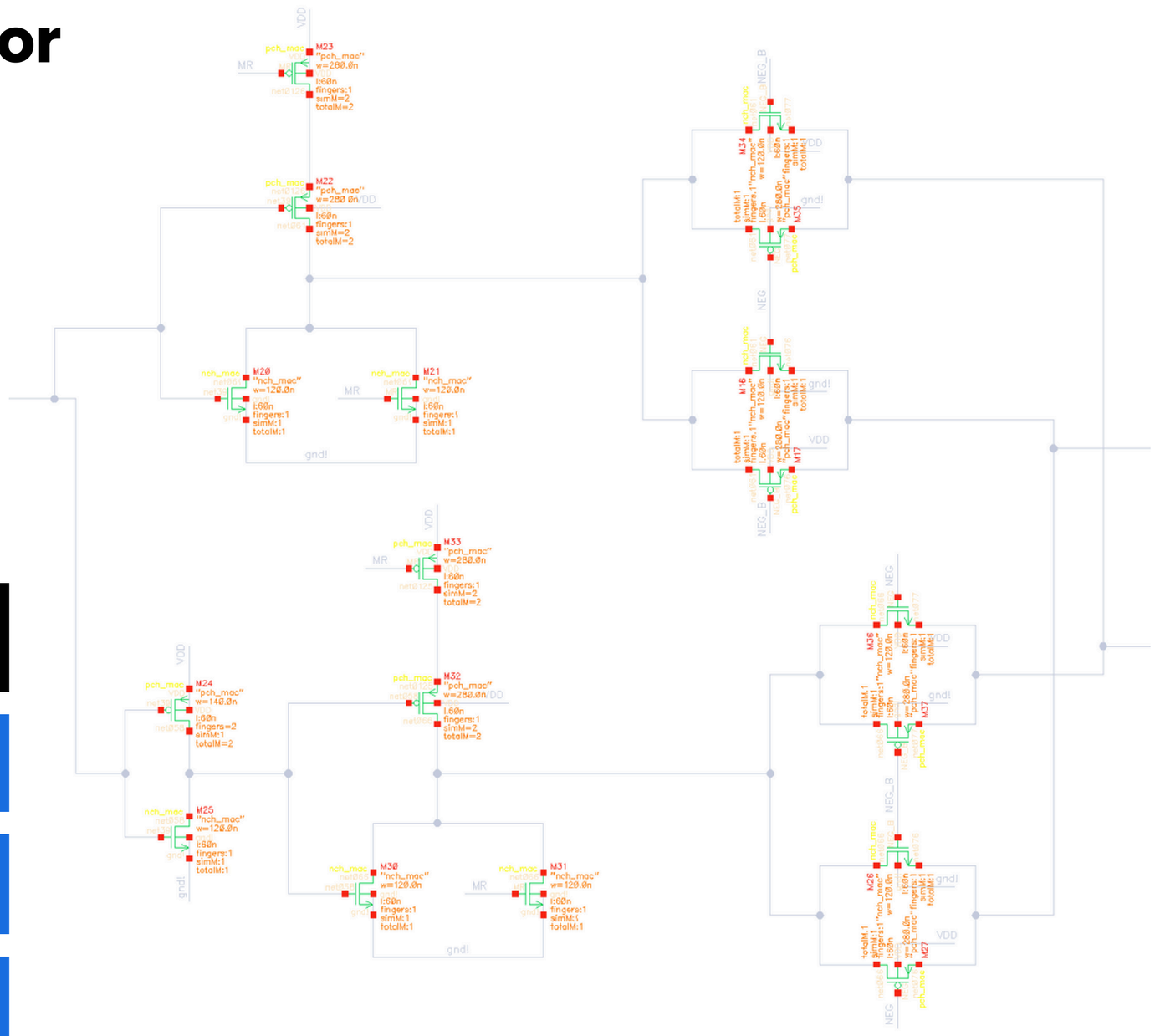


MUX & PRE_DRIVR

Logic stage is responsible for two functions:

- Master Reset (MR): Both outputs of the Pre-DRVR are pulled up, used to specify a number of UDRVRs fixed at low state to control the swing.
- Negate (NEG): Swaps Y and YB outputs so that it can be adding or subtracting at the output of the DRVR.

MR	NEG	Y	YB
1	X	1	1
0	0	INPUT	!(INPUT)
0	1	!(INPUT)	INPUT



MUX & PRE_DRIVR

Buffering

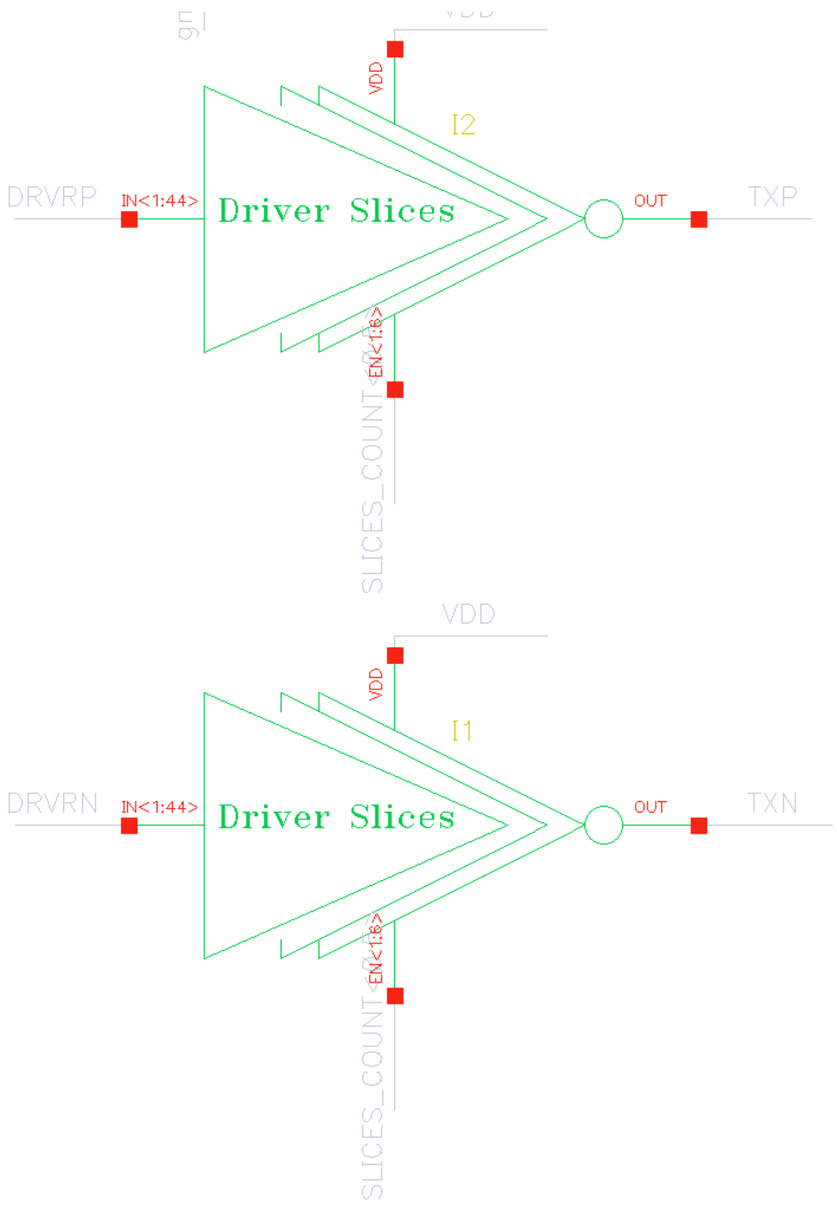
- Buffering is implemented using a chain of FO3 inverters to support high speed while maintaining duty cycle.
- The next stage may include up to 64 slices, each with a 44-unit inverter driven by a Pre-DRVR through a transmission gate.
- The load capacitance can be approximated as: 64-unit inverter + 128-unit transmission gate + 3×64-unit inverter capacitance.

DIFF VM DRIVR

- **We have two block positive and negative DRIVR slices for differential output each block have the following:**

- input data (input <1:44>)

- Control signal controls the number of slices



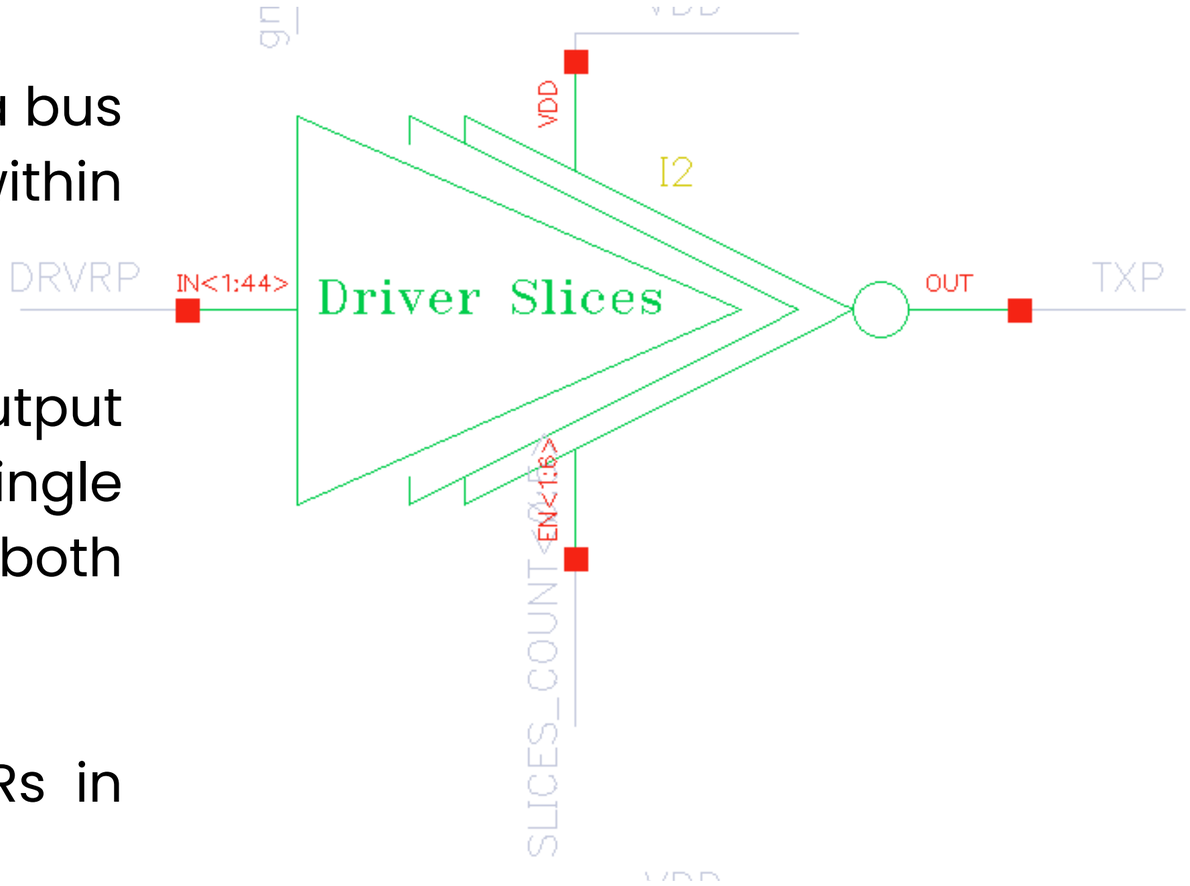
DRIVR SLICES

- **Driver Slice (DRVR):** It is composed of multiple Unit Drivers (UDRVR) connected in parallel with split inputs.

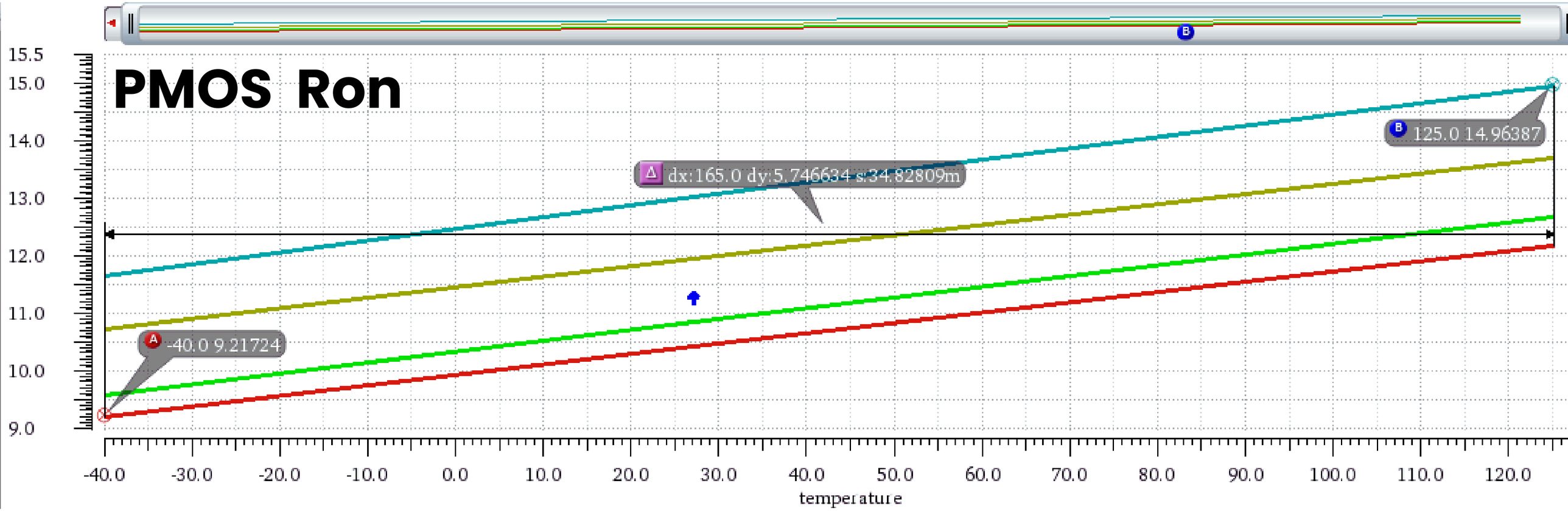
- **Input Structure:** The input of the DRVRS is a bus that distributes signals to all unit drivers within the slice.

- **Output Impedance:** The total output impedance remains constant whether a single slice or multiple slices are active, since both PUN and PDN have equal ON resistance.

- **Unit Driver Count:** The number of UDRVRs in each slice will be specified later.

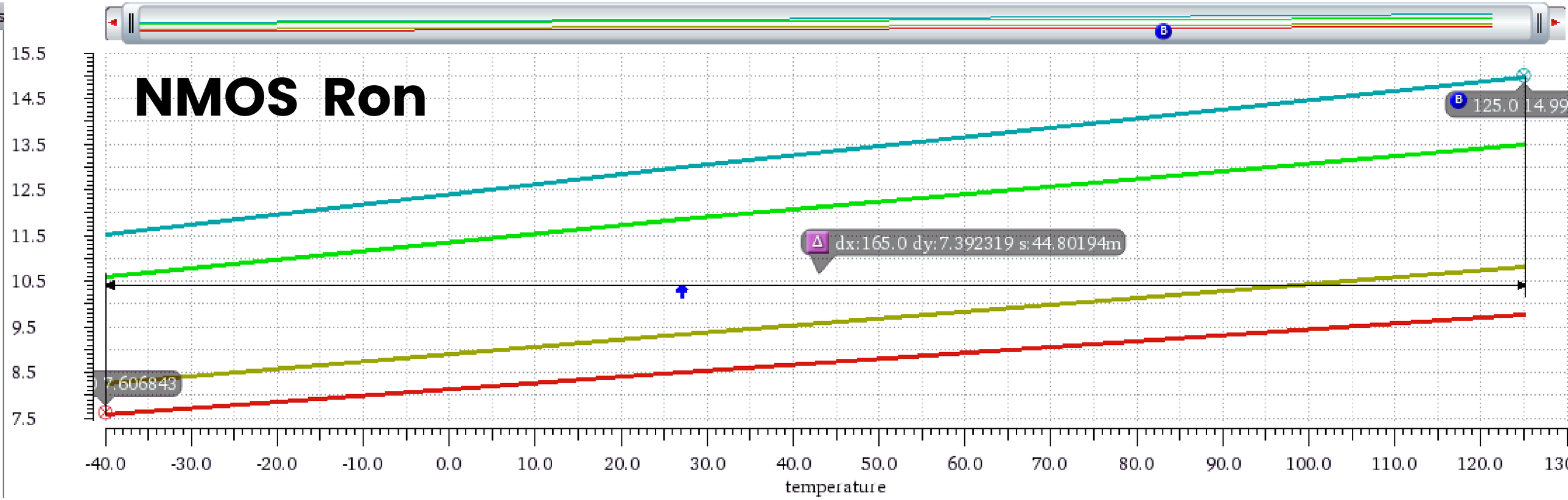


UNIT DRIVR ACROSS CORNERS



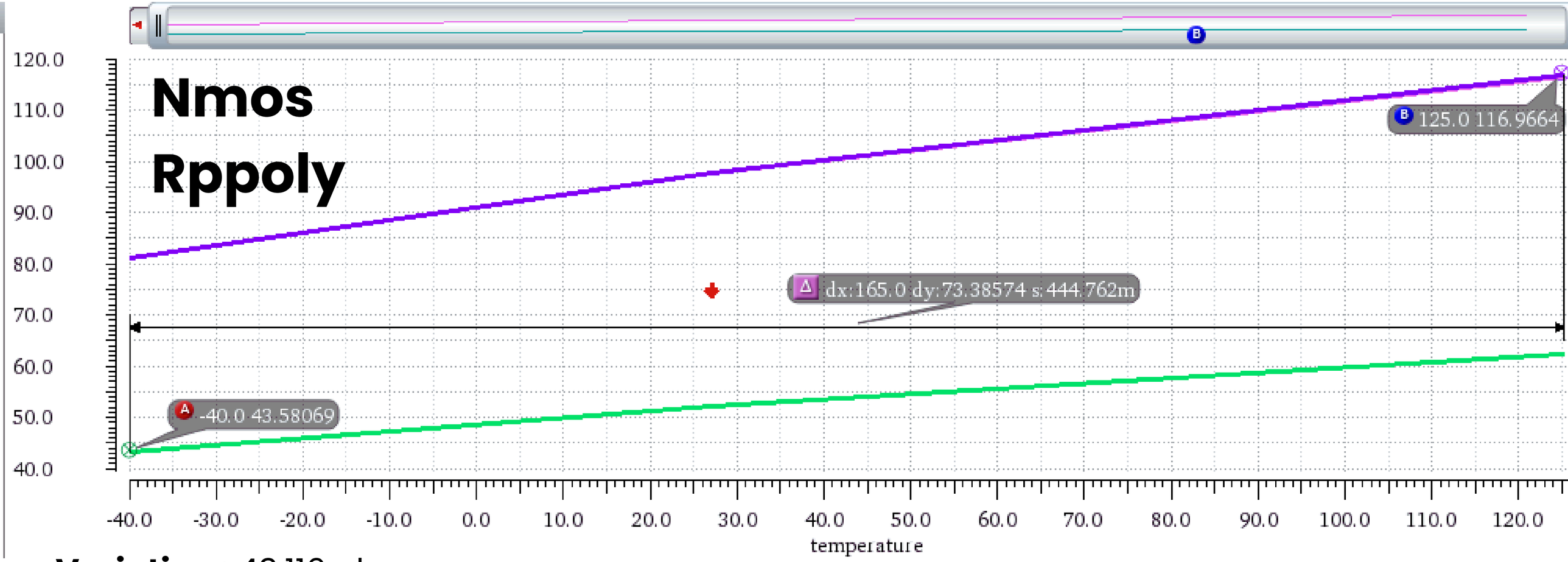
- **Variation :** 9:15 ohm

UNIT DRIVR CORNERS



- **Variation :** 7:15 ohm

UNIT DRIVR CORNERS



- **Variation :** 43:116 ohm

UNIT DRIVR CORNERS

Pmos

Rppoly

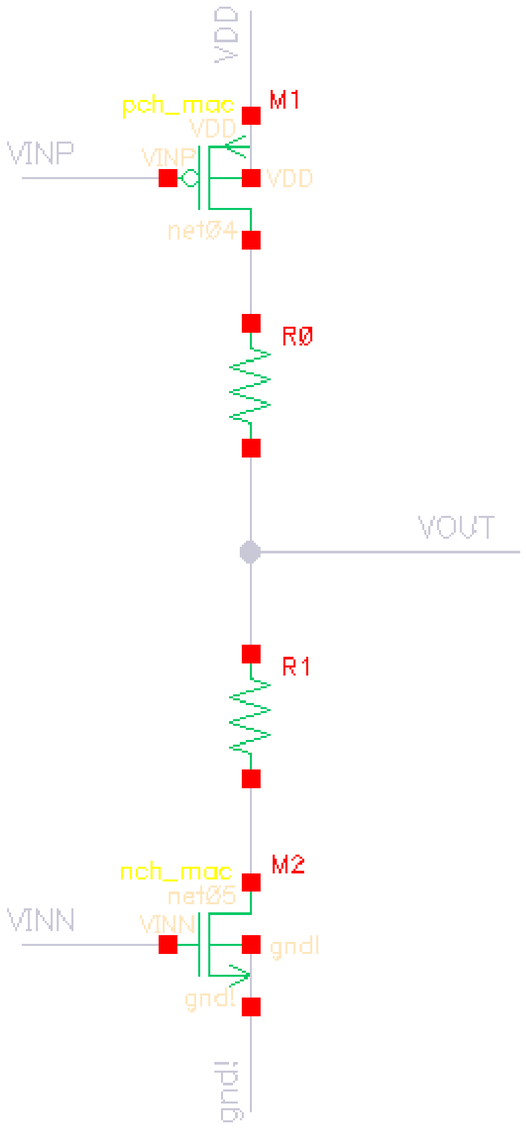
Output	Nominal	Spec	Weight	Pass/Fail	Min	Max
OP("/R1" "res")	70.51				40.64	70.51

UNIT DRIVR DISSCUSION

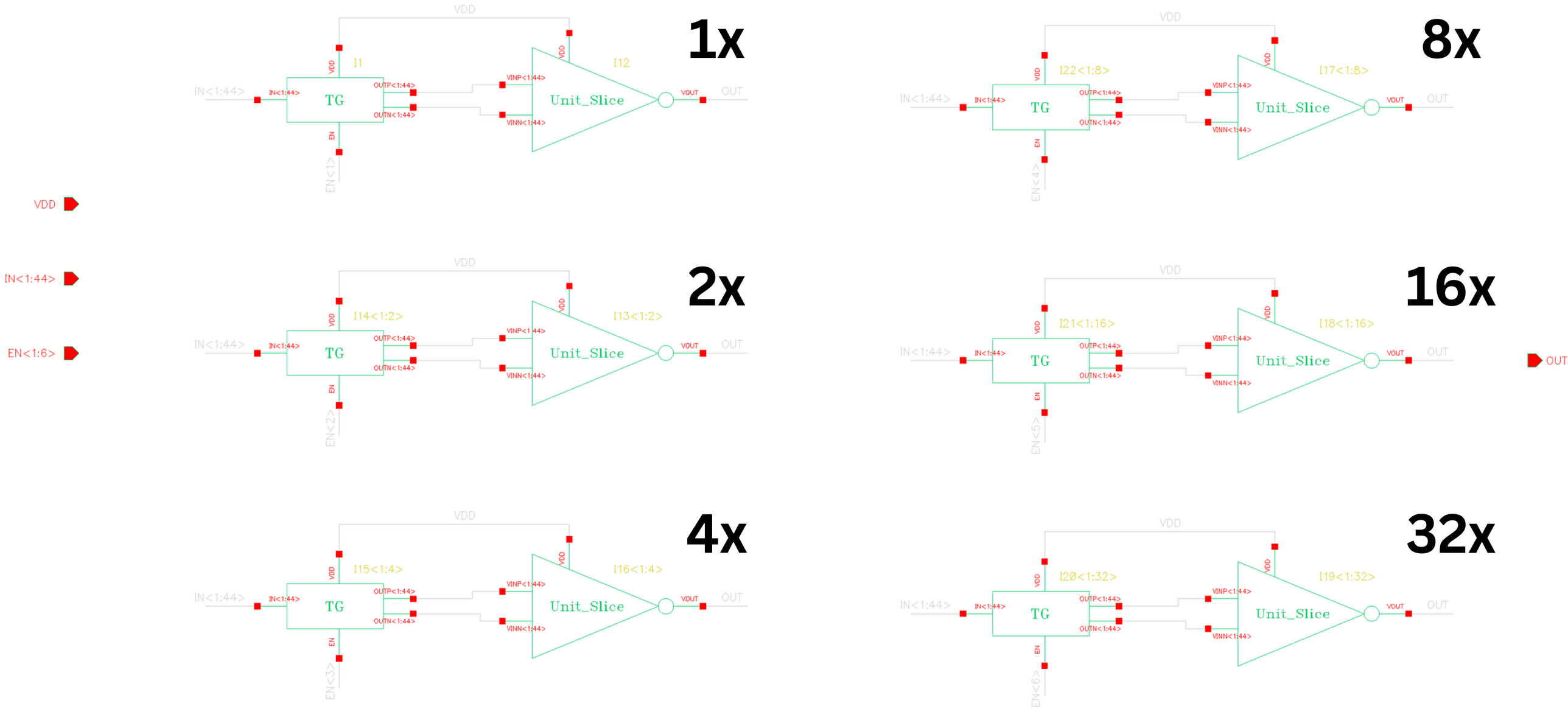
- A unit driver is designed as single INVERTER with a series termination poly resistor.

- Sizing is divided into 5 slice to make control more precise. Termination control precision trades off with within-slice equalization precision, a fine slice step will reduce UDRVR count per slice and hence swing control becomes coarser. For 5 slices:
- PDN: 44 multiplier/slice
- PUN: 44 multiplier/slice

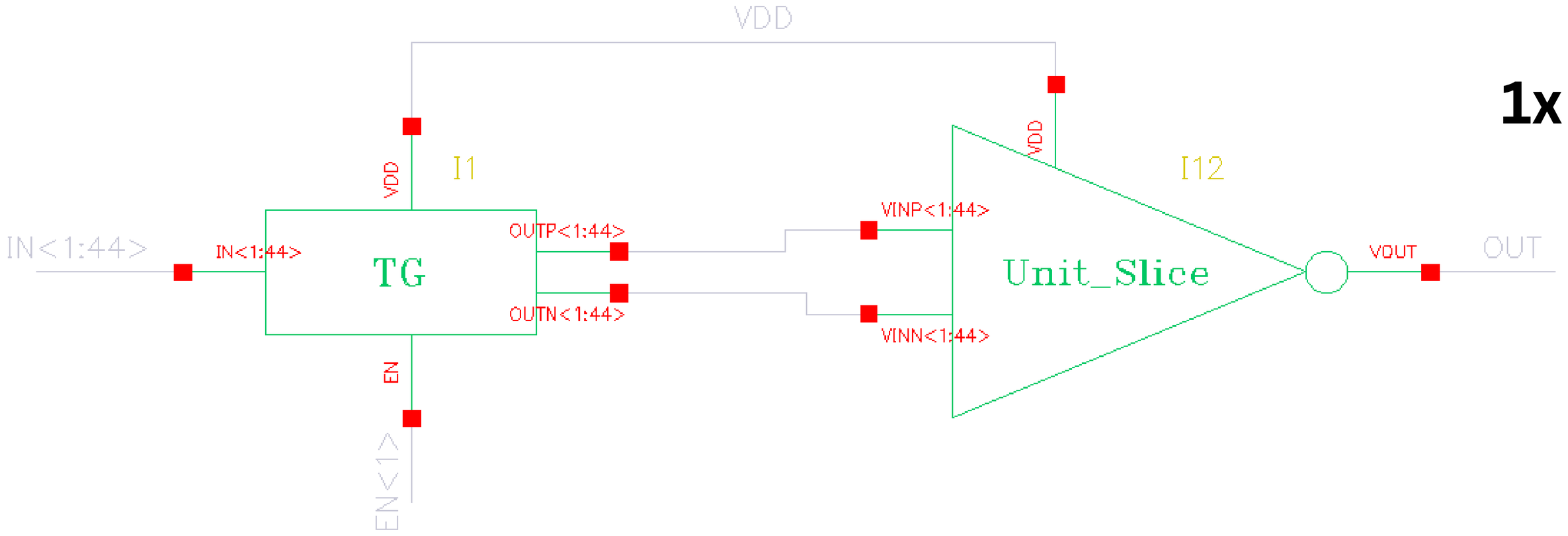
- a 64x (binary weighted) is chosen so that a termination calibration has wide range of flexibility



VM DRVR SLICES



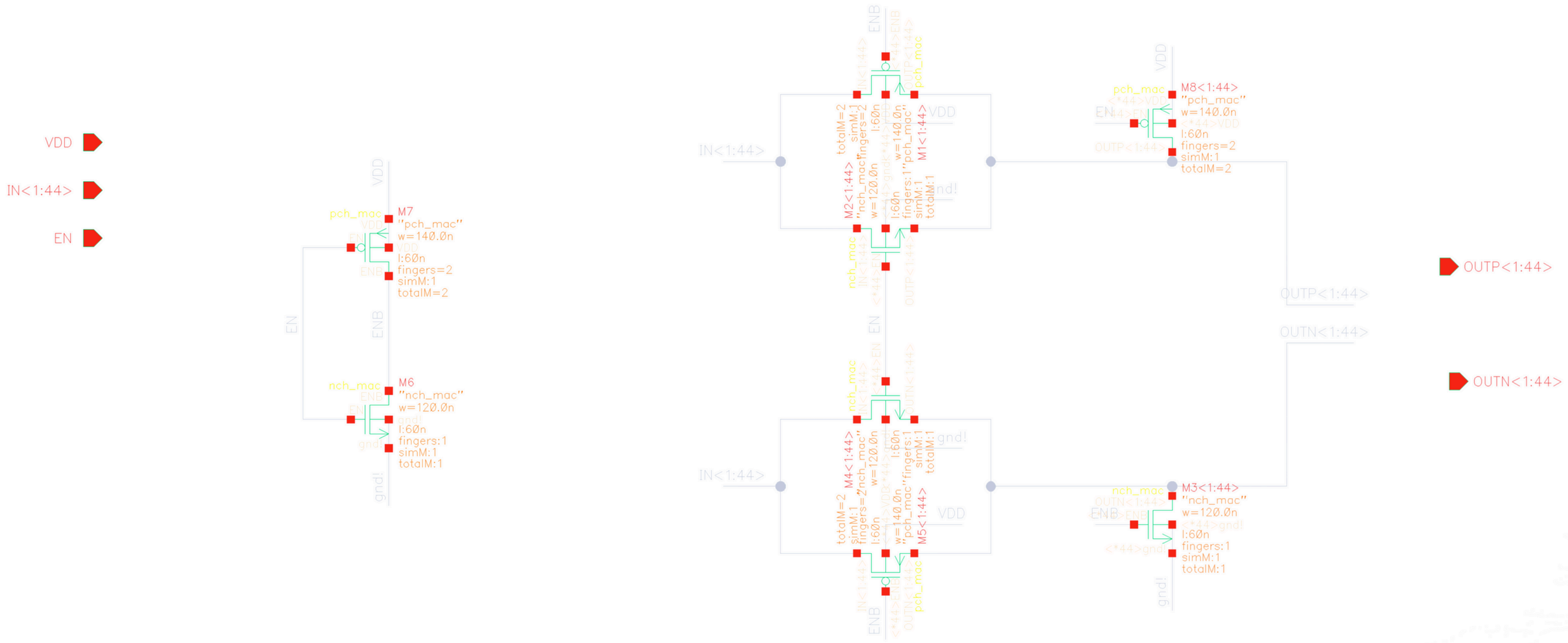
VM DRVR SLICES



- We have binary weighted Driver Slice from 1X to 32X to control the termination

- The slice will have 44 unit inverter SST every one has 8kΩ which are divided into 6.7 KΩ from fixed rppoly and 1.3KΩ from the transistors (NMOS or PMOS)

TRANSMISSION GATE

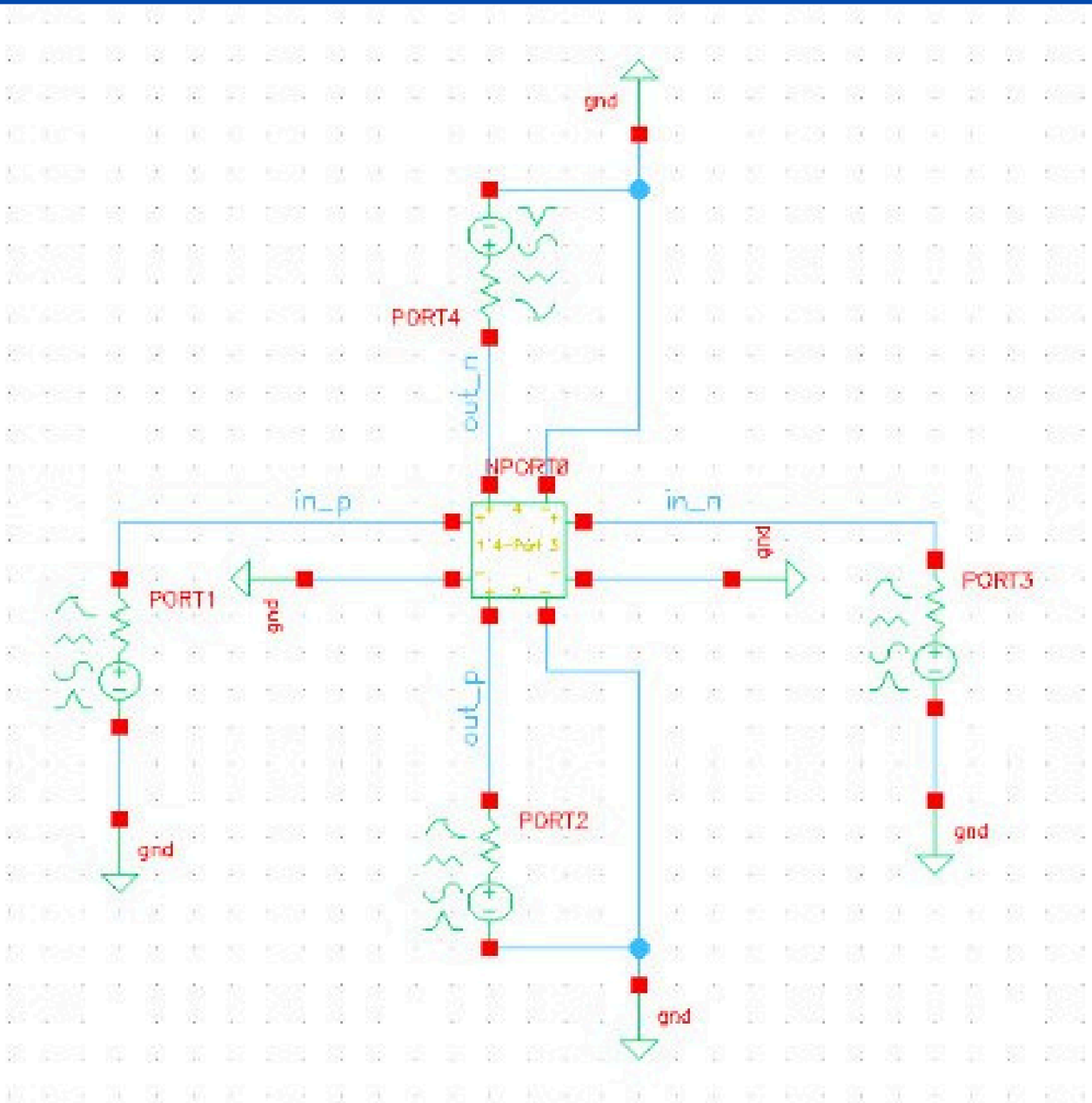


- Transmission gate is an array of transmission gates as well, for the bus of 44 lines. Sizing is done as a min. sized switches since it drives a min. sized inverter in the UDRVR

CHANNEL CHARACTERISTIC

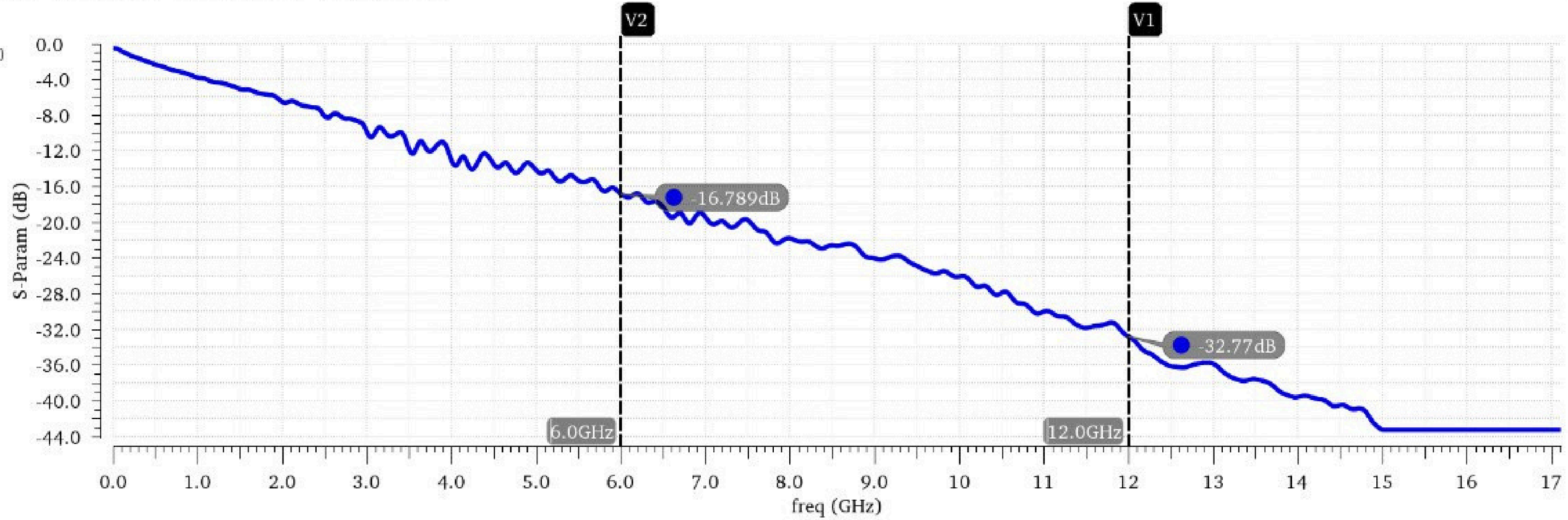
CHANNEL CARACTARISTIC

Test bench



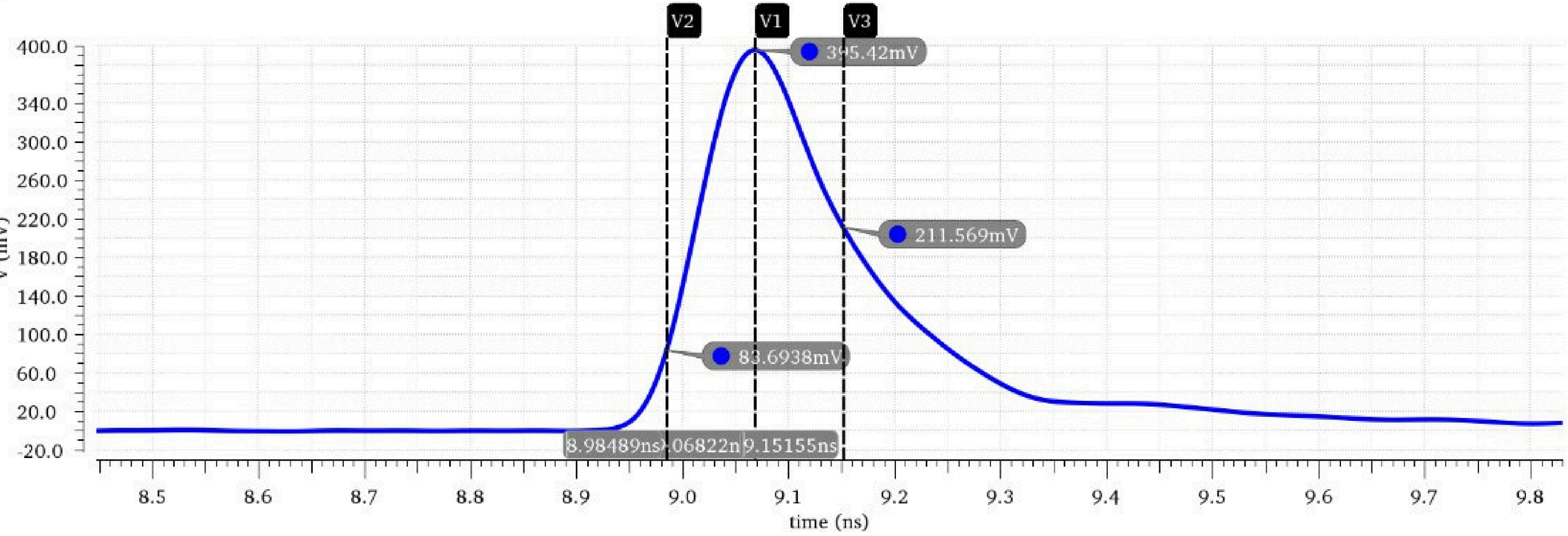
CHANNEL CARACTARISTIC

S21



CHANNEL CARACTARISTIC

Channel Response For FFE Tap



FFE TAPS WEIGHTS

- Taps values are obtained by solving the following system of equations:

$$\begin{pmatrix} h_n & h_{n+1} \\ 0 & h_n \end{pmatrix} \begin{pmatrix} a_{n+1} \\ a_n \end{pmatrix} = \begin{pmatrix} 0 \\ 1 \end{pmatrix}$$

- The desired out is 1 for the main.

$$h_n = 0.39542$$

$$h_{n+1} = 0.08369$$

$$a_{n+1} = -0.53525$$

$$a_n = 2.5289$$

- SUM of normalized taps = 2.5289 + 0.53525
- The pre-cursor weight = 2.5289/norm taps = 0.825318
- The main-cursor weight = -0.53525/norm taps = -0.174681

TX CONTROLLER

CODE FLOW

START

Parameters initialization

Initialize the controller module and load all parameters including SWING, TAP1, TAP2, TRF, and VTHF values.

Set up internal variables, arrays (MUX_SEL0_INT, MUX_MR_INT, NEG_INT), and configure driver slice counts based on input parameters.

SWING Sittings

Calculate UDRVR_OFF and UDRVR_ON values based on SWING and VDD parameters. Initialize MUX_MR_INT array with appropriate values for driver control.

FFE taps weights

Compute tap weights (UDRVR_TAP1, UDRVR_TAP2) using absolute values and configure MUX_SEL0_INT and NEG_INT arrays for signal processing.

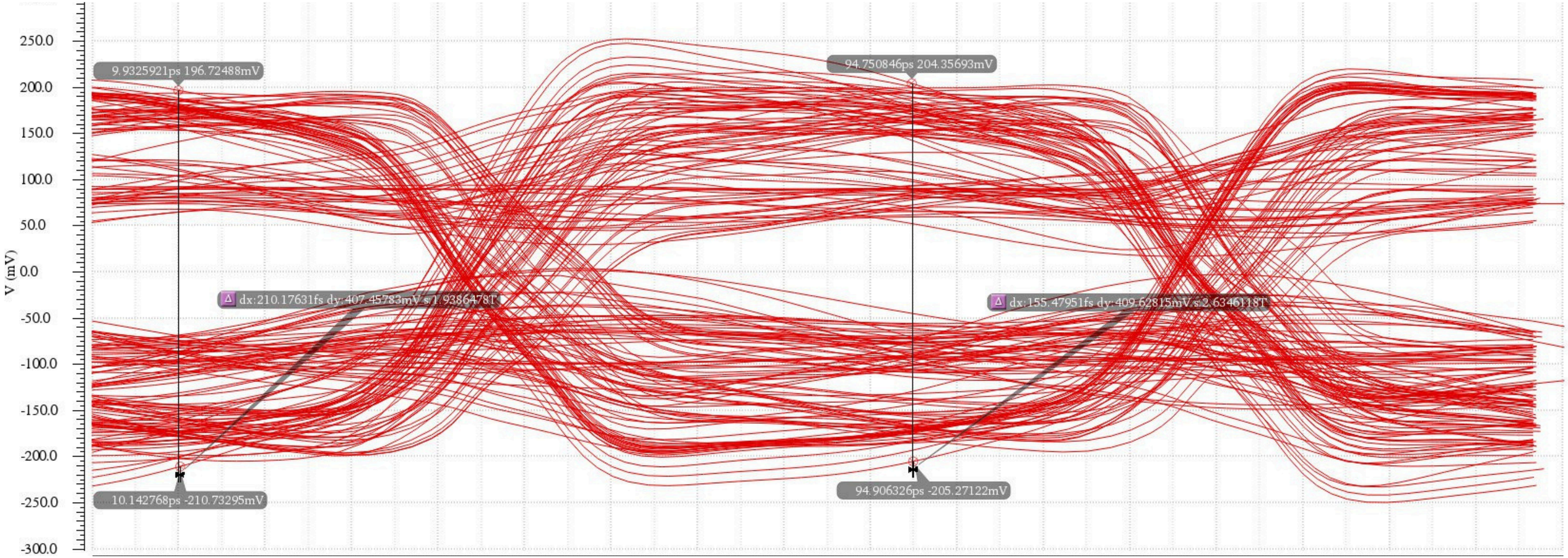
Swing & Termination Control

Implement clock crossing detection logic and calculate SLICES_COUNT based on VSWING input. Update slice count arrays for proper timing control.

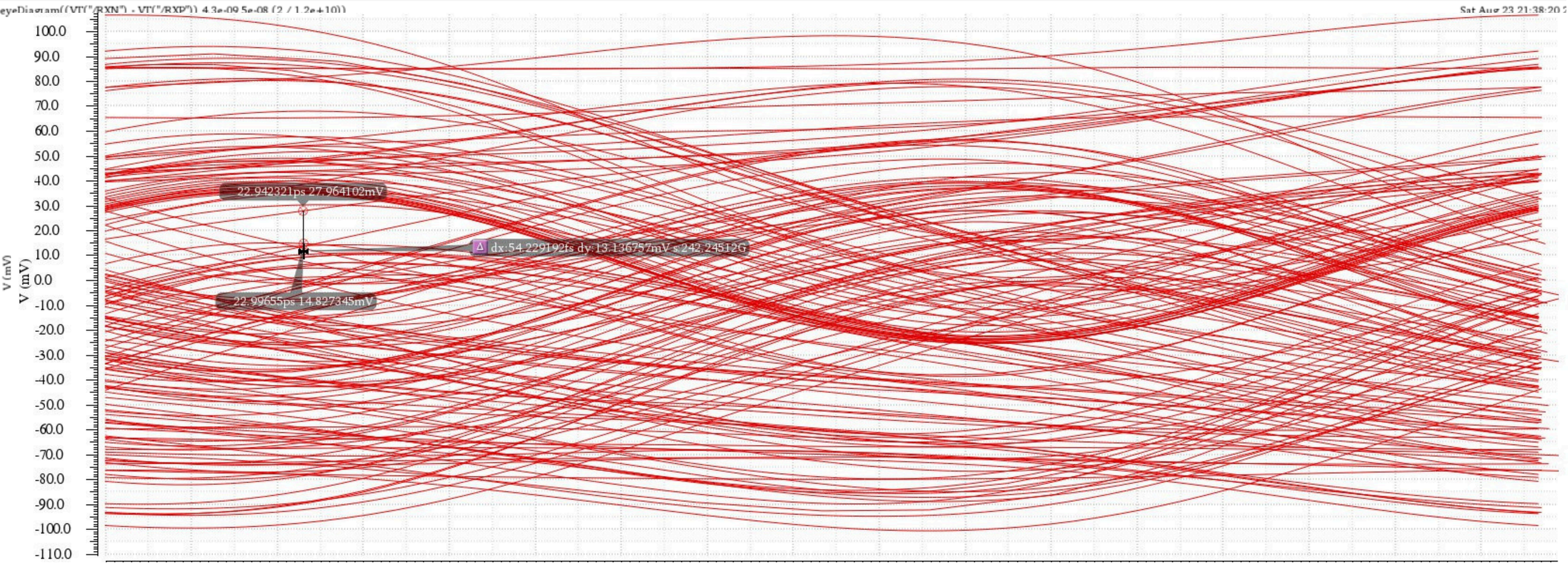
Output Assignment

END

TX RESULT

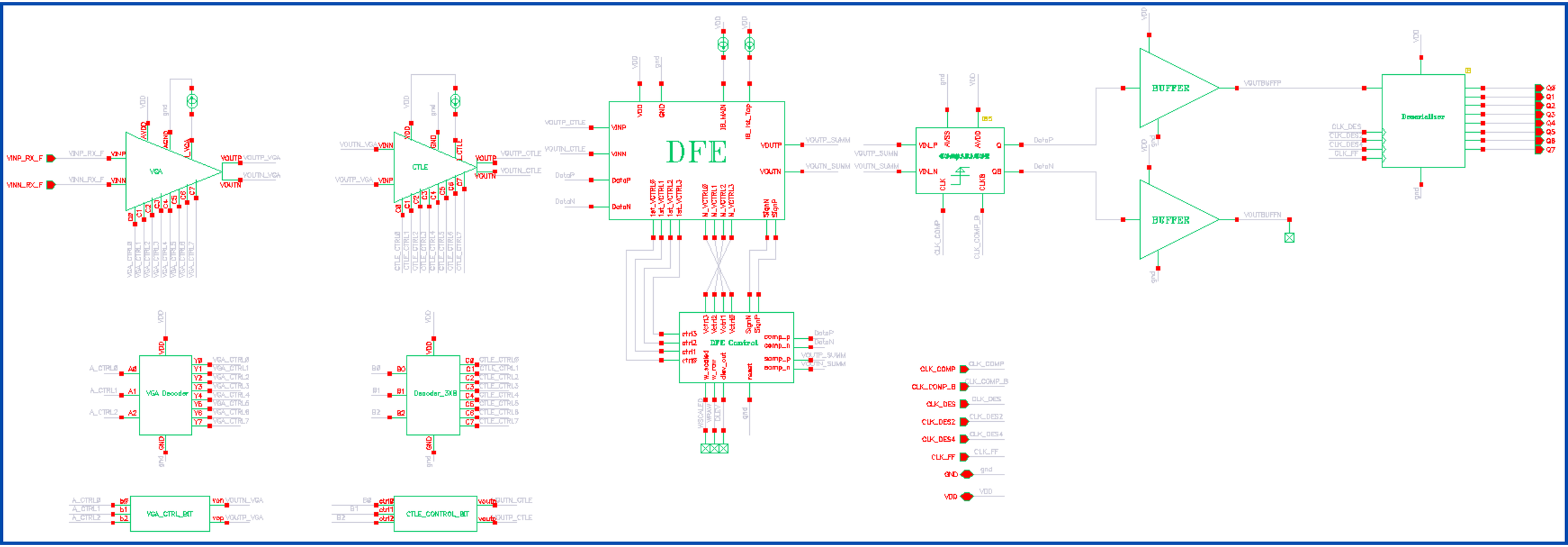

250.0
200.0
150.0
100.0
50.0
0.0
-50.0
-100.0
-150.0
-200.0
-250.0
-300.0
V (mV)
9.9325921ps 196.72488mV
94.750846ps 204.35693mV
dx:210.17631fs dy:407.45783mV s:1.9386478T
dx:155.47951fs dy:409.62815mV s:2.6346118T
10.142768ps -210.73295mV
94.906326ps -205.27122mV

RX INPUT RESULT



RX LINK

RX TOP LEVEL


VGA
CTLE
DFE
DFE Control
BUFFER
BUFFER
Deserializer
VGA Decoder
Decoder_3X8
VGA_CTRL_BIT
CTLE_CONTROL_BIT
VINP_RX_F
VINN_RX_F
VOUTP_VGA
VOUTN_VGA
VOUTP_CTLE
VOUTN_CTLE
VOUTP_SUMM
VOUTN_SUMM
DataP
DataN
VOUTBUFFP
VOUTBUFFN
CLK_COMP
CLK_COMP_B
CLK_DES
CLK_DES2
CLK_DES4
CLK_FF
GND
VDD

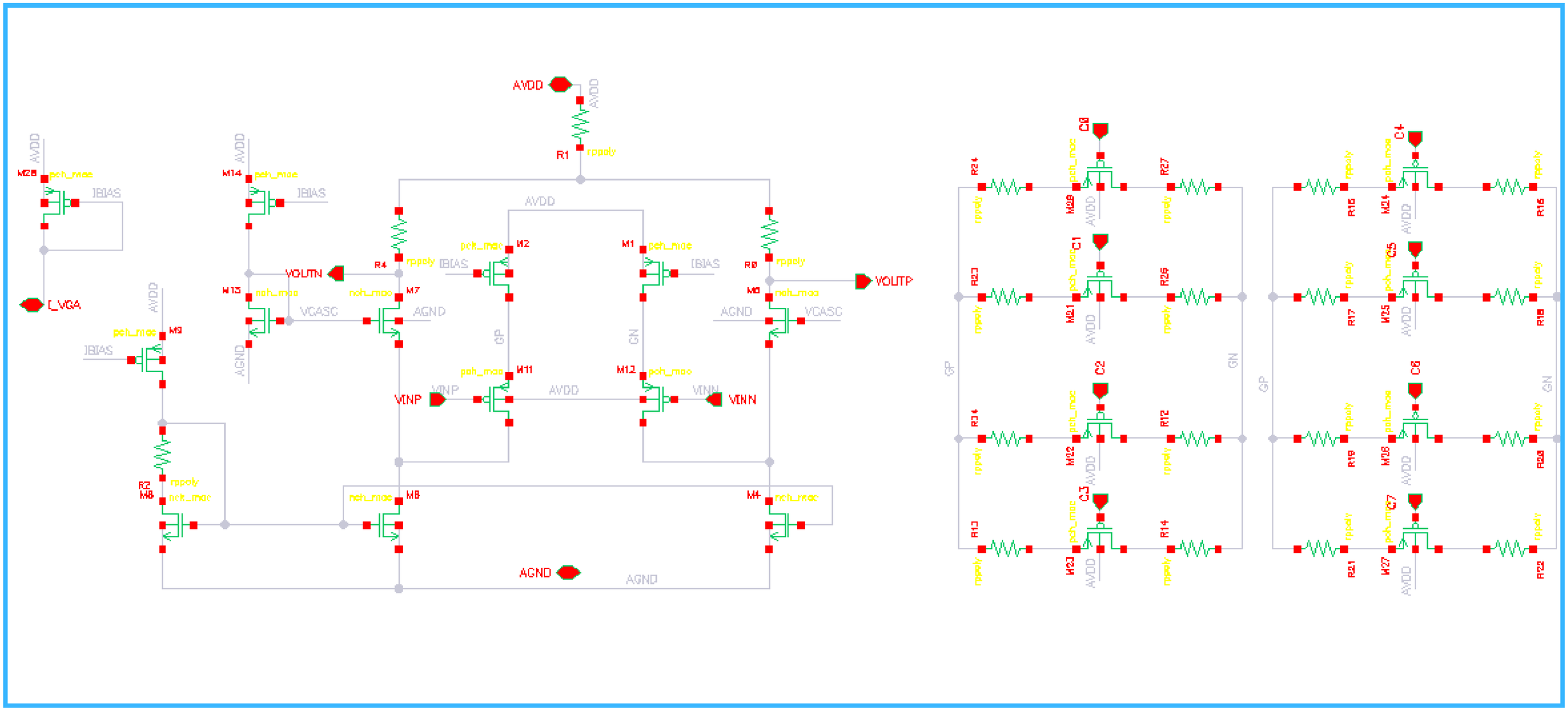
VARIABLE GAIN AMPLIFIER (VGA) DESIGN

Introduction

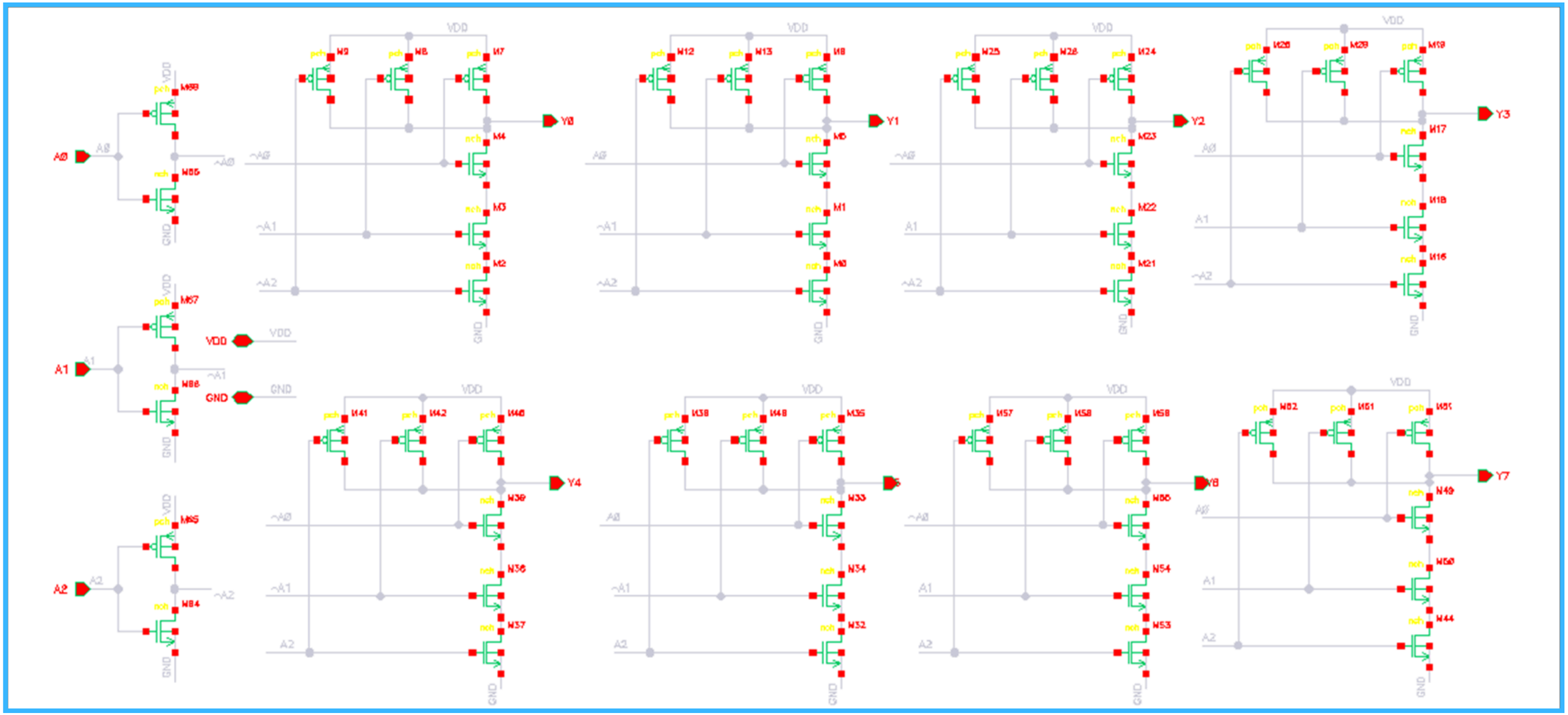
Variable Gain Amplifier (VGA) is an amplifier with adjustable gain used in high-speed receivers.
Gain can be varied using digital control bits or an analog control voltage.
Ensures the signal amplitude is suitable for further equalization and detection.

Received signals may be too weak (long channel) or too strong (short channel).
VGA normalizes the amplitude so that:
CTLE can work on a properly scaled signal.
Comparator/DFE can make accurate decisions.

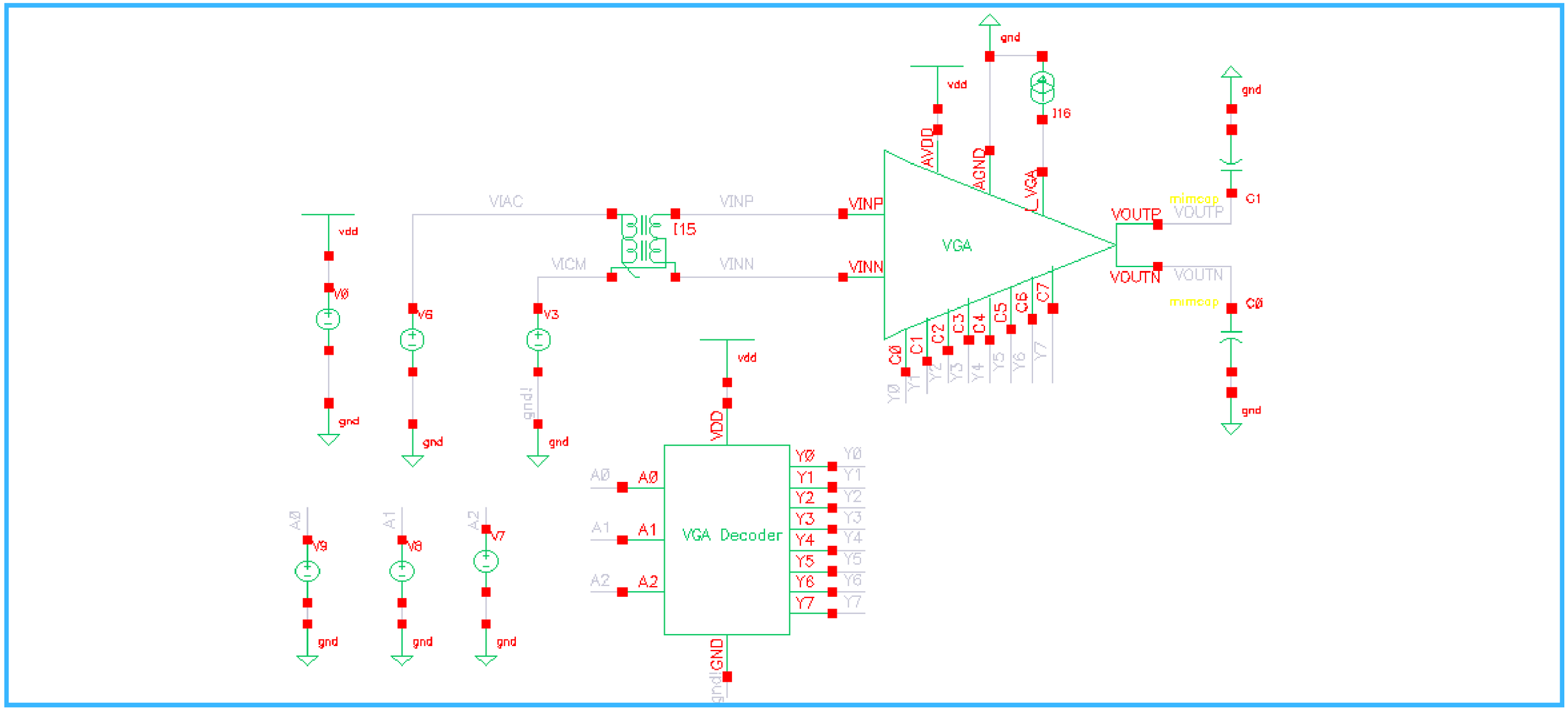
SCHEMATIC OF VGA



3X8 DECODER SCHEMATIC

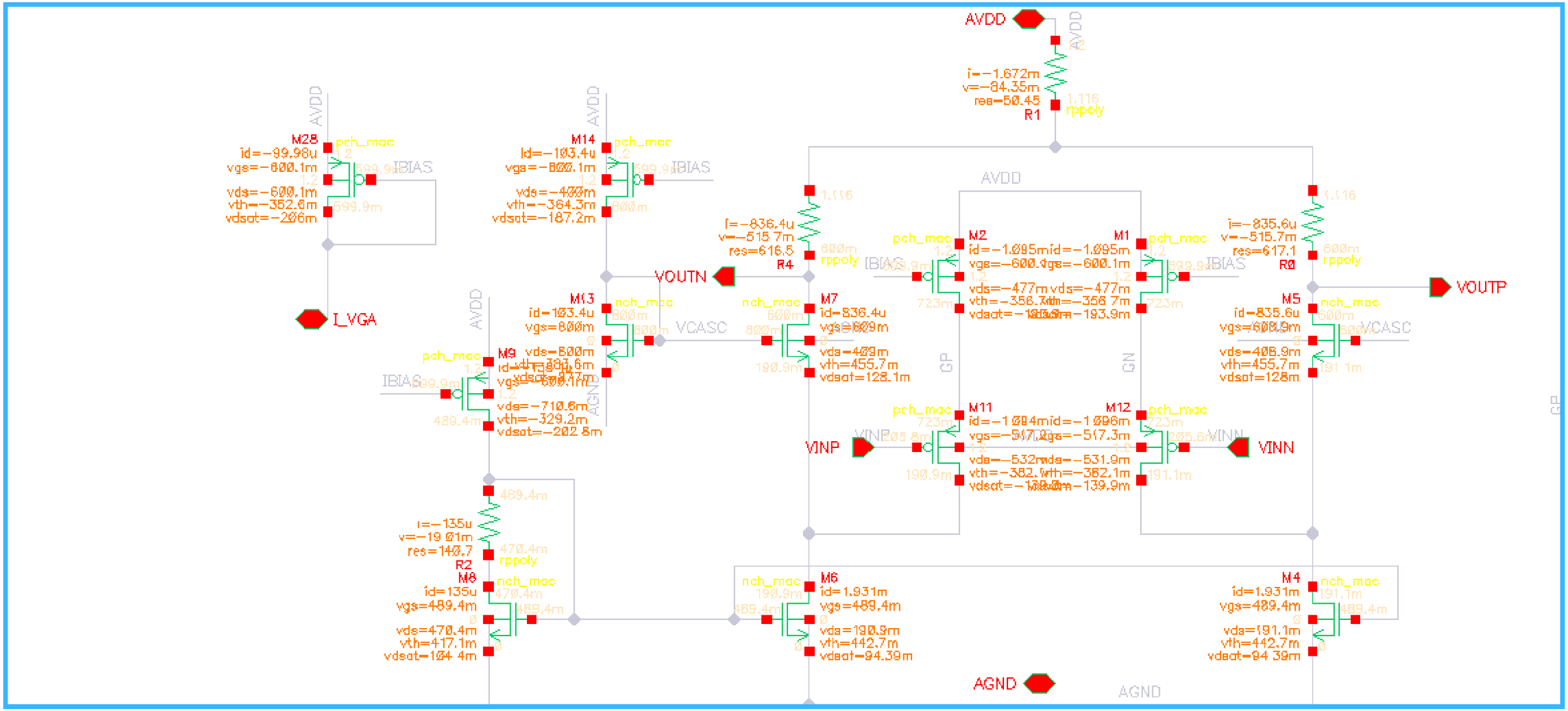


TESTBENCH FOR VGA (AC AND DC ANALYSIS):



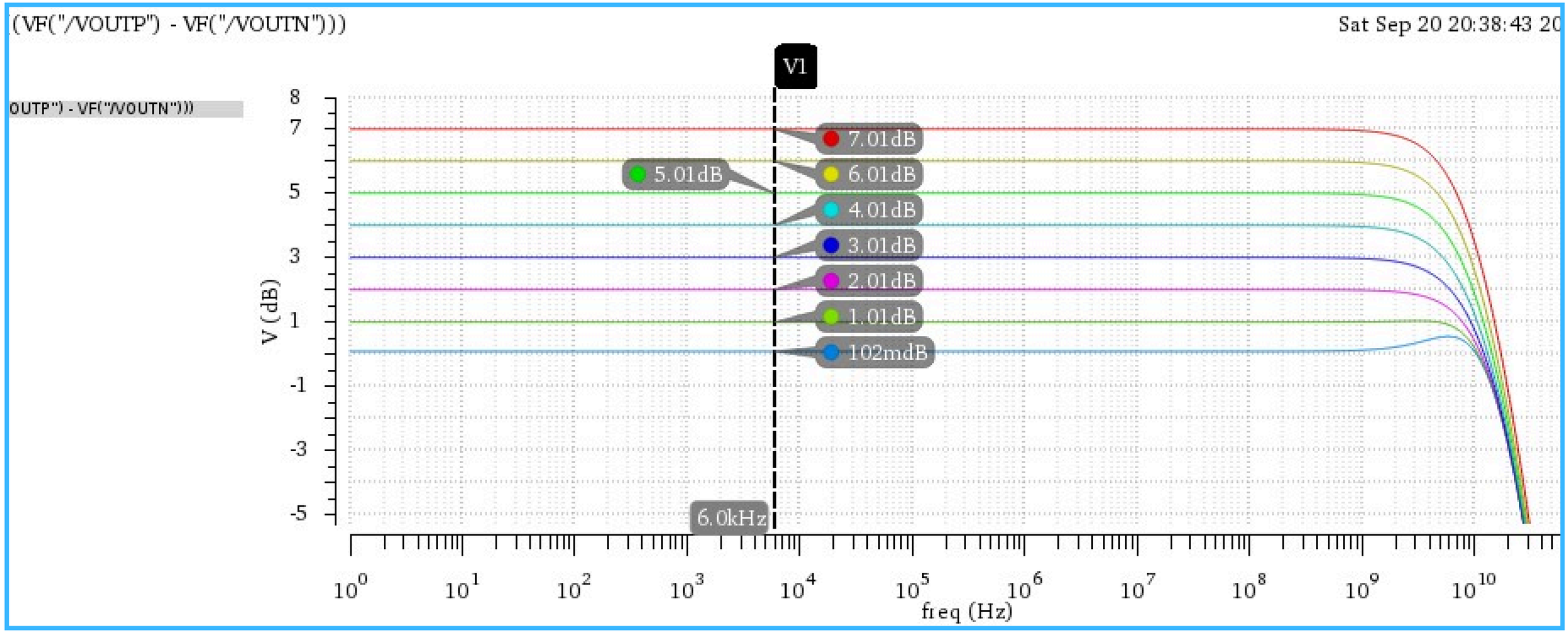
DC ANALYSIS

DC operating point

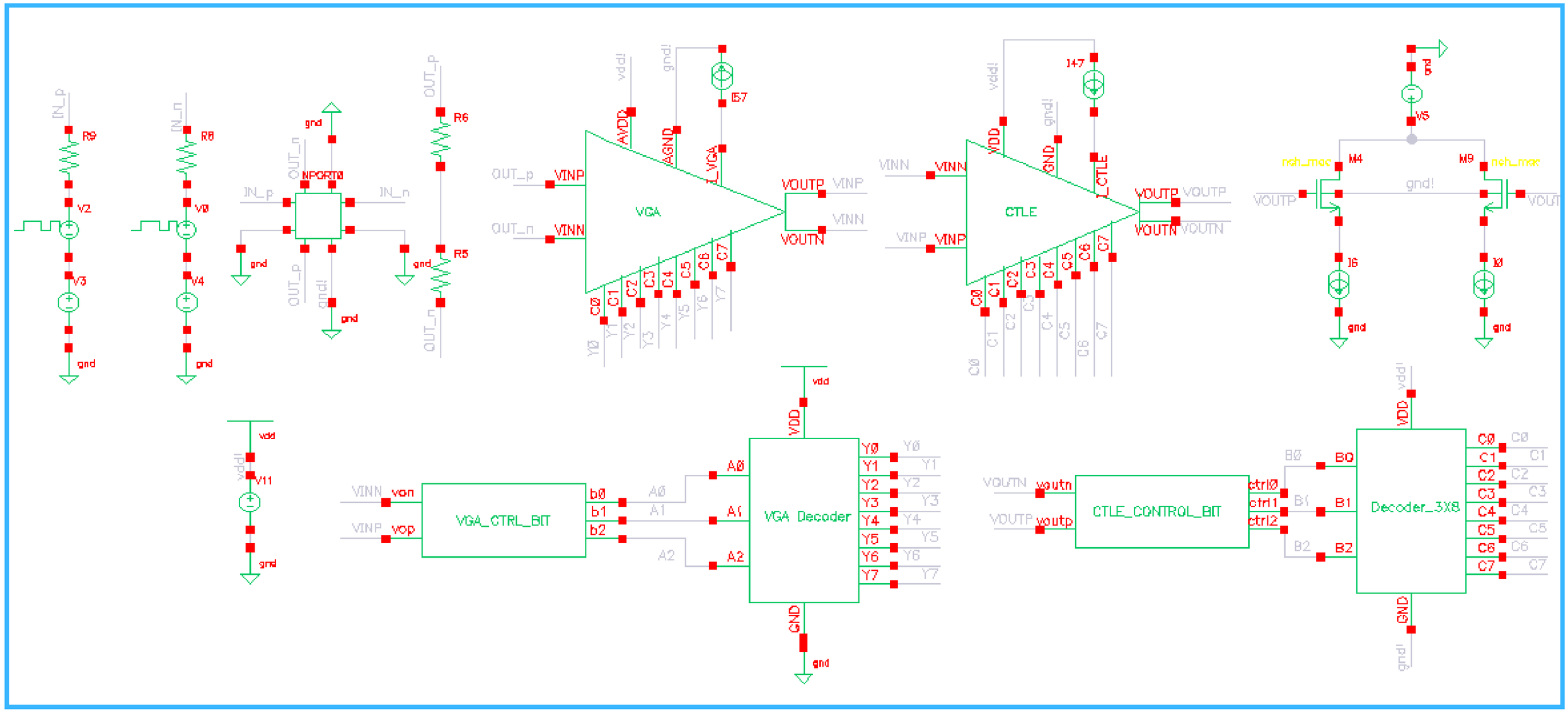


AC ANALYSIS

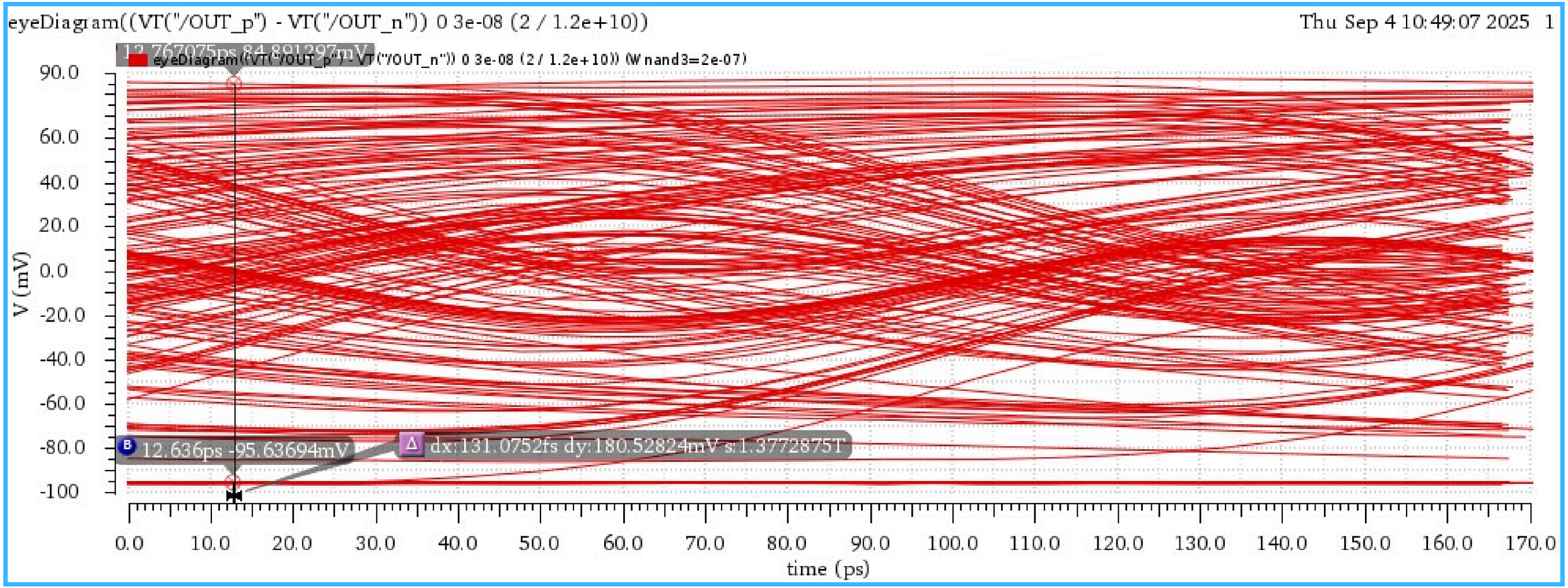
AC response



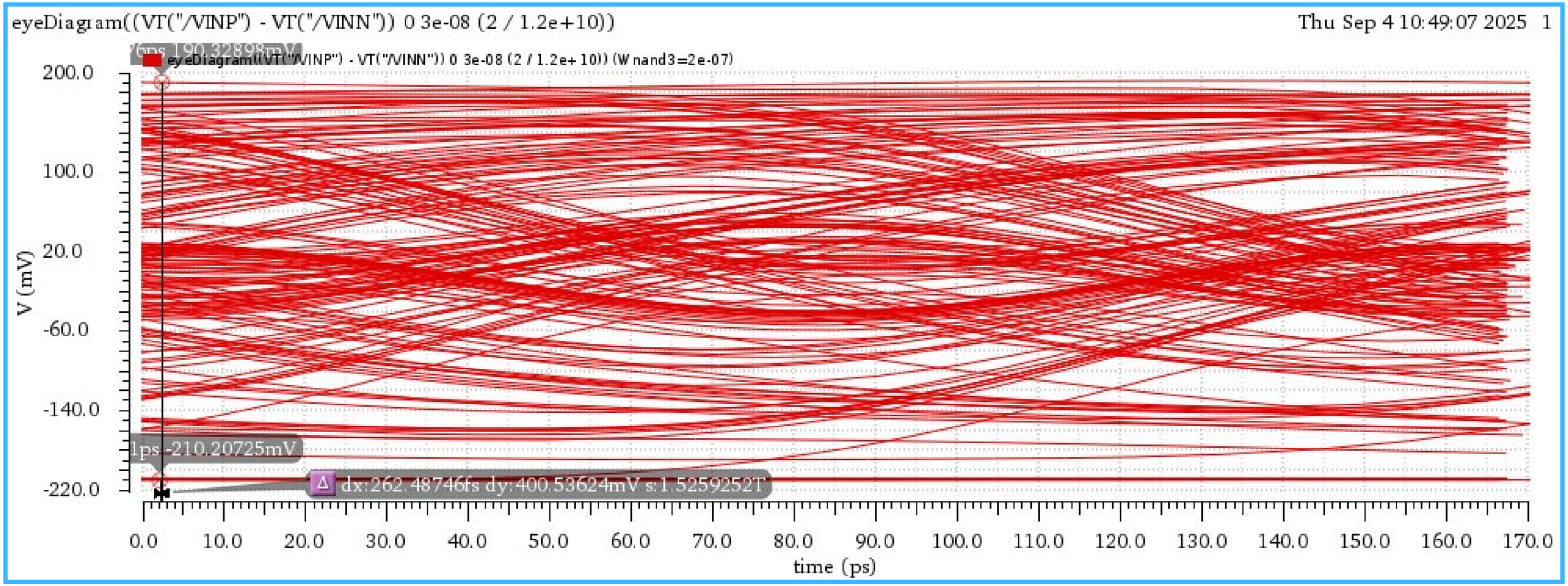
TESTBENCH FOR VGA (TRANSIENT ANALYSIS):



CHANNEL EYE DIAGRAM (BEFORE VGA)



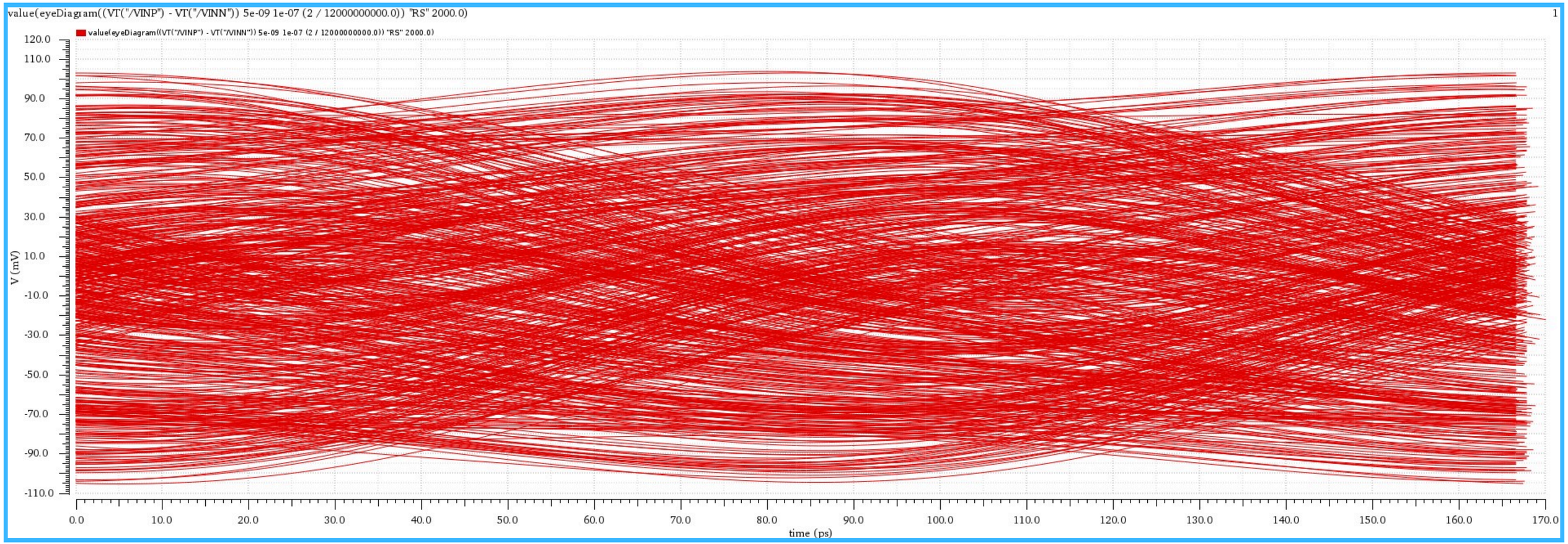
OUTER EYE DIAGRAM (AFTER VGA)



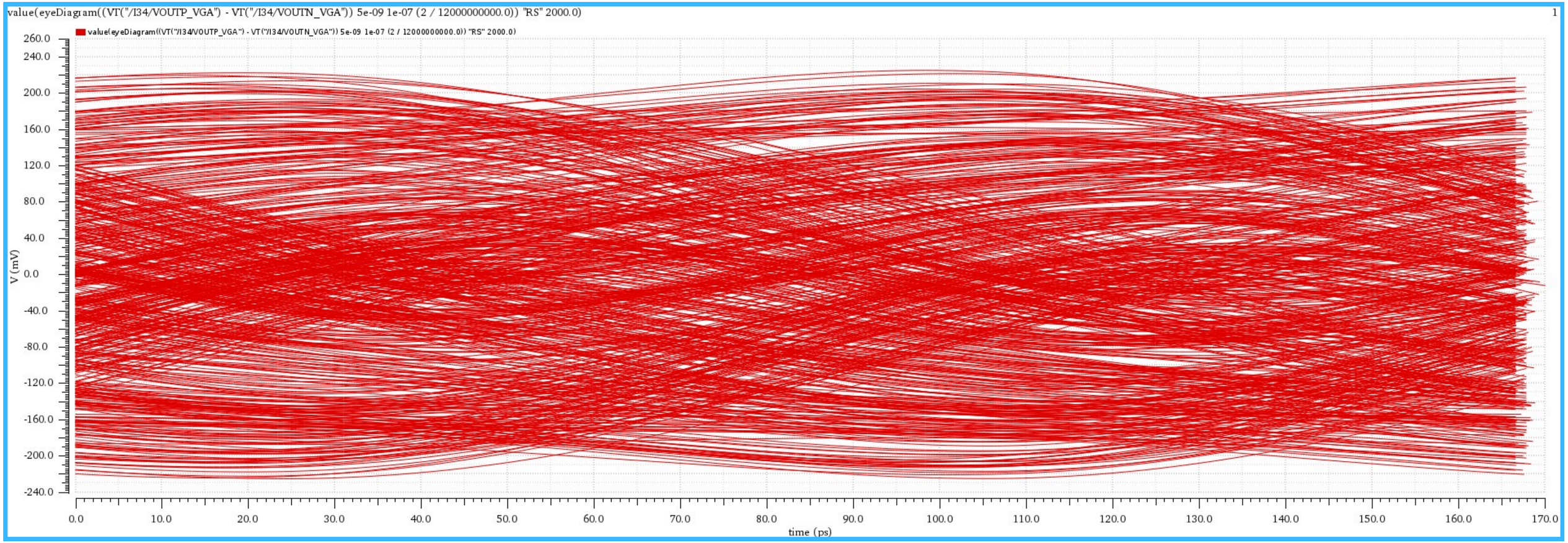
EYE DIAGRAM RESULT

	Inner Eye Opening	Outer Eye Opening	horizontal Opening
Before VGA	0	182.5mV	0
After VGA	0	400.5mV	0

CHANNEL EYE DIAGRAM FOR THE SYSTEM



EYE DIAGRAM AFTER VGA FOR THE SYSTEM



EYE DIAGRAM RESULT

	Inner Eye Opening	Outer Eye Opening	horizontal Opening
Before VGA	0	182.5mV	0
After VGA	0	420.mV	0

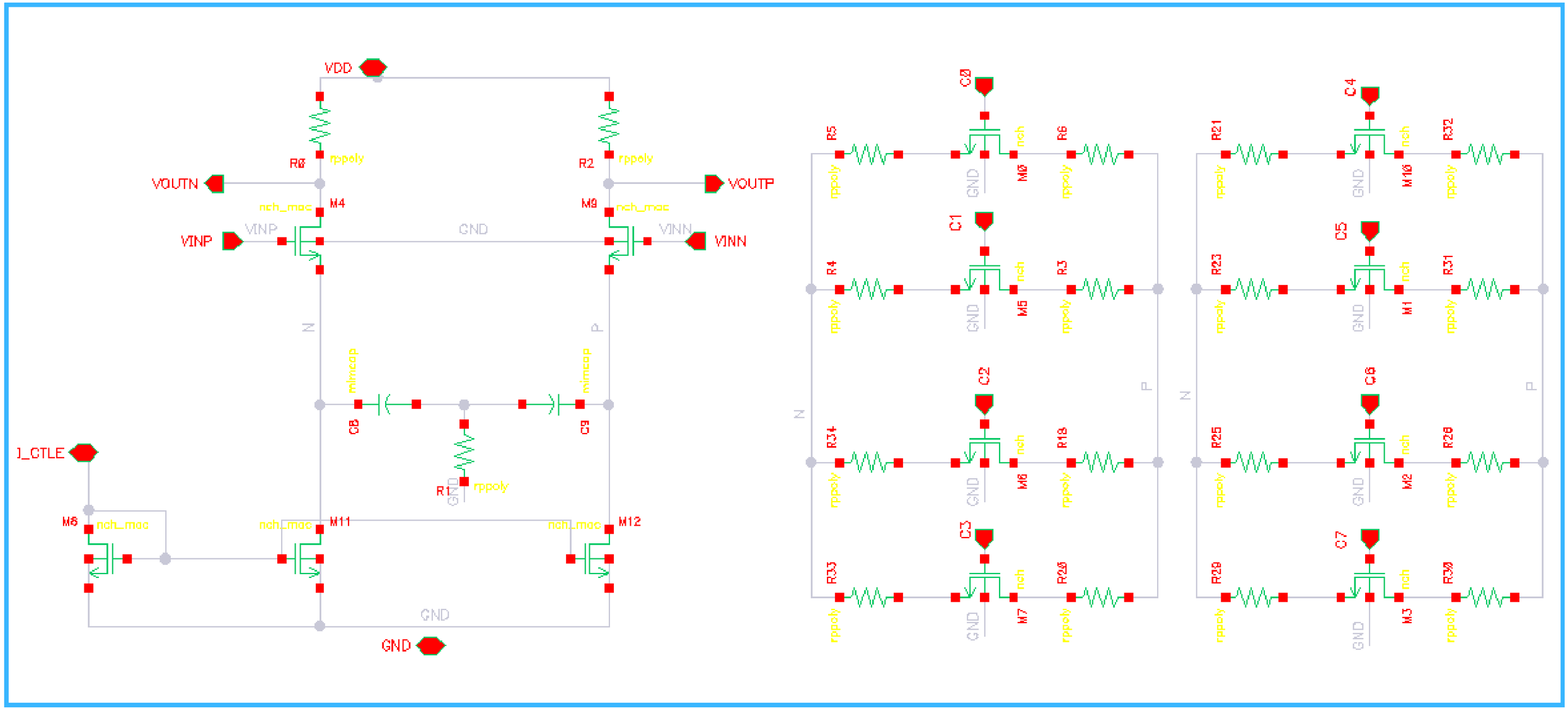
CONTINUOUS-TIME LINEAR EQUALIZER (CTLE) DESIGN

Introduction

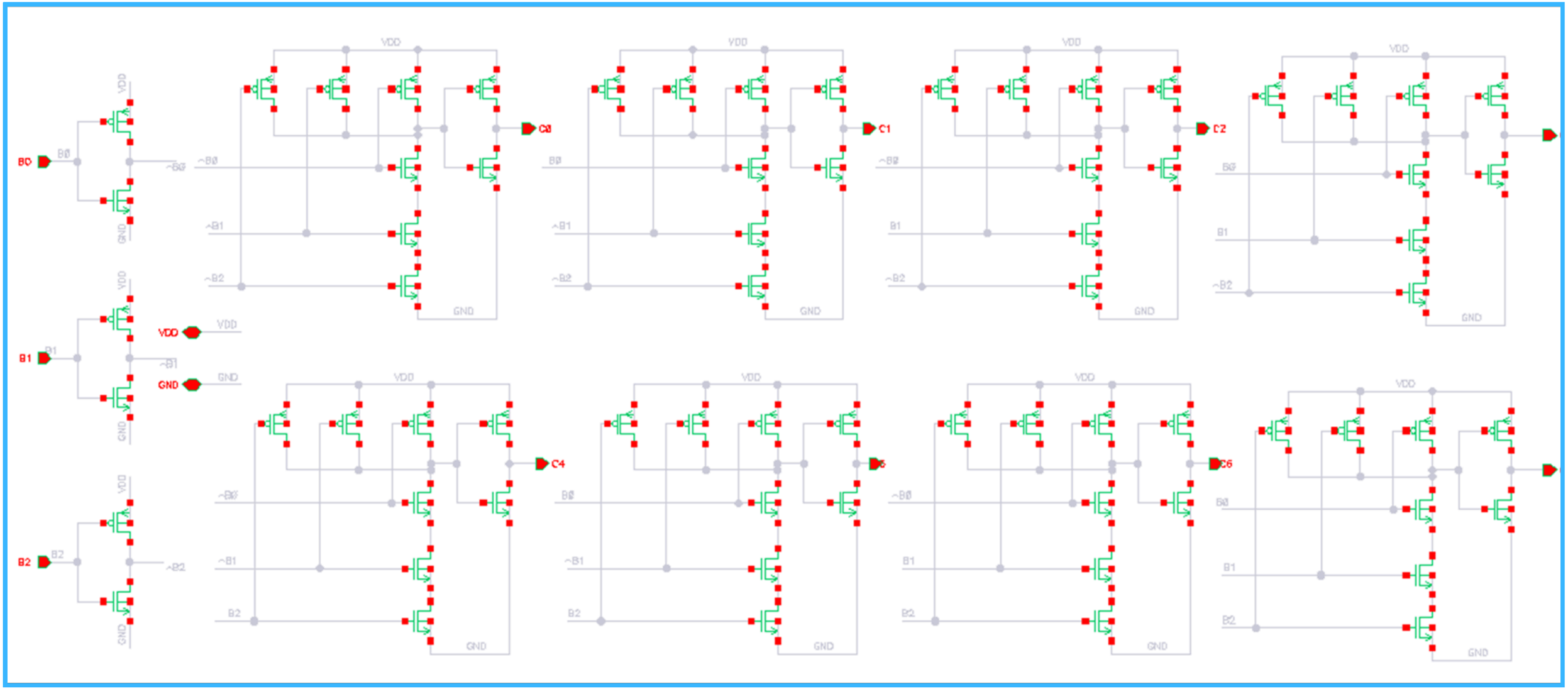
A Continuous-Time Linear Equalizer (CTLE) is an analog equalizer used in high-speed receivers. It compensates for frequency-dependent channel loss, particularly the attenuation of high-frequency components, and operates in the continuous-time domain rather than being sampled like digital filters. High-speed channels such as PCB traces, cables, and backplanes behave like low-pass filters that attenuate fast edges and transitions, leading to closed eye diagrams and higher detection errors.

To overcome this, the CTLE implements a frequency-shaped amplifier. It boosts high frequencies to recover sharp edges, suppresses low frequencies to maintain signal balance, and is typically realized using RC networks combined with MOSFET stages.

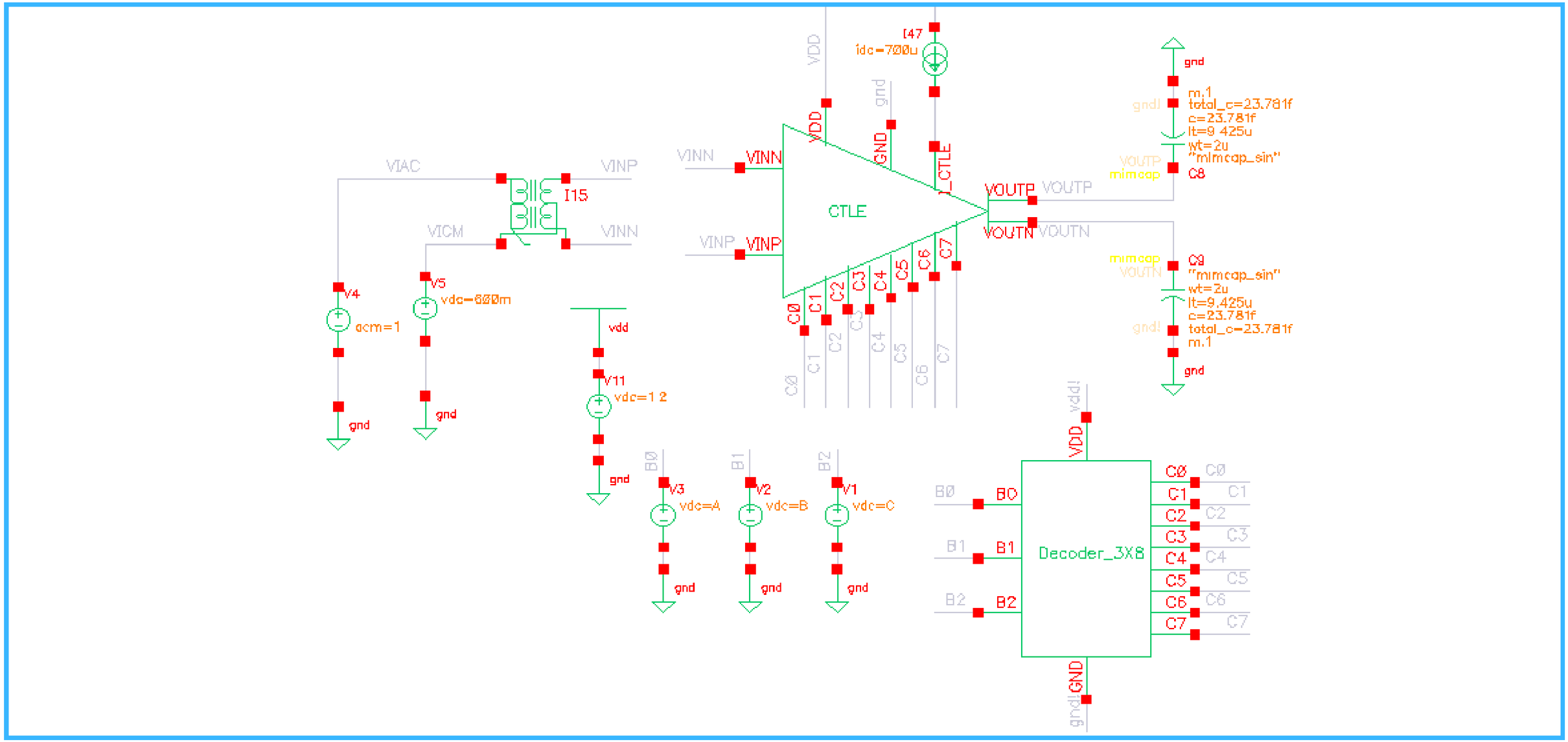
SCHEMATIC OF CTLE



3X8 DECODER SCHEMATIC

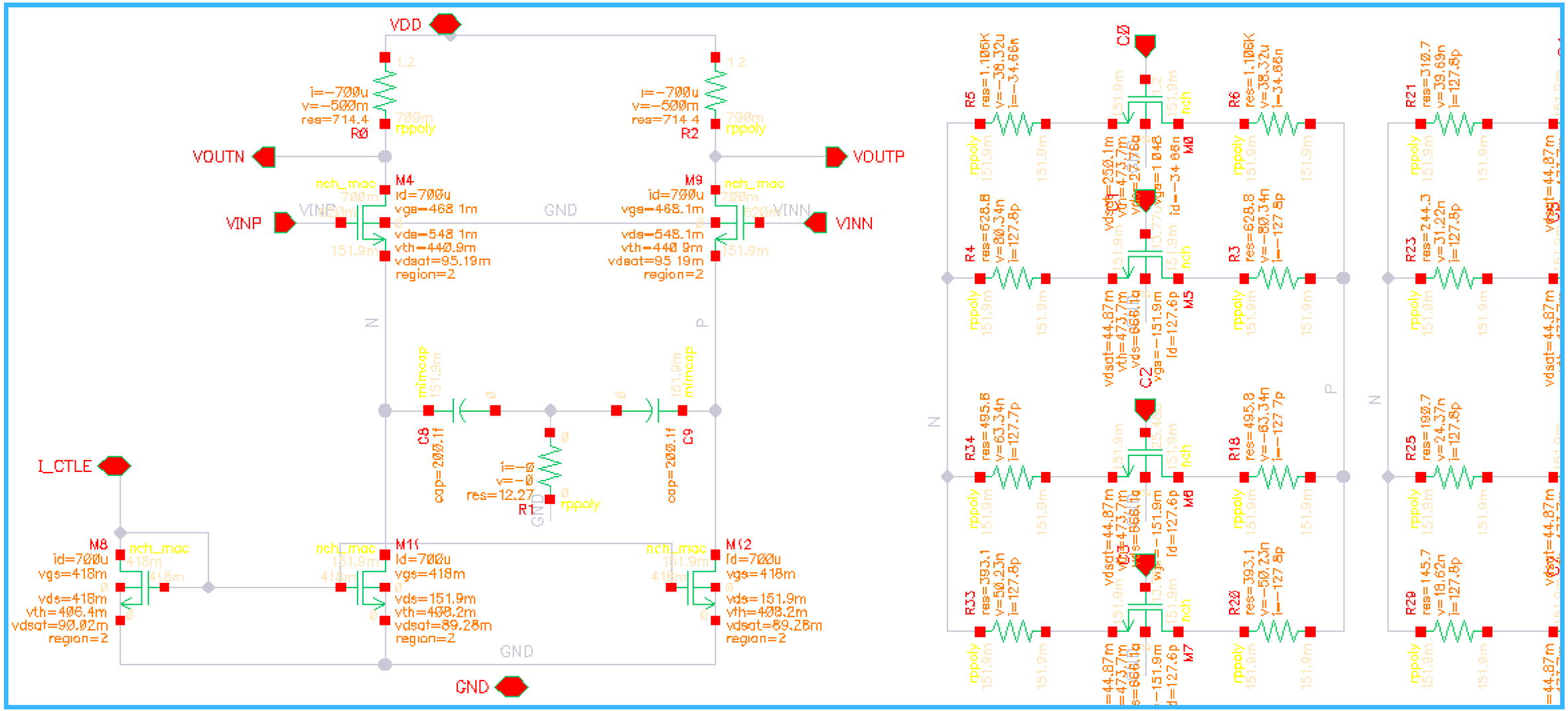


TESTBENCH FOR CTLE (AC AND DC ANALYSIS):



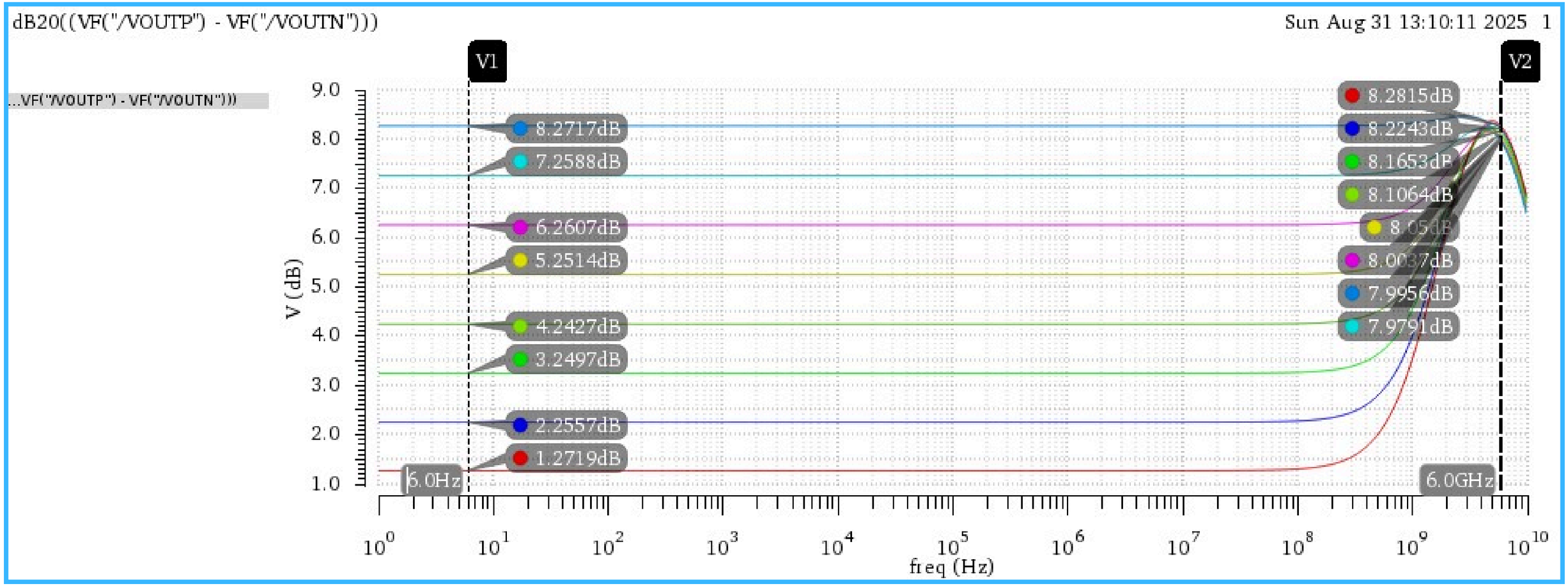
DC ANALYSIS

DC operating point

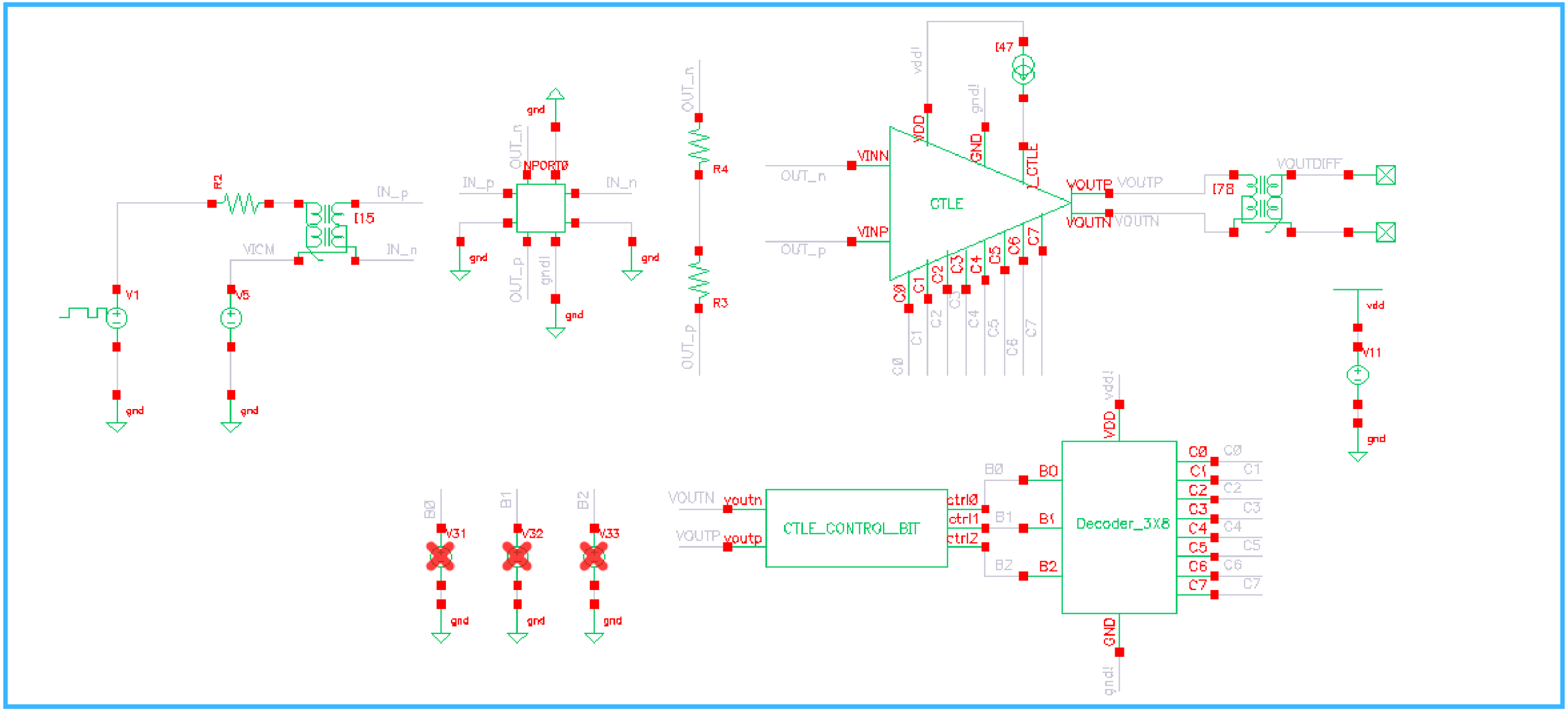


AC ANALYSIS

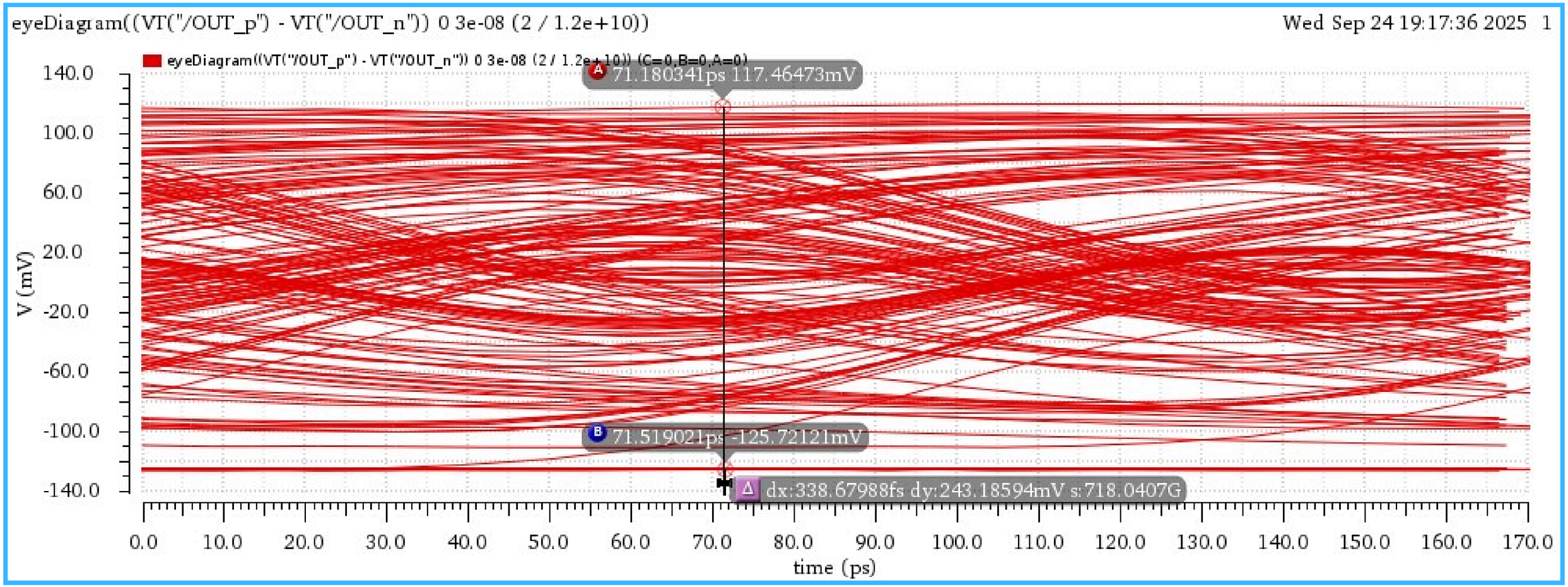
AC response



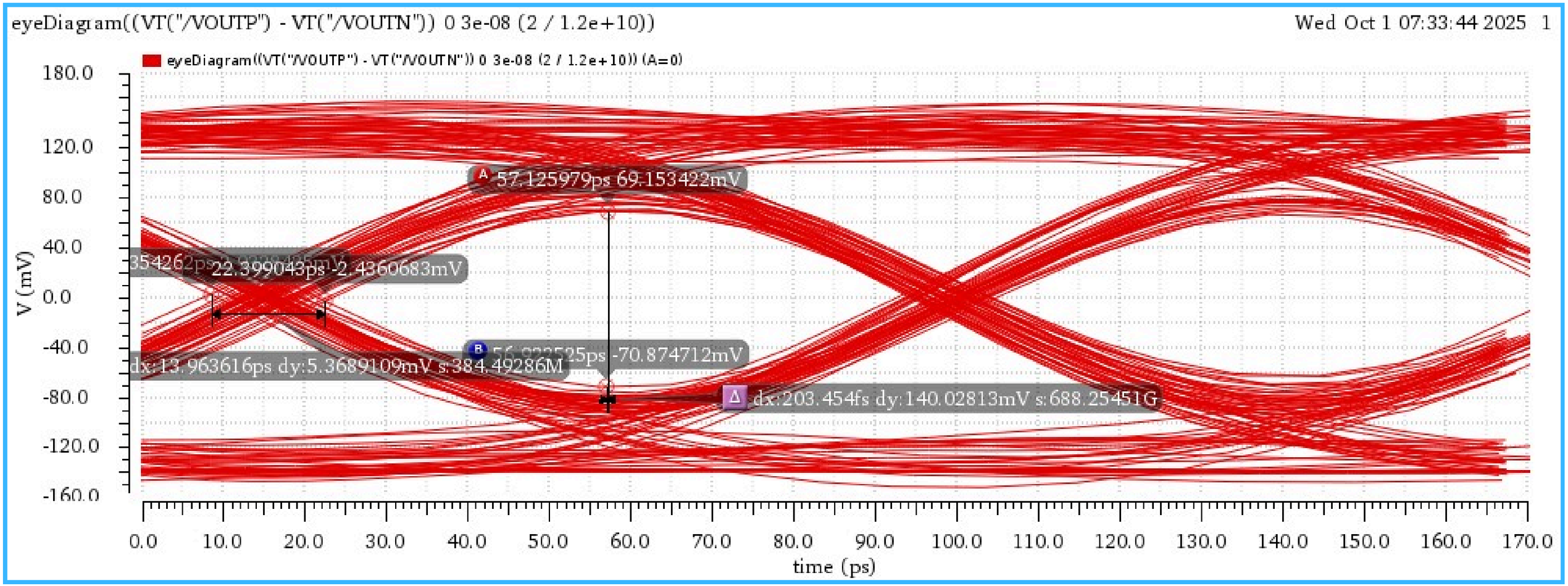
TESTBENCH FOR CTLE (TRANSIENT ANALYSIS):



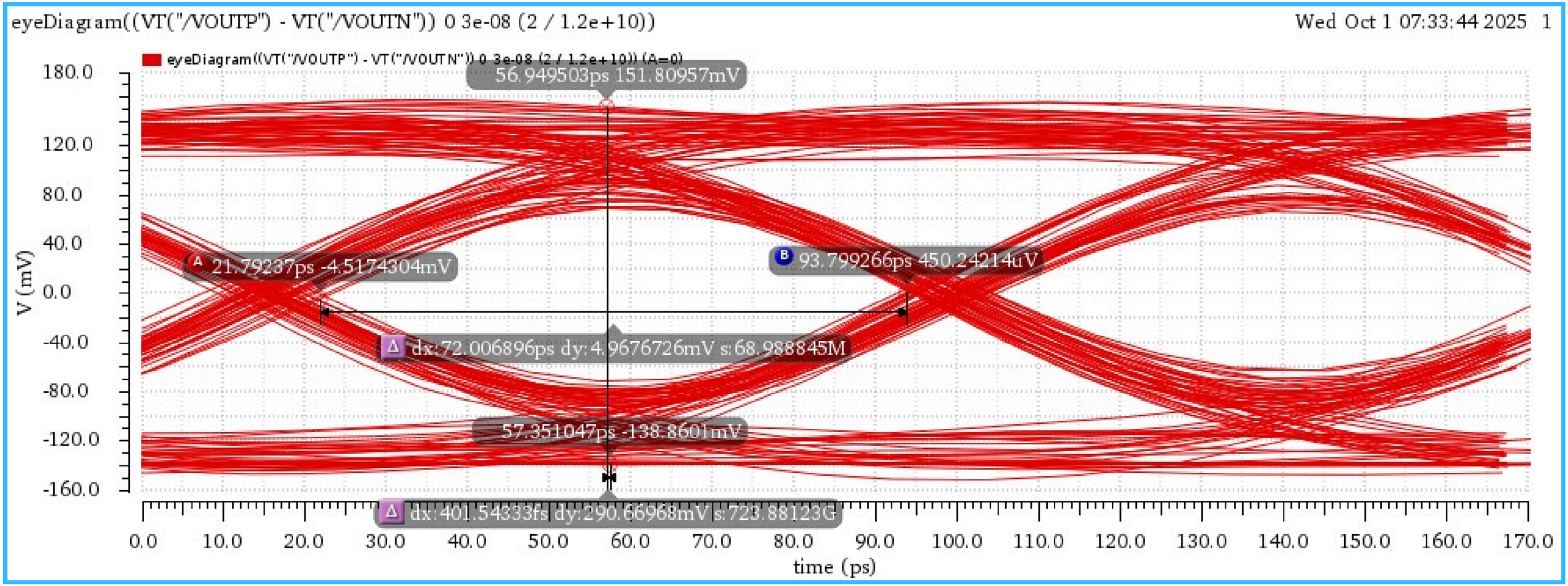
VGA EYE DIAGRAM (BEFORE CTLE)



INNER EYE DIAGRAM OPENING (AFTER CTLE)



OUTER EYE DIAGRAM OPENING (AFTER CTLE)



EYE DIAGRAM RESULT

	Inner Eye Opening	Outer Eye Opening	horizontal Opening	Jitter
Before CTLE	0	242mv	0	∞
After CTLE	140mV	290.7mV	72ps	13.96ps

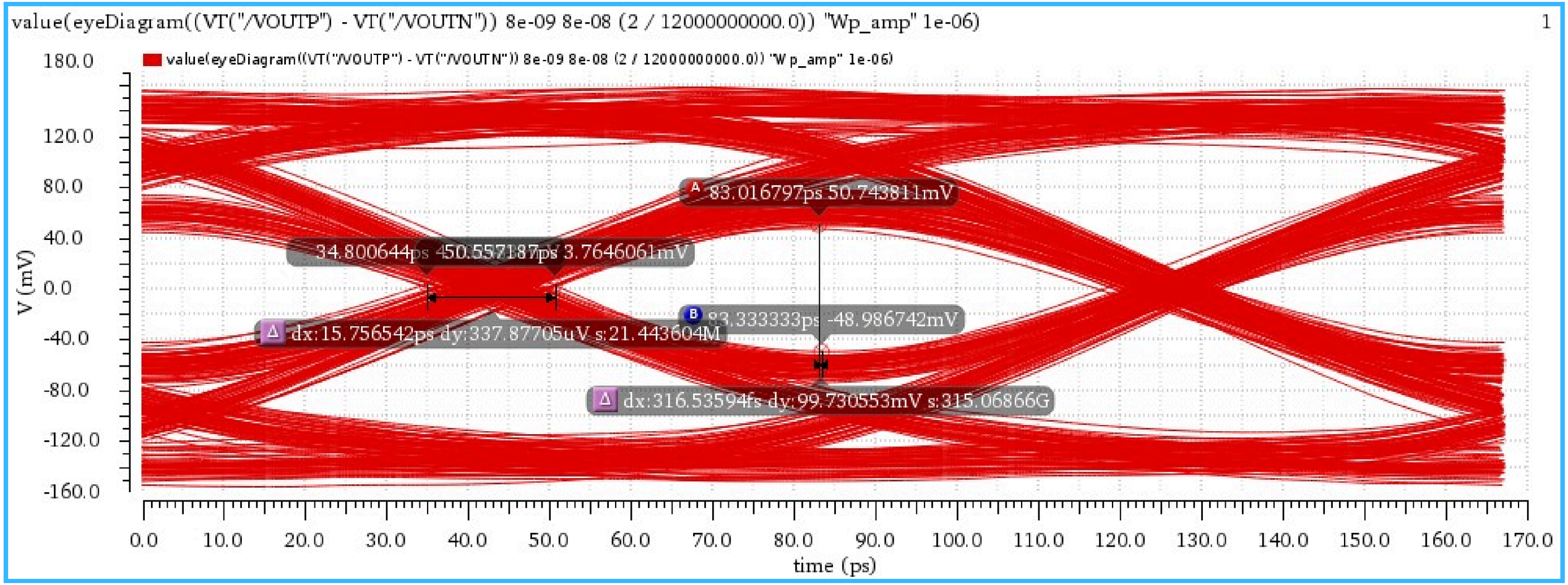
	Eye Opening %
Before CTLE	0%
After CTLE	48.00%

EYE OPENING

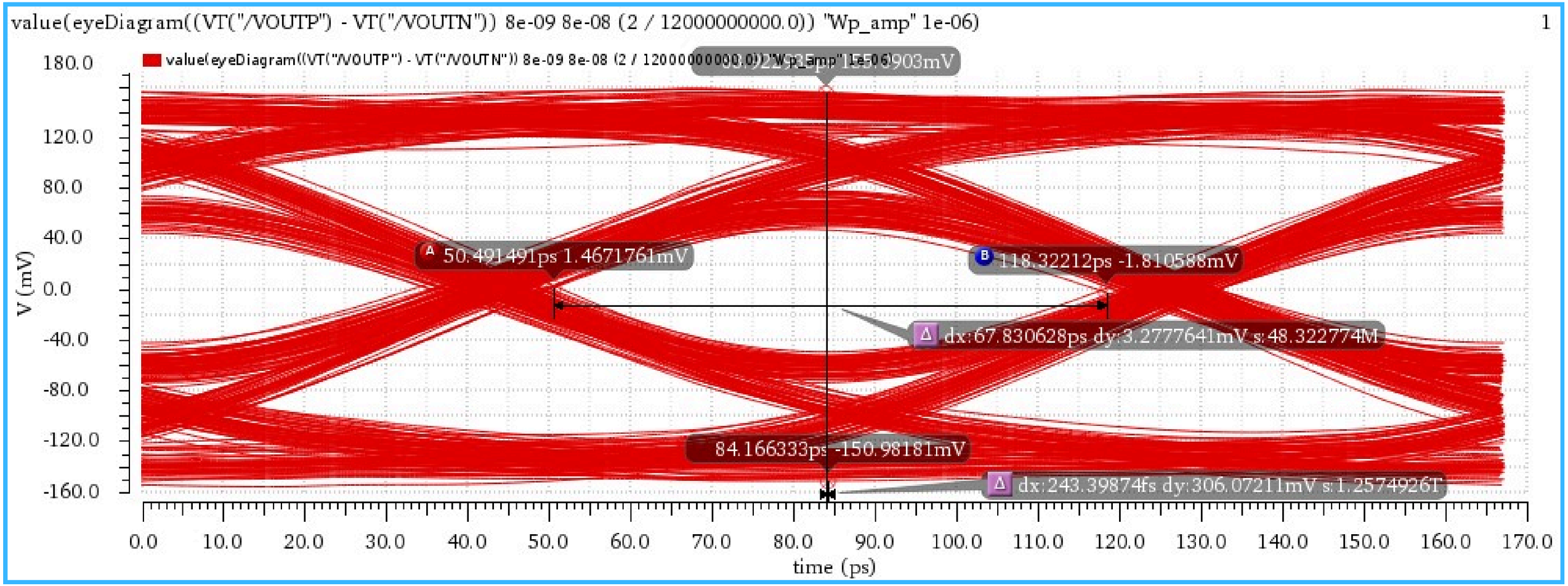
THE BEST Eye Opening FOR CONTROL BIT

	PEAKING	Eye Opening %
000	8dB	48.00%
001	7dB	47.30%
010	6dB	41.10%
011	5dB	35.65%
100	4dB	22.38%
101	3dB	14.15%
110	2dB	7.15%
111	1dB	1%

EYE DIAGRAM OPENING FOR RX



EYE DIAGRAM OPENING FOR RX



EYE DIAGRAM COMPARASION FOR RX

	Inner Eye Opening	Outer Eye Opening	horizontal Opening	Jitter
Before CTLE	0	420mv	0	∞
After CTLE	99.74mV	306mV	67.83ps	15.73ps

	Eye Opening %
Before CTLE	0%
After CTLE	32.60%

POWER CONSUMPTIOM

For VGA :

IDC("/V0/MINUS")*VDC("/vdd!")

	Expression	Value
1	IDC("/V0/MINUS")*VDC("/vdd!")	5.050E-3

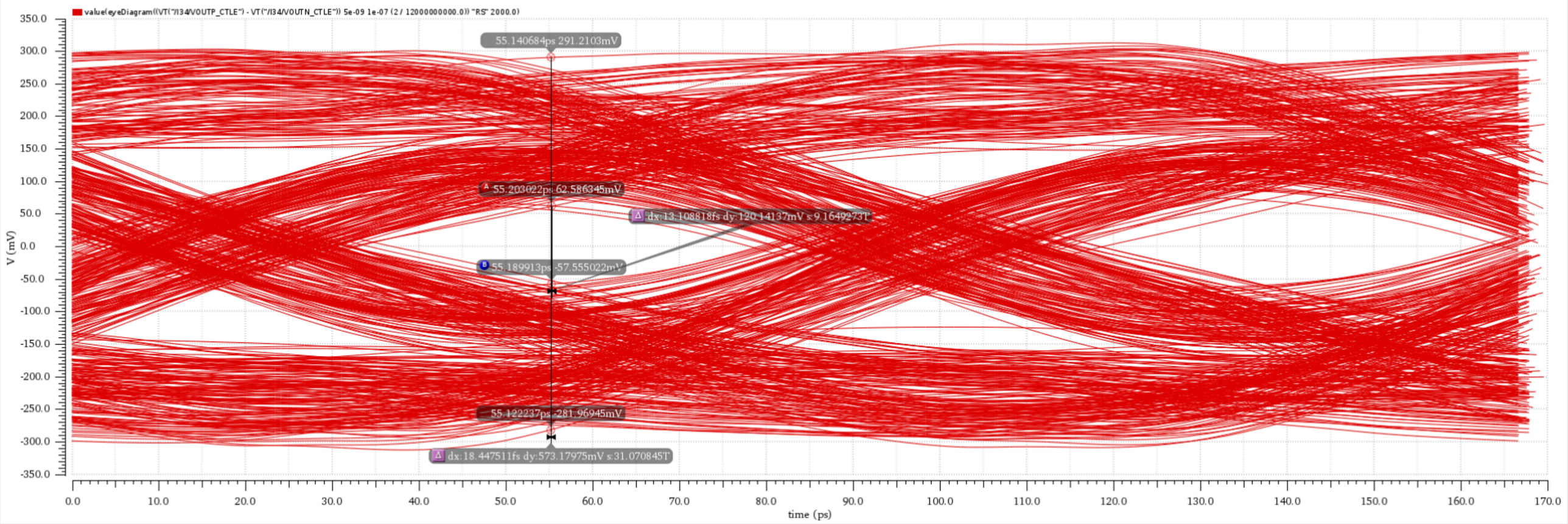
	1
Wnand3	200.0E-9
ymax(dB20(VF("/VOUTP")/VF("/VINP")))	5.325
bandwidth(VF("/VOUTP")/VF("/VINP") 3 "low")	10.42E9
gainBwProd(VF("/VOUTP")/VF("/VINP"))	19.27E9

For CTLE :

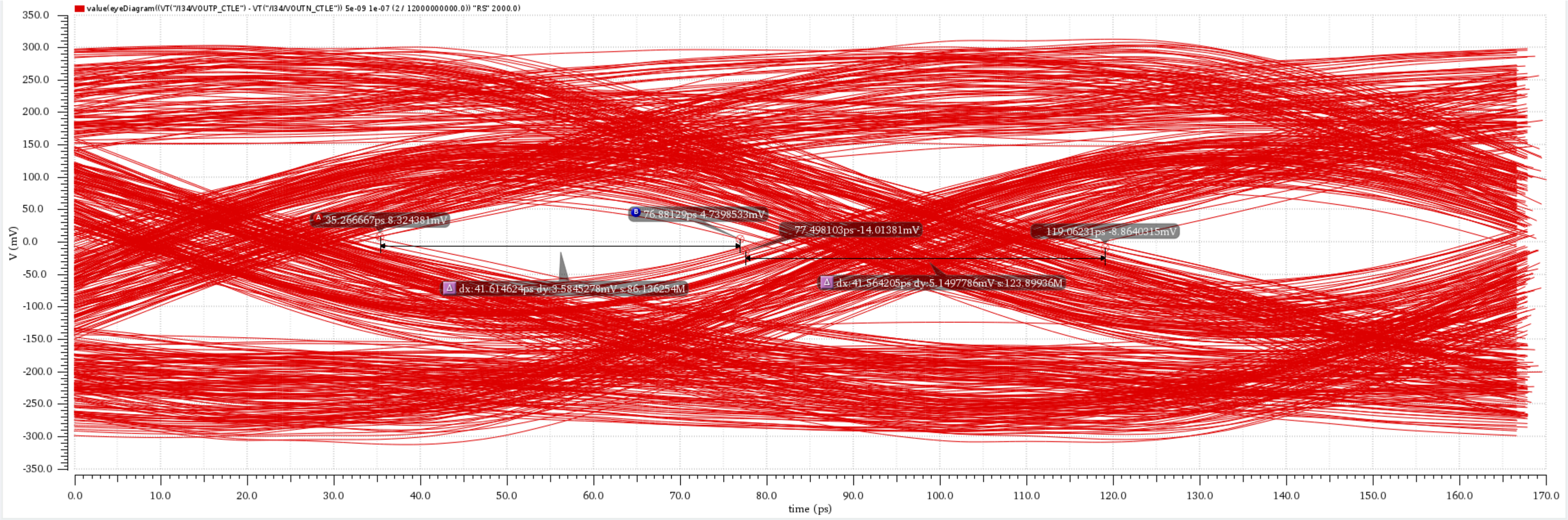
ymax(IT("/V11/MINUS")*VT("/vdd!"))

	A	ymax(IT("/V11/MINUS")*VT("/vdd!"))
1	0.000	2.229E-3

EYE DIAGRAM OPENING INSIDE THE SYSTEM



EYE DIAGRAM OPENING INSIDE THE SYSTEM



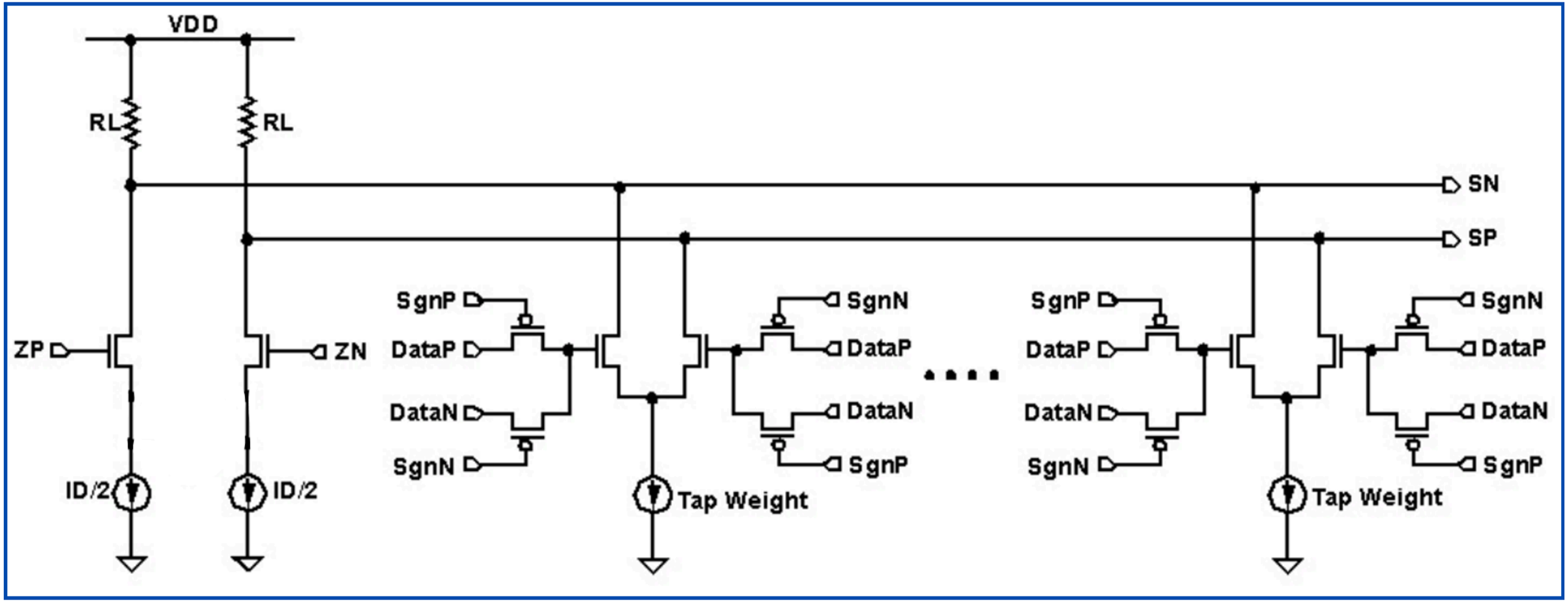
EYE DIAGRAM FROM SYSTEM RESULT

	Inner Eye Opening	Outer Eye Opening	horizontal Opening	Jitter
Before CTLE	0	420mv	0	∞
After CTLE	120.14mV	573.18mV	41.6ps	41.6ps

	Eye Opening %
Before CTLE	0%
After CTLE	21.00%

DECISION FEEDBACK EQUALIZER (DFE) DESIGN

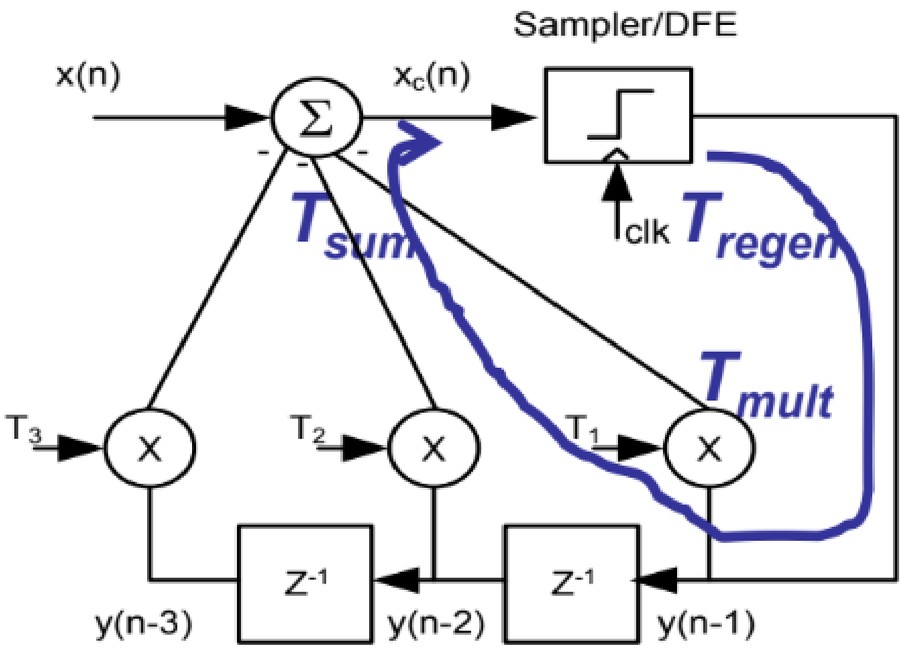
topology


VDD
RL
RL
SN
SP
ZP
ZN
SgnP
DataP
DataN
SgnN
SgnN
DataP
DataN
SgnP
SgnP
DataP
DataN
SgnN
SgnN
DataP
DataN
SgnP
ID/2
ID/2
Tap Weight
Tap Weight

SPECS REQIRED

Number of taps	1-tap
input CM	700m
output CM	700m
Swing	1000m Vp-p
Opening	>40%
tap weight	up to 150m

BIG CHALLENGE

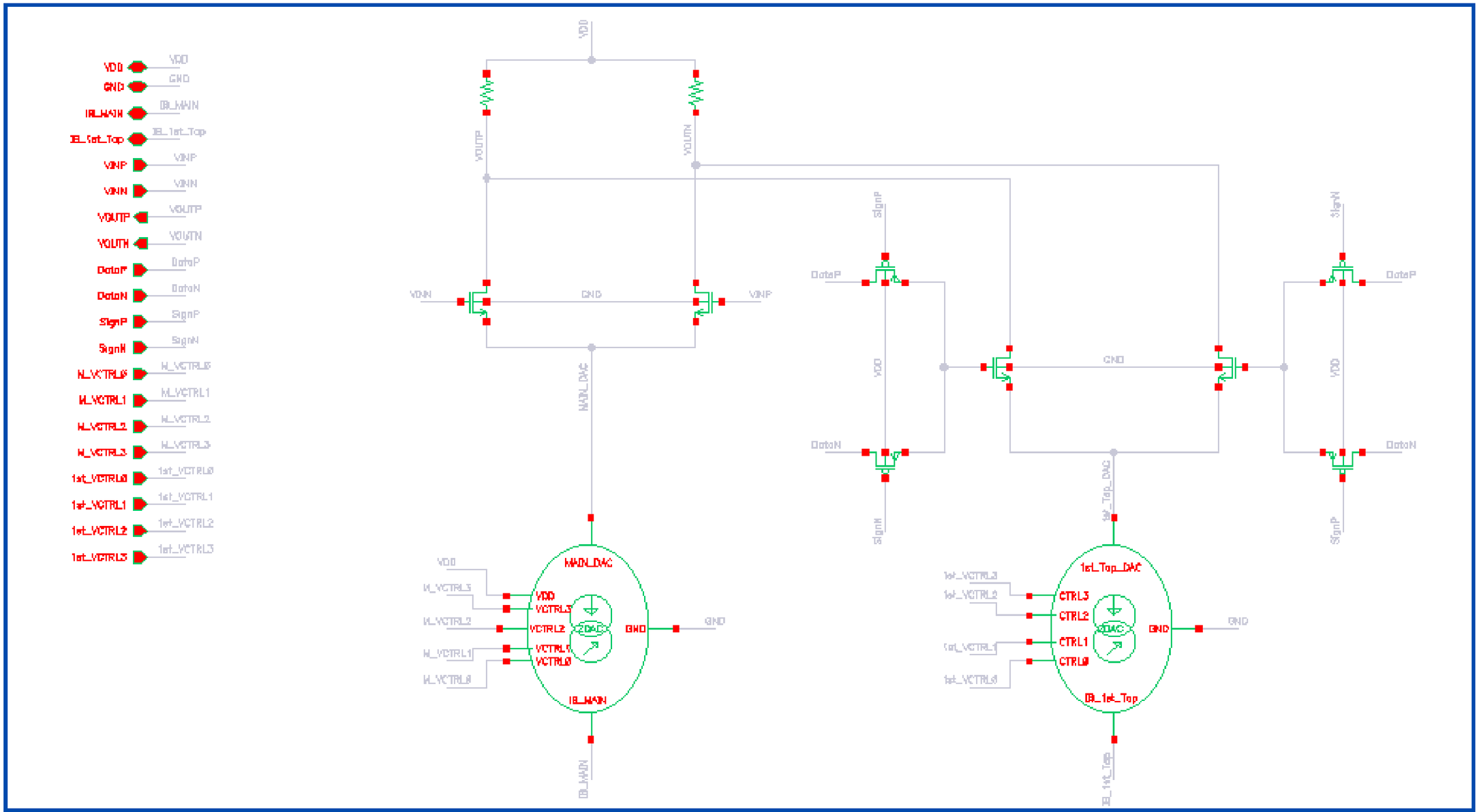


- Once the DFE comparator takes a decision it has to propagate through the multiplier and the summer and be ready before the next clock edge

$$T_{regen} + T_{mult} + T_{sum} + T_{setup} < T_{clk}$$

- T_{setup} is the comparator setup time, and $T_{regen}=T_{ck\text{-}Q}$
- For 12 Gbps, the sum of these delays has to be less than **83.333ps**
- Consequent taps don't have the same tough timing constraint due to the relaxed T_{regen}
- Capacitance at the summing node limits the maximum number of DFE taps

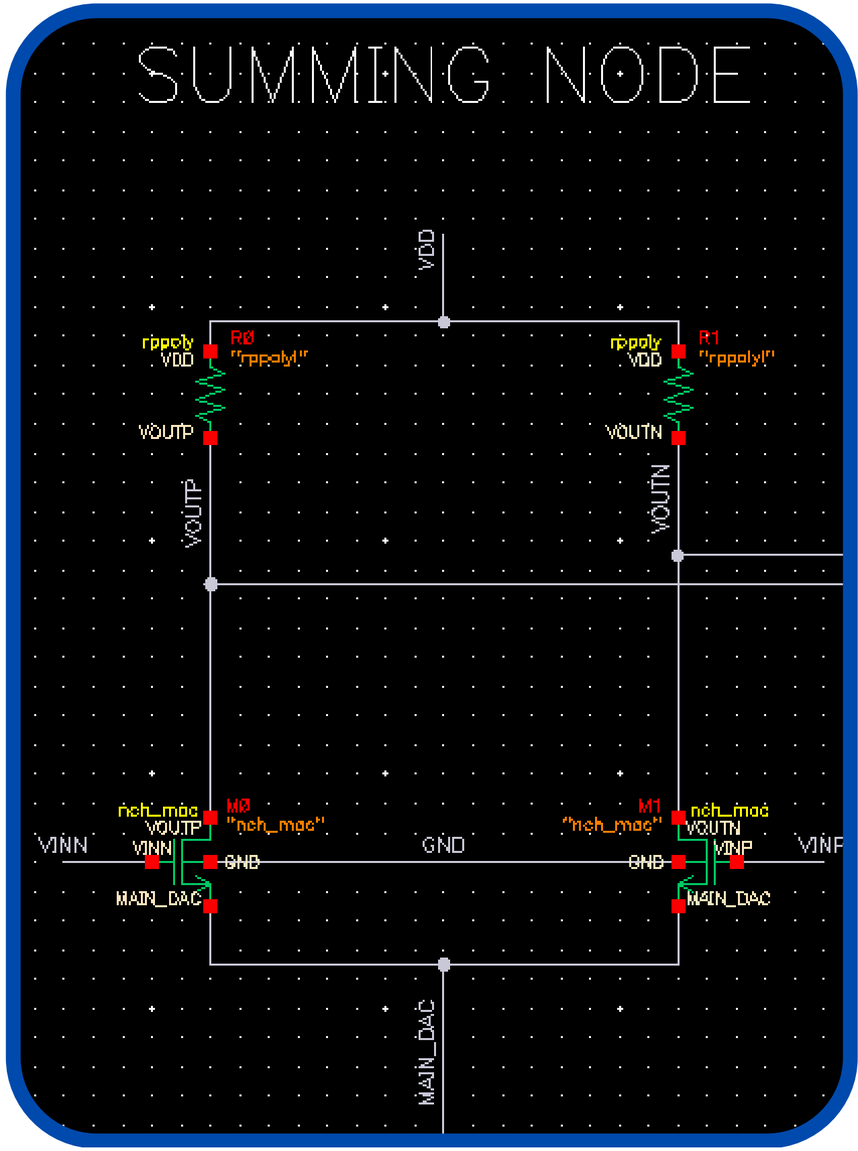
SCHEMATIC OF DFE



SUMMING NODE

The summing node integrates the incoming signal, the main DAC current, and the feedback DAC current. Its transconductance and capacitance are sized to:

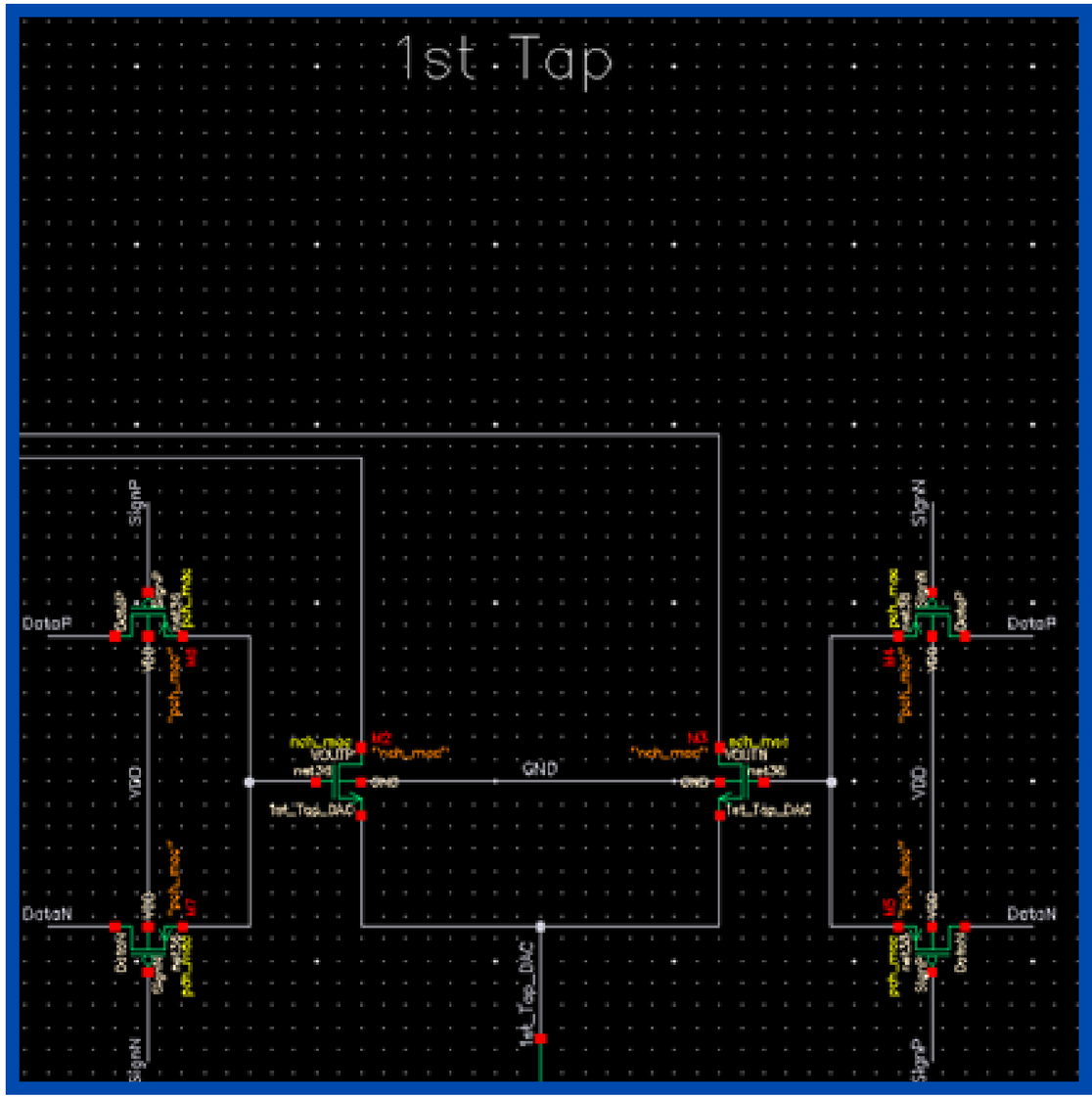
- Provide sufficient bandwidth for the target data rate (e.g., > 12 Gb/s).
- Minimize distortion while maintaining stability.
- RL Chosen to give an output Common-Mode of 700m As Imax/2 pass through it
- Since VCM = (Vcmp+Vcmn)/2 while keeping a strong Swing for the comparator



1ST-TAP

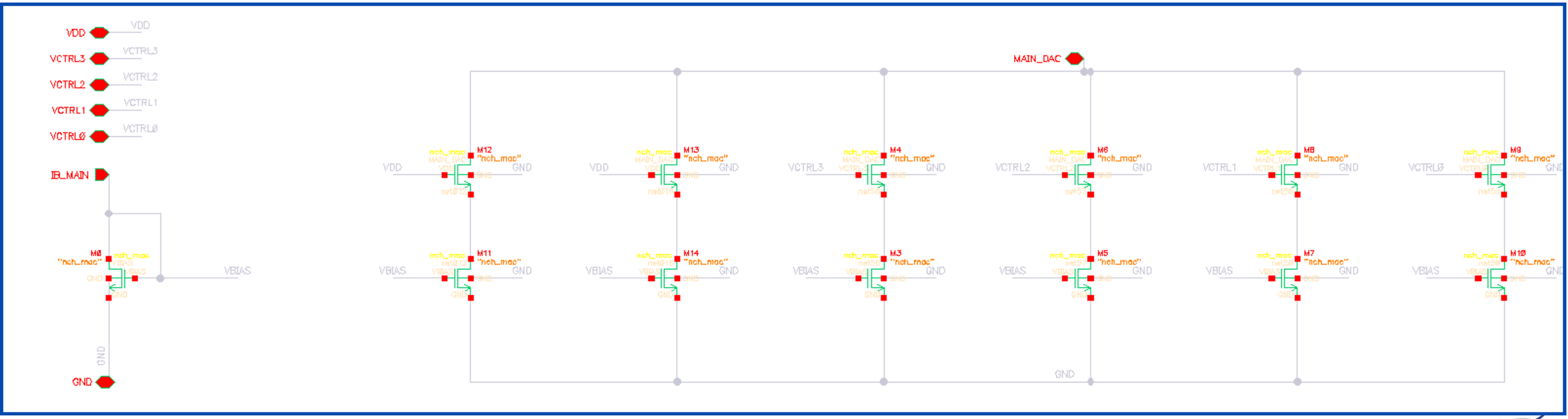
The first tap compensates the post-cursor ISI. It is implemented using a current DAC controlled by the previous decision.

- Feedback strength is proportional to the DAC current and programmable weight.
- Device sizing ensures that the maximum correction current corresponds to ~15% of the main cursor amplitude



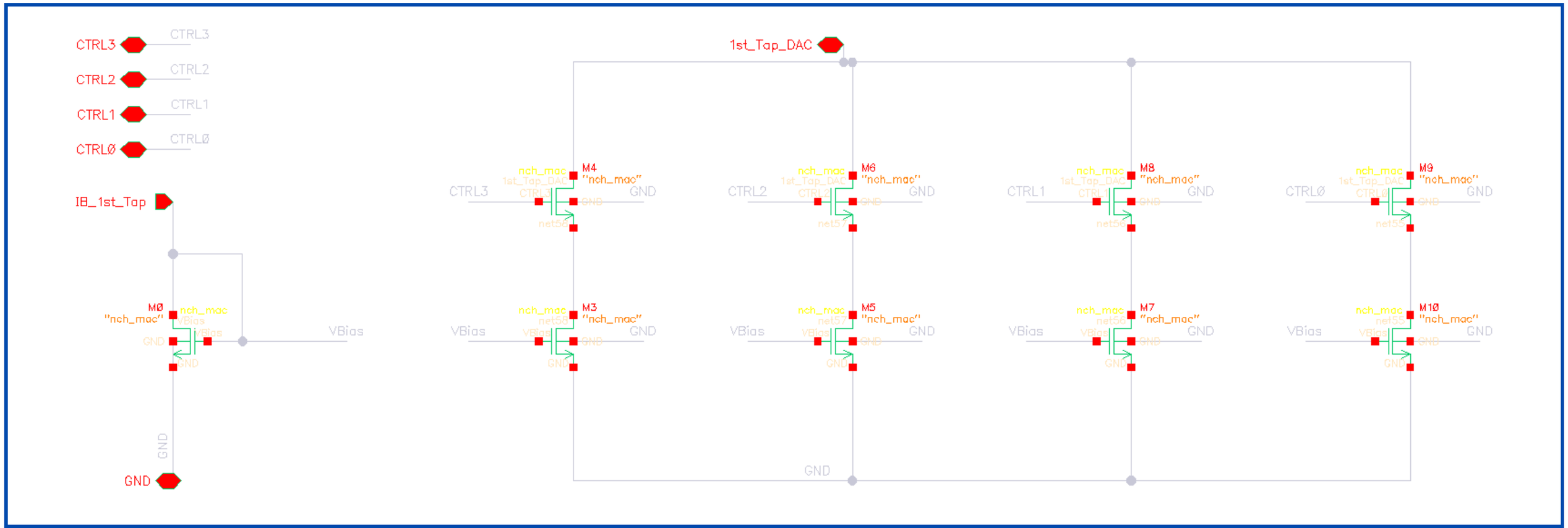
MAIN DAC

- a 4-bit DAC
- Converts digital input sequence (Control signals) into current pulses that feed the summing node.
- Current source sizing chosen for linearity and matching.



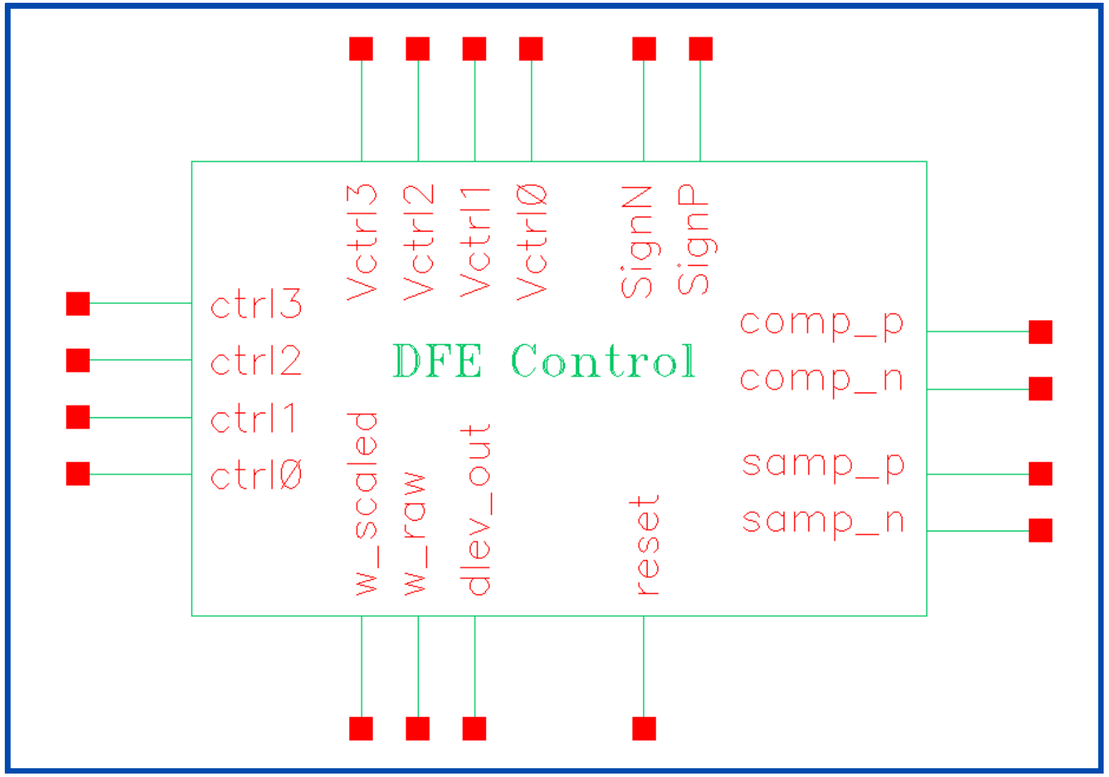
1ST-TAP

- **a 4-bit DAC**
- **Generates compensating current from previous decision using Control signals .**
- **Scaled relative to main DAC (up to 15% of main current).**
- **Current source sizing chosen for linearity and matching.**



CONTROL BLOCK

This module implements a 1-tap decision feedback equalizer (DFE) using the Sign-Sign LMS (SSLMS) adaptation method. At every unit interval, the comparator decision is compared to the analog input, and the sign of the error is used to increment or decrement the feedback weight. In parallel, the decision level (dLev) is adapted with the same sign-based rule to track signal swing and offset. The module exports monitor outputs showing the raw weight, the adapted decision level, and a scaled version of the weight for analysis.



CONTROL BLOCK FLOW CHART

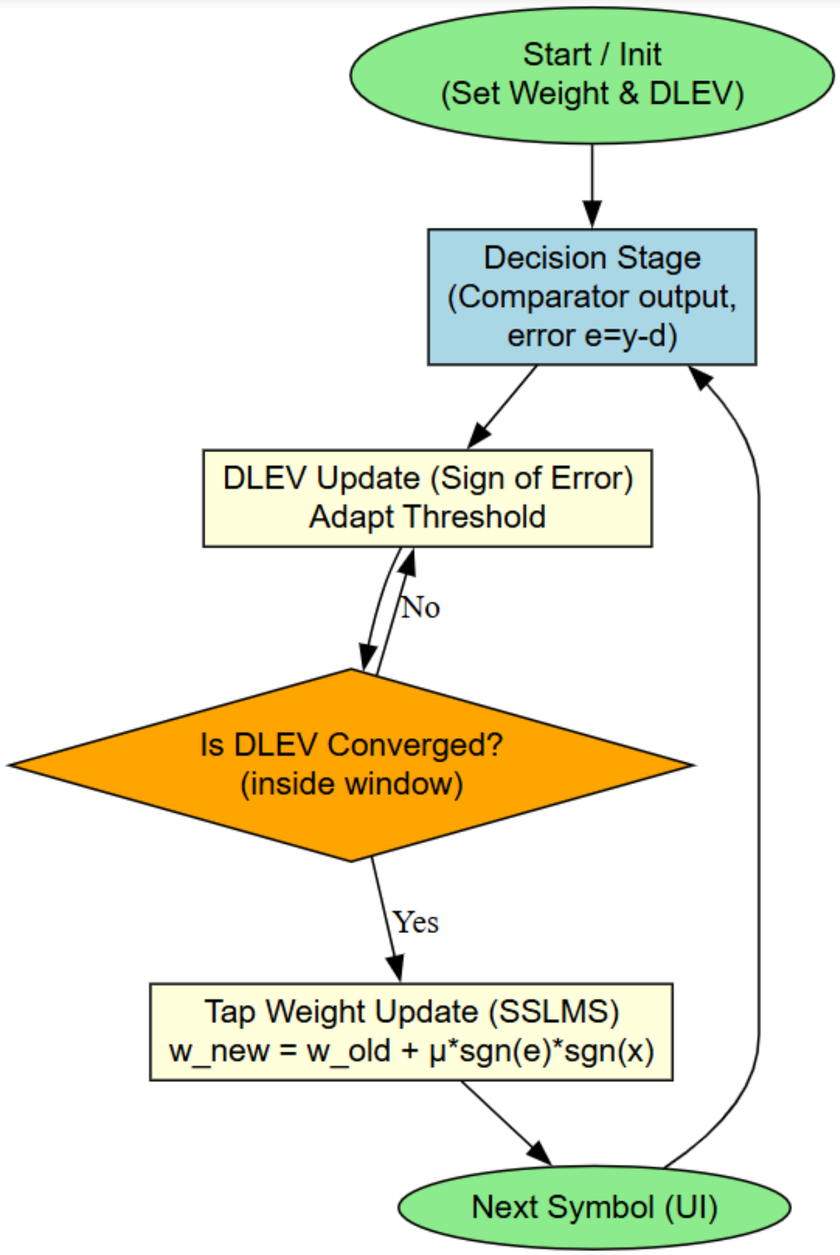
$$dlev_{n+1} = dlev_n + \mu\, x\, sign(e_n)$$

$$e_n = x_c(n) - dlev$$

$$w_{n+1}^k = w_n^k + \Delta_w \text{sign}(d_{n-k})\text{sign}(e_n)$$

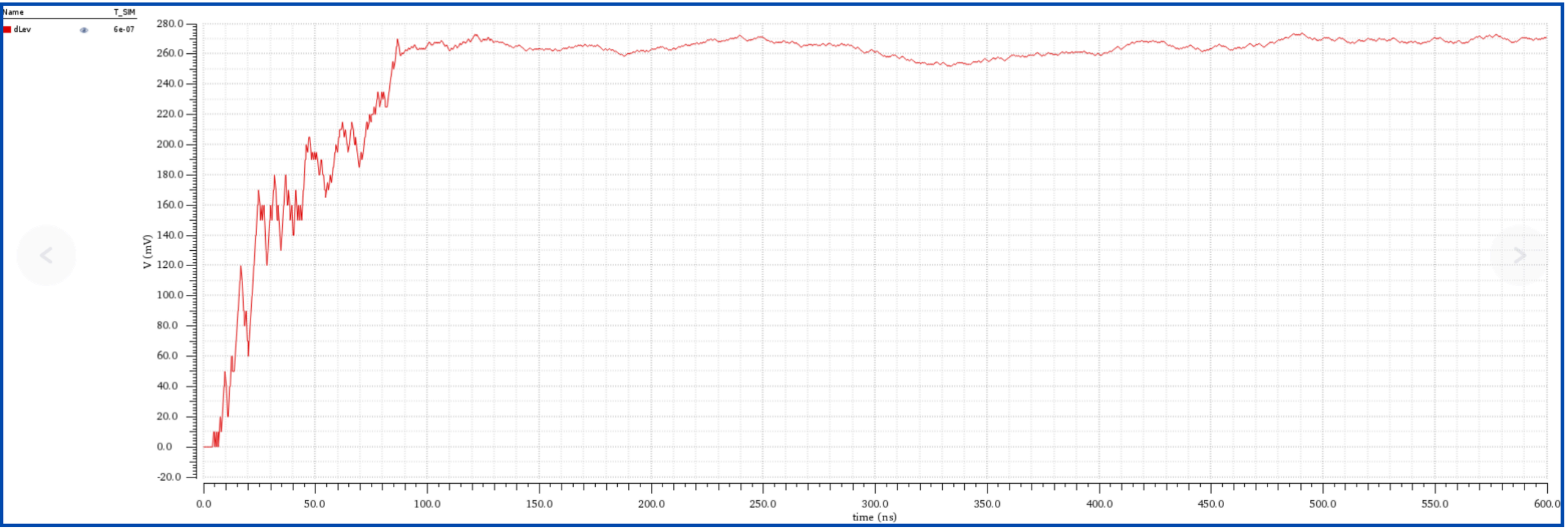
w = tap coefficients, n = time instant, k = tap index, d_n = received data,

e_n = error with respect to desired data level, $dLev$



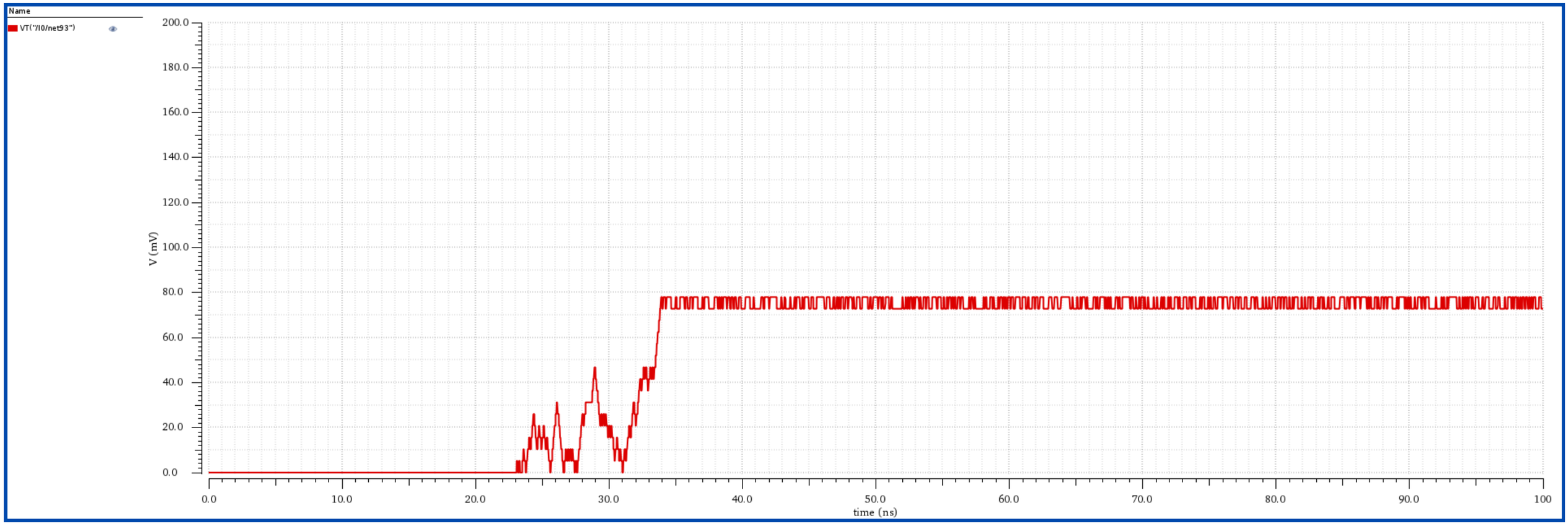
SIGN-SIGN LMS

DLEV behavior with Dynamic Coefficient

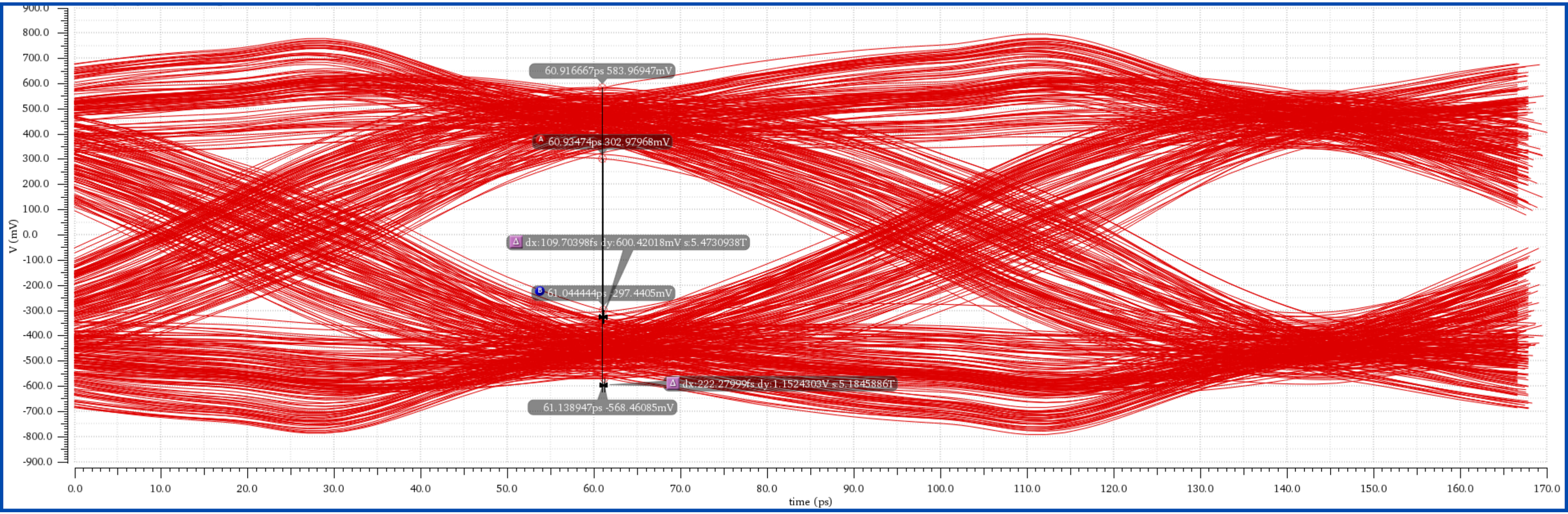


SIGN-SIGN LMS

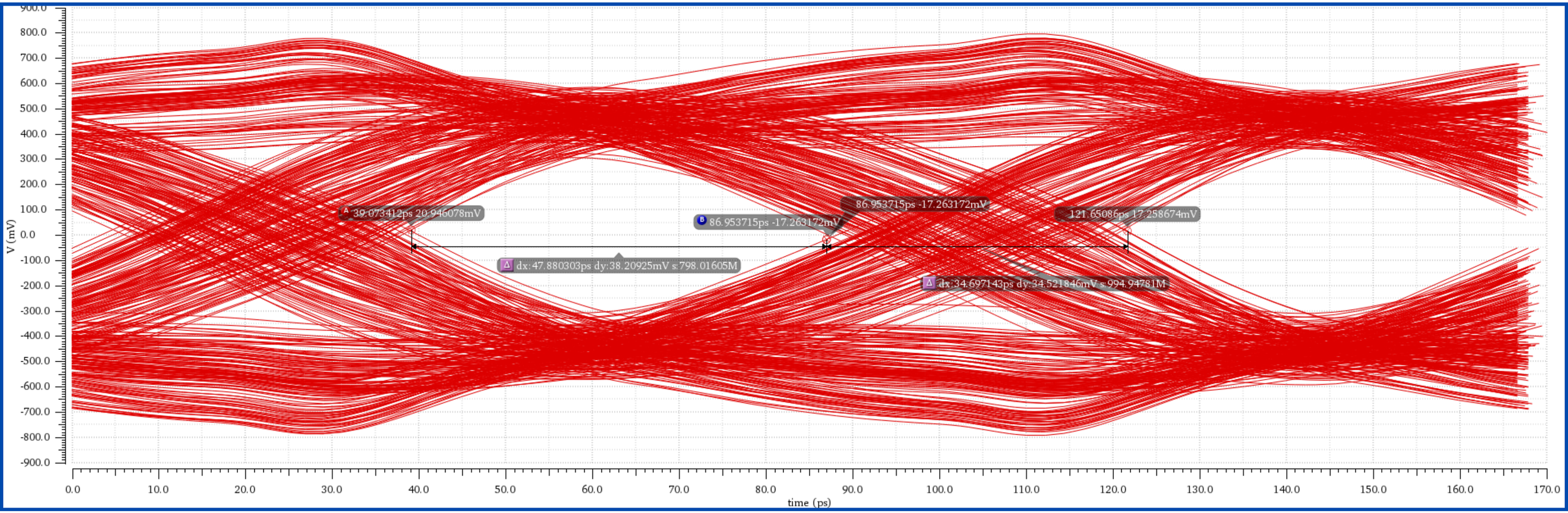
1st Tap Weight behavior



EYE DIAGRAM AT SUMMING NODE



EYE DIAGRAM AT SUMMING NODE



EYE RESULT AT SUMMING NODE

Vertical opening

	Inner Eye Opening	Outer Eye Opening	Eye Opening %
Before DFE	120.14mV	573.188mV	21%
After DFE	600.4mV	1.1524V	52.10%

EYE RESULT AT SUMMING NODE

Horizontal opening and jitter

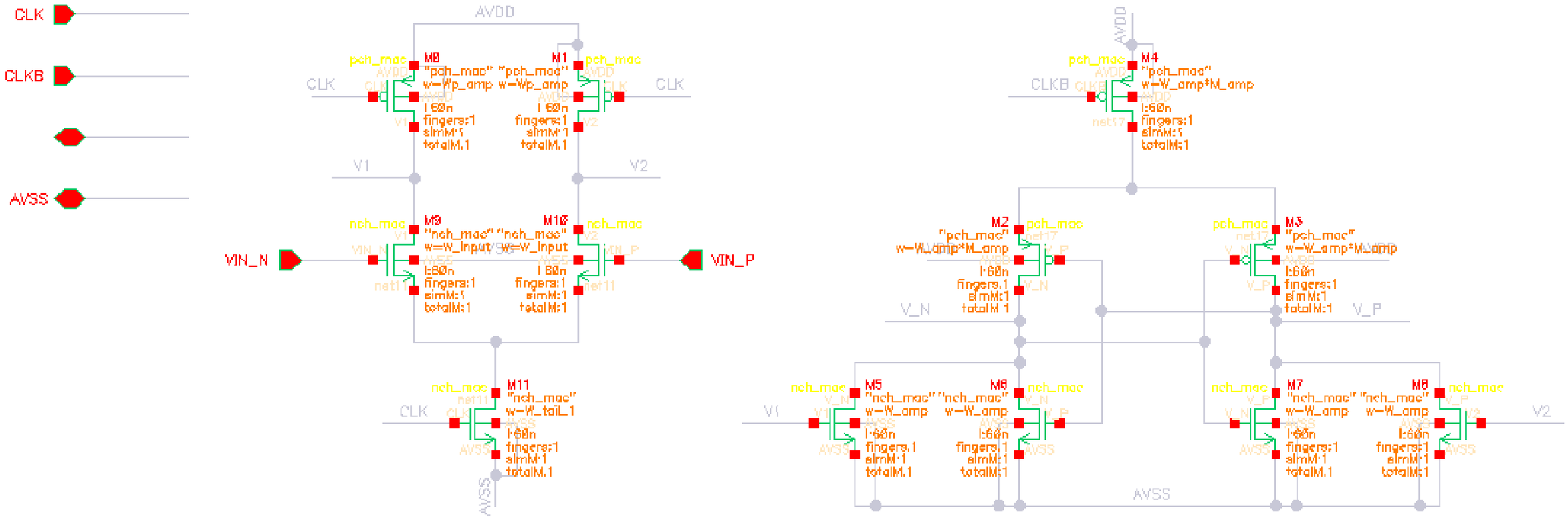
	Eye Opening	Jitter
Before DFE	41.6ps	41.6ps
After DFE	47.8ps	34.6ps

POWER CONSUMPTION

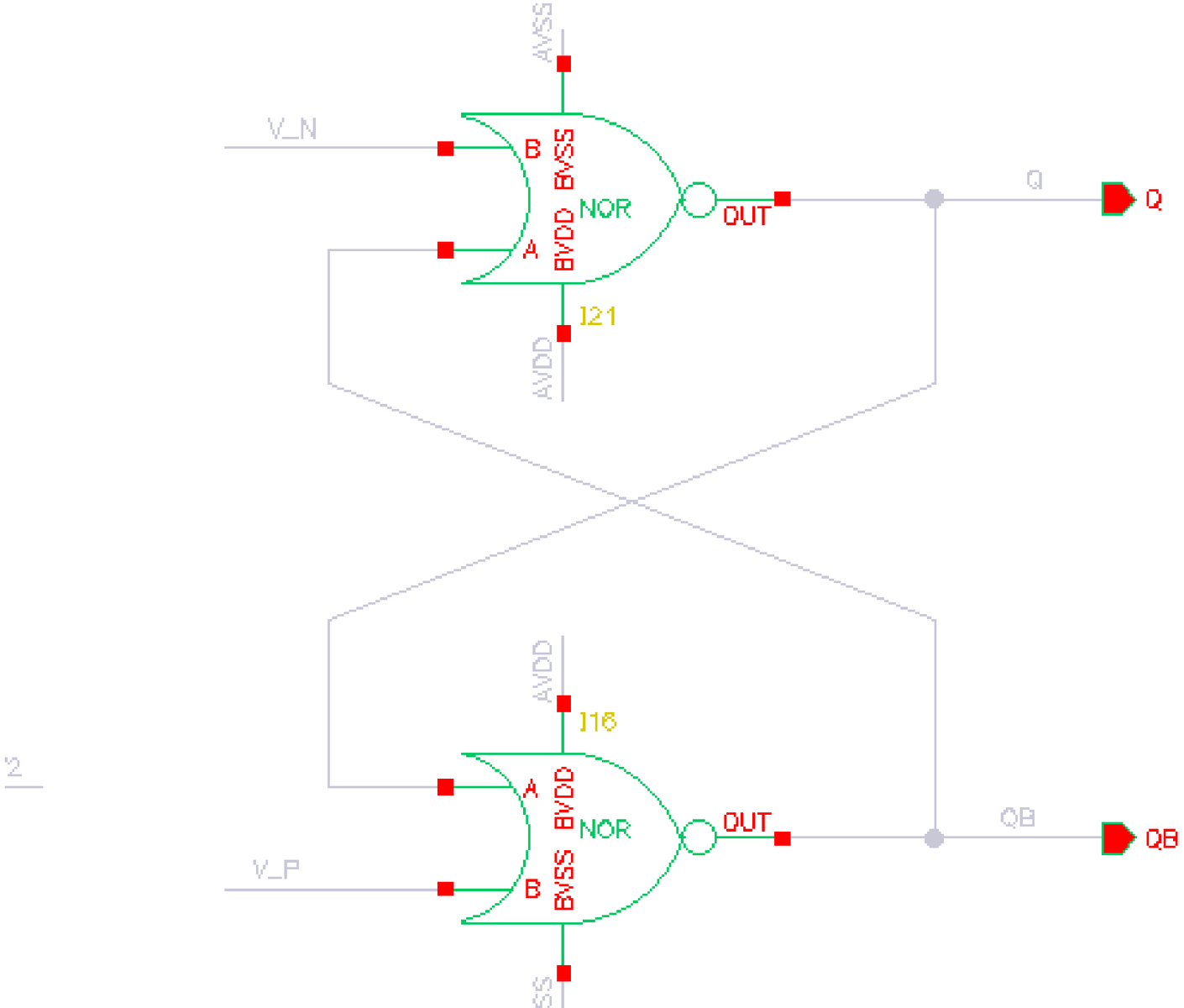
Power Consumption	3.651mW
Area	242.77 um2
Path Latency	62.24 ps
Energy per bit	0.3 pJ/bit

COMPARATOR DESIGN

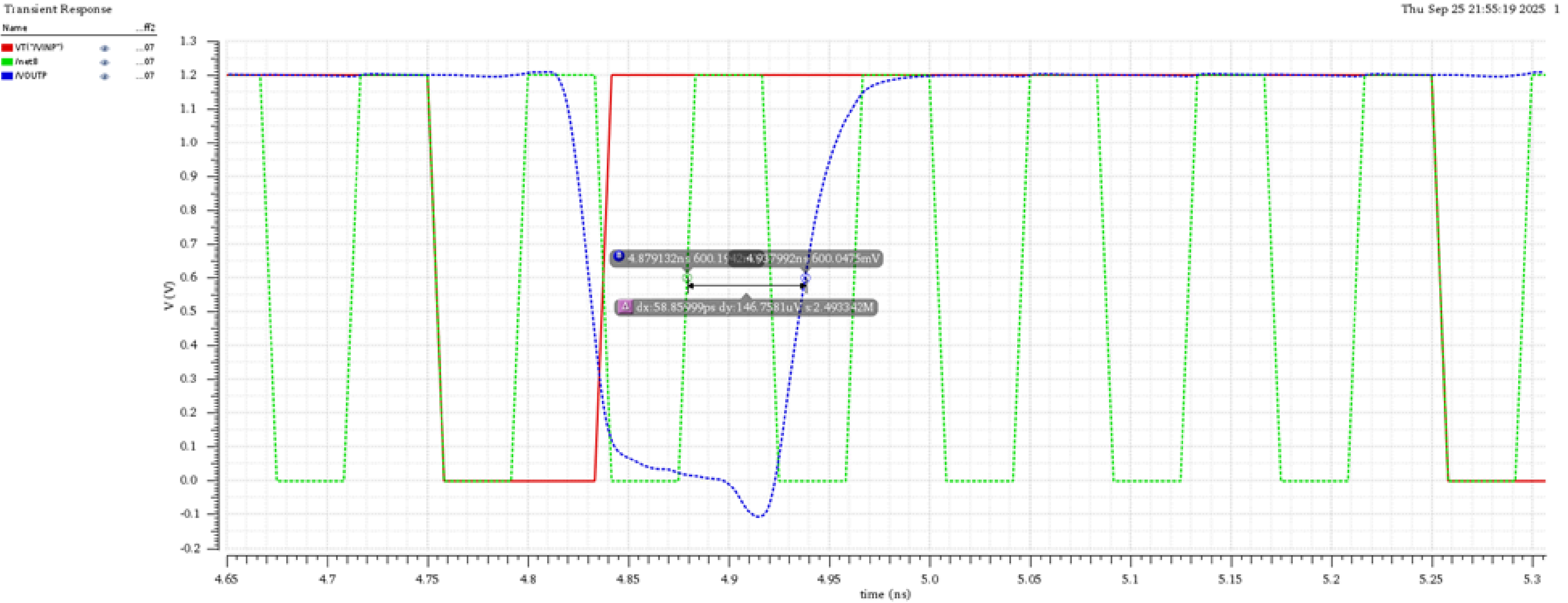
COMPARATOR SCHEMATIC



LATCH SCHEMATIC

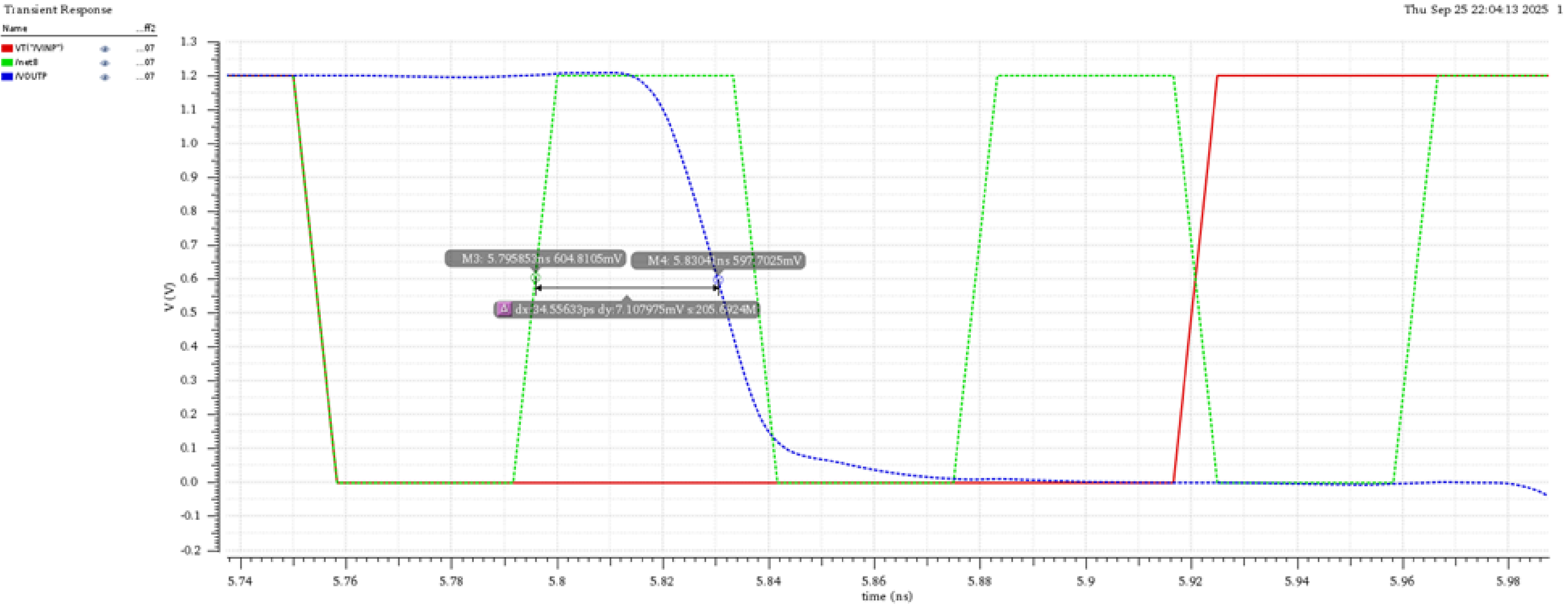


DELAY



- **Rising delay =** 58.86 ps

DELAY



- **falling delay =** 34.56 ps

Average delay = 46.71 ps

DELAY

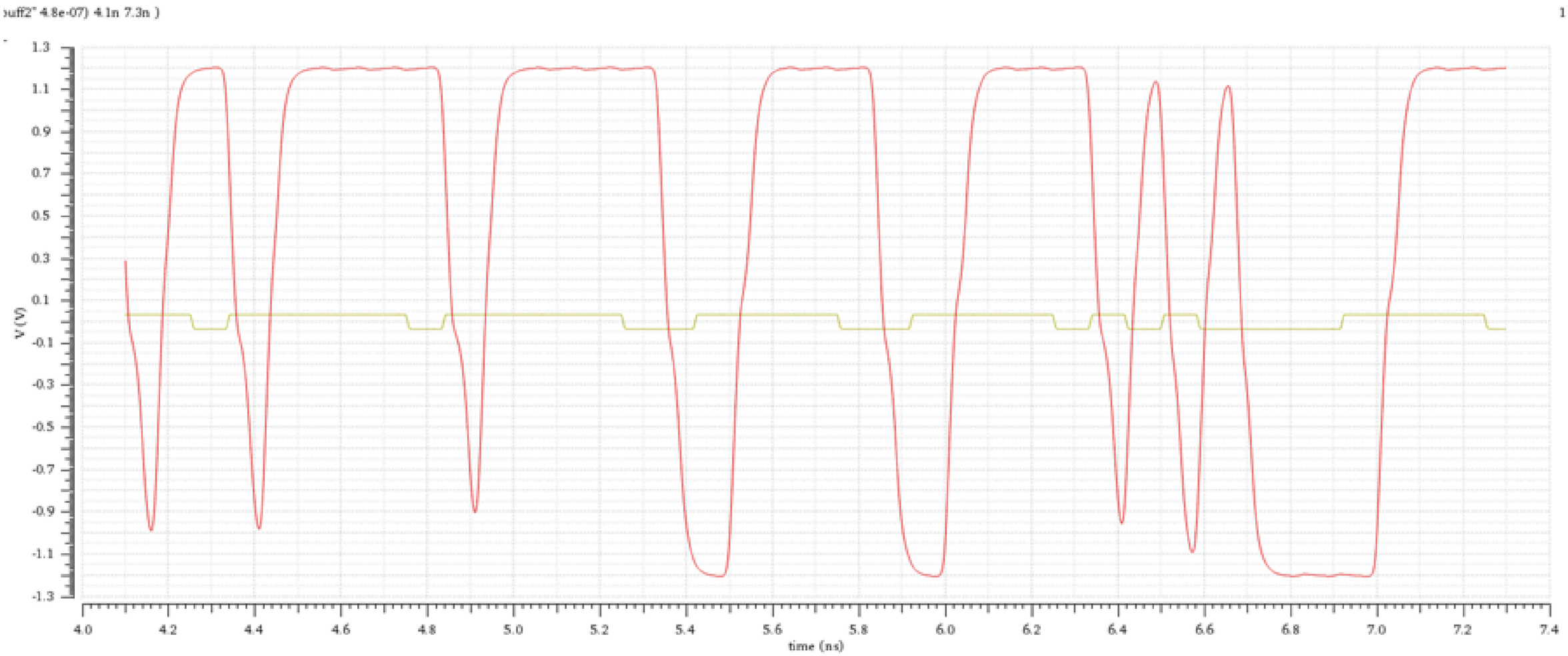
- **Average delay :**
  - For one comparator : 47.3 ps
  - For two comparators : 129 ps

- We see that there is one clock extra delay if we add another comparator because the second comparator samples the output of the first comparator not the input signal , this may cause a problem in the sampling the deserializer but we can fix it by delaying the deserializer clock.

THE POWER CONSUMPTION IN 2 NS :

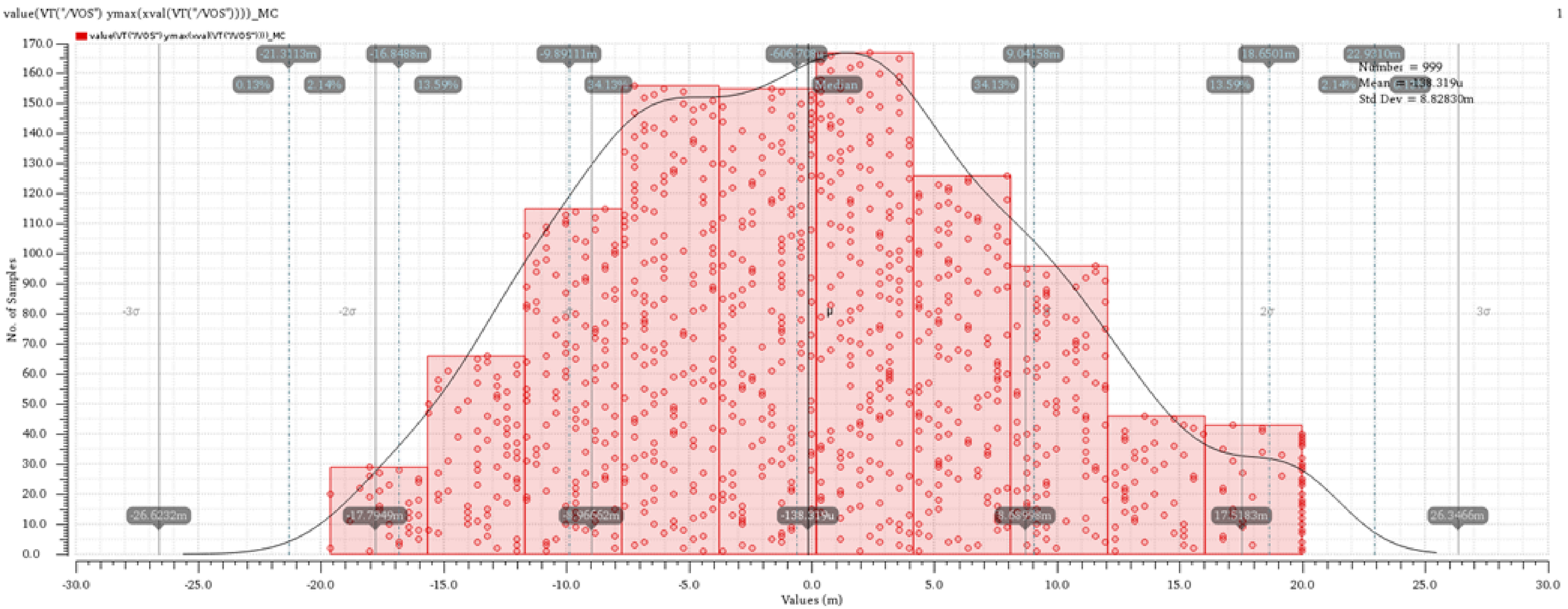
power	75.17u

SENSITIVITY



Practically the minimum input swing required for the output to reach its maximum value of 1.2V is 34 mV

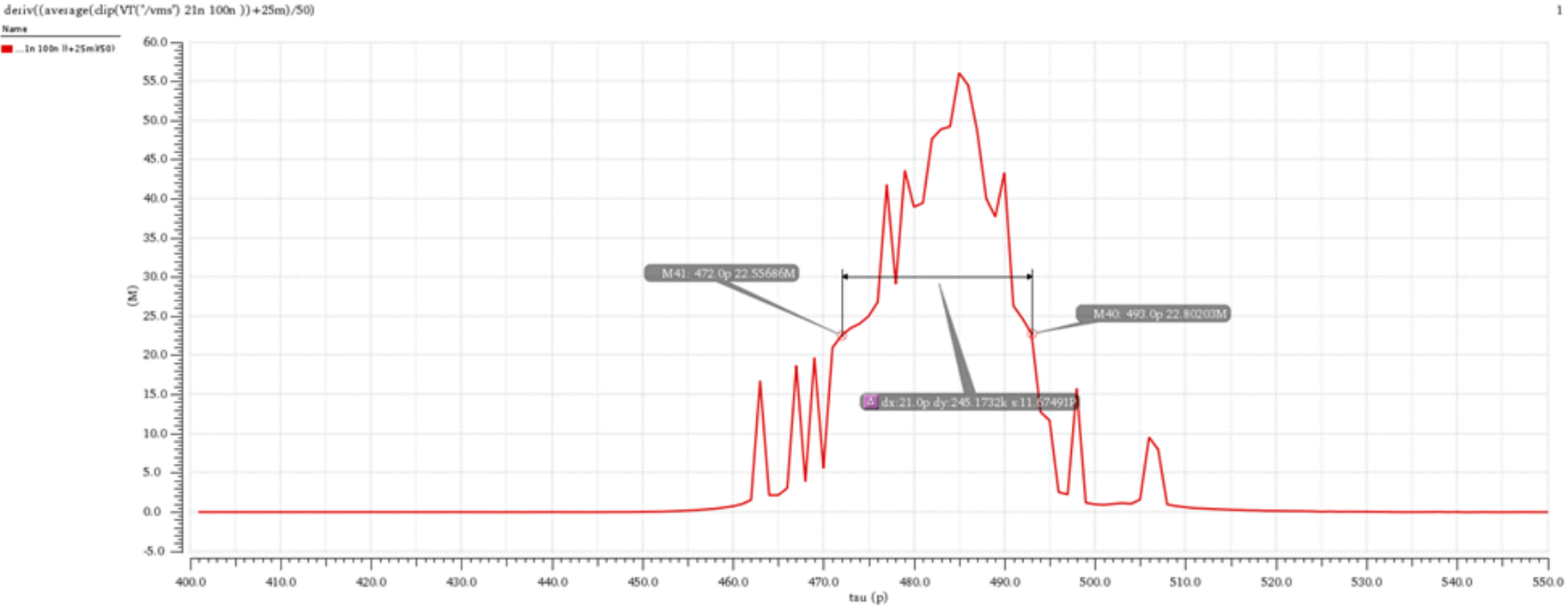
OFFSET VOLTAGE

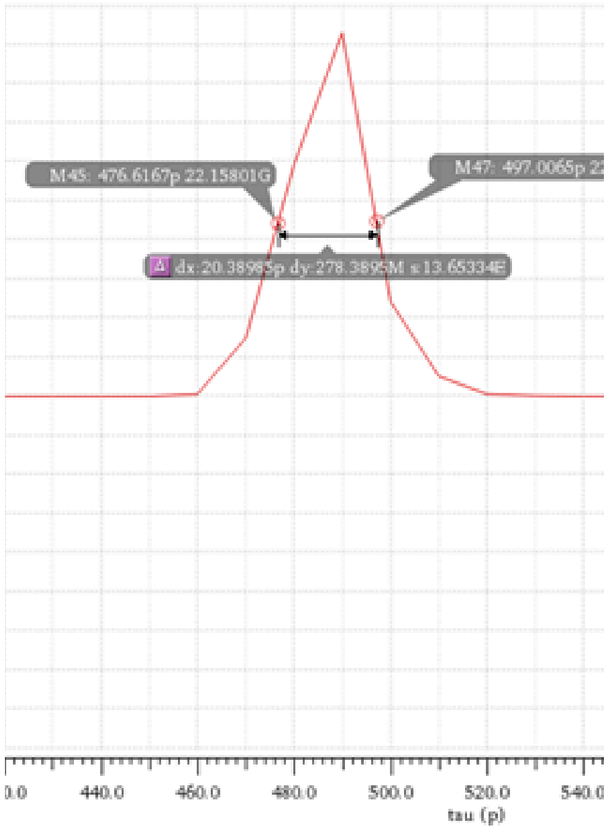


Mean = -0.138 mV

Standard deviation = 8.828mV (one sigma)

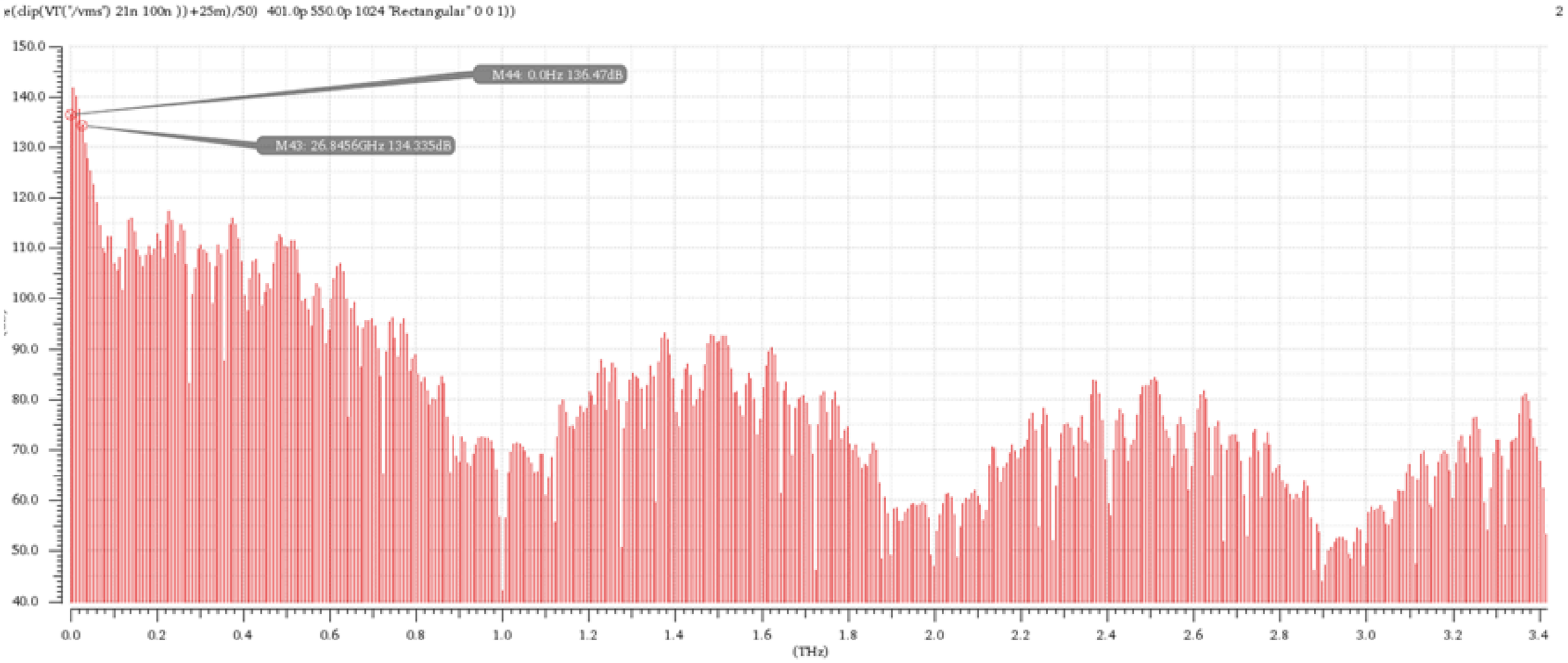
ISF





Aperture time = 21 ps

ISF BANDWIDTH



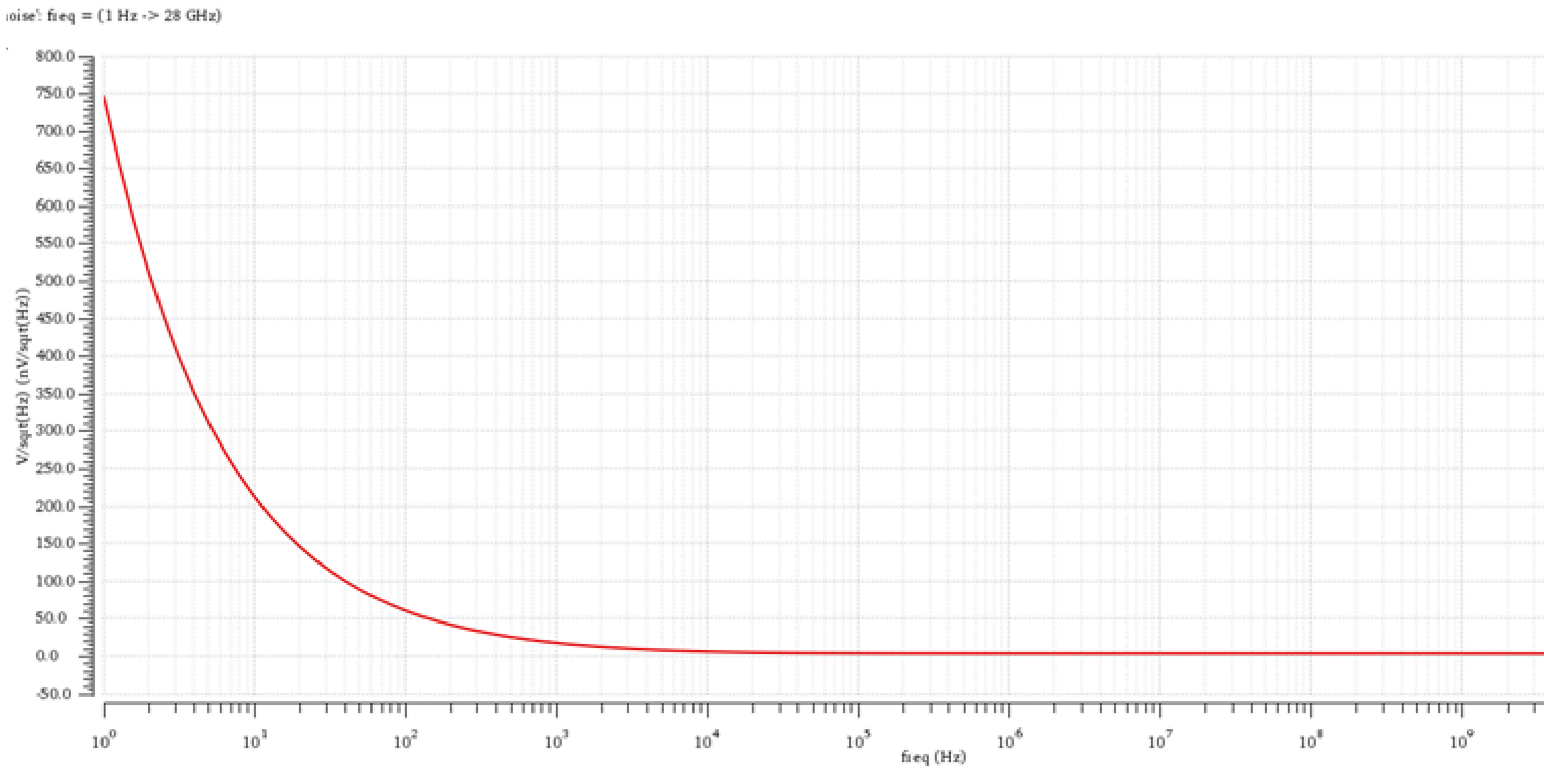
Bandwidth = 26.8GHz

NOISE ANALYSIS

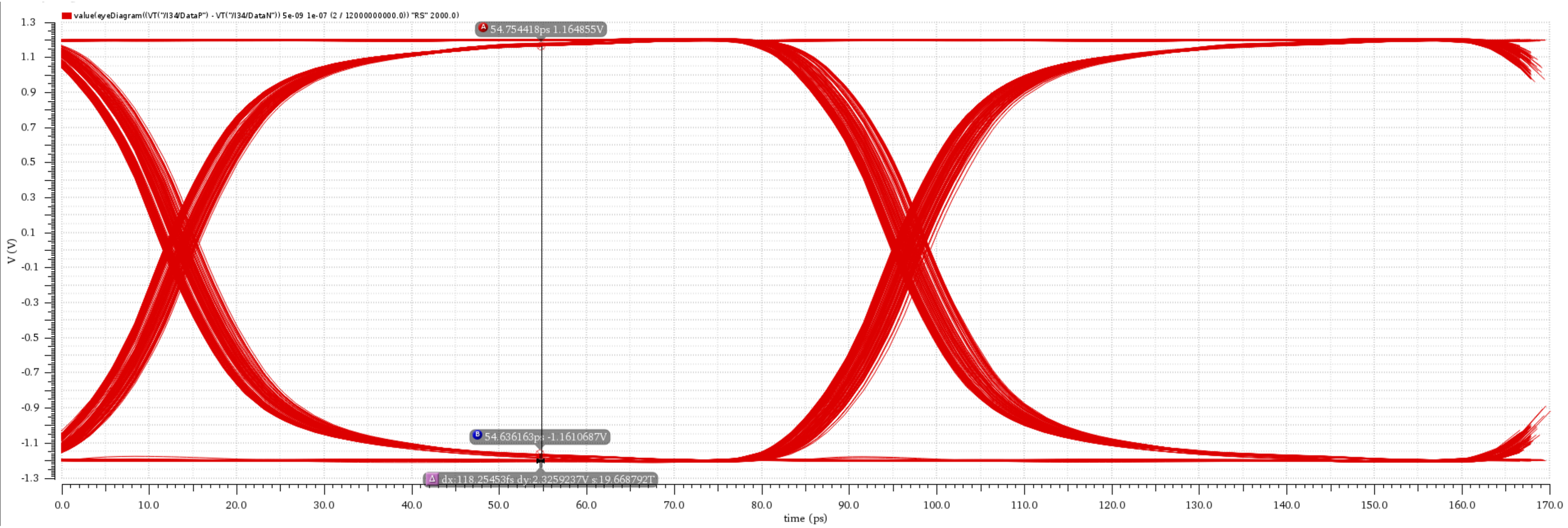
- Running PSS analysis
  - setting the differential input = 40mV.
  - The differential output = 410m , so the periodic DC gain = 10.25 v/v

- Running pnoise simulation
  - output referred noise :

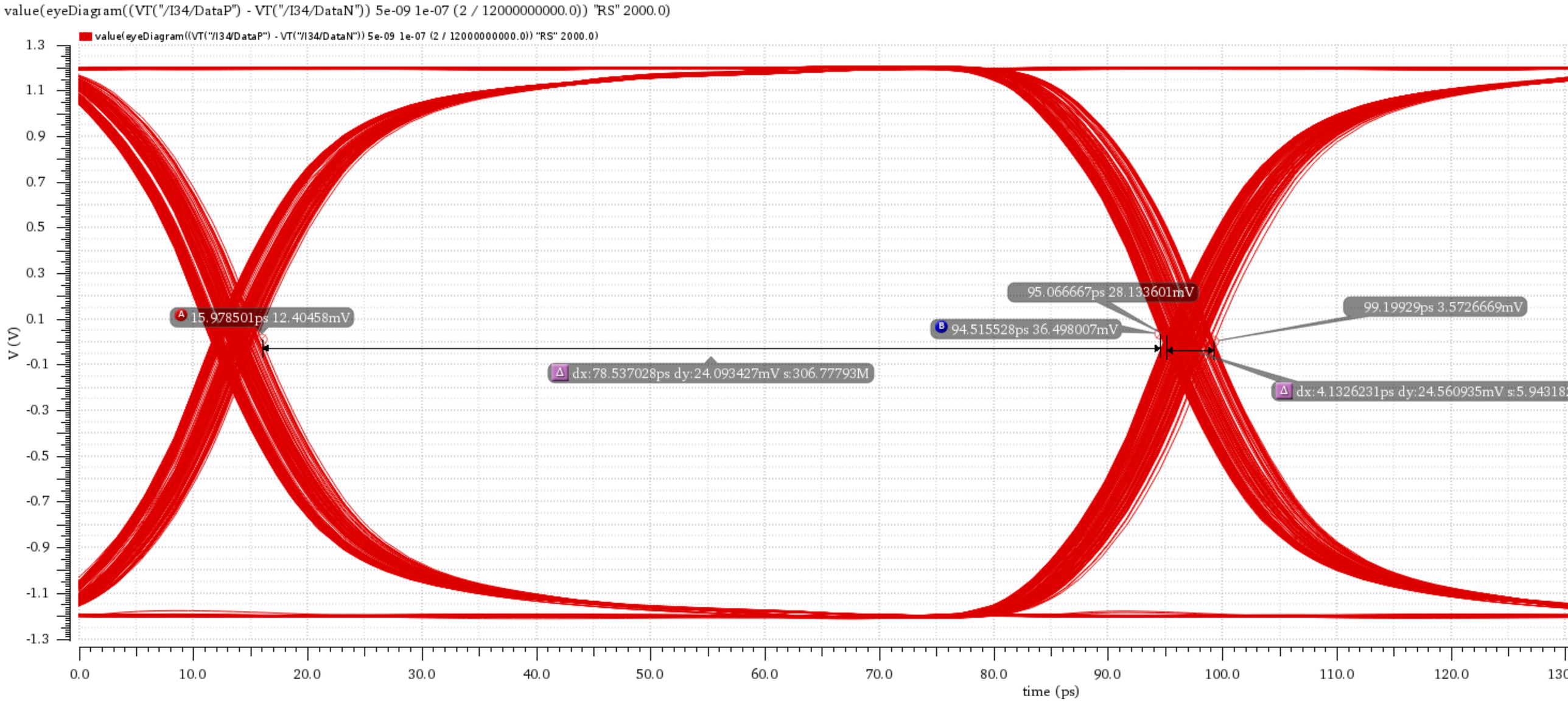
  - peak = 746.5 n V/sqr(HZ)
  - output RMS = 3.565n V/sqr(HZ)
  - input referred RMS noise = Vrms,n,out/Gain = 0.3478 n V/sqr(HZ)



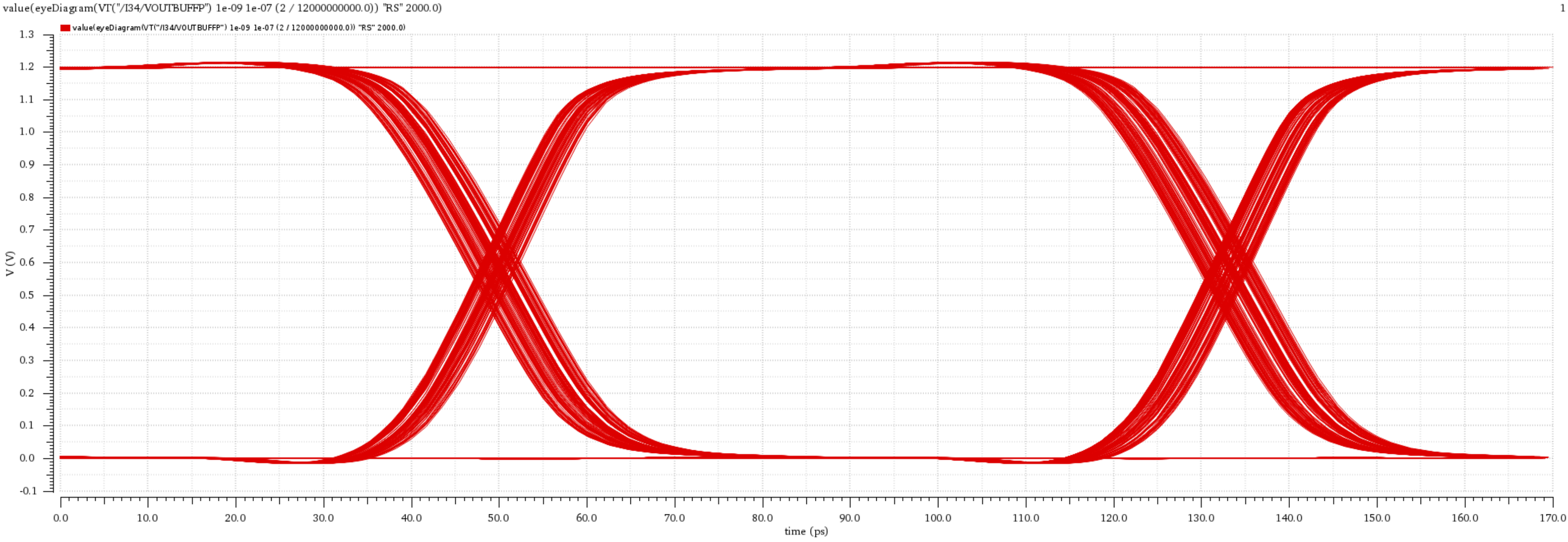
EYE DIAGRAM AFTER ONE COMPARATOR



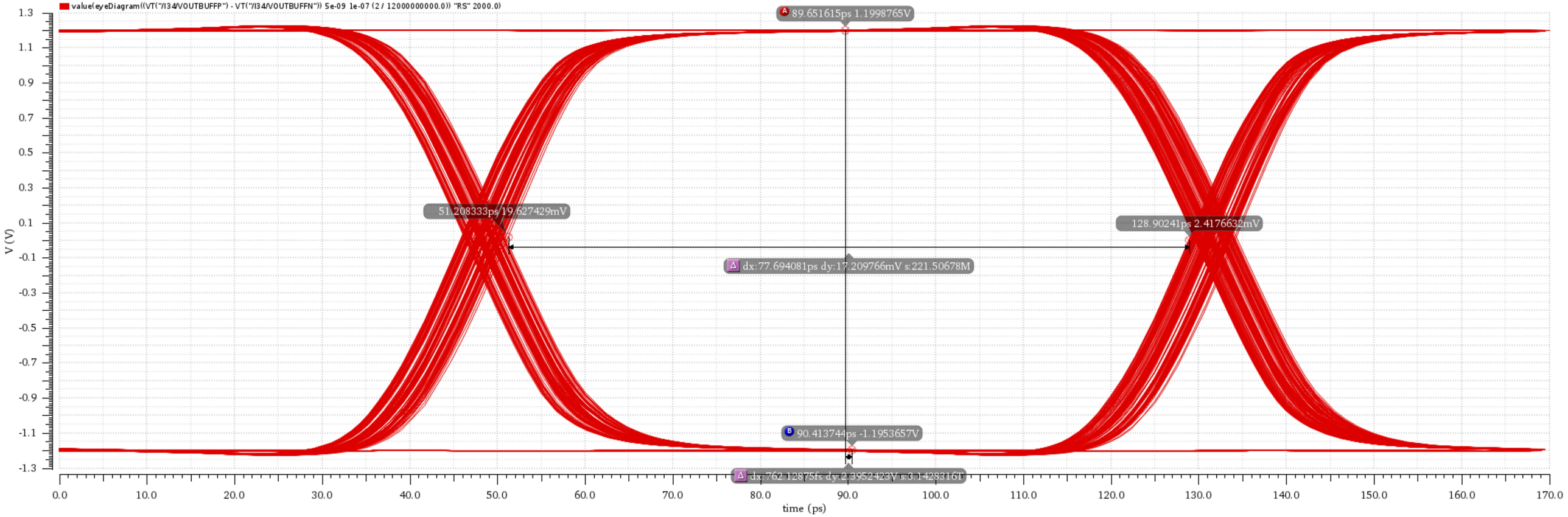
EYE DIAGRAM AFTER ONE COMPARATOR



SINGLE ENDED EYE DIAGRAM AFTER BUFFER



DIFF EYE DIAGRAM AFTER BUFFERING

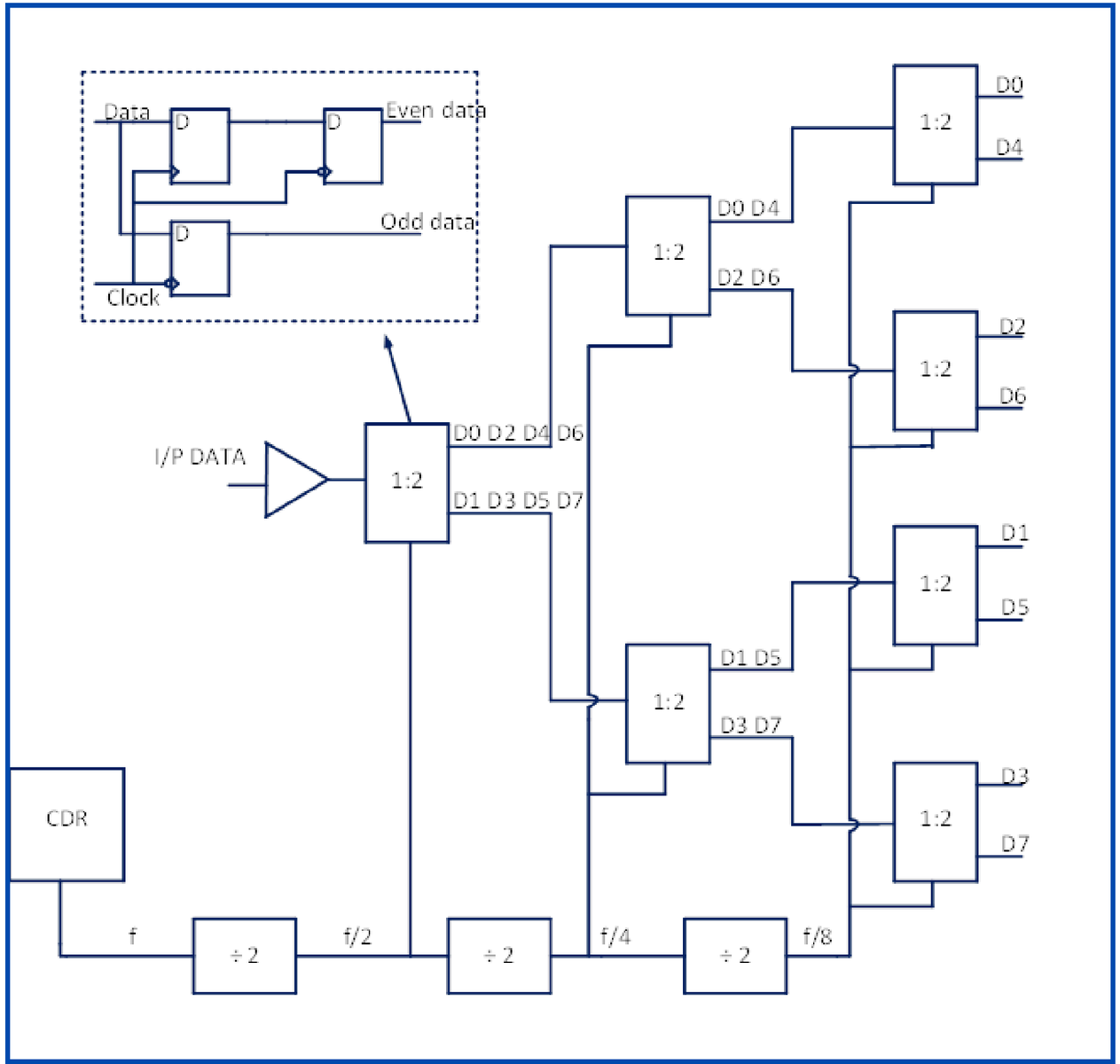


DESERIALIZER

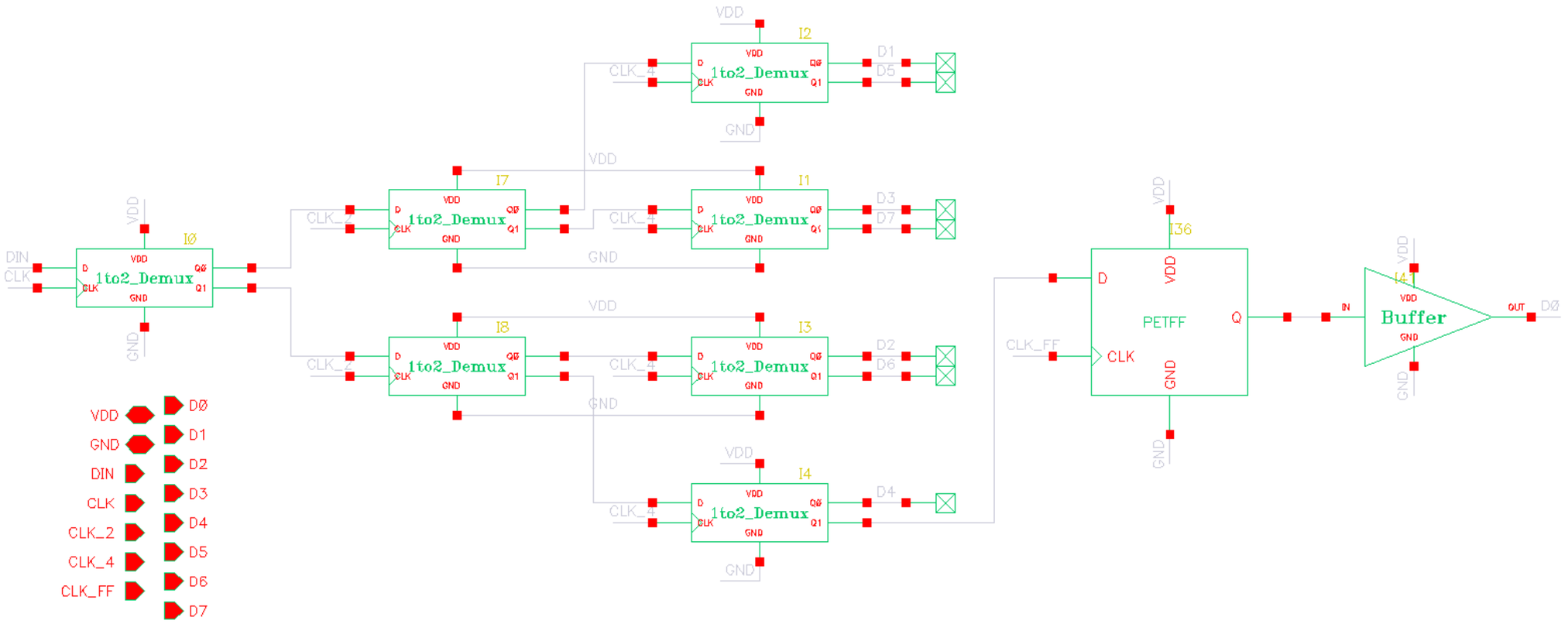
OVERVIEW

Deserializer Function

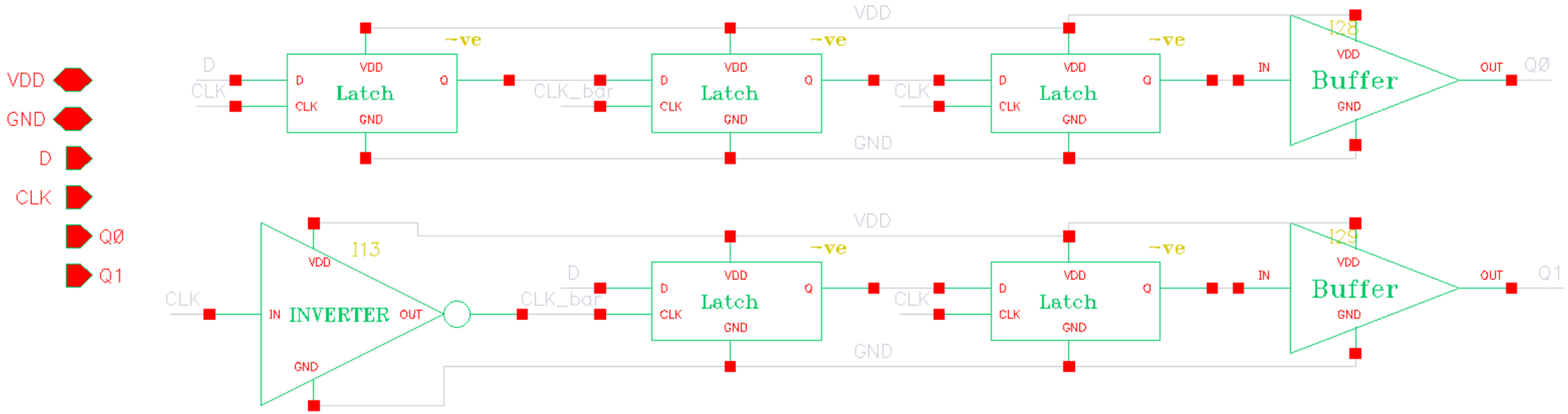
- A Deserializer is the block that converts data from serial form back into parallel form
- It takes in a single high-speed serial bit stream.
- Splits the stream into multiple parallel data bits (e.g., 8, 16, or 32)
- Works with a recovered clock to sample incoming bits correctly.
- Ensures data alignment so parallel words are valid.
- Acts as the interface between serial communication channel and digital logic system.



DESERIALIZER SCHEMATIC



1 TO 2 DEMUX


VDD
GND
D
CLK
Q0
Q1
D
CLK
Latch
VDD
GND
Q
~ve
CLK_bar
I28
Buffer
IN
OUT
I13
INVERTER
I29

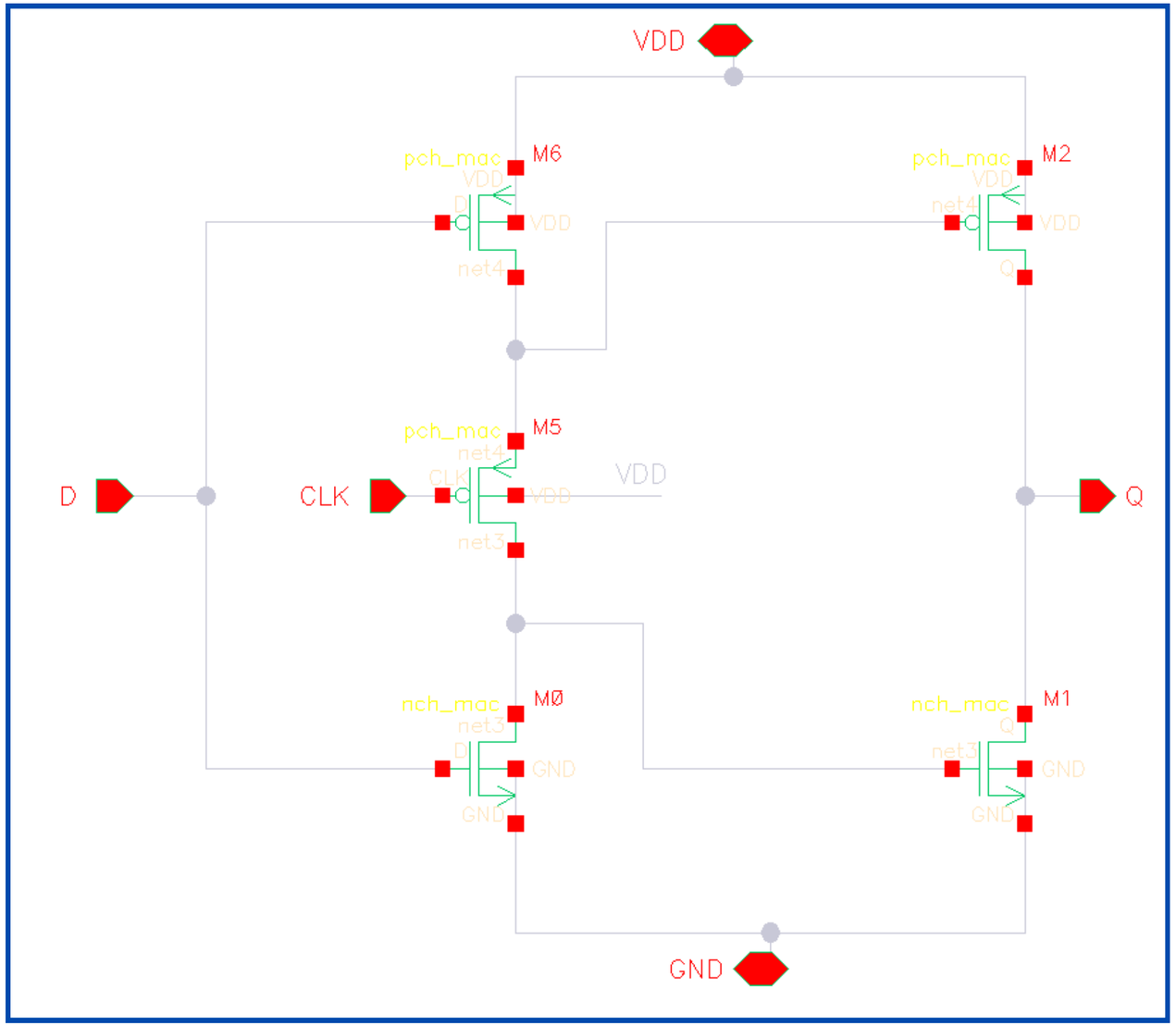
LATCH

Latch Function

- A storage element that holds a single bit of data for a short period.

Role in Demux

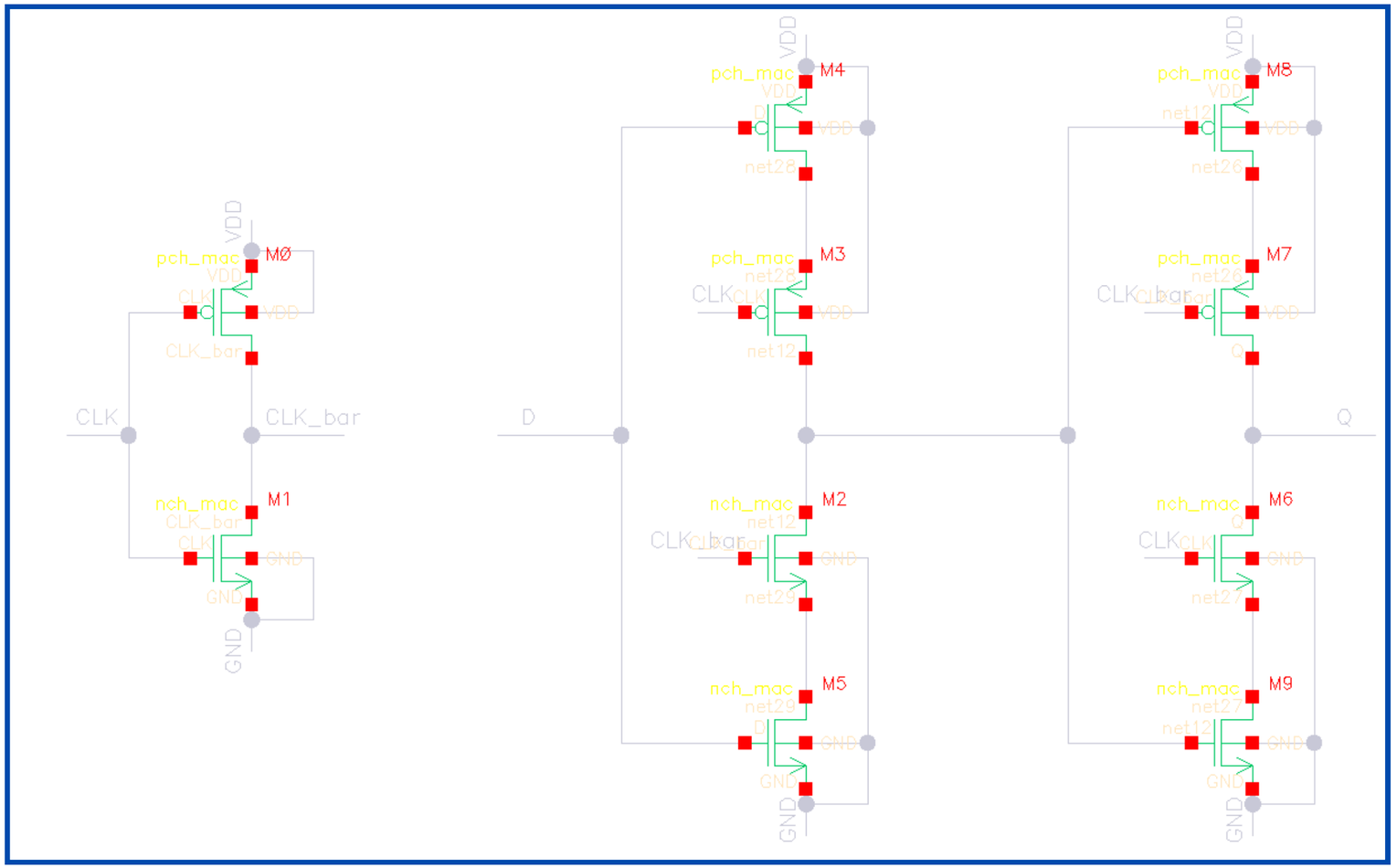
- Captures incoming serial bits at the right clock edge.
- Temporarily stores data before passing it to the correct output path..
- Enables demultiplexing by holding data until the clock signals which branch to send it to.
- Ensures timing alignment between high-speed serial input and parallel outputs.



FLIP FLOP

Flip Flop function

- A problem we faced in the design is that bit D0 was delayed compared to the other 7 bits (D1–D7).
- To fix this, we added one PET flip-flop in the D0 path.
- The flip-flop was driven by an external clock to control its delay.
- As a result, D0 became synchronized with the rest of the bits.



BUFFER

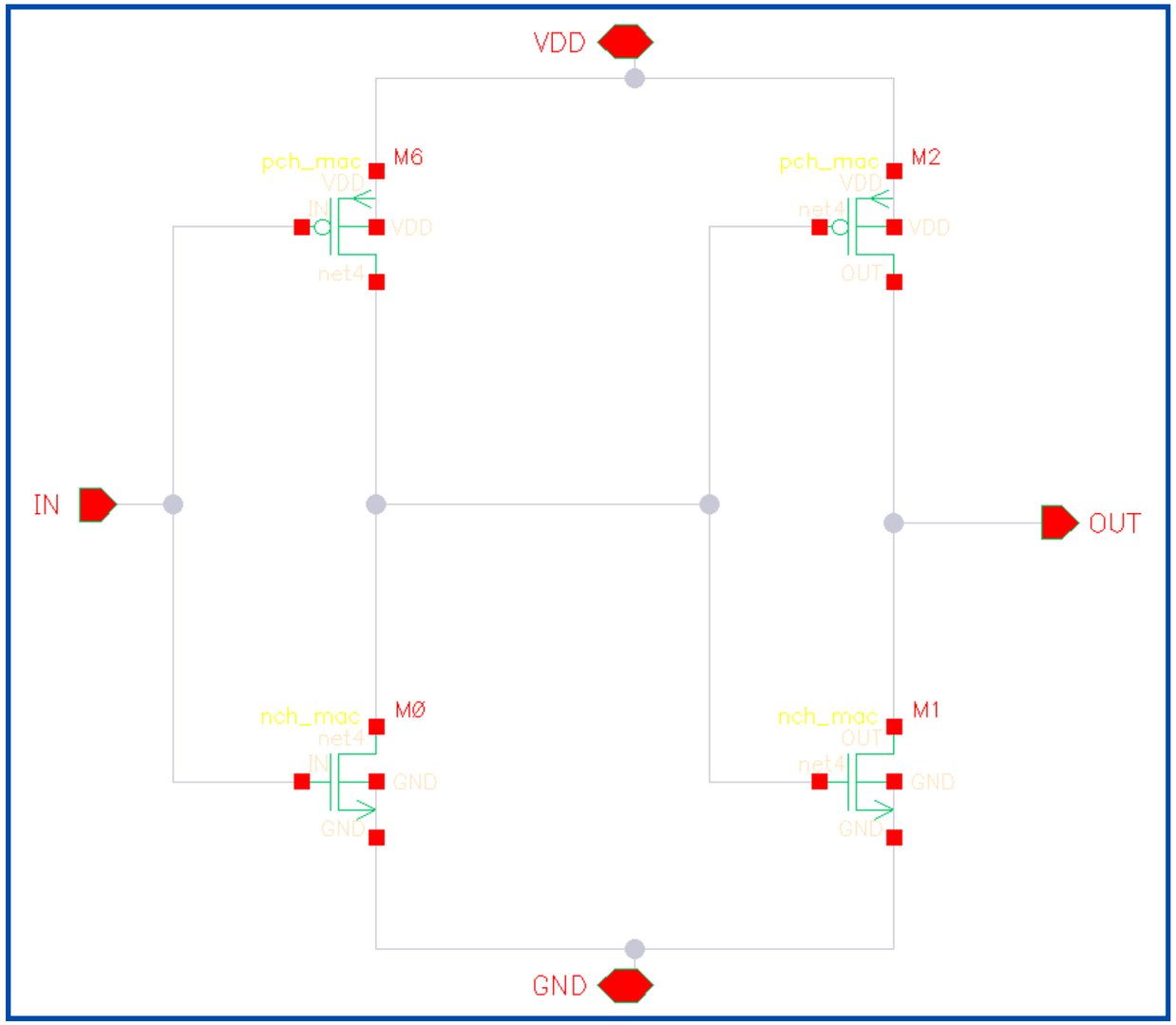
Buffer function

- A buffer is a circuit that copies the input to the output without changing the logic value.

- It is used to prevent loading effect, so the previous stage is not heavily loaded by the next stage.

- The buffer restores signal integrity by cleaning and strengthening a weak or degraded signal.

- In our design, the buffer ensured that deserialized bits clean and reliable.



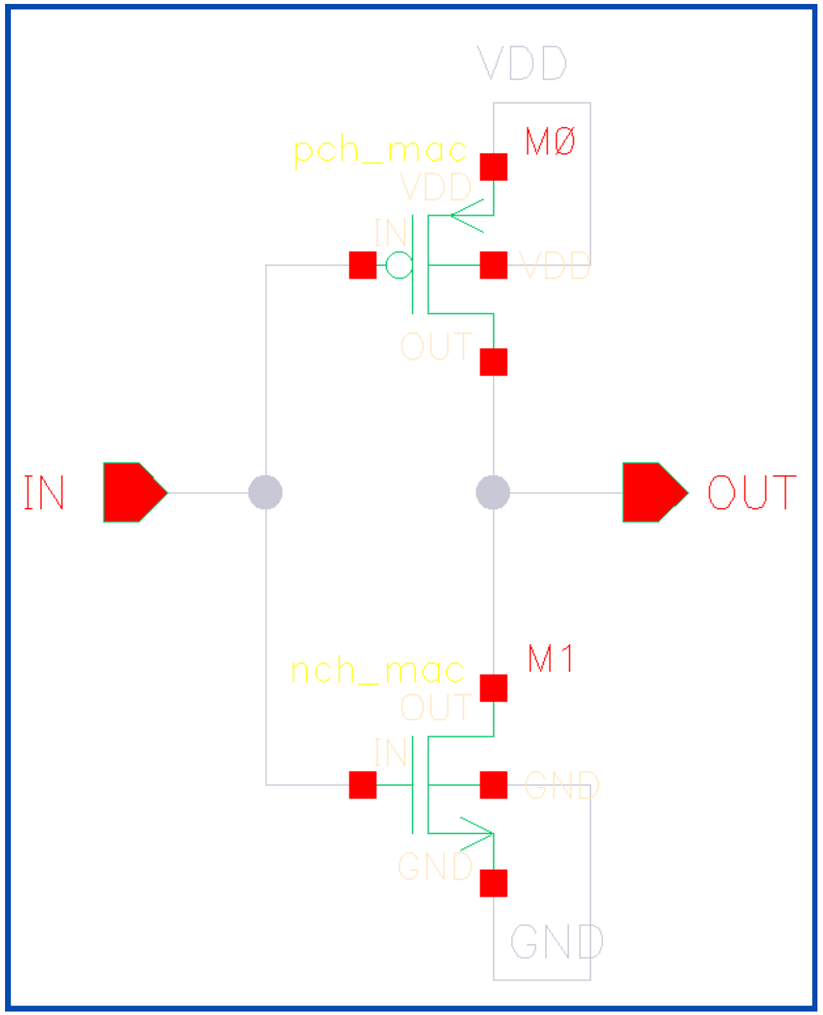
INVERTER

Inverter function

- In clocking circuits, an inverter is used to create an inverted clock (often called clock-bar, $\overline{clk}$, or clk′).

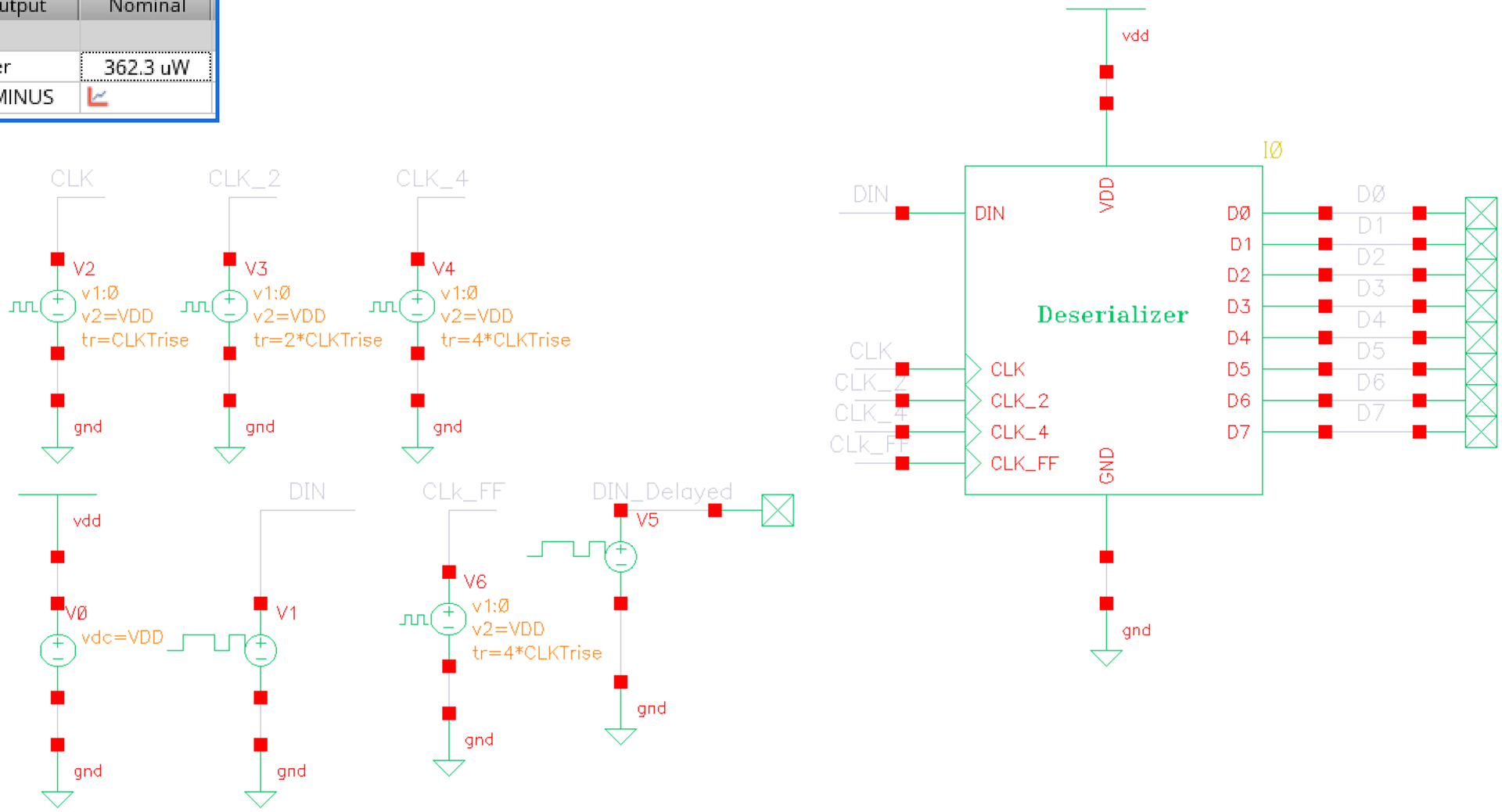
- This inverted clock can be used for timing control, latch/FF triggering, or phase alignment.

- In our design, we used an inverter to generate the inverted clock needed to drive specific elements in the deserializer.

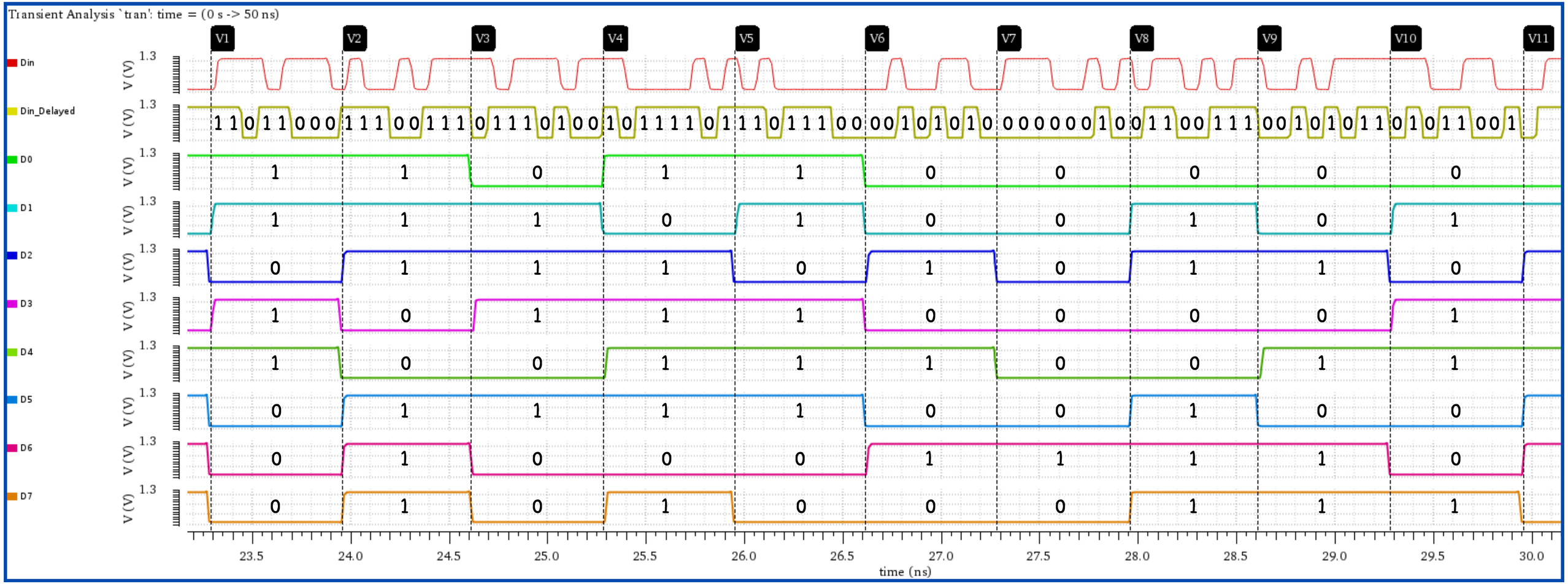


TESTBENCH

Test	Output	Nominal
GP_TRV_P1...	Power	362.3 uW
GP_TRV_P1...	/V0/MINUS	



RESULTS

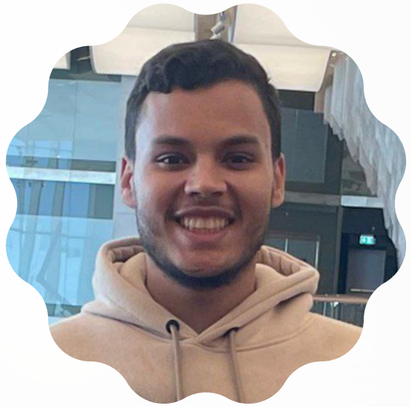

Transient Analysis `tran': time = (0 s -> 50 ns)
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
Din
Din_Delayed
D0
D1
D2
D3
D4
D5
D6
D7
V (V)
1.3
1 1 0 1 1 0 0 0 1 1 1 0 0 1 1 1 0 1 1 1 0 1 0 0 1 0 1 1 1 1 0 1 1 1 0 1 1 1 0 0 0 0 1 0 1 0 1 0 0 0 0 0 0 0 1 0 0 1 1 0 0 1 1 1 0 0 1 0 1 0 1 1 0 1 0 1 1 0 0 1
23.5
24.0
24.5
25.0
25.5
26.0
26.5
27.0
27.5
28.0
28.5
29.0
29.5
30.0
time (ns)

MEET OUR

TEAM MEMBERS

Belal Soliman

Mostafa Mohamed



Mahmoud Ahmed

Adham Khaled

Mohamed Yahia

Moaz Adel

MEET OUR

SUPERVISORS

- Eng. Mahmoud Sofy
- Eng. Hesham Ashraf
- Eng. Ziad Essam
- Eng. Mohamed Fares
- Eng. Youssef Ali
- Eng. Abdelrahman Mamoun

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