



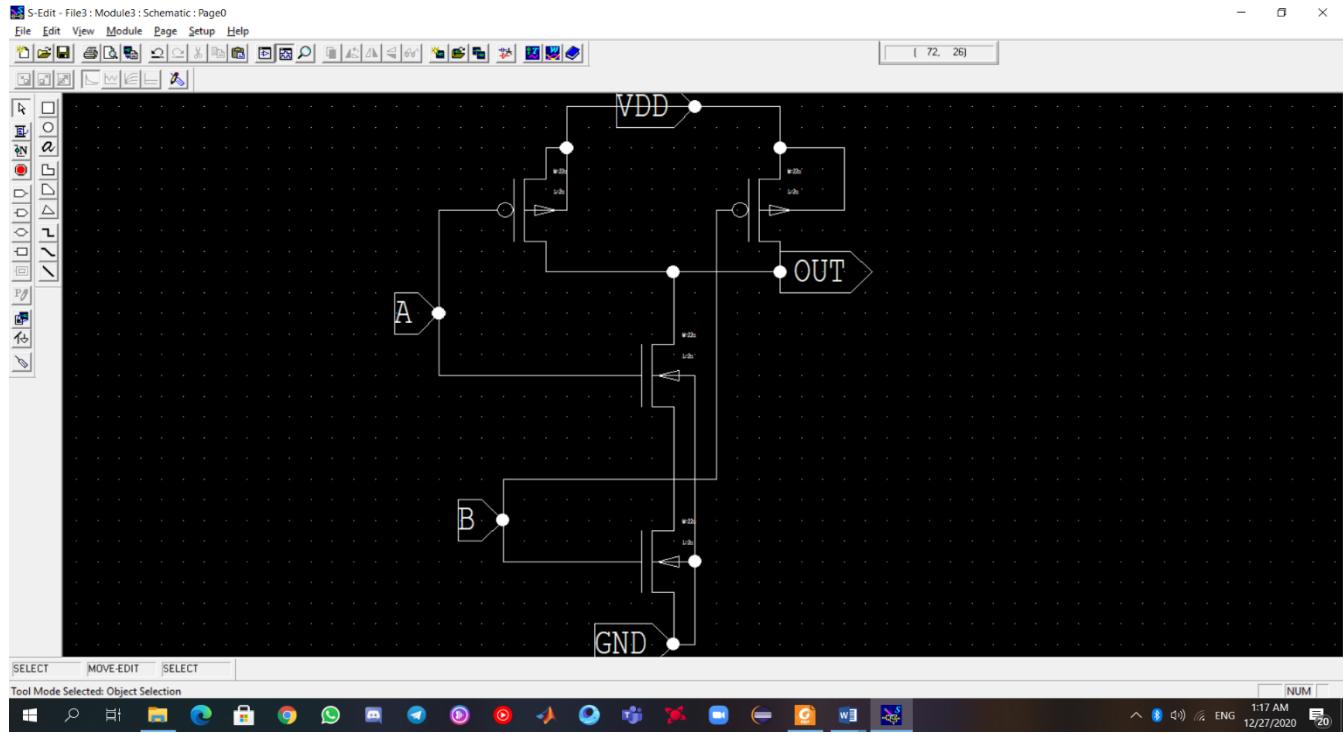
**Alexandria University.
Faculty of Engineering.
Electronics & Communication Department
(Fourth Year).
Digital ICs Lab.**

(3rd Lab.)

CMOS Combinational Logic Gates: *NAND Gate*

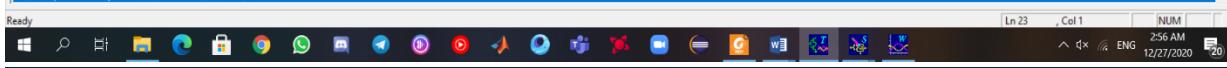
Name	Section	ID
Amr Hany Mohammed Dawod	5	179
Mahmoud Mohamed Kamal	7	250
Mahmoud Alaa Eldin Mahmoud	7	249
Aya Abdallah Abdelmoaty Mohamed	1	10
Aya Shaaban Mahmoud Elsayed	1	7

Screenshot of Schematic:

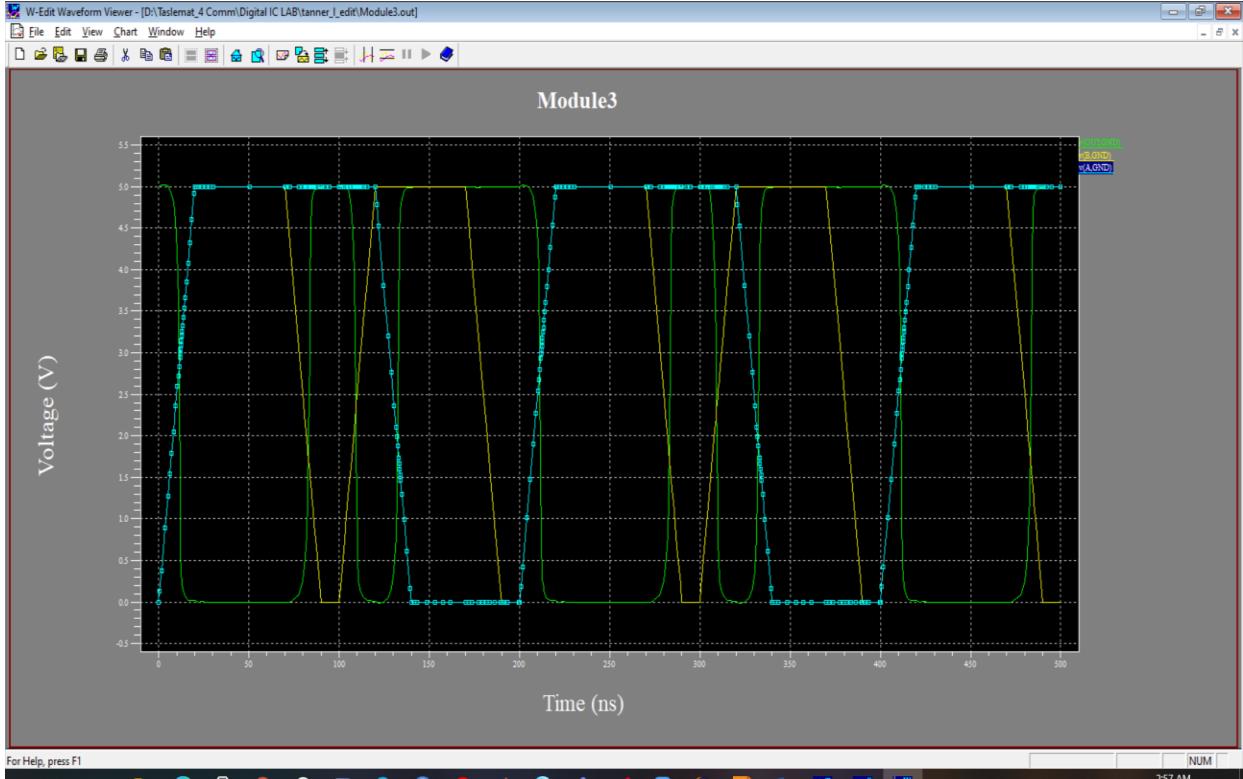
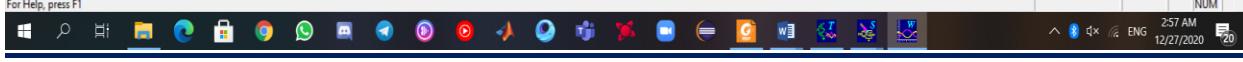
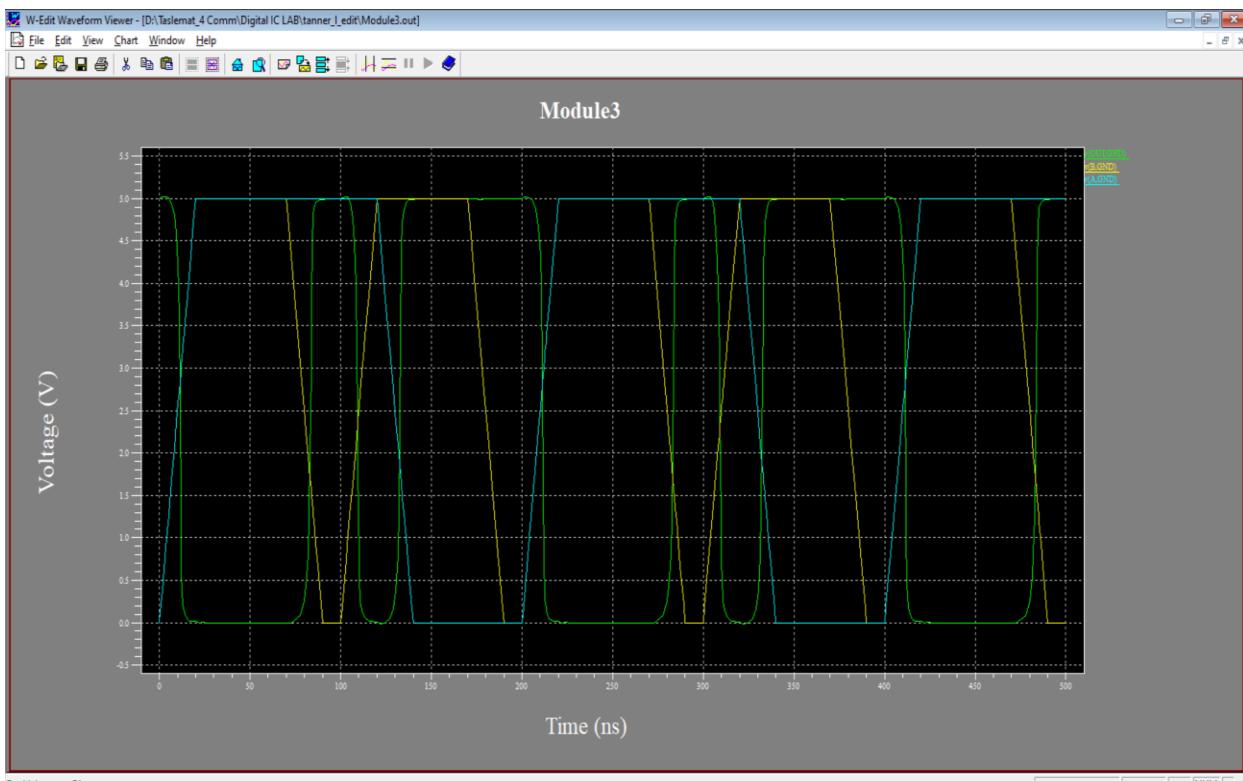


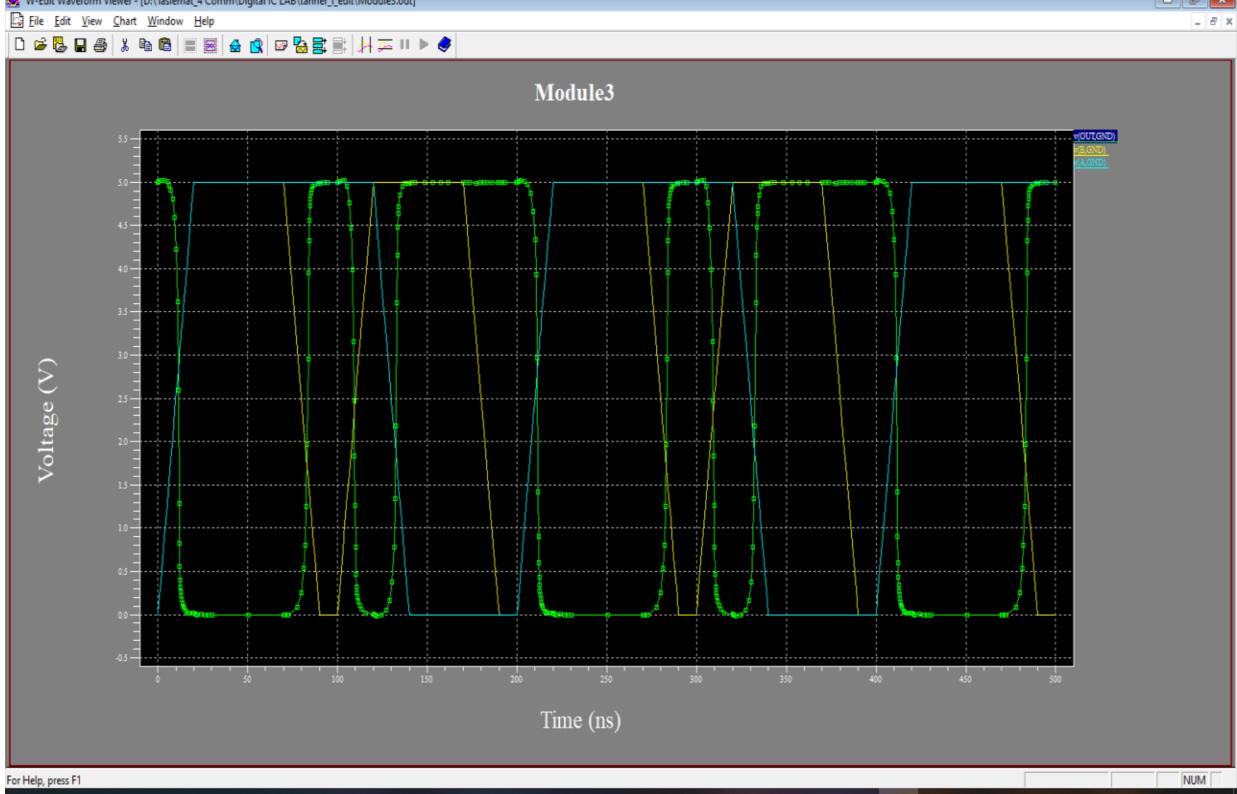
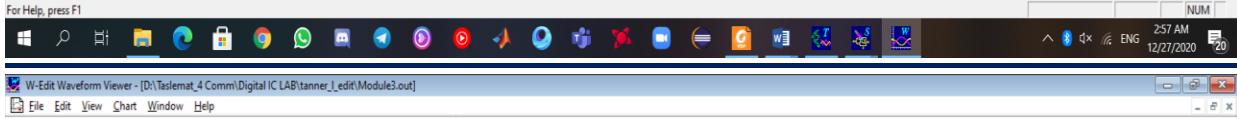
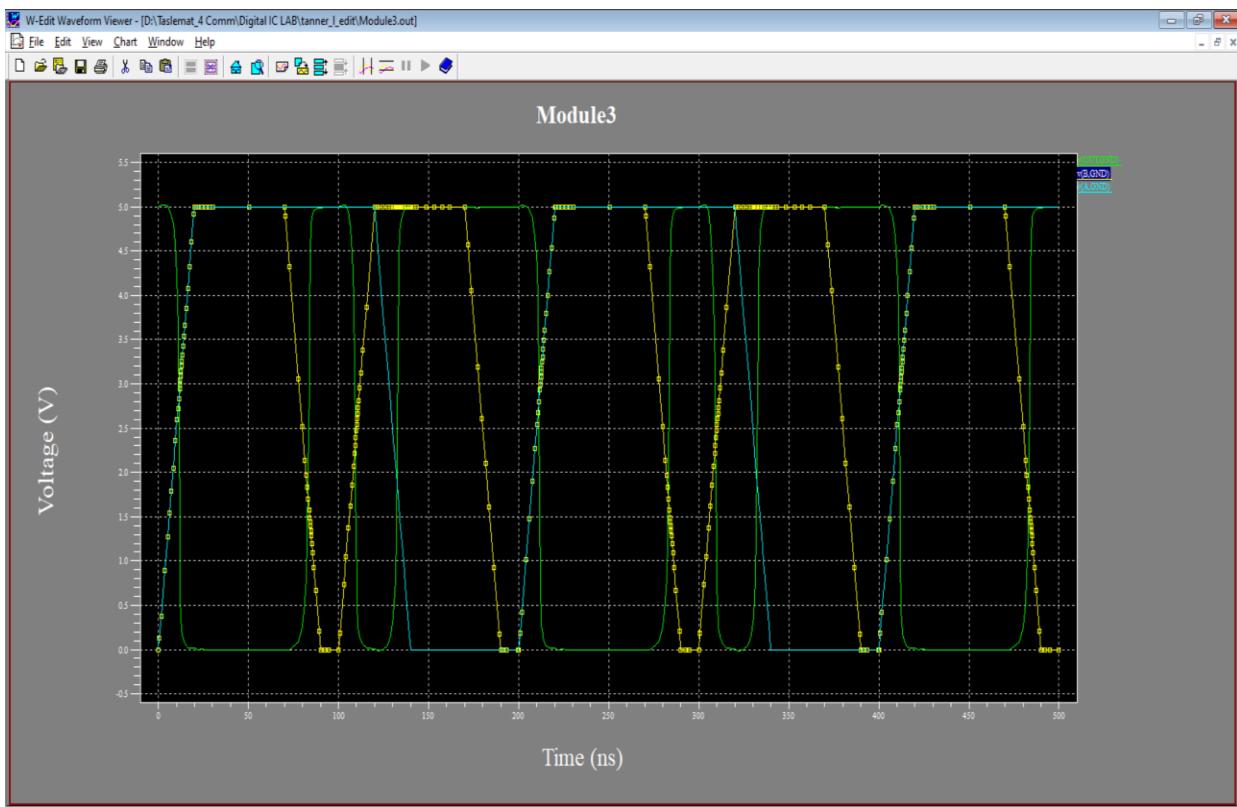
Logic Functionality Test:

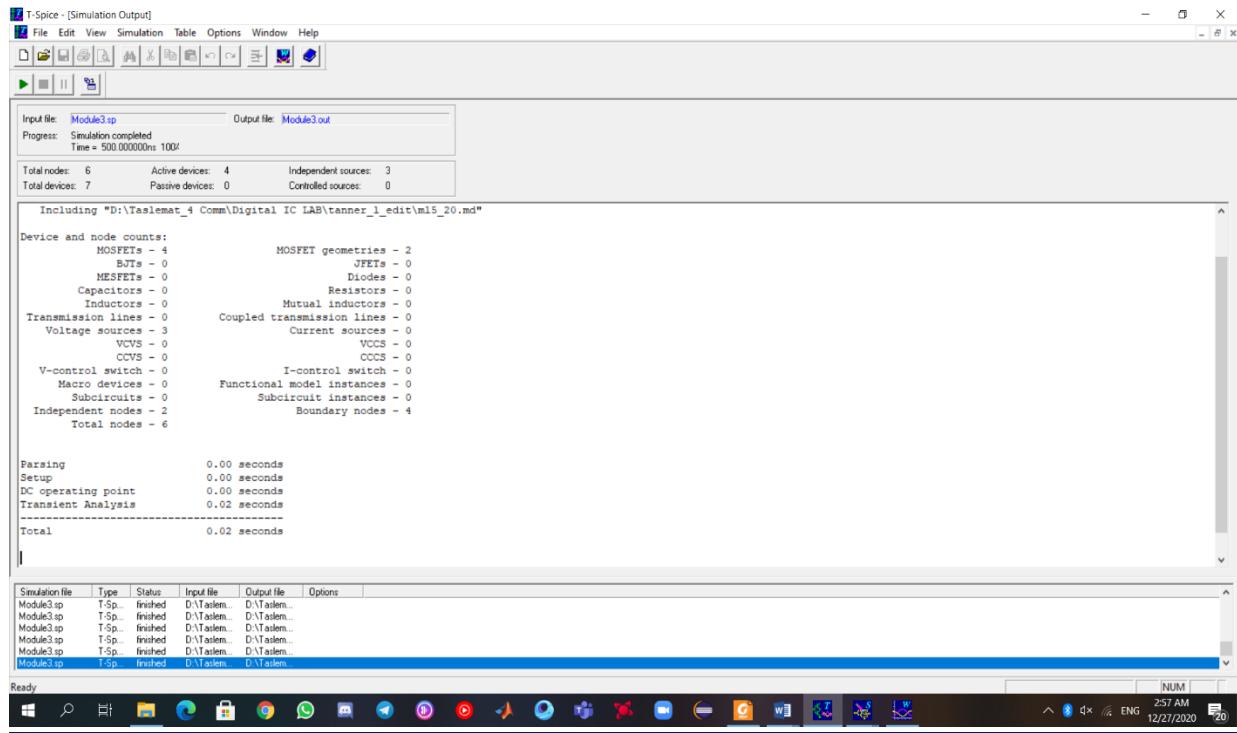
- The Netlist:



- Screenshots of the Results from Simulation:







From above Screenshots of the Results waveforms from Simulation we found that the logic functionality of the design satisfies the NAND gate properties.

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

Transistors Sizing in “Worst Case” Scenario:

1- For the “worst case” delay we can size the Transistors in the PUN (Pull-Up Network) as follows:

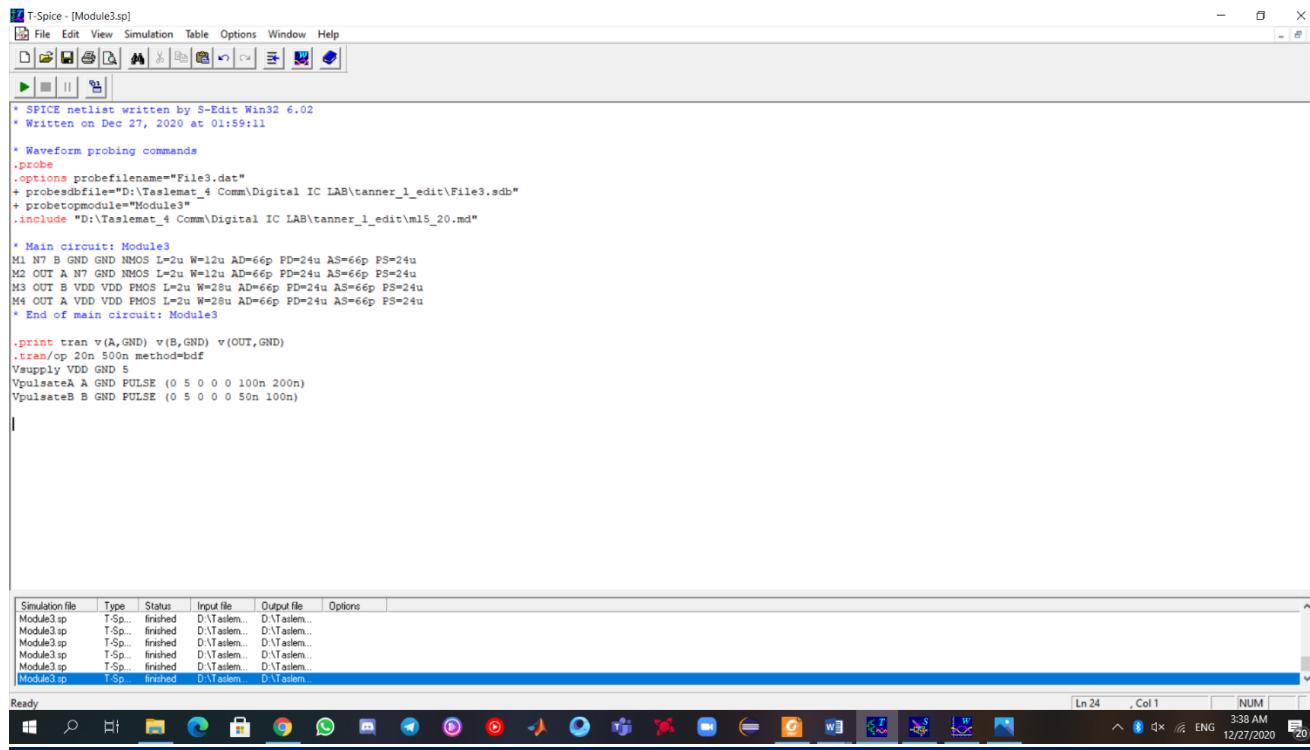
(W/L) for PUN Transistors = (W/L) for P-MOS in the basic Matched Inverter.

So, we will put (W) for PUN Transistors = 28 μm .

2- For the “worst case” delay we can size the Transistors in the PDN (Pull-Down Network) as follows:

(W/L) for PDN Transistors = 2 * (W/L) for N-MOS in the basic Matched Inverter.

So, we will put (W) for PDN Transistors = 12 μm .



The screenshot shows the T-Spice software interface with the following details:

- Netlist Content:**

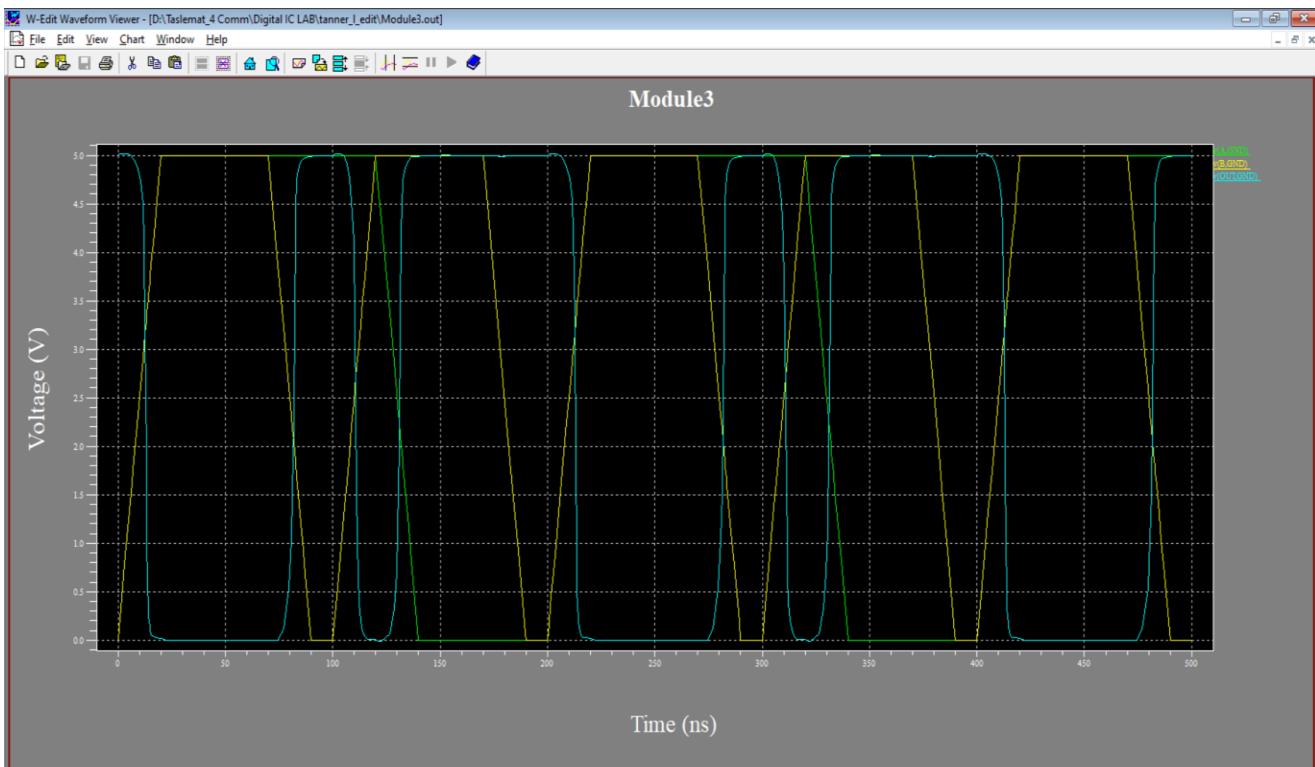
```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 27, 2020 at 01:59:11

* Waveform probing commands
.probe
.options probefilename="File3.dat"
+ probefilename="D:\Tasleem_4 Comm\Digital IC LAB\tanner_1_edit\File3.sdb"
+ probetopmodule="Module3"
.include "D:\Tasleem_4 Comm\Digital IC LAB\tanner_1_edit\l15_20.md"

* Main circuit: Module3
M1 N7 B GND GND NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M2 OUT A N7 GND NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M3 OUT B VDD VDD PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
M4 OUT A VDD VDD PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module3

.print tran v(A,GND) v(B,GND) v(OUT,GND)
.tran/op 20n 500n method=bdf
Vsupply VDD GND 5
VpulseA A GND PULSE (0 5 0 0 0 100n 200n)
VpulseB B GND PULSE (0 5 0 0 0 50n 100n)
```
- Simulation Results Table:**

Simulation file	Type	Status	Input file	Output file	Options
Module3.sp	T-Sp.	Finished	D:\Tasleem..	D:\Tasleem..	
Module3.sp	T-Sp.	Finished	D:\Tasleem..	D:\Tasleem..	
Module3.sp	T-Sp..	finished	D:\Tasleem..	D:\Tasleem..	
Module3.sp	T-Sp..	finished	D:\Tasleem..	D:\Tasleem..	
Module3.sp	T-Sp..	finished	D:\Tasleem..	D:\Tasleem..	
Module3.sp	T-Sp..	finished	D:\Tasleem..	D:\Tasleem..	
- System Taskbar:** Shows various application icons and system status.



For Help, press F1

T-Spice - [Simulation Output]

File Edit View Simulation Table Options Window Help

Input file: Module3.sp Output file: Module3.out

Progress: Simulation completed
Time = 500.000000ns 100%

Total nodes: 6	Active devices: 4	Independent sources: 3
Total devices: 7	Passive devices: 0	Controlled sources: 0

```
Including "D:\Tasleemat_4 Comm\Digital IC LAB\tanner_1_edit\m15_20.md"

Device and node counts:
    MOSFETs - 4          MOSFET geometries - 2
    BJTs - 0              JFETs - 0
    MESFETs - 0           Diodes - 0
    Capacitors - 0        Resistors - 0
    Inductors - 0         Mutual inductors - 0
    Transmission lines - 0 Coupled transmission lines - 0
    Voltage sources - 3   Current sources - 0
    VCVS - 0              VCCS - 0
    CCVS - 0              CCCS - 0
    V-control switch - 0  I-control switch - 0
    Macro devices - 0     Functional model instances - 0
    Subcircuits - 0        Subcircuit instances - 0
    Independent nodes - 2 Boundary nodes - 4
    Total nodes - 6

Parsing          0.00 seconds
Setup           0.00 seconds
DC operating point 0.01 seconds
Transient Analysis 0.02 seconds
-----
Total           0.03 seconds
```

Simulation file	Type	Status	Input file	Output file	Options
Module3.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module3.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module3.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module3.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module3.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	

Ready

File Edit View Chart Window Help

3:38 AM 12/27/2020

• τ_P Calculation

```

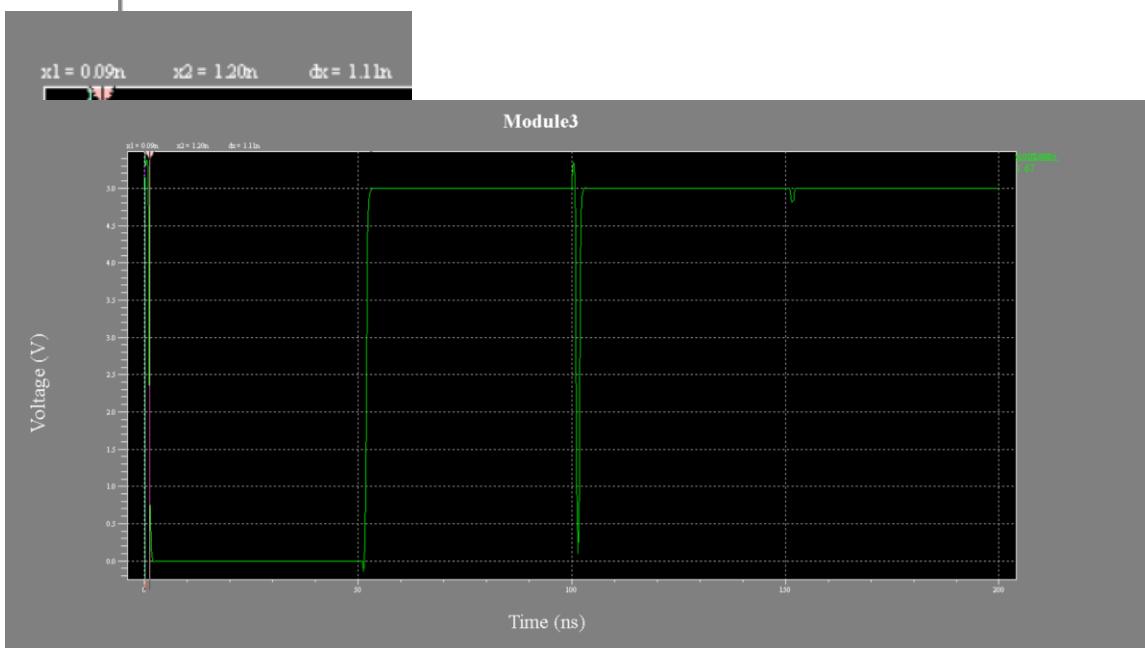
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 27, 2020 at 01:59:11

* Waveform probing commands
.probe
.options probefilename="File3.dat"
+ probesdbfile="H:\F.O.E\4th Year\Digital ICs"
+ probetopmodule="Module3"
.include "H:\tanner_1_edit\m15_20.md"

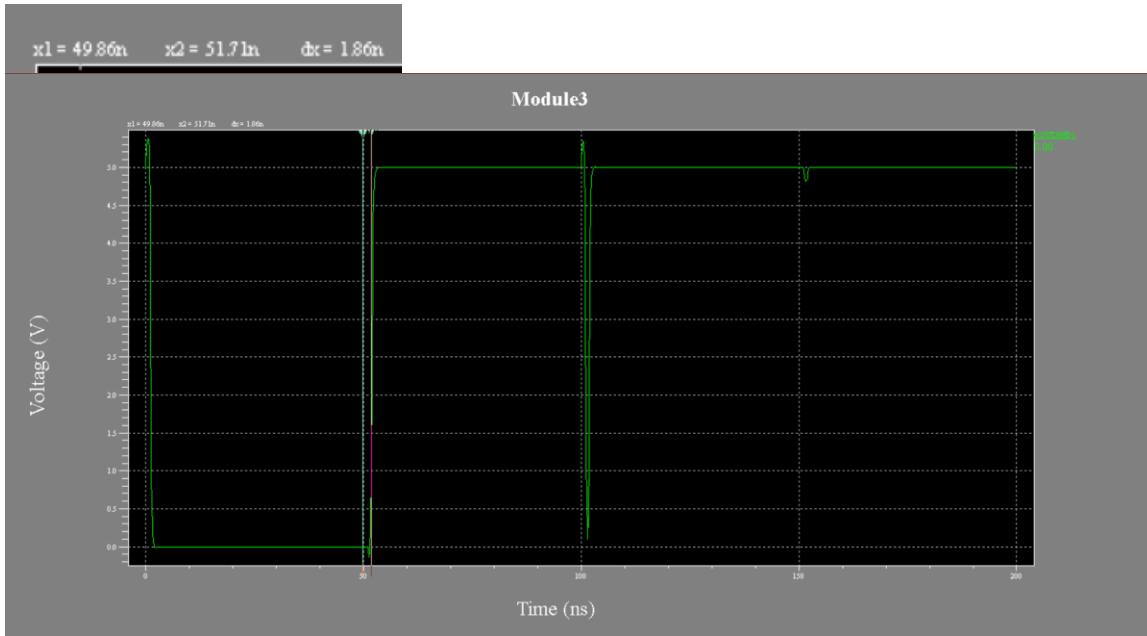
* Main circuit: Module3
M1 N7 B GND GND NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M2 OUT A N7 GND NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M3 OUT B VDD VDD PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
M4 OUT A VDD VDD PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module3

.print tran v(OUT,GND)
.tran/op 1n 200n method=bdf
Vsupply VDD GND 5
VpulseA A GND PULSE (0 5 0 0 0 100n 200n)
VpulseB B GND PULSE (0 5 0 0 0 50n 100n)

```



$$\tau_{PHL} = 1.11 \text{ nsec}$$



$$\tau_{PLH} = 1.86 \text{ nsec}$$

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \frac{1.11 + 1.86}{2} = 1.485 \text{ nsec}$$

VTC

- DC Sweep for two inputs (A&B)

```

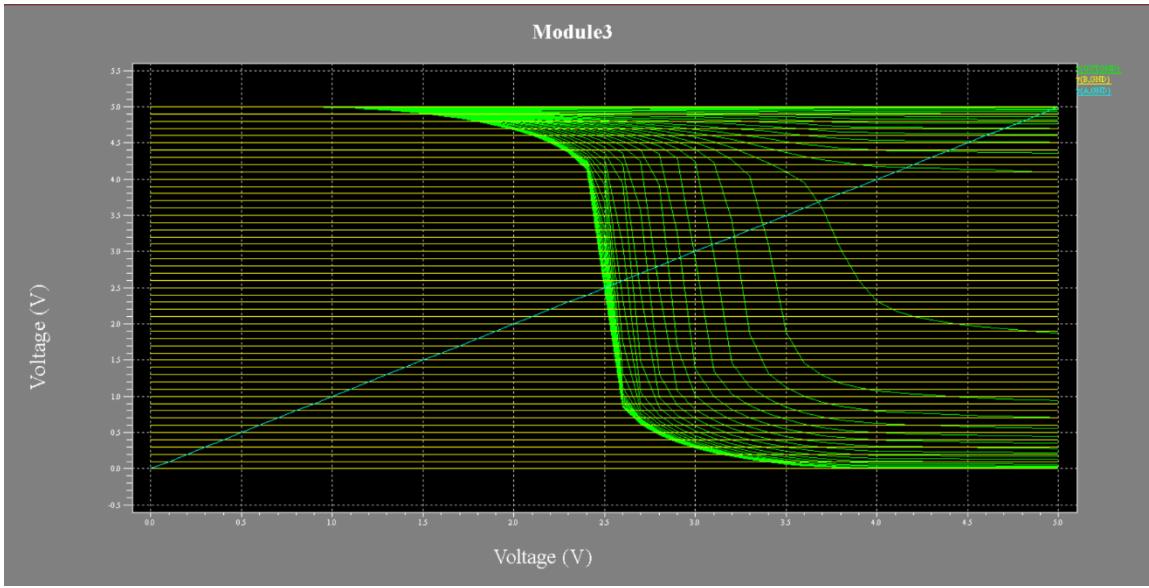
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 27, 2020 at 01:59:11

* Waveform probing commands
.probe
.options probefilename="File3.dat"
+ probesdbfile="H:\F.O.E\4th Year\Digital ICs"
+ probetopmodule="Module3"
.include "H:\tanner_1_edit\m15_20.mdc"

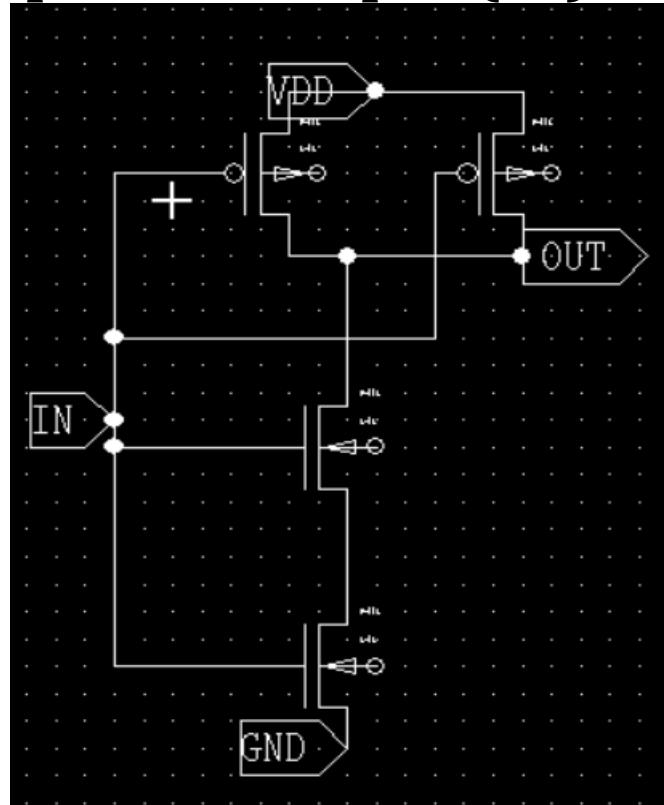
* Main circuit: Module3
M1 N7 B GND GND NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M2 OUT A N7 GND NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M3 OUT B VDD VDD PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
M4 OUT A VDD VDD PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module3

.dc lin source VpulsateA 0 5 0.1 sweep lin source VpulsateB 0 5 0.1
.print dc v(A,GND) v(B,GND) v(OUT,GND)
Vsupply VDD GND 5
VpulsateA A GND PULSE (0 5 0 0 0 100n 200n)
VpulsateB B GND PULSE (0 5 0 0 0 50n 100n)

```



- **DC Sweep for one input (IN)**



```

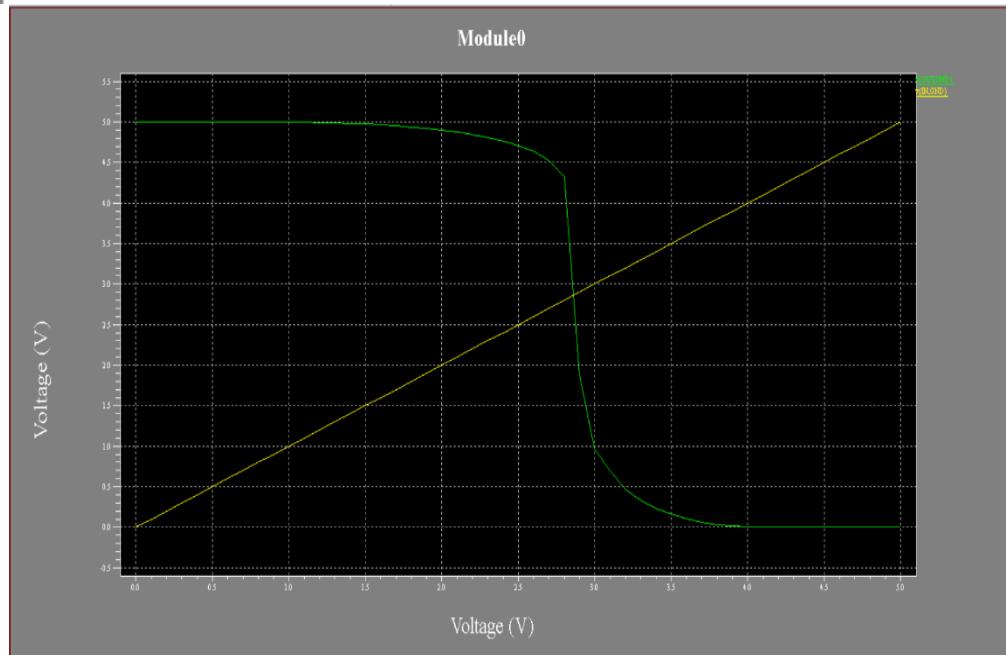
* SPICE netlist written by S-Edit Win32 6.02
* Written on Jan 8, 2021 at 14:21:32

* Waveform probing commands
.probe
.options probefilename="Module3.dat"
+ probesdbfile="H:\F.p.E\4th Year\Digital ICs\Module3.sdb"
+ probetopmodule="Module0"
.include "H:\tanner_1_edit\m15_20.md"

* Main circuit: Module0
M1 OUT IN N15 N3 NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M2 N15 IN GND N16 NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M3 OUT IN VDD N2 PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
M4 OUT IN VDD N4 PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module0

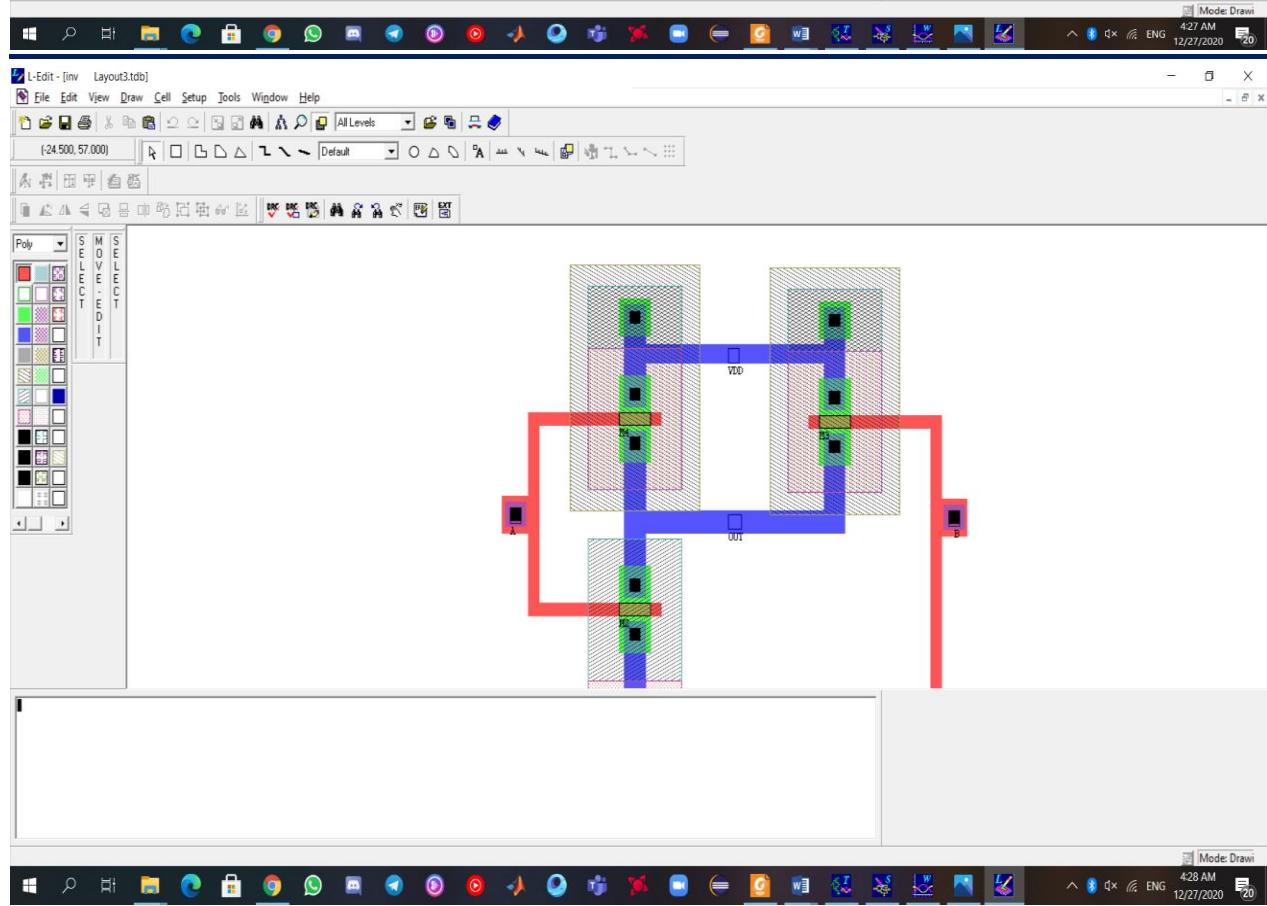
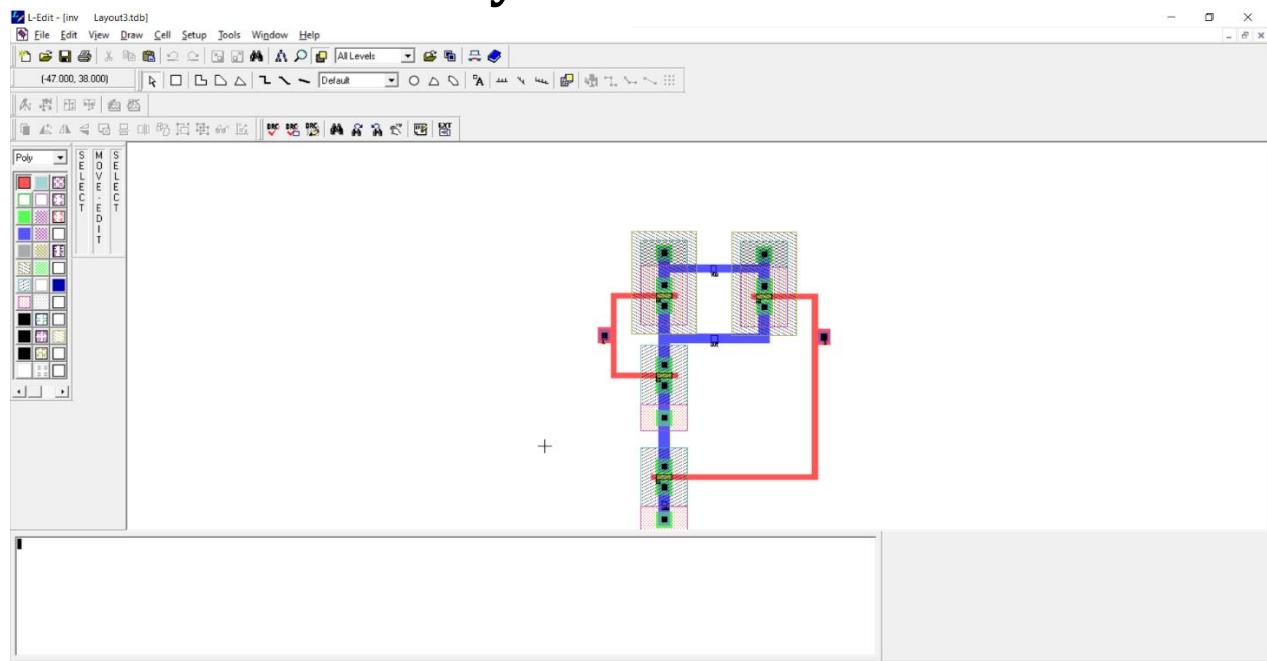
.dc lin source Vpulse 0 5 0.1
.print dc v(IN,GND) v(OUT,GND)
Vsupply VDD GND 5
Vpulse IN GND PULSE (0 5 0 0 0 50n 100n)

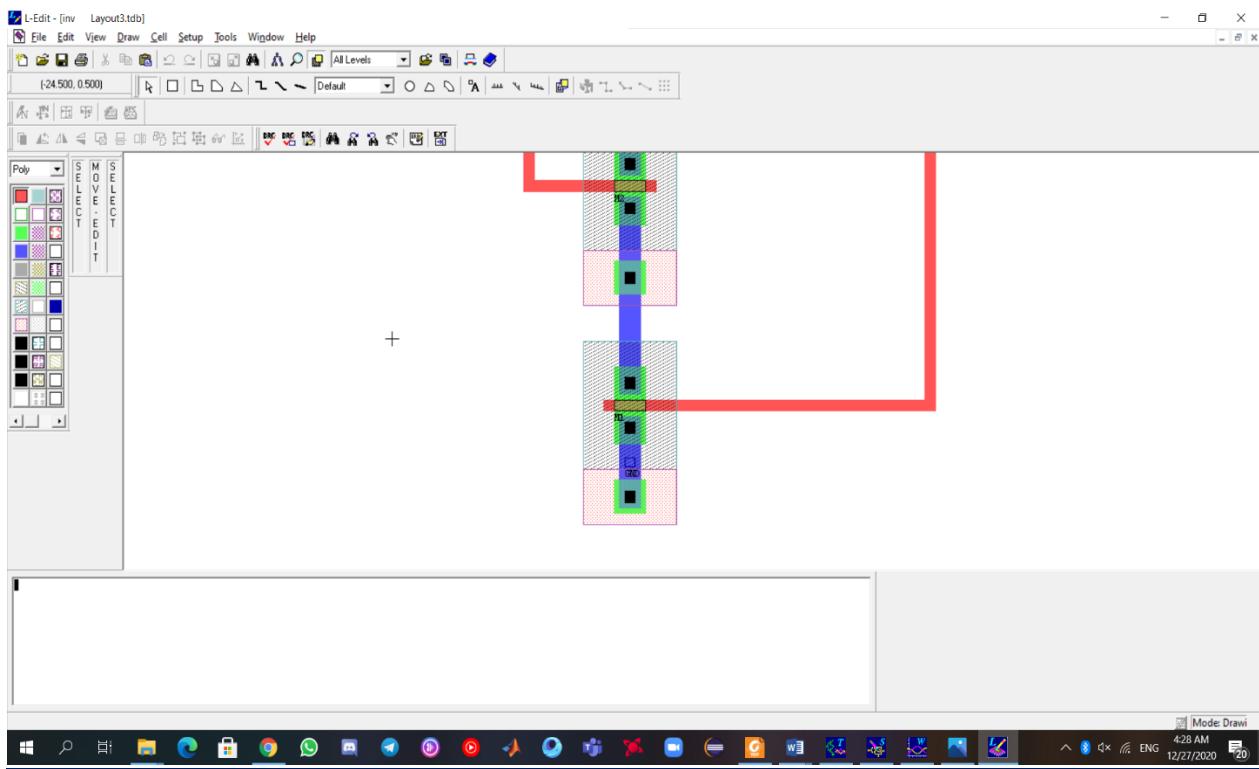
```



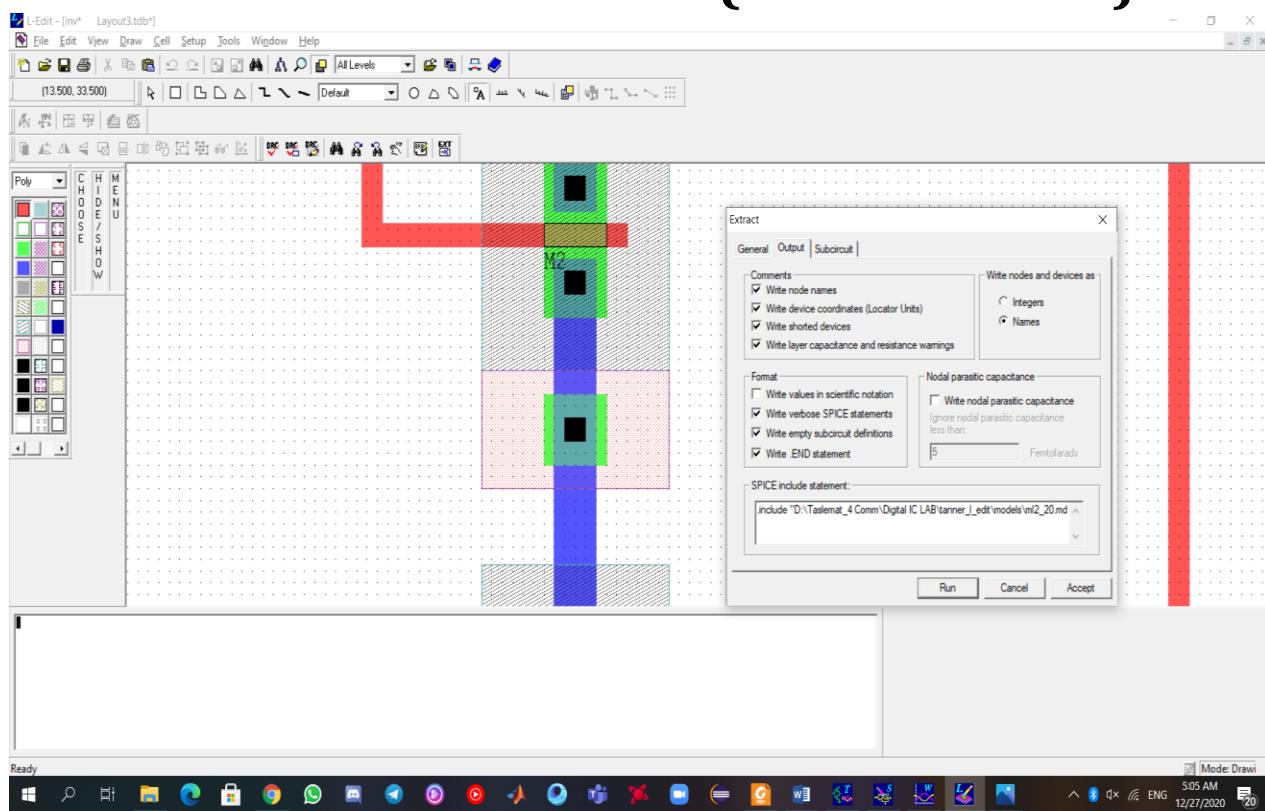
The Layout:

• Screenshots of Layout:





● Screenshots of Netlist File (Extracted File):



T-Spice - [NAND.spc]

* Circuit Extracted by Tanner Research's L-Edit Version 8.30 / Extract Version 8.30 ;
 * TDB File: D:\Tasilemat_4 Comm\Digital IC LAB\tanner_1_edit\Layout3.tdb
 * Cell: inv Version 1.05
 * Extract Definition File: morbn20.ext
 * Extract Date and Time: 12/27/2020 - 04:42

```
.include "D:\Tasilemat_4 Comm\Digital IC LAB\tanner_1_edit\models\m12_20.md"

* Warning: Layers with Unassigned AREA Capacitance.
* <P Diff Resistor>
* <Poly Resistor>
* <N Diff Resistor>
* <P Base Resistor>
* <N Well Resistor>
* <Poly2 Resistor>
* Warning: Layers with Unassigned FRINGE Capacitance.
* <P Diff Resistor>
* <Poly Resistor>
* <N Diff Resistor>
* <P Base Resistor>
* <N Well Resistor>
* <Poly1-Poly2 Capacitor>
* <Poly2 Resistor>
* <Pad Comment>
* Warning: Layers with Zero Resistance.
* <NMOS Capacitor>
* <PMOS Capacitor>
* <Poly1-Poly2 Capacitor>
* <Pad Comment>

* NODE NAME ALIASES
*   1 = B (106.5,41)
*   2 = GND (45,-23)
*   3 = A (22,41.5)
*   4 = OUT (64,40.5)
*   5 = VDD (64,67.5)
```

Simulation file	Type	Status	Input file	Output file	Options
Module3.sp	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	
NAND.spc	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	
NAND.spc	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	
NAND.spc	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	
NAND.spc	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	
NAND.spc	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	

Ready

Windows Taskbar: Ln 1 Col 43 NUM 5:05 AM 12/27/2020

T-Spice - [NAND.spc]

* <NMOS Capacitor>
* <PMOS Capacitor>
* <Poly1-Poly2 Capacitor>
* <Pad Comment>

* NODE NAME ALIASES
* 1 = B (106.5,41)
* 2 = GND (45,-23)
* 3 = A (22,41.5)
* 4 = OUT (64,40.5)
* 5 = VDD (64,67.5)

```
M4 OUT A VDD PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
* M4 DRAIN GATE SOURCE BULK (43 57.5 49 59.5)
M3 OUT B VDD PMOS L=2u W=28u AD=66p PD=24u AS=66p PS=24u
* M3 DRAIN GATE SOURCE BULK (81.5 57 87.5 59)
M2 OUT A N7 NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
* M2 DRAIN GATE SOURCE BULK (43 26.5 49 28.5)
M1 N7 B GND NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
* M1 DRAIN GATE SOURCE BULK (43 -13 49 -11)

.print tran v(A,GND) v(B,GND) v(OUT,GND)
.tran/op 20n 500n method=bdf
Vsupply VDD GND 5
VpulseA A GND PULSE (0 5 0 0 0 100n 200n)
VpulseB B GND PULSE (0 5 0 0 0 50n 100n)

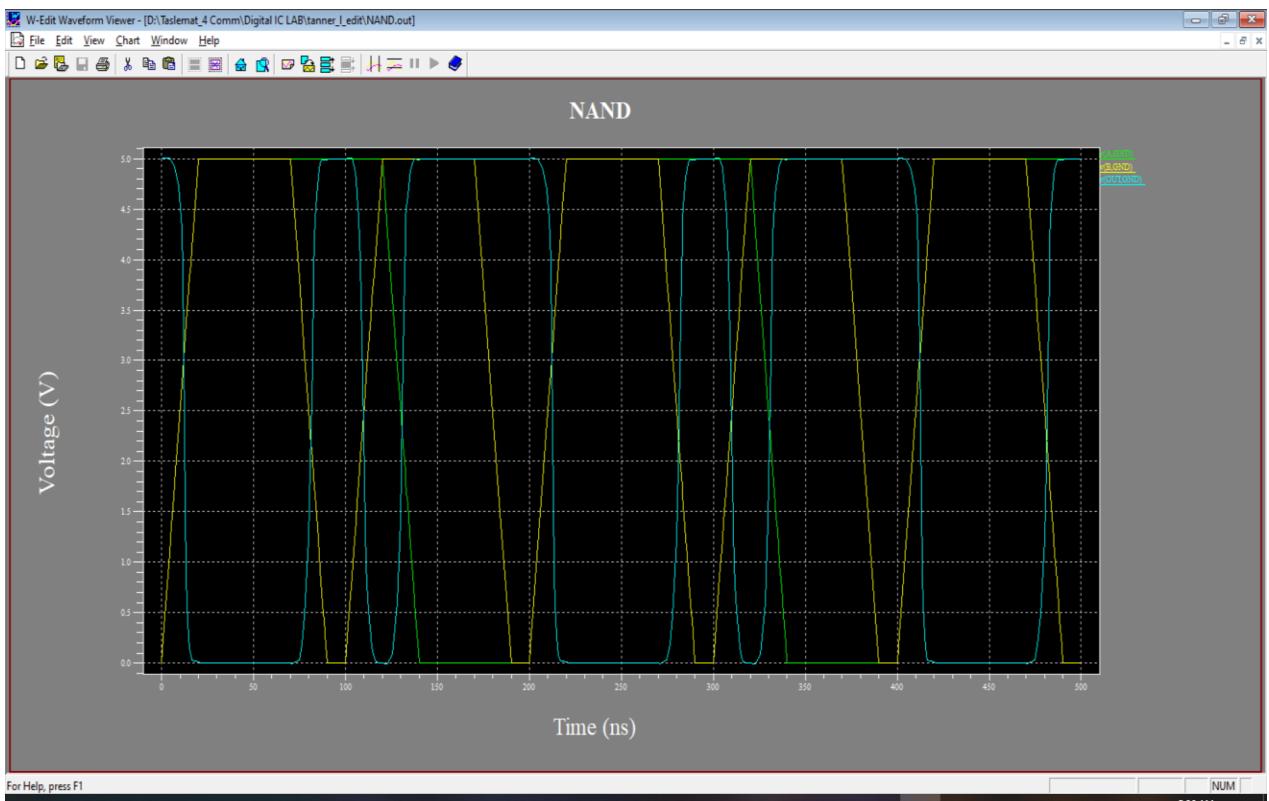
* Total Nodes: 5
* Total Elements: 4
* Total Number of Shorted Elements not written to the SPICE file: 0
* Extract Elapsed Time: 0 seconds
.END
```

Simulation file	Type	Status	Input file	Output file	Options
Module3.sp	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	
NAND.spc	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	
NAND.spc	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	
NAND.spc	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	
NAND.spc	T-Spice	finished	D:\Tasilem...	D:\Tasilem...	

Ready

Windows Taskbar: Ln 60 Col 1 NUM 5:05 AM 12/27/2020

• Screenshots of the Results from Simulation:



The LVS:

- The Netlist of the Layout:

T-Spice - [NAND.spic]

File Edit View Simulation Table Options Window Help

* <Poly1-Poly2 Capacitor>
* <Poly1 Resistor>
* <Pad Comment>
Warning: Layers with Zero Resistance.
* <NMOS Capacitor>
* <PMOS Capacitor>
* <Poly1-Poly2 Capacitor>
* <Pad Comment>

* NODE NAME ALIASES
1 = B (106.5,41)
2 = GND (45,-23)
3 = A (22,41.5)
4 = OUT (64,40.5)
5 = VDD (64,67.5)

.include m1s_20.md

M4 OUT A VDD VDD PMOS L=2u W=20 AD=66p PD=24u AS=66p PS=24u
* M4 DRAIN GATE SOURCE BULK (43 57.5 49 59.5)
M3 OUT B VDD VDD PMOS L=2u W=20 AD=66p PD=24u AS=66p PS=24u
* M3 DRAIN GATE SOURCE BULK (61.5 57 67.5 59)
M2 OUT A N7 GND NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
* M2 DRAIN GATE SOURCE BULK (43 26.5 49 28.5)
M1 N7 B GND GND NMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
* M1 DRAIN GATE SOURCE BULK (43 -13 49 -11)

* Total Nodes: 5
* Total Elements: 4
* Total Number of Shorted Elements not written to the SPICE file: 0
* Extract Elapsed Time: 0 seconds

.END

Simulation File	Type	Status	Input File	Output File	Options
NAND.spic	T-Spice	finished	D:\Taslem..	D:\Taslem..	
NAND.spic	T-Spice	finished	D:\Taslem..	D:\Taslem..	
NAND.spic	T-Spice	finished	D:\Taslem..	D:\Taslem..	
NAND.spic	T-Spice	finished	D:\Taslem..	D:\Taslem..	
NAND.spic	T-Spice	finished	D:\Taslem..	D:\Taslem..	
NAND.spic	T-Spice	finished	D:\Taslem..	D:\Taslem..	

Ready

Ln 56 Col 1 NUM

12/27/2020

• The Netlist of the Schematic:

T-Spice - [Module3.sp]

File Edit View Simulation Table Options Window Help

* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 27, 2020 at 01:59:11

* Waveform probing commands
.probe
.options probefilename="File3.dat"
+ probesdbfile="D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit\File3.sdb"
+ probetopmodule="Module3"

.include m15_20.md

* Main circuit: Module3
M1 N7 B GND GND NMOS L=2u W=12u AD=66p FD=24u AS=66p PS=24u
M2 OUT A N7 GND NMOS L=2u W=12u AD=66p FD=24u AS=66p PS=24u
M3 OUT B VDD VDD PMOS L=2u W=25u AD=66p FD=24u AS=66p PS=24u
M4 OUT A VDD VDD PMOS L=2u W=25u AD=66p FD=24u AS=66p PS=24u
* End of main circuit: Module3

Simulation file Type Status Input file Output file Options

NAND.spc	T-Spice	finished	D:\Tasleem...	D:\Tasleem...	
NAND.spc	T-Spice	finished	D:\Tasleem...	D:\Tasleem...	
NAND.spc	T-Spice	finished	D:\Tasleem...	D:\Tasleem...	
NAND.spc	T-Spice	finished	D:\Tasleem...	D:\Tasleem...	
NAND.spc	T-Spice	finished	D:\Tasleem...	D:\Tasleem...	
NAND.spc	T-Spice	finished	D:\Tasleem...	D:\Tasleem...	

Ready Ln 17 Col 31 NUM 5:14 AM ENG 12/27/2020

• The LVS Output:

