



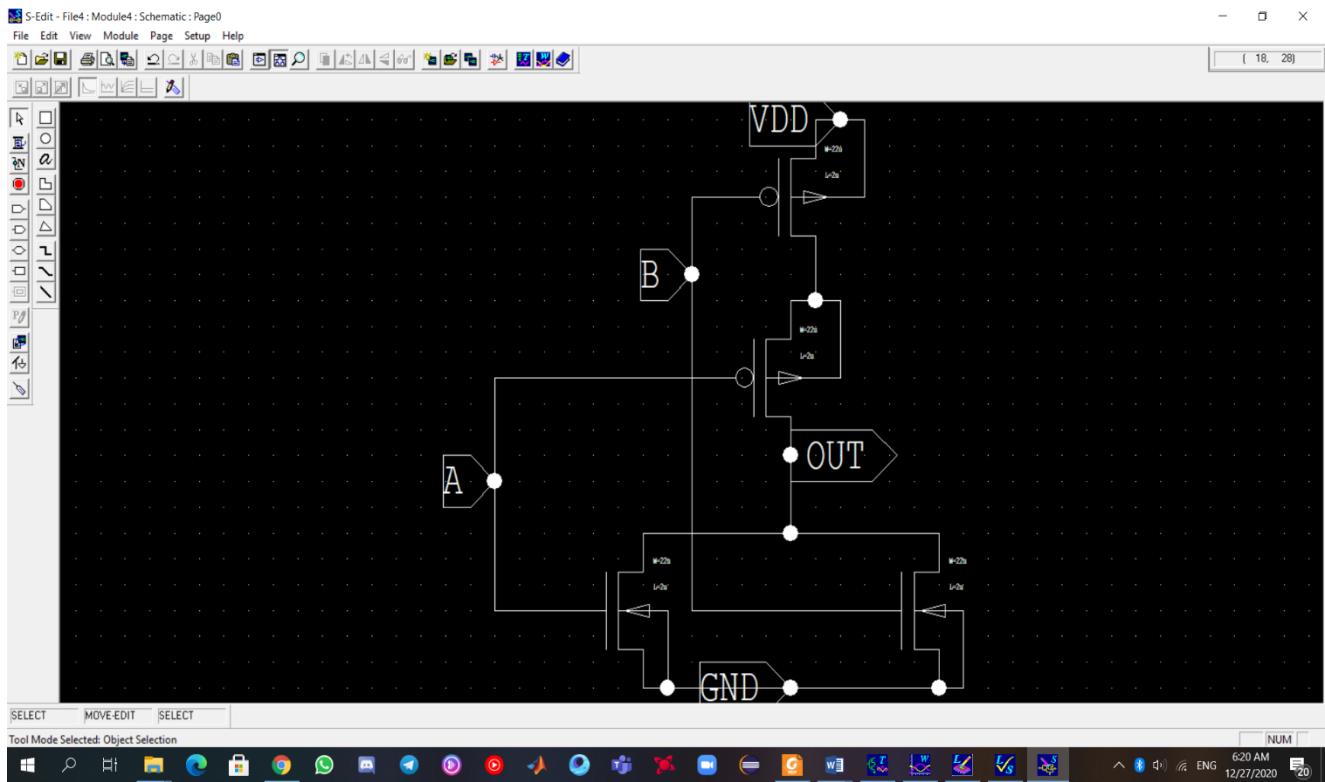
**Alexandria University.**  
**Faculty of Engineering.**  
**Electronics & Communication Department**  
**(Fourth Year).**  
**Digital ICs Lab.**

## **(3rd Lab.)**

### **CMOS Combinational Logic Gates: NOR Gate**

<b>Name</b>	<b>Section</b>	<b>ID</b>
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<b>Aya Shaaban Mahmoud Elsayed</b>	<b>1</b>	<b>7</b>

# Screenshot of Schematic:



# Logic Functionality Test:

- The Netlist:

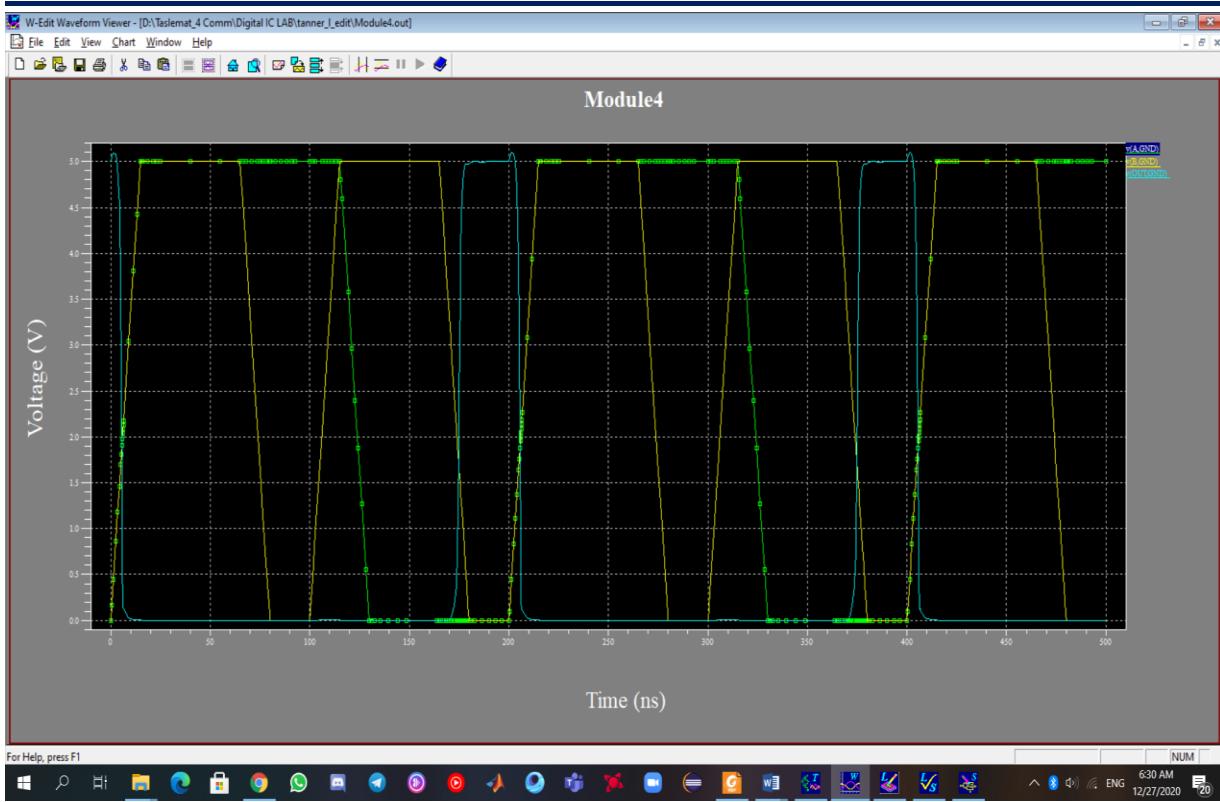
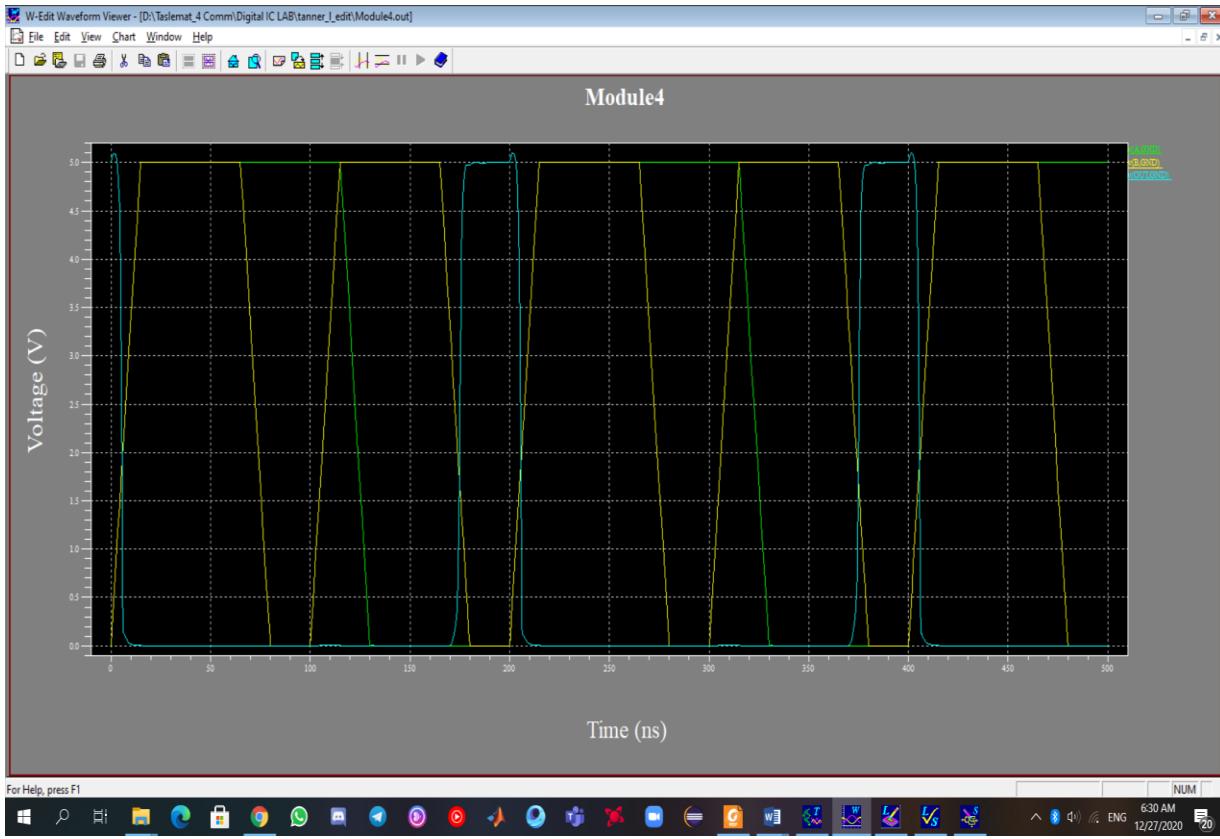
```
T-Spice - [Module4.sp]
File Edit View Simulation Table Options Window Help
[Icons]
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 27, 2020 at 06:21:28
* Waveform probing commands
*.PROBE
*.OPTIONS probefilename="sedit.dat"
+ probesdbfile="file4.sdb"
+ probetopmodule="Module4"
.include "D:\Tasleemar_4 Comm\Digital IC LAB\tanner_1_edit\ml5_20.md"

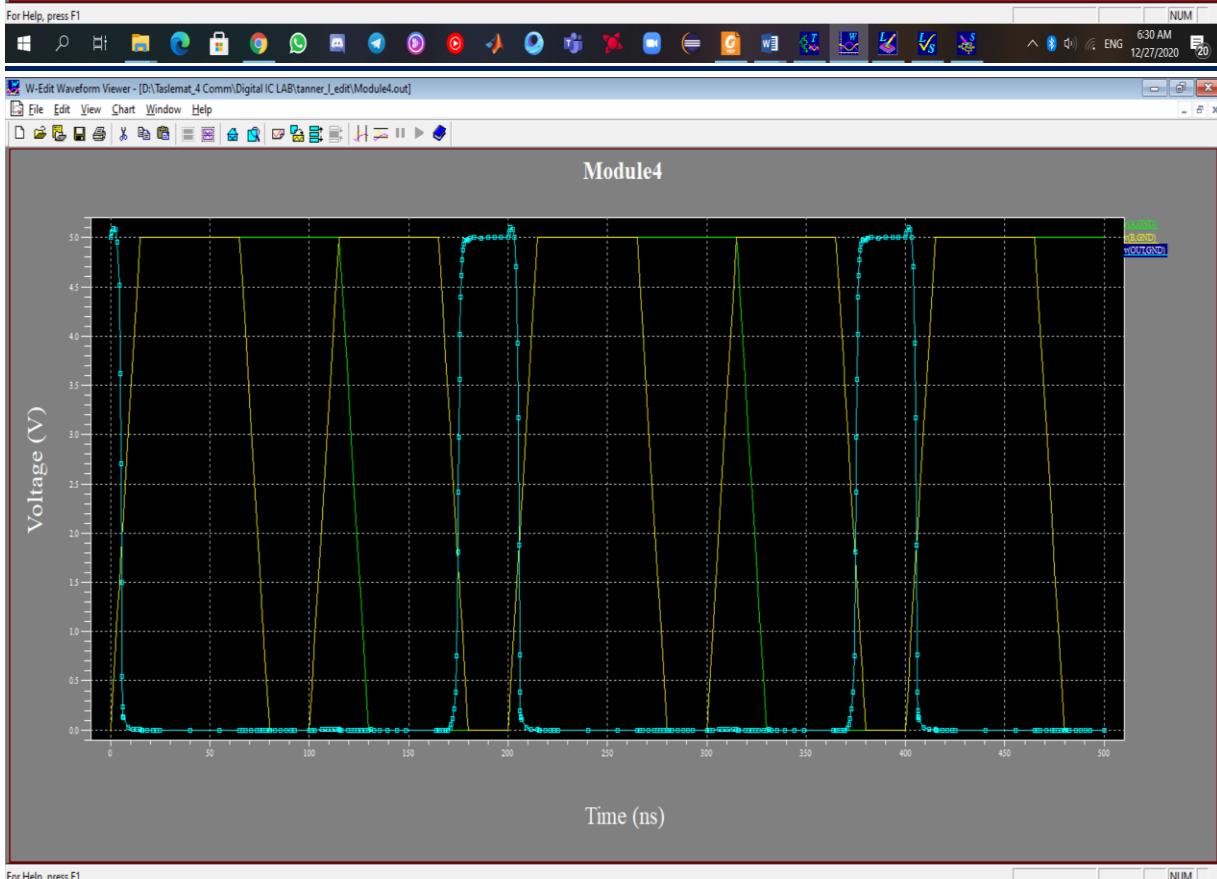
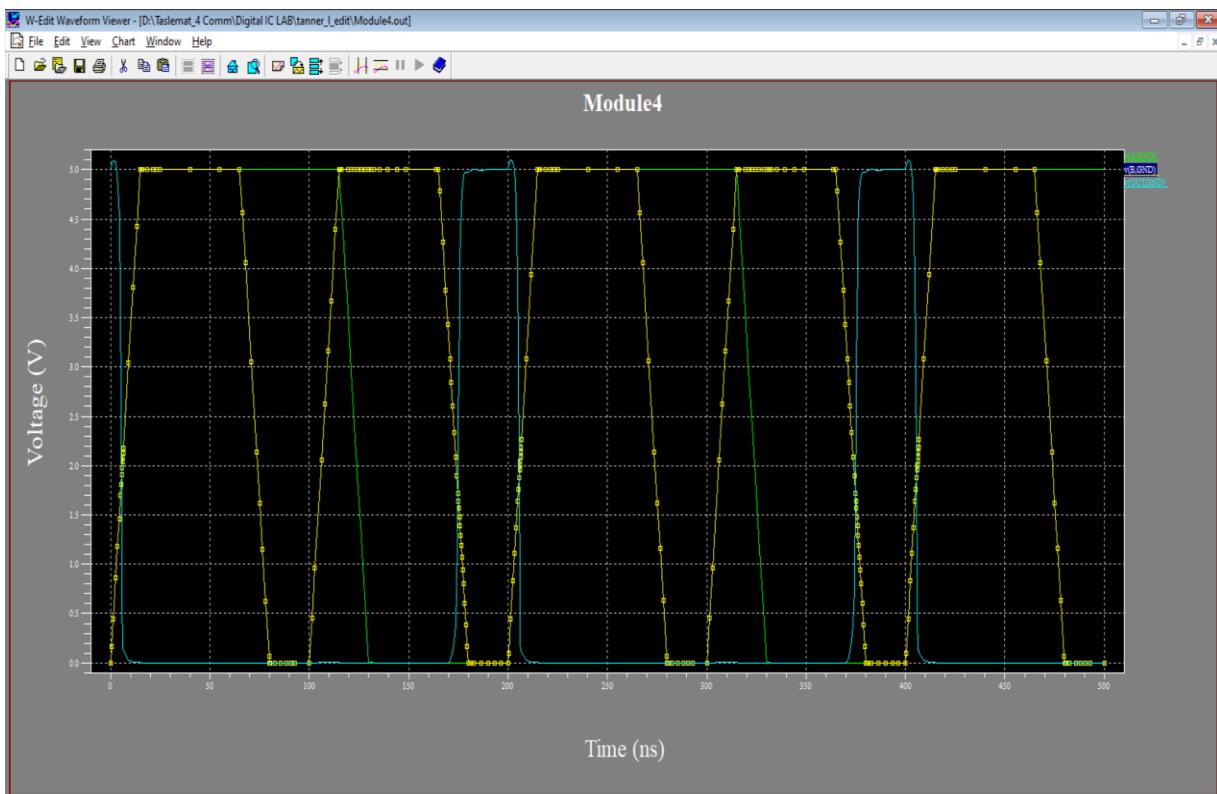
* Main circuit: Module4
M1 OUT A GND NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 OUT B GND NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M3 N1 B VDD VDD PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M4 OUT A N1 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module4

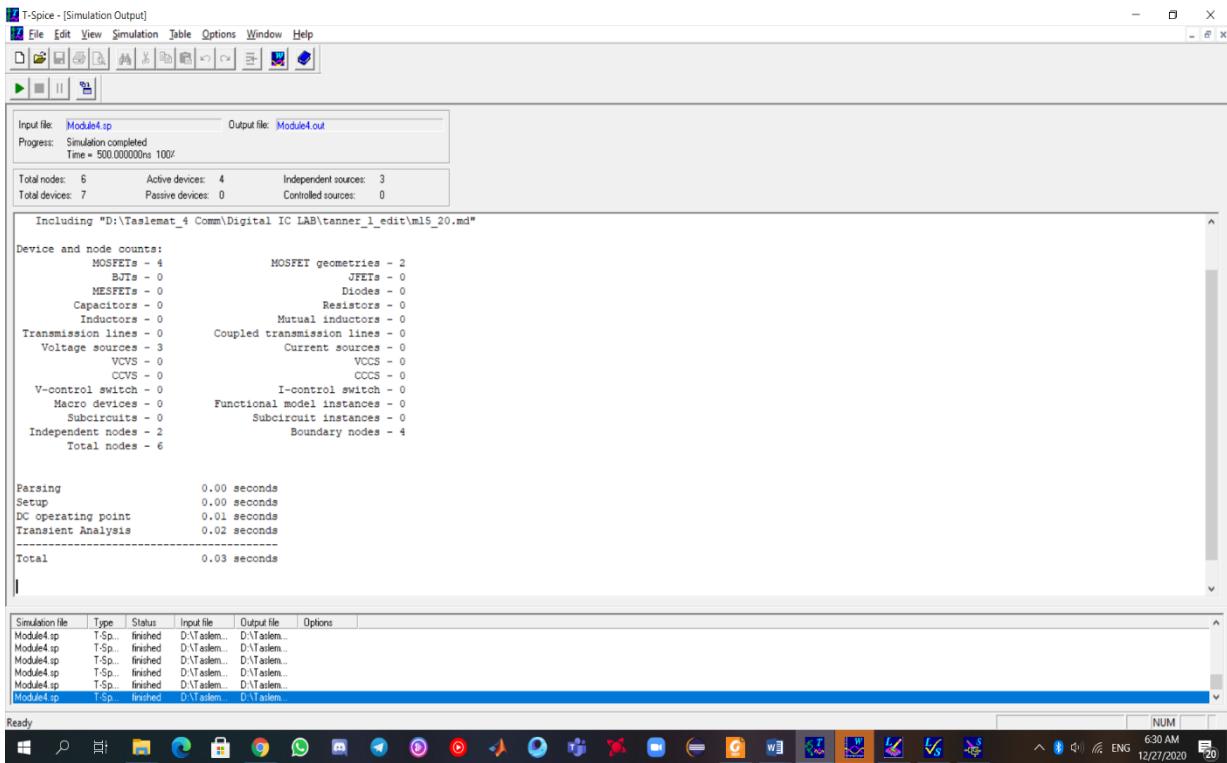
.print tran v(A,GND) v(B,GND) v(OUT,GND)
.tran/op 15m 50n method=bdf
Vsupply VDD GND 5
VpulsestateA A GND PULSE (0 5 0 0 0 100n 200n)
VpulsestateB B GND PULSE (0 5 0 0 0 50n 100n)

Simulation file Type Status Input file Output file Options
NAND.spc T-Sp.. finished D:\Tasleemar_4 Comm\Digital IC LAB\tanner_1_edit\ml5_20.spc
Module4.sp T-Sp.. finished D:\Tasleemar_4 Comm\Digital IC LAB\tanner_1_edit\Module4.spc
Module4.spc T-Sp.. finished D:\Tasleemar_4 Comm\Digital IC LAB\tanner_1_edit\Module4.spc
Module4.spc T-Sp.. finished D:\Tasleemar_4 Comm\Digital IC LAB\tanner_1_edit\Module4.spc
Module4.spc T-Sp.. finished D:\Tasleemar_4 Comm\Digital IC LAB\tanner_1_edit\Module4.spc
```

## • Screenshots of the Results from Simulation:







**From above Screenshots of the Results waveforms from Simulation we found that the logic functionality of the design satisfies the NOR gate properties.**

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

## Transistors Sizing in “Worst Case” Scenario:

**1- For the “worst case” delay we can size the Transistors in the PUN (Pull-Up Network) as follows:**

**(W/L) for PUN Transistors = 2 \* (W/L) for P-MOS  
in the basic Matched Inverter.**

**So, we will put (W) for PUN Transistors = 56  $\mu\text{m}$ .**

**2- For the “worst case” delay we can size the Transistors in the PDN (Pull-Down Network) as follows:**

**(W/L) for PDN Transistors = (W/L) for N-MOS in the basic Matched Inverter.**

**So, we will put (W) for PDN Transistors = 6  $\mu\text{m}$ .**

T-Spice - [Module4.sp]

File Edit View Simulation Table Options Window Help

□ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □

\* SPICE netlist written by S-Edit Win32 6.02  
\* Written on Dec 27, 2020 at 06:21:28

\* Waveform probing commands  
.probe  
.options probefilename="sedit.dat"  
+ probesdbfile="file4.sdb"  
+ probetopmodule="Module4"  
.include "D:\Tasleemat\_4 Comm\Digital IC LAB\tanner\_1\_edit\ml5\_20.msd"

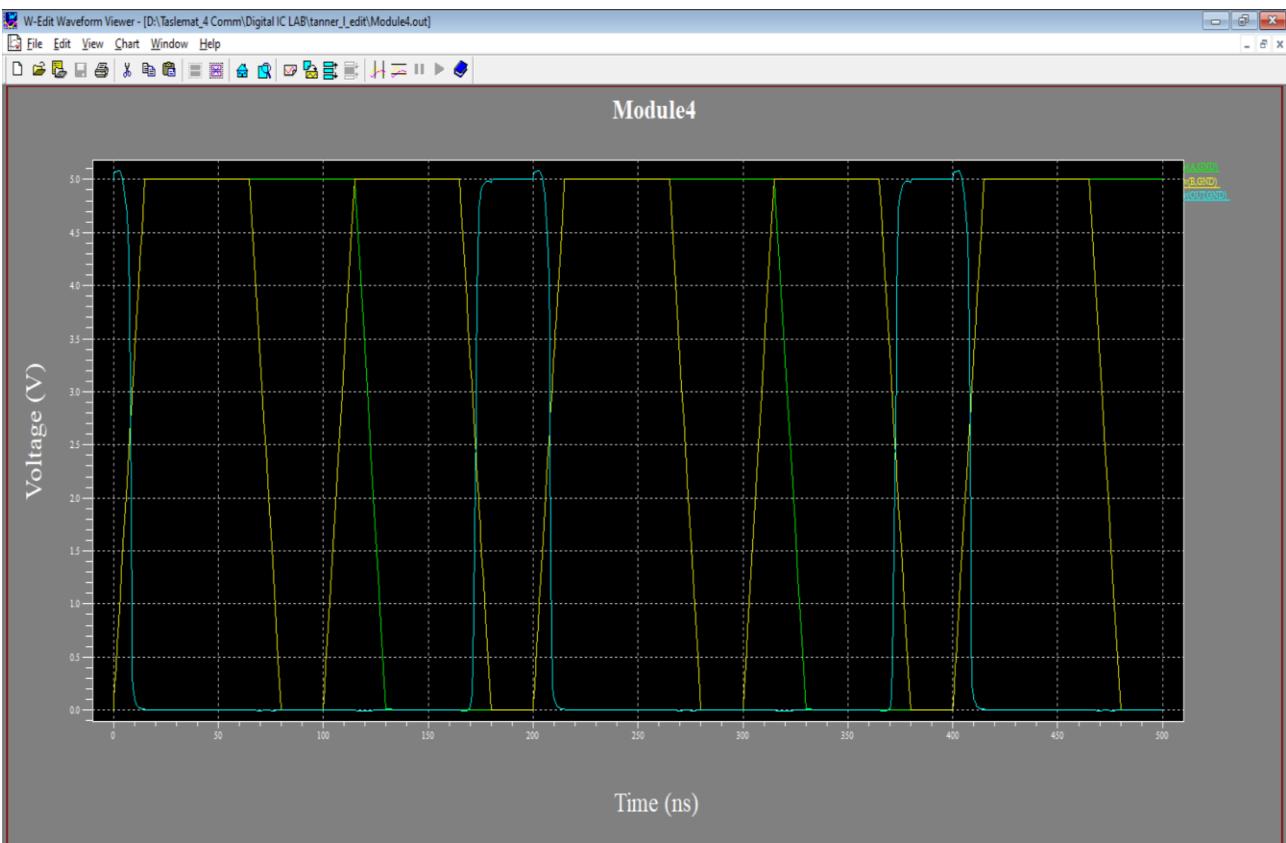
\* Main circuit: Module4  
M1 OUT A GND GND NMOS L=2u W=6u AD=66p PD=24u AS=66p FS=24u  
M2 OUT B GND GND NMOS L=2u W=6u AD=66p PD=24u AS=66p FS=24u  
M3 N4 B VDD VDD PMOS L=2u W=56u AD=66p PD=24u AS=66p FS=24u  
M4 OUT A N4 N4 PMOS L=2u W=56u AD=66p PD=24u AS=66p FS=24u  
\* End of main circuit: Module4

.print tran v(A,GND) v(B,GND) v(OUT,GND)  
.tran/op 15n 500n method=bdf  
Vsupply VDD GND 5  
VpulseateA A GND PULSE (0 5 0 0 0 100n 200n)  
VpulseateB B GND PULSE (0 5 0 0 0 50n 100n)

Simulation file	Type	Status	Input file	Output file	Options
Module4.sp	T-Sp.	finished	D:\Tasleem...	D:\Tasleem...	
Module4.sp	T-Sp.	finished	D:\Tasleem...	D:\Tasleem...	
Module4.sp	T-Sp.	finished	D:\Tasleem...	D:\Tasleem...	
Module4.sp	T-Sp.	finished	D:\Tasleem...	D:\Tasleem...	
Module4.sp	T-Sp.	finished	D:\Tasleem...	D:\Tasleem...	
Module4.sp	T-Sp.	finished	D:\Tasleem...	D:\Tasleem...	

Ready Ln 15 , Col 31 NUM

Windows Taskbar icons: File Explorer, Edge, Google Chrome, WhatsApp, Telegram, YouTube, MATLAB, Python, Powerpoint, Word, Excel, SolidWorks, and others.



For Help, press F1

T-Spice - [Simulation Output]

File Edit View Simulation Table Options Window Help

Input file: Module4.sp      Output file: Module4.out

Progress: Simulation completed  
Time = 500.000000ns 100%

Total nodes: 6      Active devices: 4      Independent sources: 3  
Total devices: 7      Passive devices: 0      Controlled sources: 0

Including "D:\Tasleemat\_4\Comm\Digital IC LAB\tanner\_1\_edit\ml5\_20.md"

Device and node counts:

MOSFETs - 4	MOSFET geometries - 2
BJTIs - 0	JFETIs - 0
MESFETIs - 0	Diodes - 0
Capacitors - 0	Resistors - 0
Inductors - 0	Mutual inductors - 0
Transmission lines - 0	Coupled transmission lines - 0
Voltage sources - 3	Current sources - 0
VCVS - 0	VCOS - 0
CCVS - 0	CCCS - 0
V-control switch - 0	I-control switch - 0
Macro devices - 0	Functional model instances - 0
Subcircuits - 0	Subcircuit instances - 0
Independent nodes - 2	Boundary nodes - 4
Total nodes - 6	

Parsing                    0.00 seconds  
Setup                    0.00 seconds  
DC operating point    0.01 seconds  
Transient Analysis    0.02 seconds  
-----  
Total                    0.03 seconds

Simulation file	Type	Status	Input file	Output file	Options
Module4.sp	T-Spice	finished	D:\Tasleemat...	D:\Tasleemat...	
Module4.in	T-Spice	finished	D:\Tasleemat...	D:\Tasleemat...	

## • $\tau$ P Calculation

```

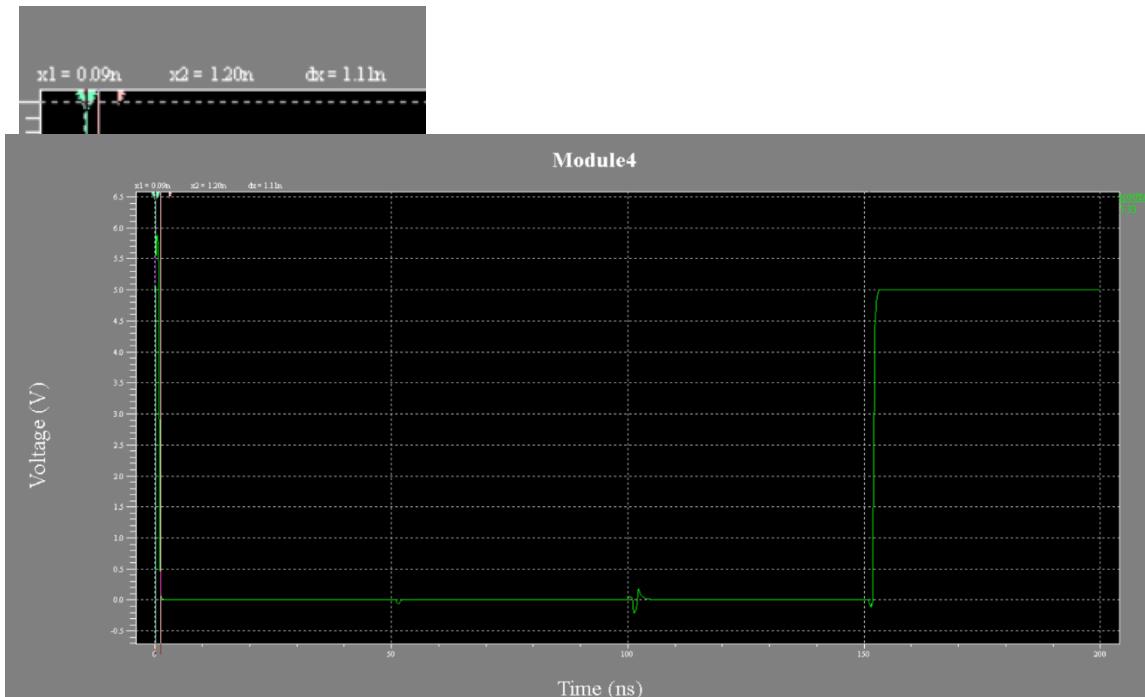
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 27, 2020 at 06:21:28

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="File4.sdb"
+ probetopmodule="Module4"
.include "H:\tanner_1_edit\m15_20.md"

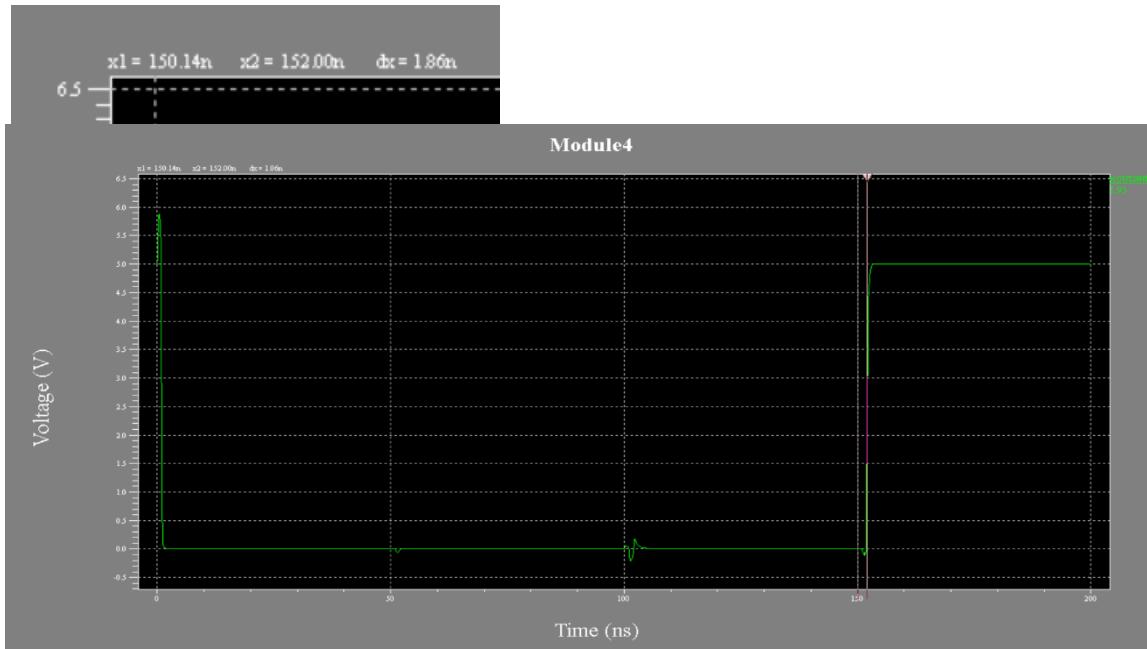
* Main circuit: Module4
M1 OUT A GND GND NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u
M2 OUT B GND GND NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u
M3 N4 B VDD VDD PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u
M4 OUT A N4 N4 PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module4

.print tran v(OUT,GND)
.tran/op 1n 200n method=bdf
Vsupply VDD GND 5
VpulseA A GND PULSE (0 5 0 0 0 100n 200n)
VpulseB B GND PULSE (0 5 0 0 0 50n 100n)

```



$$\tau_{PHL} = 1.11 \text{ nsec}$$



$$\tau_{PLH} = 1.86 \text{ nsec}$$

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \frac{1.11 + 1.86}{2} = 1.485 \text{ nsec}$$

## VTC

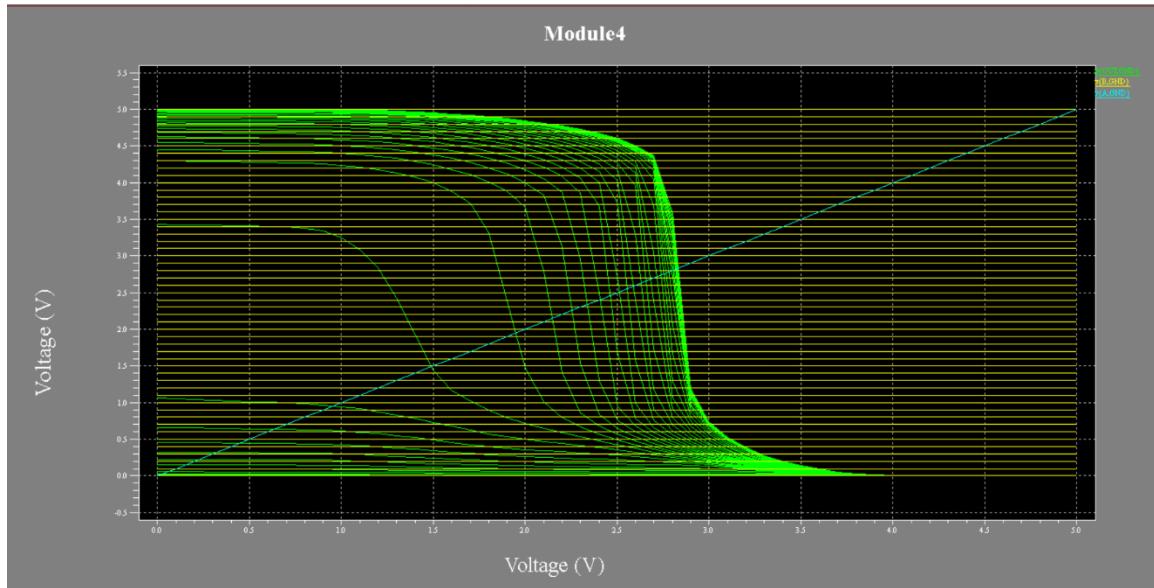
- DC Sweep for two inputs (A&B)

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 27, 2020 at 06:21:28

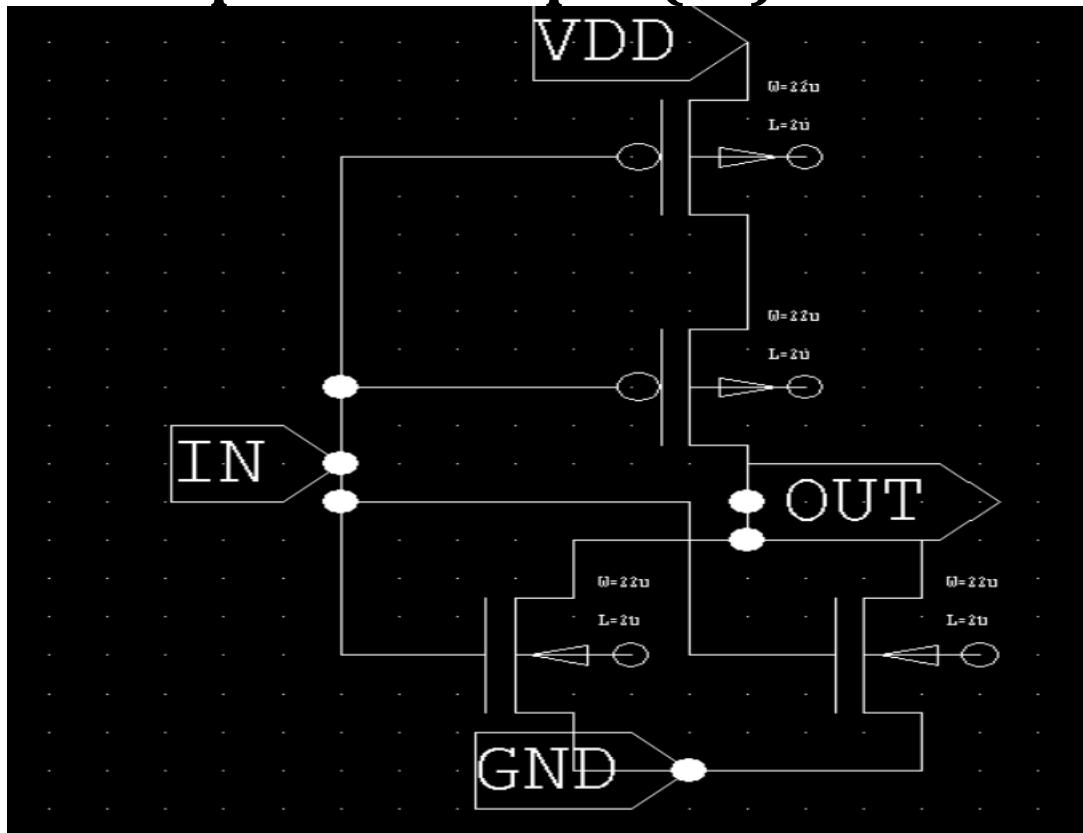
* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="File4.sdb"
+ probetopmodule="Module4"
.include "H:\tanner_1_edit\m15_20.md"

* Main circuit: Module4
M1 OUT A GND GND NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u
M2 OUT B GND GND NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u
M3 N4 B VDD VDD PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u
M4 OUT A N4 N4 PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module4

.dc lin source VpulsateA 0 5 0.1 sweep lin source VpulsateB 0 5 0.1
.print dc v(A,GND) v(B,GND) v(OUT,GND)
Vsupply VDD GND 5
VpulsateA A GND PULSE (0 5 0 0 0 100n 200n)
VpulsateB B GND PULSE (0 5 0 0 0 50n 100n)
```



- DC Sweep for one input (IN)



```

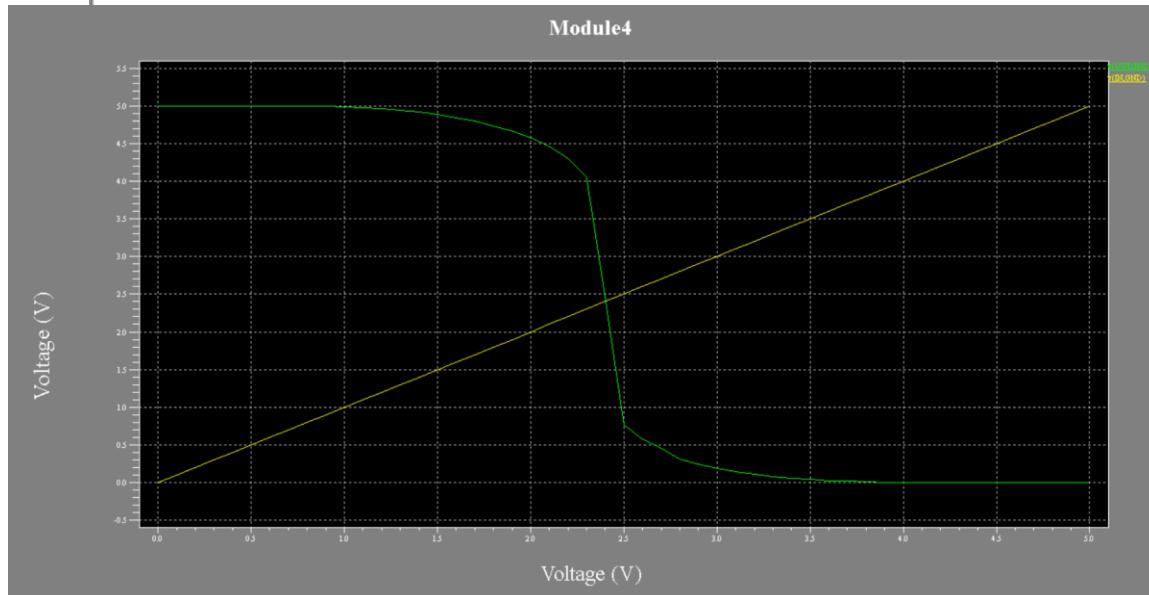
* SPICE netlist written by S-Edit Win32 6.02
* Written on Jan 8, 2021 at 15:38:46

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="modele4.sdb"
+ probetopmodule="Module4"
.include "H:\tanner_1_edit\m15_20.md"

* Main circuit: Module4
M1 OUT IN GND N2 NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u
M2 OUT IN GND N6 NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u
M3 N3 IN VDD N4 PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u
M4 OUT IN N3 N5 PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module4

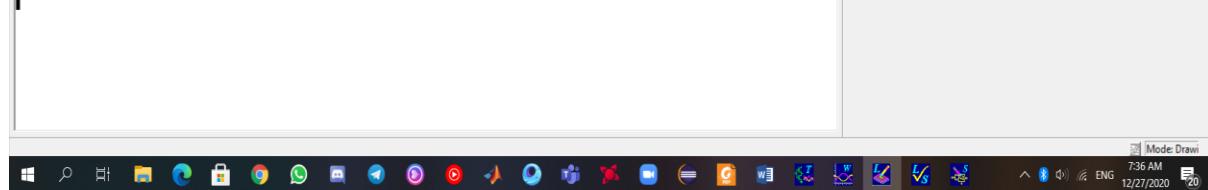
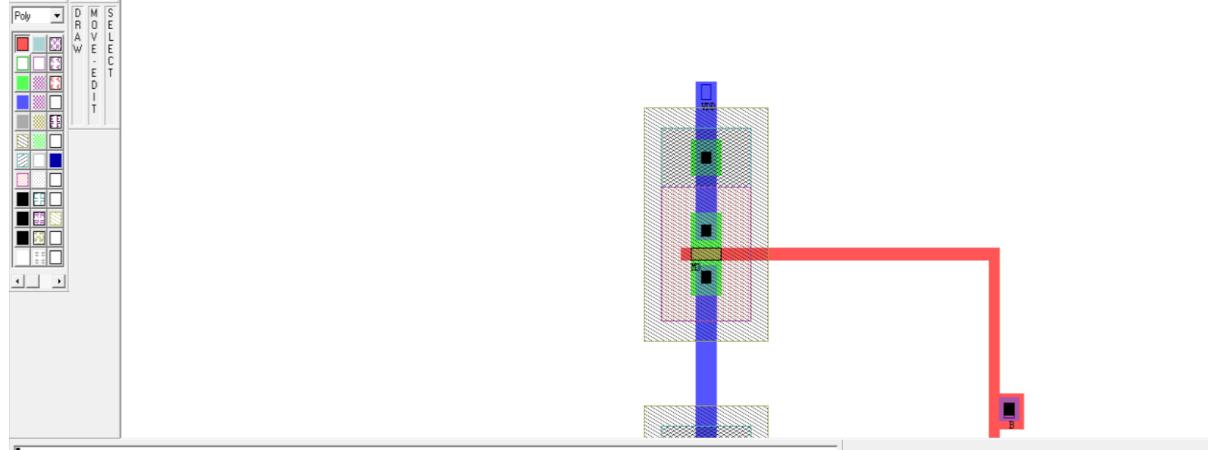
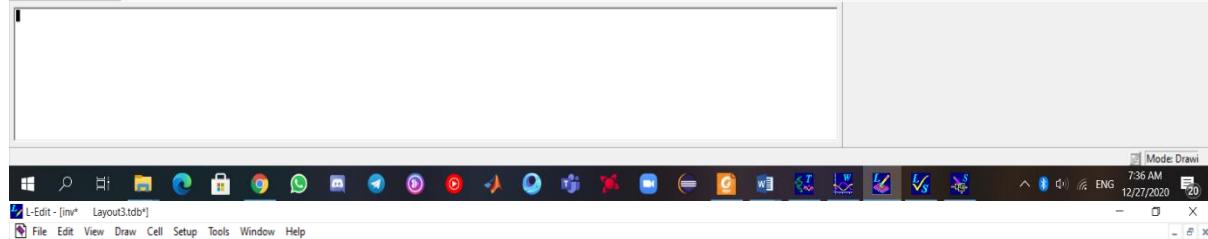
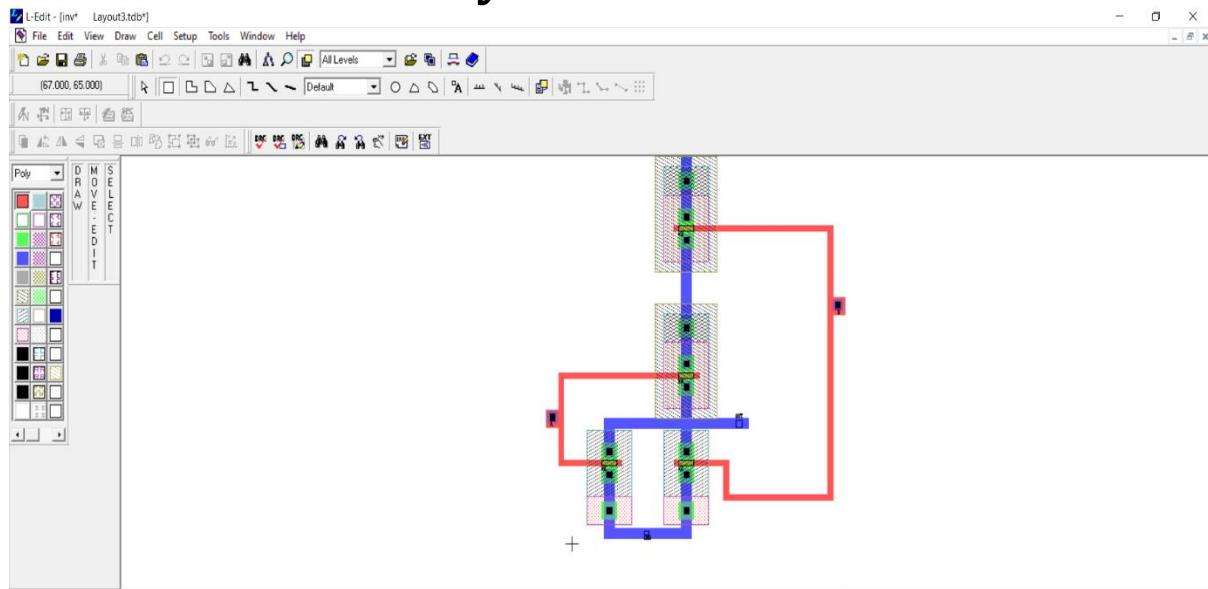
.dc lin source Vpulse 0 5 0.1
.print dc v(IN,GND) v(OUT,GND)
Vsupply VDD GND 5
Vpulse IN GND PULSE (0 5 0 0 0 50n 100n)

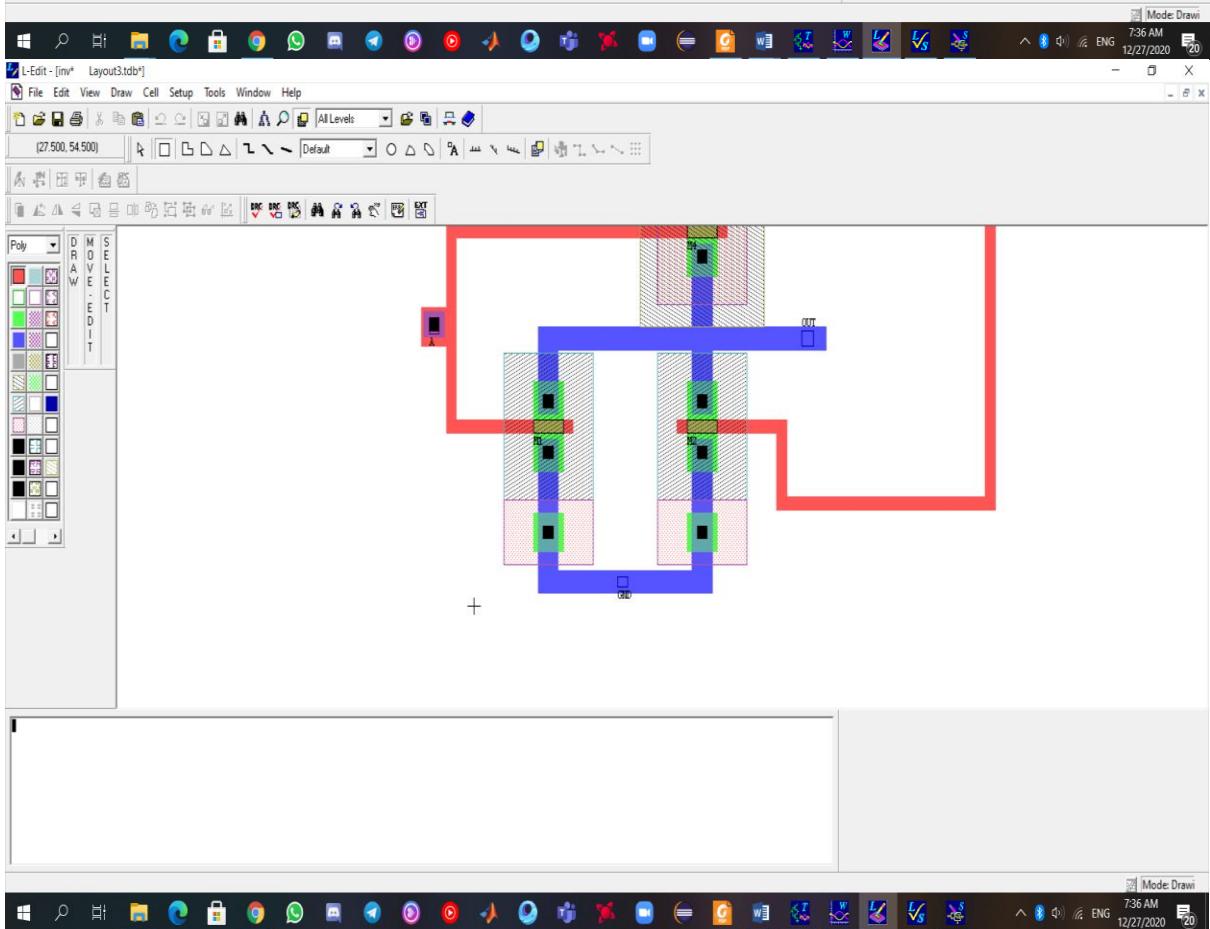
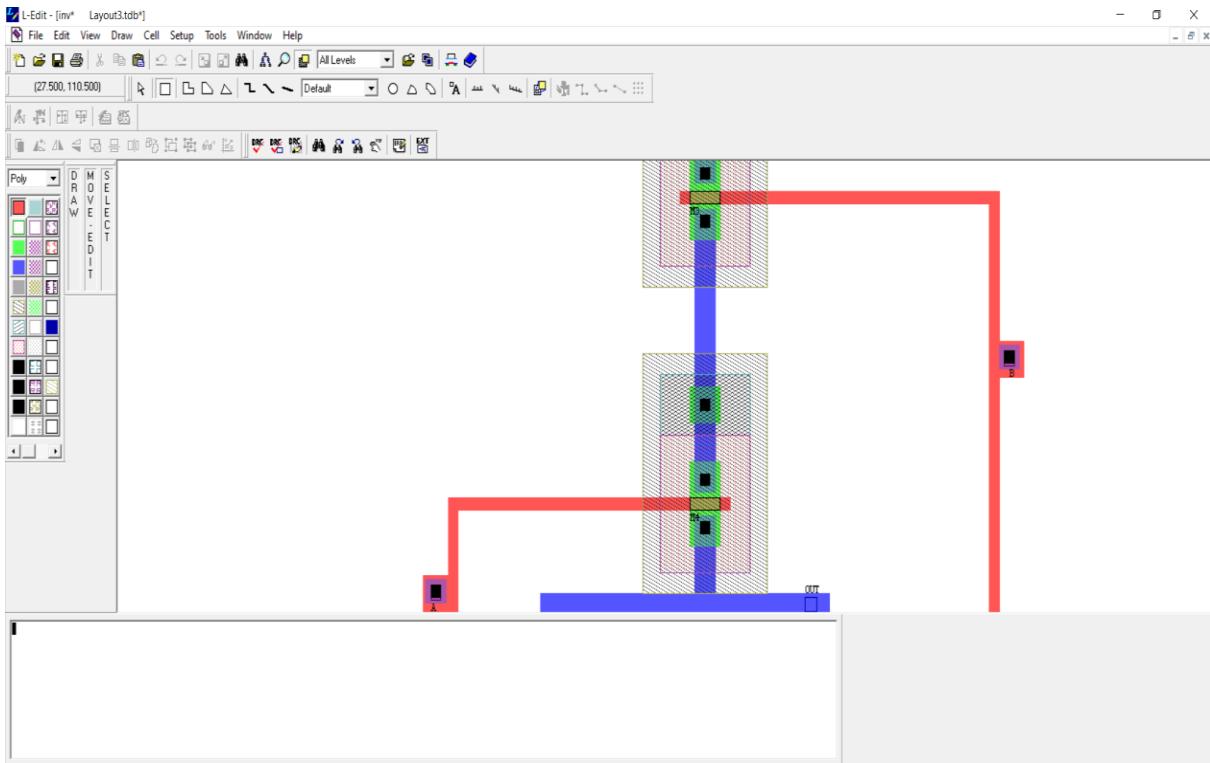
```



# The Layout:

## • Screenshots of Layout:





# Screenshots of Netlist File (Extracted File):

L-Edit - [inv Layout3.tdb]

File Edit View Draw Cell Setup Tools Window Help

42 000 58 000

Poly H M

Extract

General Output Subcircuit

Comments

- Write node names
- Write device coordinates (Locator Units)
- Write shorted devices
- Write layer capacitance and resistance warnings

Write nodes and devices as

- Integers
- Names

Format

- Write values in scientific notation
- Write verbose SPICE statements
- Write empty subcircuit definitions
- Write END statement

Nodal parasitic capacitance

- Write nodal parasitic capacitance
- Ignore nodal parasitic capacitance less than [5] Femtoladra

SPICE include statement:

```
include "D:\Tasleimat_4 Comm\Digital IC LAB\tanner_1_edit\models\ml2_20.md"
```

Run Cancel Accept

T-Spice - [NOR.sp]

File Edit View Simulation Table Options Window Help

Circuit Extracted by Tanner Research's L-Edit Version 8.30 / Extract Version 8.30 ;

IDB File: D:\Tasleimat\_4 Comm\Digital IC LAB\tanner\_1\_edit\Layout3.tdb

Cell: inv Version 1.06

Extract Definition File: mornbn20.ext

Extract Date and Time: 12/27/2020 - 07:21

.include "D:\Tasleimat\_4 Comm\Digital IC LAB\tanner\_1\_edit\models\ml2\_20.md"

\* Warning: Layers with Unassigned AREA Capacitance.

- <P Diff Resistor>
- <Poly Resistor>
- <N Diff Resistor>
- <P Base Resistor>
- <N Well Resistor>
- <Poly2 Resistor>

\* Warning: Layers with Unassigned FRINGE Capacitance.

- <P Diff Resistor>
- <Poly Resistor>
- <N Diff Resistor>
- <P Base Resistor>
- <N Well Resistor>
- <Poly1-Poly2 Capacitor>
- <Poly2 Resistor>
- <Pad Comment>

\* Warning: Layers with Zero Resistance.

- <NMOS Capacitor>
- <PMOS Capacitor>
- <Poly1-Poly2 Capacitor>
- <Pad Comment>

\* NODE NAME ALIASES

- 1 = B (106.5,81.5)
- 2 = A (-9,42.5)
- 4 = OUT (66,40.5)
- 5 = GND (29,3)
- 6 = VDD (44, 13A)

Simulation file	Type	Status	Input file	Output file	Options
Module4.sp	T-Sp.	finished	D:\Tasleimat...	D:\Tasleimat...	
Module4.sp	T-Sp.	finished	D:\Tasleimat...	D:\Tasleimat...	
Module4.sp	T-Sp.	finished	D:\Tasleimat...	D:\Tasleimat...	
Module4.ip	T-Sp.	finished	D:\Tasleimat...	D:\Tasleimat...	
Module4.ip	T-Sp.	finished	D:\Tasleimat...	D:\Tasleimat...	
NOR.sp	T-Sp.	finished	D:\Tasleimat...	D:\Tasleimat...	

Ready

T-Spice - [NOR.sp]

File Edit View Simulation Table Options Window Help

Warning: Layers with Zero Resistance.

<NMOS Capacitor>

<PMOS Capacitor>

<Poly+Poly2 Capacitor>

<Pad Comment>

\* NODE NAME ALIASES

1 = B (106.5,81.5)  
 2 = A (-9,42.5)  
 4 = OUT (66,40.5)  
 5 = GND (29,3)  
 6 = VDD (45,136)

M3 N4 B VDD VDD PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u  
 \* M3 DRAIN GATE SOURCE BULK (43 108.5 49 110.5)  
 M4 OUT A N4 N4 PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u  
 \* M4 DRAIN GATE SOURCE BULK (43 57.5 49 59.5)  
 M1 OUT A GND NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u  
 \* M1 DRAIN GATE SOURCE BULK (12 27 18 29)  
 M2 OUT B GND NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u  
 \* M2 DRAIN GATE SOURCE BULK (43 27 49 29)

.print tran v(A,GND) v(B,GND) v(OUT,GND)  
 .tran/op 15n 500n method=bdf  
 Vsupply VDD GND 5  
 VpulseA A GND PULSE (0 5 0 0 0 100n 200n)  
 VpulseB B GND PULSE (0 5 0 0 0 50n 100n)

\* Total Nodes: 6  
 \* Total Elements: 4  
 \* Total Number of Shorted Elements not written to the SPICE file: 0  
 \* Extract Elapsed Time: 0 seconds  
 ,END

Simulation file	Type	Status	Input file	Output file	Options
Module4.sp	T-Spice	finished	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	
Module4.sp	T-Spice	finished	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	
Module4.sp	T-Spice	finished	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	
Module4.sp	T-Spice	finished	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	
NOR.sp	T-Spice	finished	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	D:\Tasleem\4 Comm\Digital IC LAB\tanner_1_edit	

Ready

## • Screenshots of the Results from Simulation:



T-Spice - [Simulation Output]

File Edit View Simulation Table Options Window Help

Input file: NOR.spc      Output file: NOR.out

Progress: Simulation completed  
Time = 500.000000ns 100%

Total nodes:	6	Active devices:	4	Independent sources:	3
Total devices:	7	Passive devices:	0	Controlled sources:	0

Including "D:\Tasleimat\_4\Comm\Digital IC LAB\tanner\_1\_edit\models\ml2\_20.md"

Device and node counts:  
 MOSFETs - 4      MOSFET geometries - 2  
 BJTs - 0      JFETs - 0  
 MESFETs - 0      Diodes - 0  
 Capacitors - 0      Resistors - 0  
 Inductors - 0      Mutual inductors - 0  
 Transmission lines - 0      Coupled transmission lines - 0  
 Voltage sources - 3      Current sources - 0  
 VCVS - 0      VCCS - 0  
 CCVS - 0      CCCS - 0  
 V-control switch - 0      I-control switch - 0  
 Macro devices - 0      Functional model instances - 0  
 Subcircuits - 0      Subcircuit instances - 0  
 Independent nodes - 2      Boundary nodes - 4  
 Total nodes - 6

Parsing      0.00 seconds  
 Setup      0.00 seconds  
 DC operating point      0.00 seconds  
 Transient Analysis      0.01 seconds  
 -----  
 Total      0.01 seconds

Simulation file	Type	Status	Input file	Output file	Options
Module4.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module4.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module4.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module4.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
NOR.spc	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
NOR.spc	T-Sp.	finished	D:\Taslem...	D:\Taslem...	

Ready

## The LVS:

- The Netlist of the Layout:

T-Spice - [NOR.spc]

File Edit View Simulation Table Options Window Help

\* <P Base Resistor>  
 \* <N Well Resistor>  
 \* <Poly1-Poly2 Capacitor>  
 \* <Pad Comment>  
 \* <Pad Comment>  
 \* Warning: Layers with Zero Resistance.  
 \* <NMOS Capacitor>  
 \* <PMOS Capacitor>  
 \* <Poly1-Poly2 Capacitor>  
 \* <Pad Comment>

\* NODE NAME ALIASES  
 \* 1 = B (106.5,81.5)  
 \* 2 = A (-9,42.5)  
 \* 4 = OUT (66,40.5)  
 \* 5 = GND (29,3)  
 \* 6 = VDD (45,136)

.include ml5\_20.md

M3 N4 B VDD VDD PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u  
 \* M3 DRAIN GATE SOURCE BULK (43 108.5 49 110.5)  
 M4 OUT A N4 NMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u  
 \* M4 DRAIN GATE SOURCE BULK (43 57.5 49 59.5)  
 M1 OUT B GND GND MNOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u  
 \* M1 DRAIN GATE SOURCE BULK (12 27 18 29)  
 M2 OUT B GND GND MNOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u  
 \* M2 DRAIN GATE SOURCE BULK (43 27 49 29)

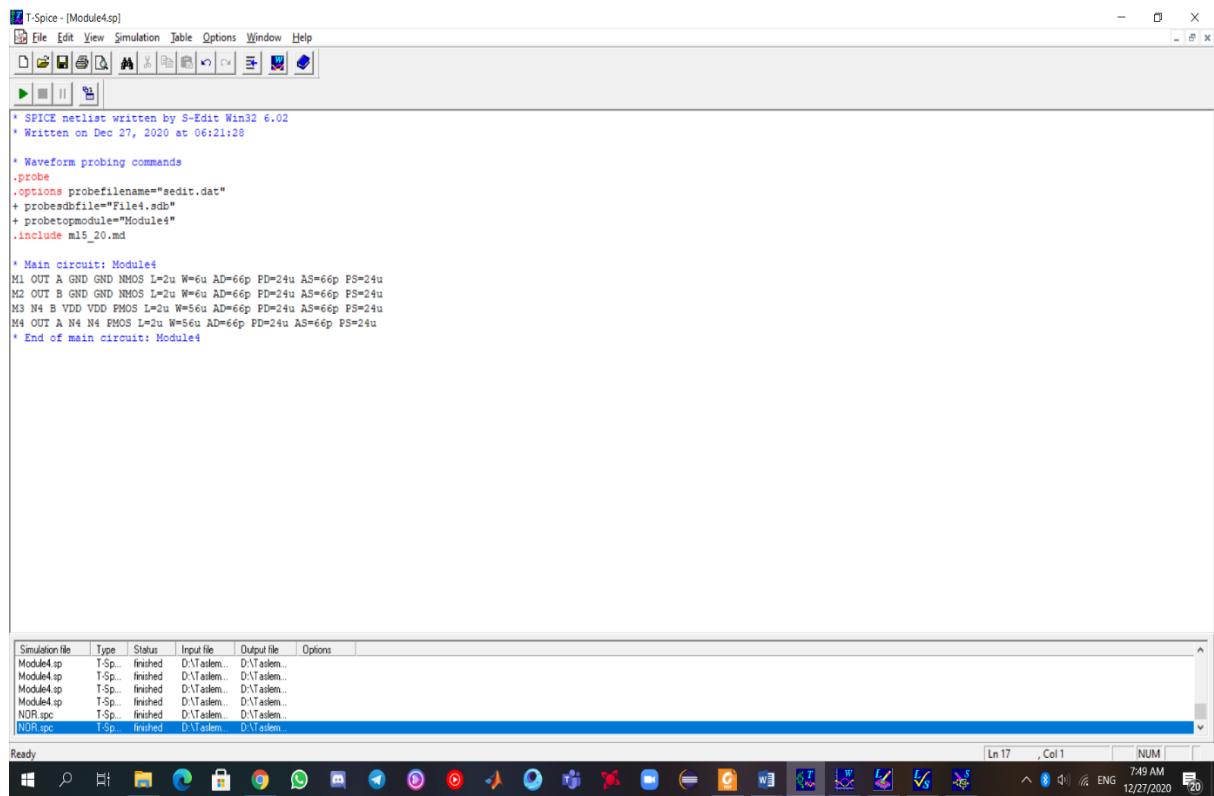
\* Total Nodes: 6  
 \* Total Elements: 4  
 \* Total Number of Shorted Elements not written to the SPICE file: 0  
 \* Extract Elapsed Time: 0 seconds

,END

Simulation file	Type	Status	Input file	Output file	Options
Module4.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module4.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module4.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
Module4.sp	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
NOR.spc	T-Sp.	finished	D:\Taslem...	D:\Taslem...	
NOR.spc	T-Sp.	finished	D:\Taslem...	D:\Taslem...	

Ready

- The Netlist of the Schematic:



The screenshot shows the T-Spice software interface with the file `Module4.sp` open. The window title is "T-Spice - [Module4.sp]". The menu bar includes File, Edit, View, Simulation, Table, Options, Window, and Help. The toolbar contains icons for opening files, saving, zooming, and simulation. The main text area displays the SPICE netlist, which includes probe commands for waveform analysis and a detailed description of the circuit components (NMOS and PMOS transistors) and their connections.

```

T-Spice - [Module4.sp]
File Edit View Simulation Table Options Window Help
[Icons]
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 27, 2020 at 06:21:28

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="File4.sdb"
+ probetopmodule="Module4"
.include m15_20.md

* Main circuit: Module4
M1 OUT A GND GND NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u
M2 OUT B GND GND NMOS L=2u W=6u AD=66p PD=24u AS=66p PS=24u
M3 N4 B VDD VDD PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u
M4 OUT A N4 N4 PMOS L=2u W=56u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: Module4

```

Below the netlist, a table shows the status of various simulations:

Simulation File	Type	Status	Input File	Output File	Options
Module4.sp	T-Sp	finished	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\NOR.spc	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\NOR.out	
Module4.sp	T-Sp	finished	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\Module4.sp	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\Module4.out	
Module4.sp	T-Sp	finished	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\Module4.sp	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\Module4.out	
Module4.sp	T-Sp	finished	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\Module4.sp	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\Module4.out	
NOR.spc	T-Sp	finished	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\NOR.spc	D:\Tastelma_4\Comm\Digital IC LAB\Vanner_L_Edits\NOR.out	

The status bar at the bottom indicates "Ready" and shows system information like date and time.

- The LVS Output:

