Electrical Engineering Department,

Fourth Year - Communications & Electronics.

EE 431 DIGITAL INTEGRATED CIRCUITS

Lab#1:

Physical Design and Layout of CMOS Inverter

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1. Screenshot of Layout

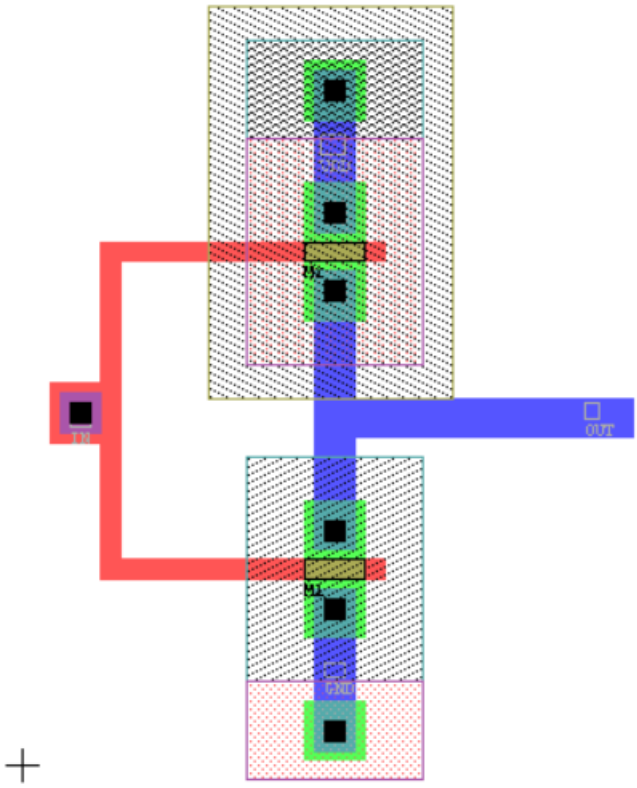

Figure 1 Screenshot of Layout

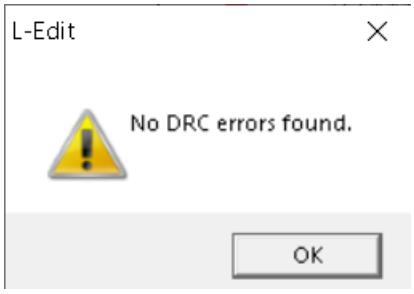

Figure 2 No DRC errors

2. Screenshot of netlist (extracted file)

```
.include "H:\tanner_1_edit\models\m15_20.md"

* Warning:  Layers with Unassigned AREA Capacitance.
*   <P Base Resistor>
*   <Poly Resistor>
*   <N Well Resistor>
*   <N Diff Resistor>
*   <Poly2 Resistor>
*   <P Diff Resistor>
* Warning:  Layers with Unassigned FRINGE Capacitance.
*   <P Base Resistor>
*   <Poly1-Poly2 Capacitor>
*   <Poly Resistor>
*   <N Well Resistor>
*   <N Diff Resistor>
*   <Poly2 Resistor>
*   <P Diff Resistor>
*   <Pad Comment>
* Warning:  Layers with Zero Resistance.
*   <Poly1-Poly2 Capacitor>
*   <NMOS Capacitor>
*   <PMOS Capacitor>
*   <Pad Comment>

* NODE NAME ALIASES


M1 GND  IN OUT GND NMOS L=2u W=6u AD=36p PD=24u AS=36p PS=24u
* M1 DRAIN GATE SOURCE BULK (29 19 35 21)
M2 OUT IN VDD VDD PMOS L=2u W=6u AD=36p PD=24u AS=36p PS=24u
* M2 DRAIN GATE SOURCE BULK (29 51.5 35 53.5)
Vin IN GND PULSE (0 5 0 1n 1n 100n 200n)
Vdd VDD GND 5
.tran/powerup 5n 500n method= bdf
.print tran v(IN) v(OUT)
* Total Nodes: 4
* Total Elements: 2
* Total Number of Shorted Elements not written to the SPICE file: 0
* Extract Elapsed Time: 0 seconds
.END
```

Figure 3 Screenshot of netlist (extracted file)

3. Screenshot of the Result from simulation

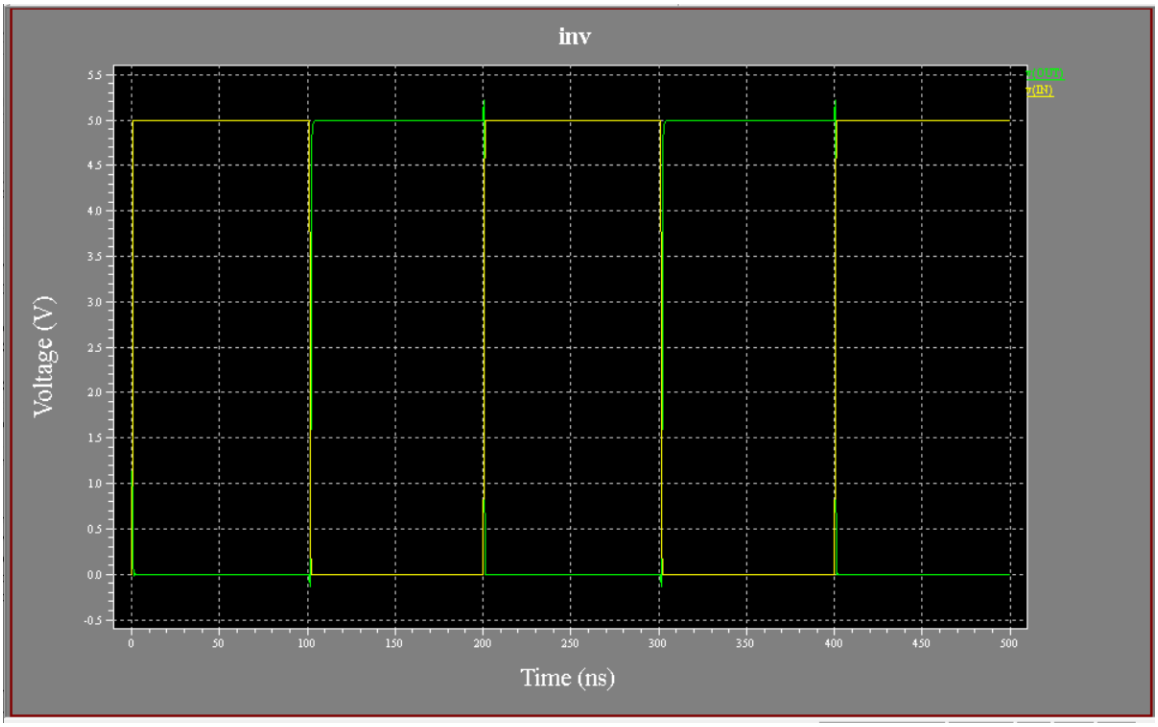

Figure 4 Screenshot of the Result from simulation