Electrical Engineering Department,

Fourth Year - Communications & Electronics.

EE 431 DIGITAL INTEGRATED CIRCUITS

Lab#2:

CMOS Inverter Characteristics

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1. Part I: Layout Versus Schematic

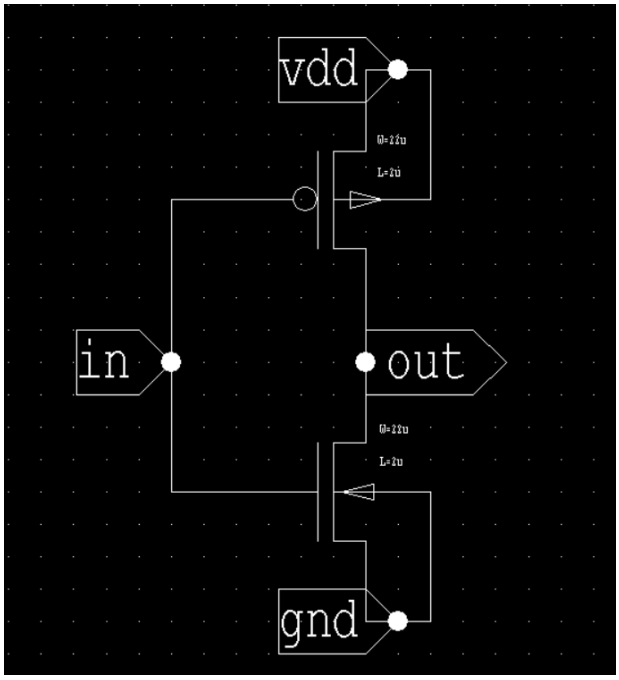

Figure 1: Screenshot of Schematic.

```
*   <Poly2 Resistor>
*   <P Diff Resistor>
*   <Pad Comment>
* Warning:  Layers with Zero Resistance.
*   <Poly1-Poly2 Capacitor>
*   <NMOS Capacitor>
*   <PMOS Capacitor>
*   <Pad Comment>

* NODE NAME ALIASES


M1 GND IN OUT GND NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* M1 DRAIN GATE SOURCE BULK (29 19 35 21)
M2 OUT IN VDD VDD PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* M2 DRAIN GATE SOURCE BULK (29 51.5 35 53.5)

* Total Nodes: 4
* Total Elements: 2
* Total Number of Shorted Elements not written to the SPICE file: 0
* Extract Elapsed Time: 0 seconds
.END
```

Figure 2: T-Spice - Layout.

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 24, 2020 at 20:18:56

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="lab2.sdb"
+ probetopmodule="lab2m"
.include ml5_20.md

* Main circuit: lab2m
M1 out in gnd gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 out in vdd vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
```

Figure 3: T-Spice – Schematic.

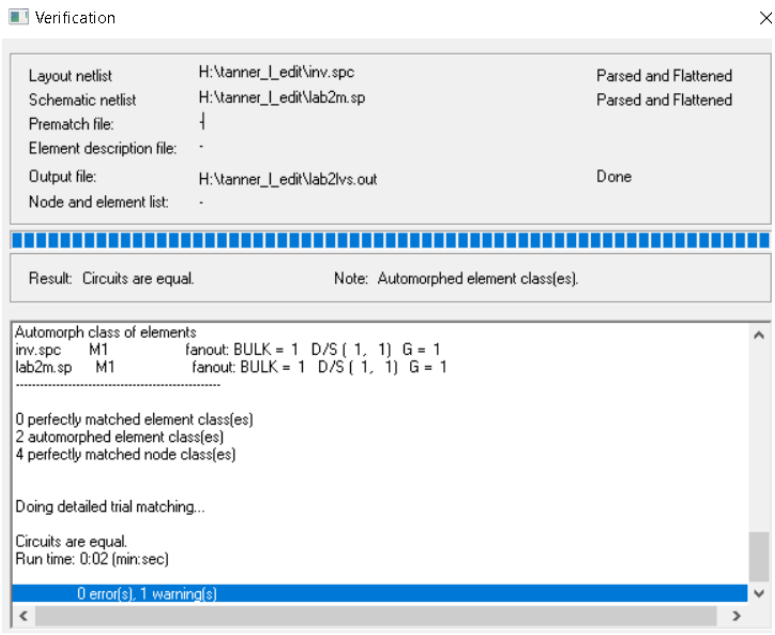

Figure 4: LVS Result "Circuits are equal".

2. Part II Inverter Characteristics

- **Transient analysis 1**

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 24, 2020 at 21:43:30

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="H:\tanner_l_edit\lab2.sdb"
+ probetopmodule="lab2m"
.include "H:\tanner_l_edit\ml5_20.md"

* Main circuit: lab2m
M1 out in gnd gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 out in vdd vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
VDC vdd gnd 5
VPULSE in gnd PULSE (0 5 0 0 0 10n 20n)
.tran/op 1n 50n method=bdf
.print tran v(in,gnd) v(out,gnd)
```

Figure 5: T-Spice – Transient analysis 1.

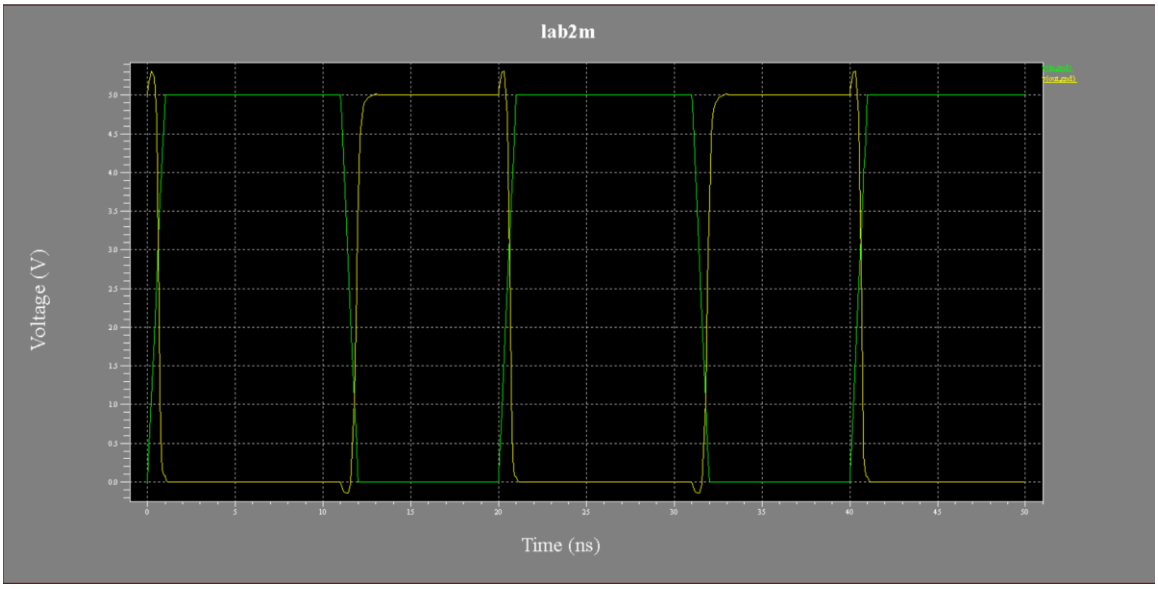

Figure 6: Result – Transient analysis 1.

- **Transient analysis 2**

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 24, 2020 at 21:43:30

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="H:\tanner_1_edit\lab2.sdb"
+ probetopmodule="lab2m"
.include "H:\tanner_1_edit\m15_20.md"

* Main circuit: lab2m
M1 out in gnd gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 out in vdd vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
VDC vdd gnd 5
VPULSE in gnd PULSE (0 5 0 0 0 10u 20u)
*.dc lin source VPULSE 0 5 0.1
*.print dc v(in,gnd) v(out,gnd)
.print tran v(in,gnd) v(out,gnd)
.tran/op 1n 50u method=bdf
```

Figure 7: T-Spice – Transient analysis 2.

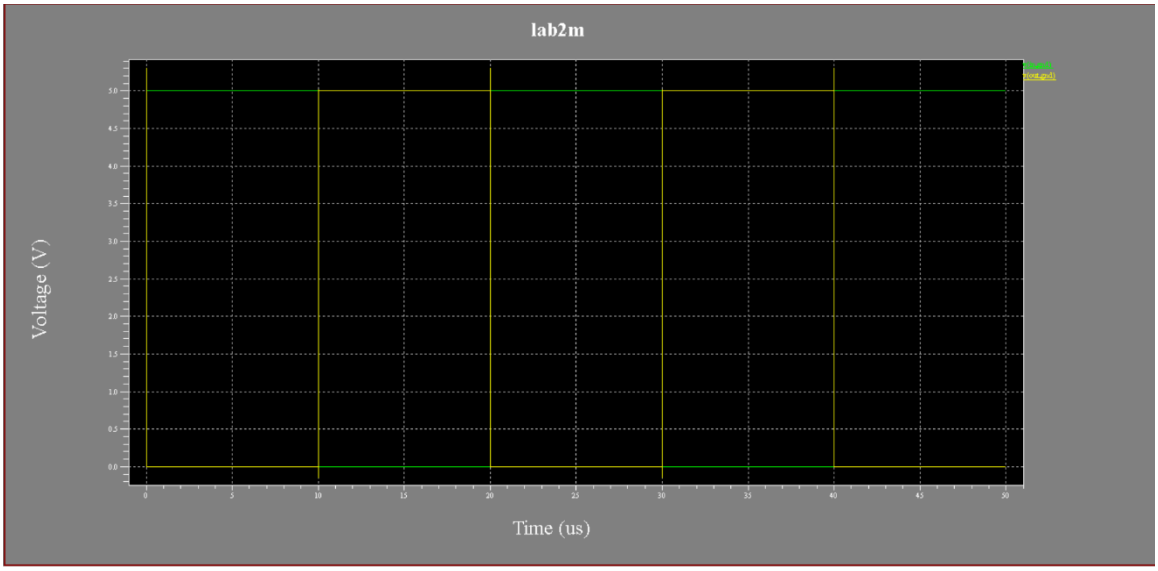

Figure 8: Result – Transient analysis 2.

- **DC sweep**

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 24, 2020 at 21:43:30

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="H:\tanner_1_edit\lab2.sdb"
+ probetopmodule="lab2m"
.include "H:\tanner_1_edit\ml5_20.md"

* Main circuit: lab2m
M1 out in gnd gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 out in vdd vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
VDC vdd gnd 5
VPULSE in gnd PULSE (0 5 0 0 0 10n 20n)
.dc lin source VPULSE 0 5 0.1
.print dc v(in,gnd) v(out,gnd)
```

Figure 9: T-Spice – DC sweep.

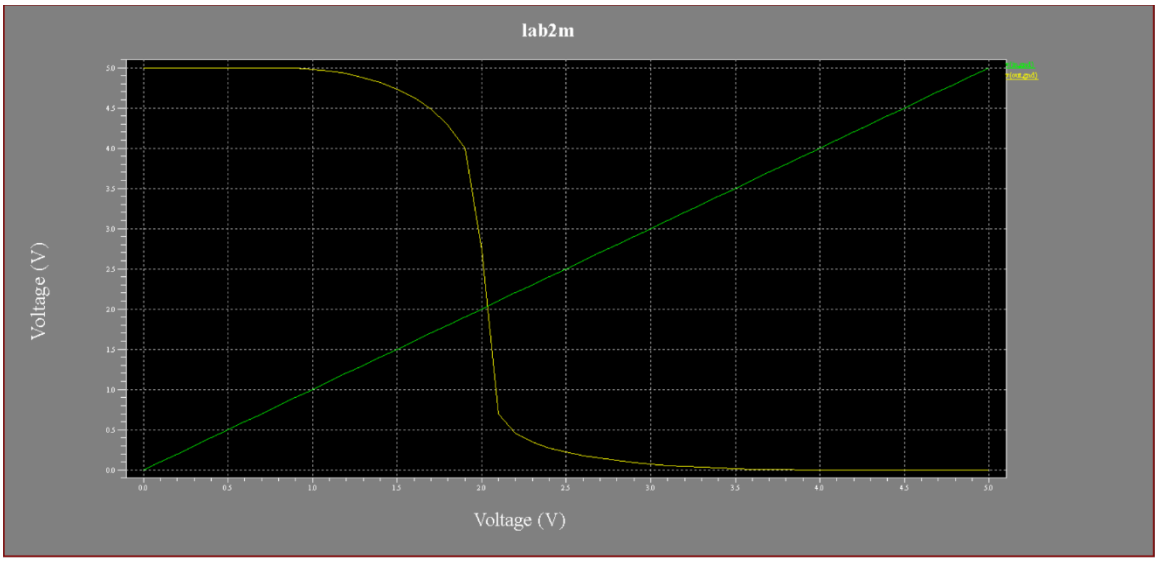

Figure 10: Result – DC sweep.

- **DC sweep (V_{th}= VDD/2) – EX1**

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 24, 2020 at 21:43:30

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="H:\tanner_1_edit\lab2.sdb"
+ probetopmodule="lab2m"
.include "H:\tanner_1_edit\m15_20.md"

* Main circuit: lab2m
M1 out in gnd gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 out in vdd vdd PMOS L=2u W=70u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
VDC vdd gnd 5
VPULSE in gnd PULSE (0 5 0 0 0 10n 20n)
.dc lin source VPULSE 0 5 0.1
.print dc v(in,gnd) v(out,gnd)
```

Figure 11: T-Spice – DC sweep (V_{th}= VDD/2) – EX1.

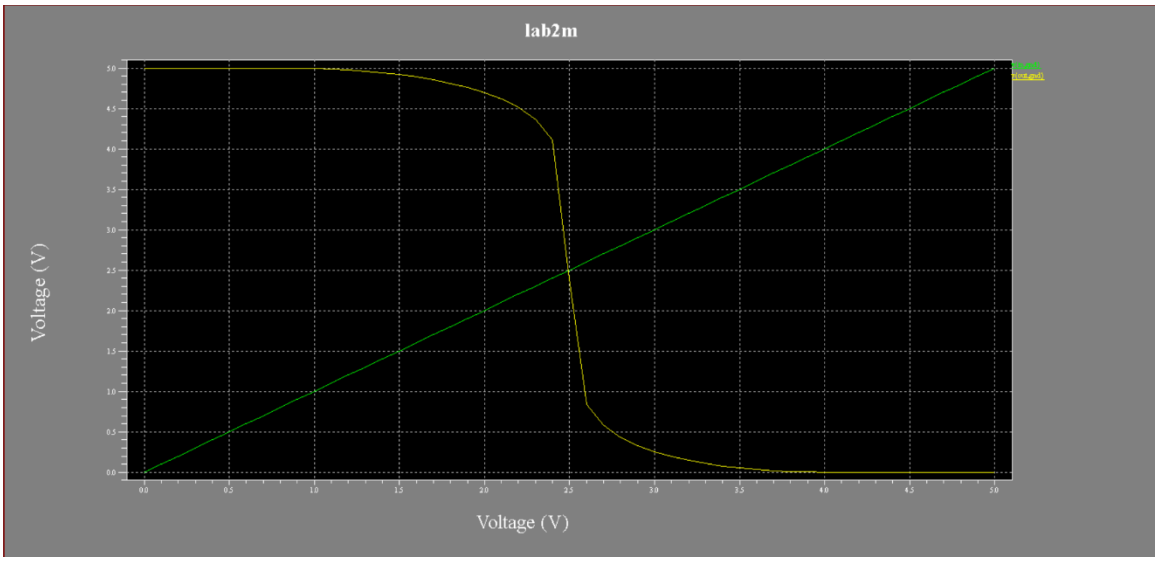

Figure 12: Result – DC sweep (V_{th}= VDD/2) – EX1.

- **DC sweep (V_{th}= VDD/2) – EX2**

T-Spice - [lab2m.sp]

File Edit View Simulation Table Options Window Help

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Jan 7, 2021 at 13:37:09
.include "H:\tanner_1_edit\m15_20.md"

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="H:\tanner_1_edit\lab2.sdb"
+ probetopmodule="lab2m"

* Main circuit: lab2m
M1 out in gnd gnd NMOS L=7u W=22u AD=66p PD=24u AS=66p PS=24u
M2 out in vdd vdd PMOS L=2u W=20u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
VDC vdd gnd 5
VPULSE in gnd PULSE (0 5 0 0 0 10n 20n)
.dc lin source VPULSE 0 5 0.1
.print dc v(in,gnd) v(out,gnd)
```

Figure 13: T-Spice – DC sweep (V_{th}= VDD/2) – EX2.

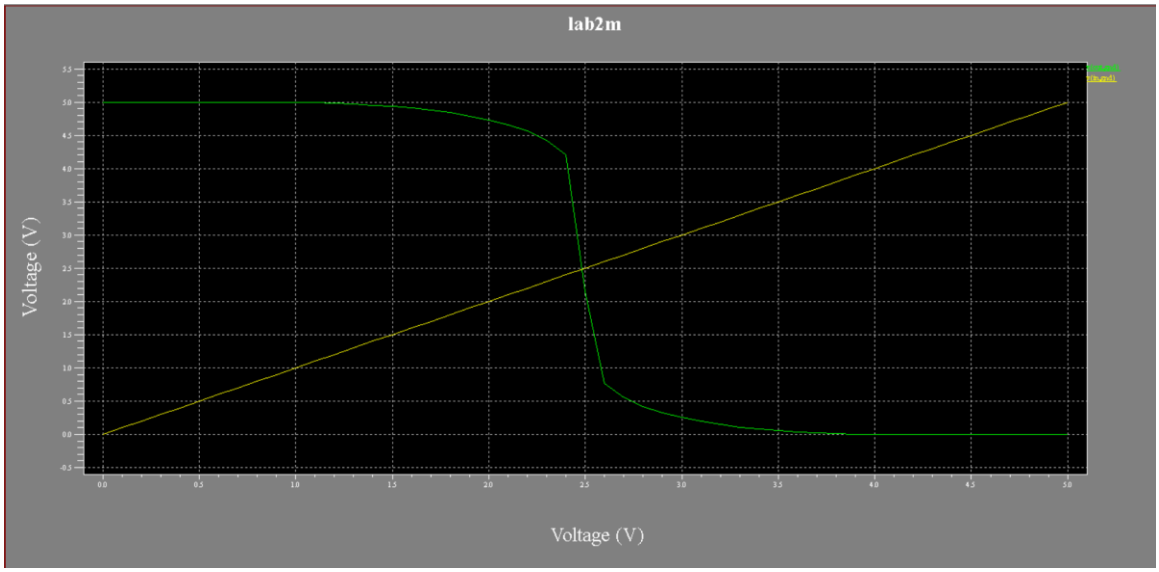

Figure 14: Result – DC sweep (V_{th}= VDD/2) – EX2.

- **Transient analysis (increase the input frequency VDD = 3 volt)**

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 24, 2020 at 21:43:30

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="H:\tanner_1_edit\lab2.sdb"
+ probetopmodule="lab2m"
.include "H:\tanner_1_edit\ml5_20.md"

* Main circuit: lab2m
M1 out in gnd gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 out in vdd vdd PMOS L=2u W=70u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
VDC vdd gnd 3
VPULSE in gnd PULSE (0 3 0 0 0 0.5n 1n)
*.dc lin source VPULSE 0 5 0.1
*.print dc v(in,gnd) v(out,gnd)
.print tran v(in,gnd) v(out,gnd)
.tran/op 1p 5n method=bdf
```

Figure 15: T-Spice – Transient analysis (increase the input frequency VDD = 3 volt).

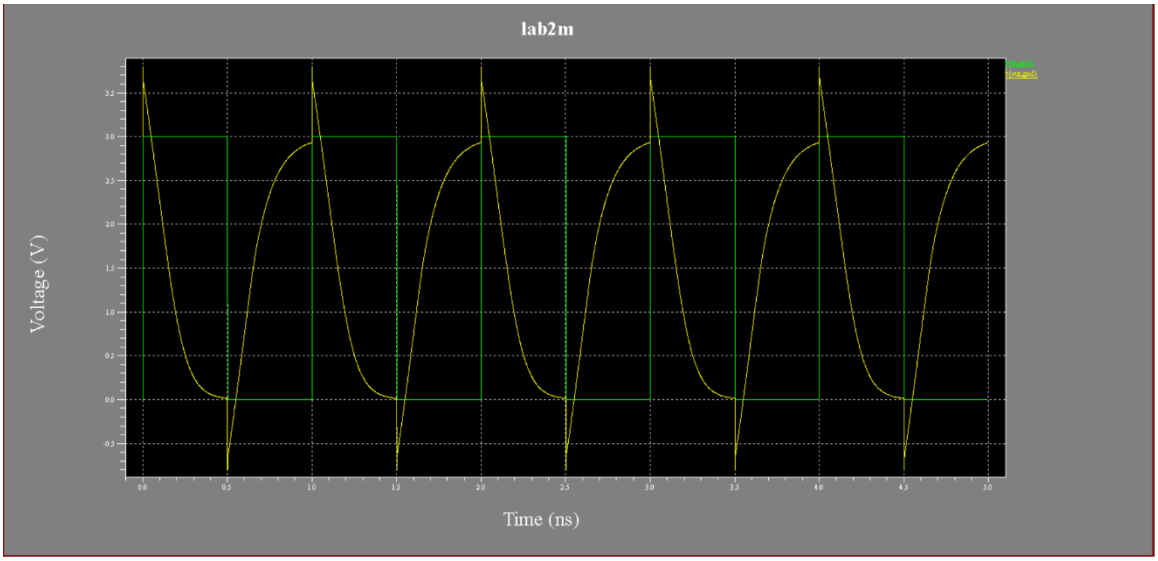

Figure 16: Result – Transient analysis (increase the input frequency VDD = 3 volt).

- **Transient analysis (increase the input frequency VDD = 5 volt)**

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 24, 2020 at 21:43:30

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="H:\tanner_1_edit\lab2.sdb"
+ probetopmodule="lab2m"
.include "H:\tanner_1_edit\ml5_20.md"

* Main circuit: lab2m
M1 out in gnd gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 out in vdd vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
VDC vdd gnd 5
VPULSE in gnd PULSE (0 5 0 0 0 0.5n 1n)
*.dc lin source VPULSE 0 5 0.1
*.print dc v(in,gnd) v(out,gnd)
.print tran v(in,gnd) v(out,gnd)
.tran/op 1p 5n method=bdf
```

Figure 17: T-Spice – Transient analysis (increase the input frequency VDD = 5 volt).

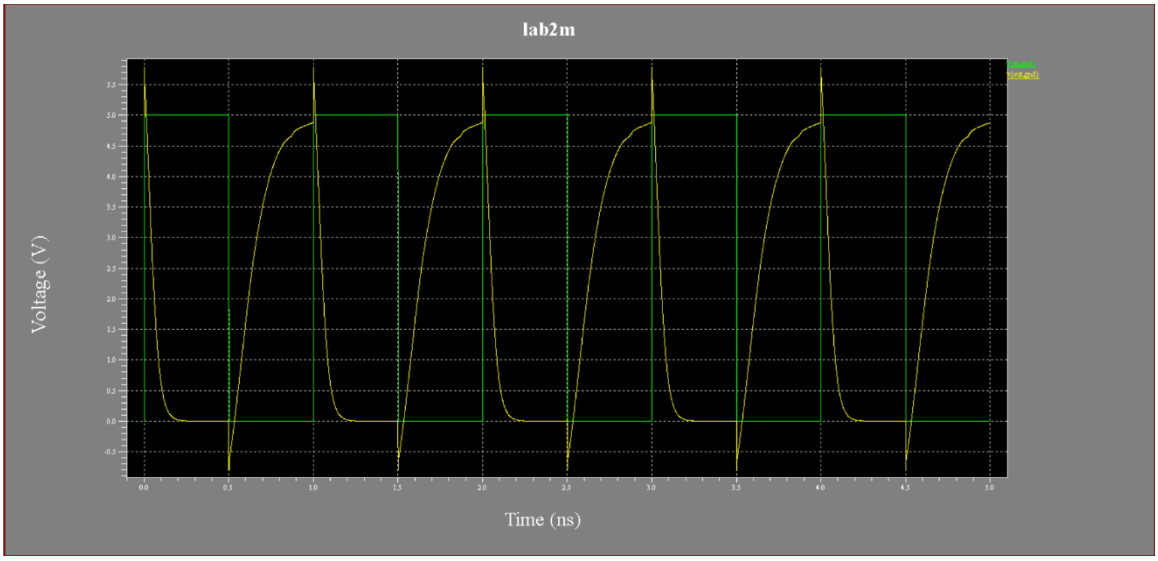

Figure 18: Result – Transient analysis (increase the input frequency VDD = 5 volt).

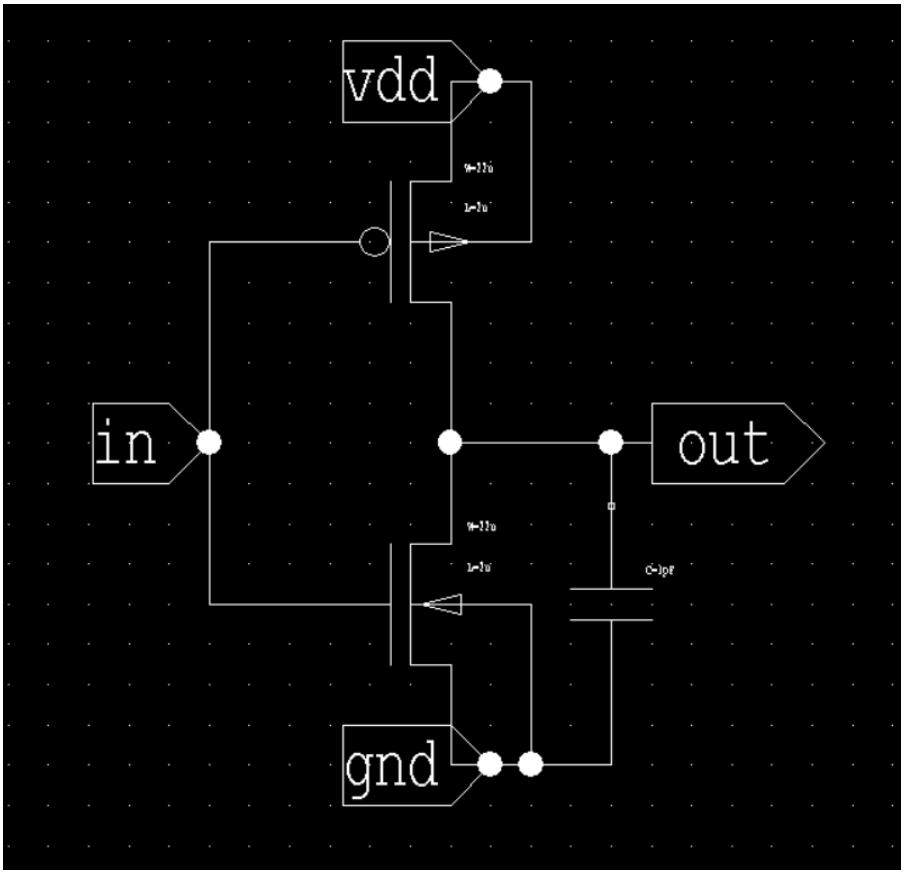

Figure 19: Screenshot of Schematic (Add a load capacitance of 1pF).

- **Measure τPHL and τPLH.**

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 26, 2020 at 03:04:25

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="H:\tanner_1_edit\lab2.sdb"
+ probetopmodule="lab2m"
.include "H:\tanner_1_edit\ml5_20.md"

* Main circuit: lab2m
C1 out gnd 1pF
M2 out in gnd gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M3 out in vdd vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
VDC vdd gnd 5
VPULSE in gnd PULSE (0 5 0 0 0 10n 20n)
.tran/op 1p 50n method=bdf
.print tran v(in,gnd) v(out,gnd)
```

Figure 20: T-Spice – Transient analysis (Measure τPHL and τPLH).

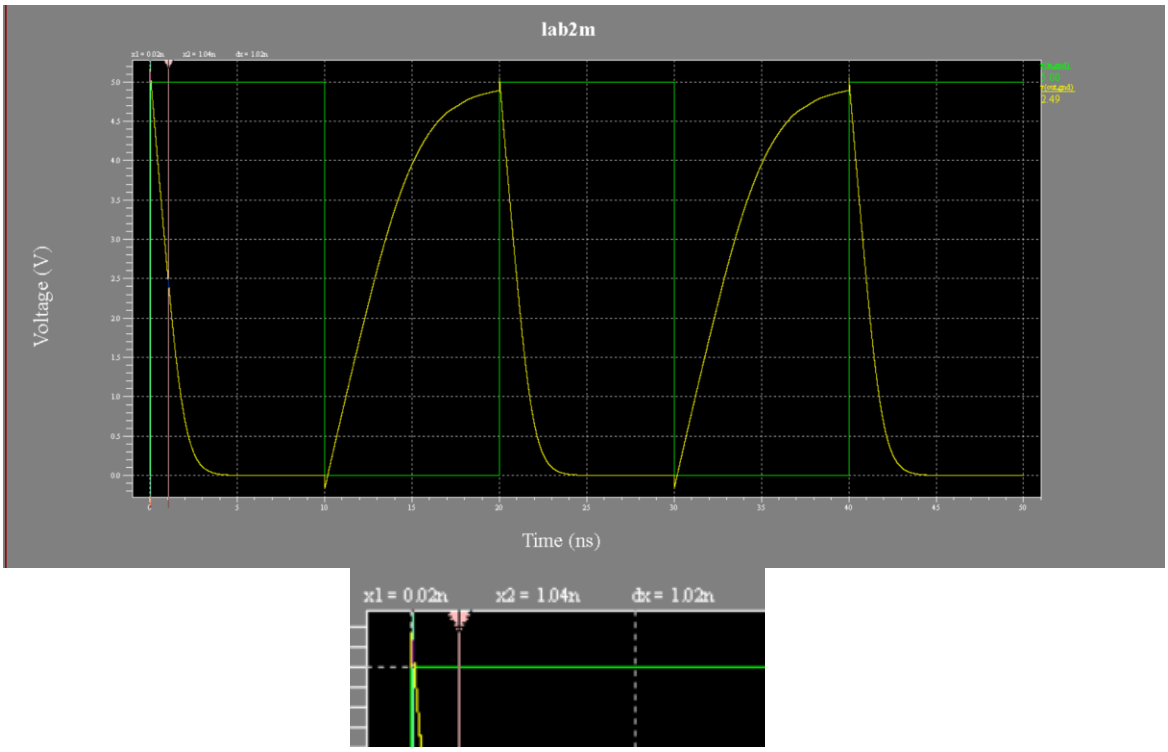

Figure 21: Result – τPHL = 1.02 nsec.

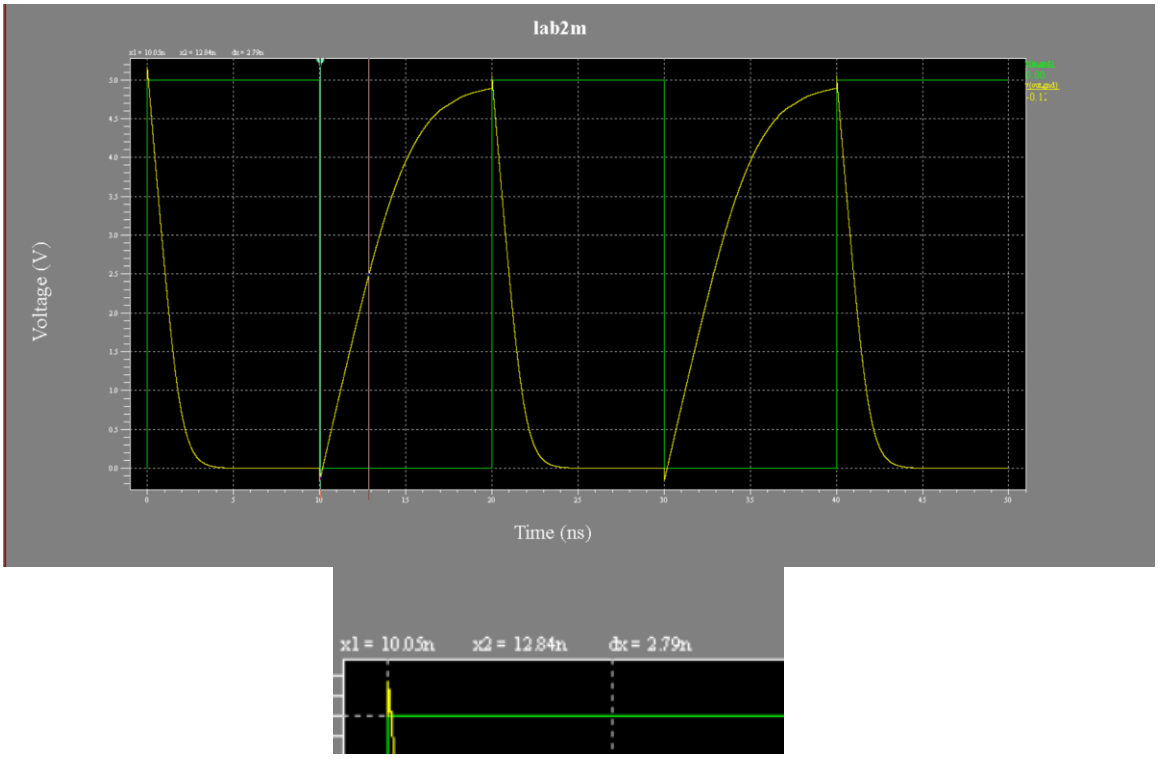

Figure 22: Result – τPLH = 2.79 nsec.

- **Resize the transistor so that τPHL and τPLH are equal**

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 26, 2020 at 03:04:25

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="H:\tanner_1_edit\lab2.sdb"
+ probetopmodule="lab2m"
.include "H:\tanner_1_edit\m15_20.md"

* Main circuit: lab2m
C1 out gnd 1pF
M2 out in gnd gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M3 out in vdd vdd PMOS L=2u W=70u AD=66p PD=24u AS=66p PS=24u
* End of main circuit: lab2m
VDC vdd gnd 5
VPULSE in gnd PULSE (0 5 0 0 0 10n 20n)
.tran/op 1p 50n method=bdf
.print tran v(in,gnd) v(out,gnd)
```

Figure 23: T-Spice – Transient analysis (Resize the transistor so that τPHL and τPLH are equal).

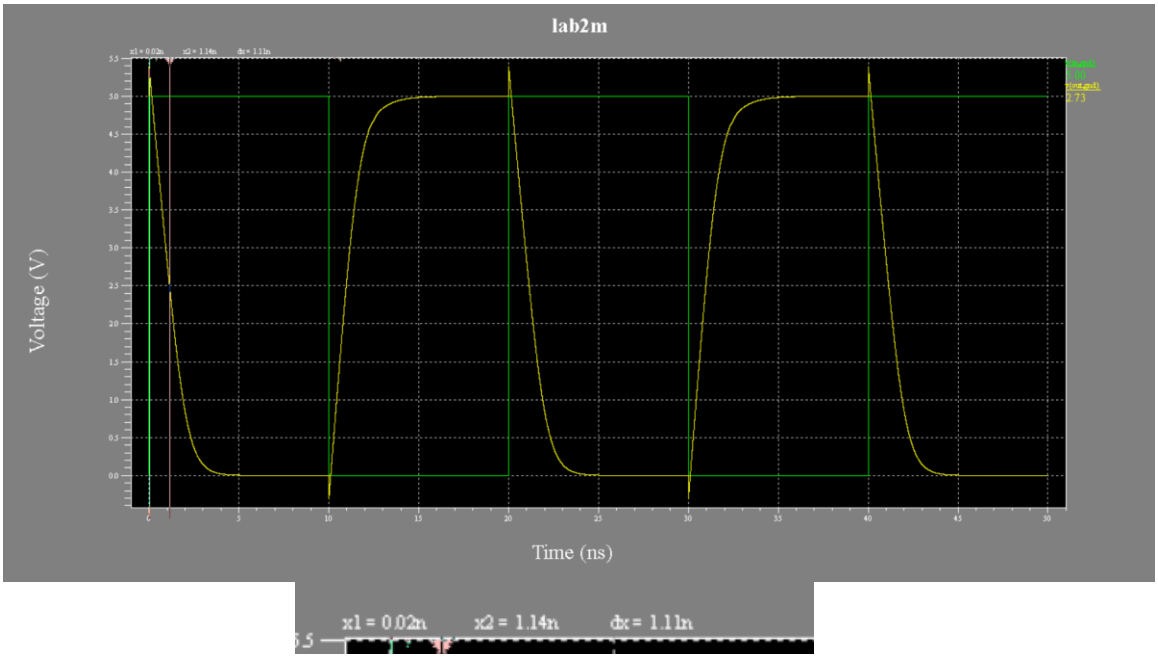

Figure 24: Result – τPHL = 1.11 nsec.

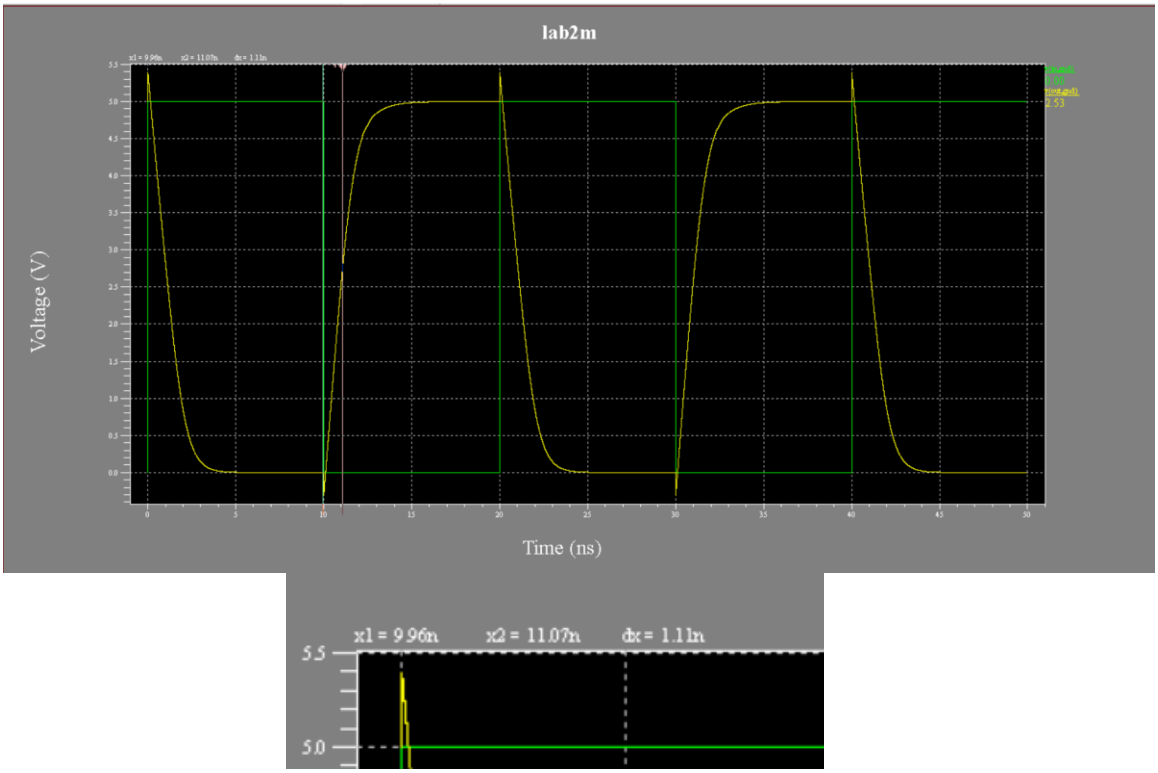

Figure 25: Result – τPLH = 1.11 nsec.