Alexandria University

Faculty of engineering

Communication department

VLSI #9

Supervised by Prof. M. EL-Banna ,prof. M. Rizk and Eng. Fouad M. Ismail

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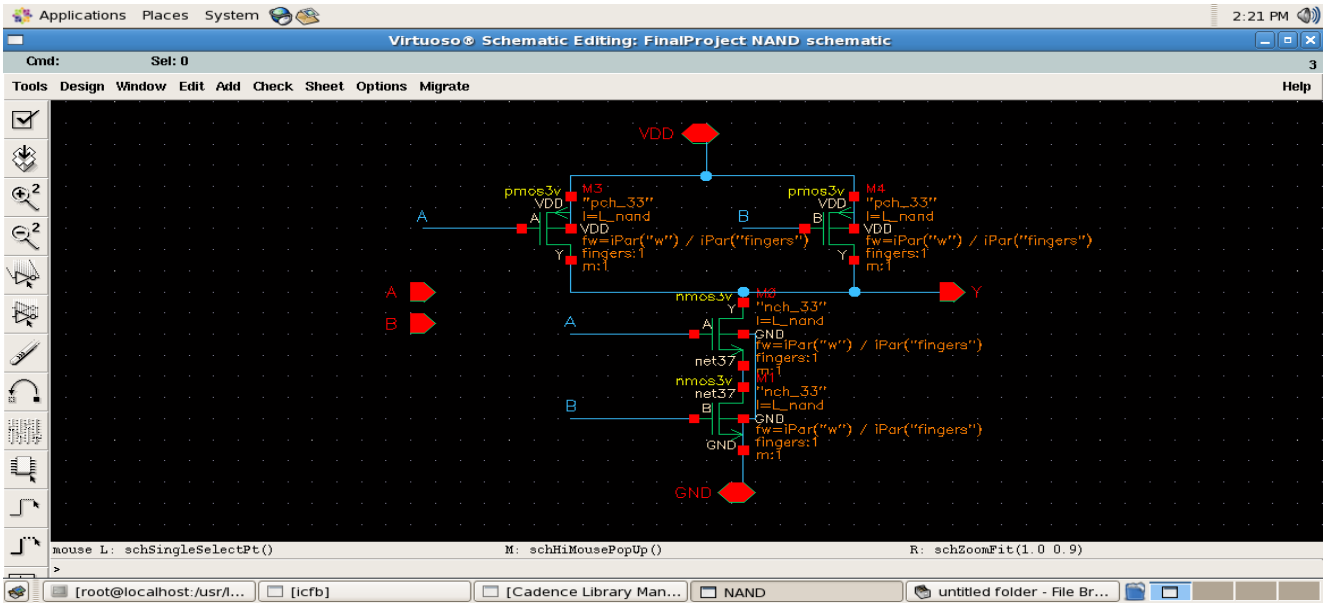
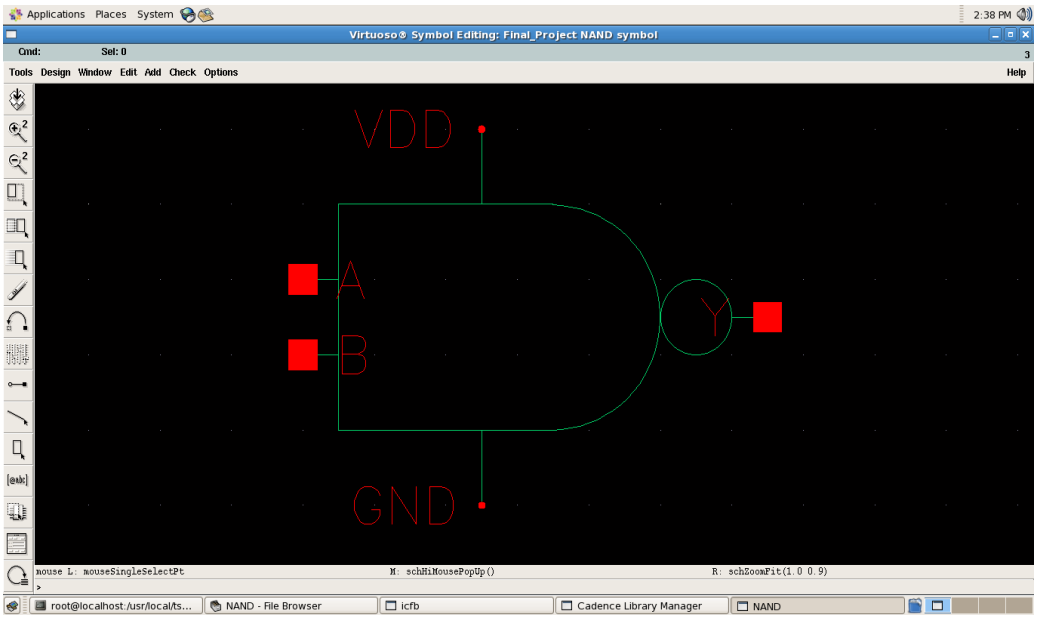
First phase: NAND and NOR cells

NAND:

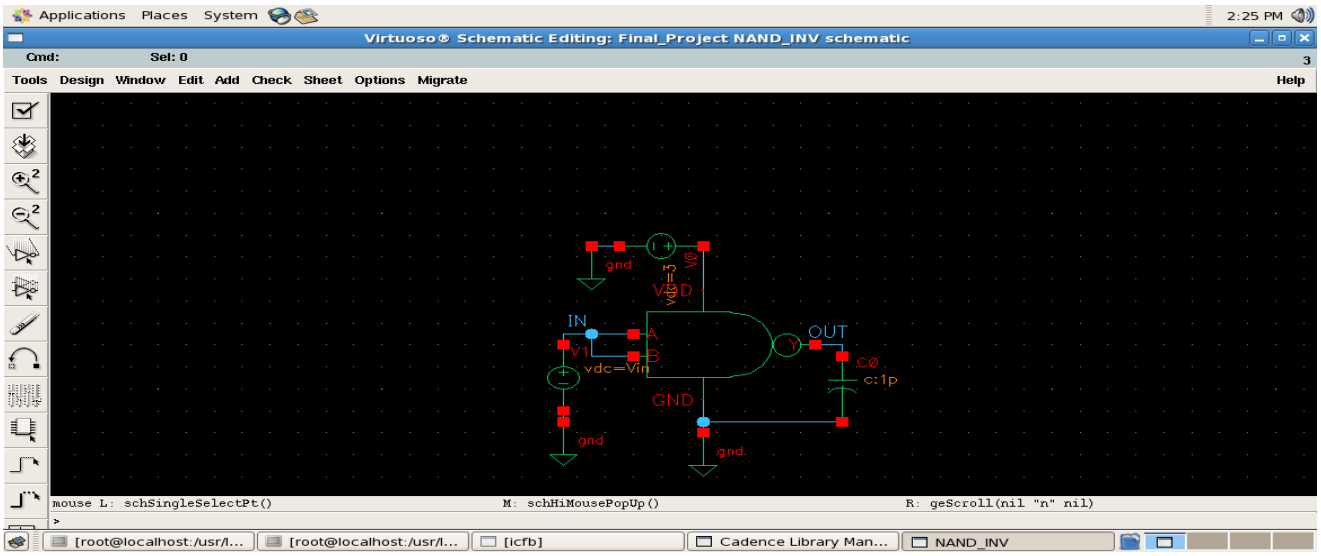
Schematic: Y=A.B

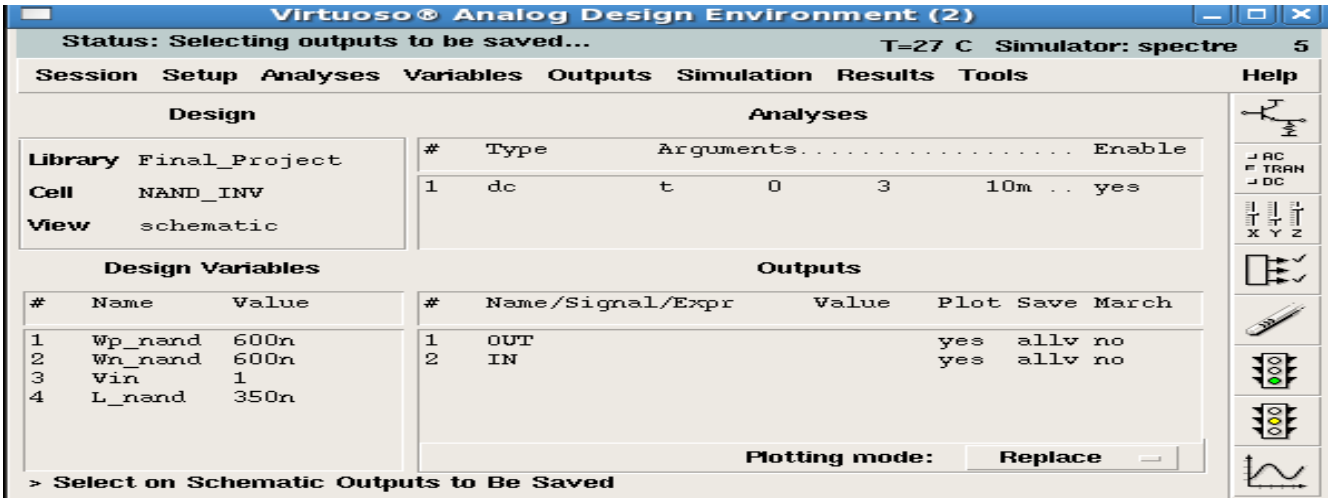


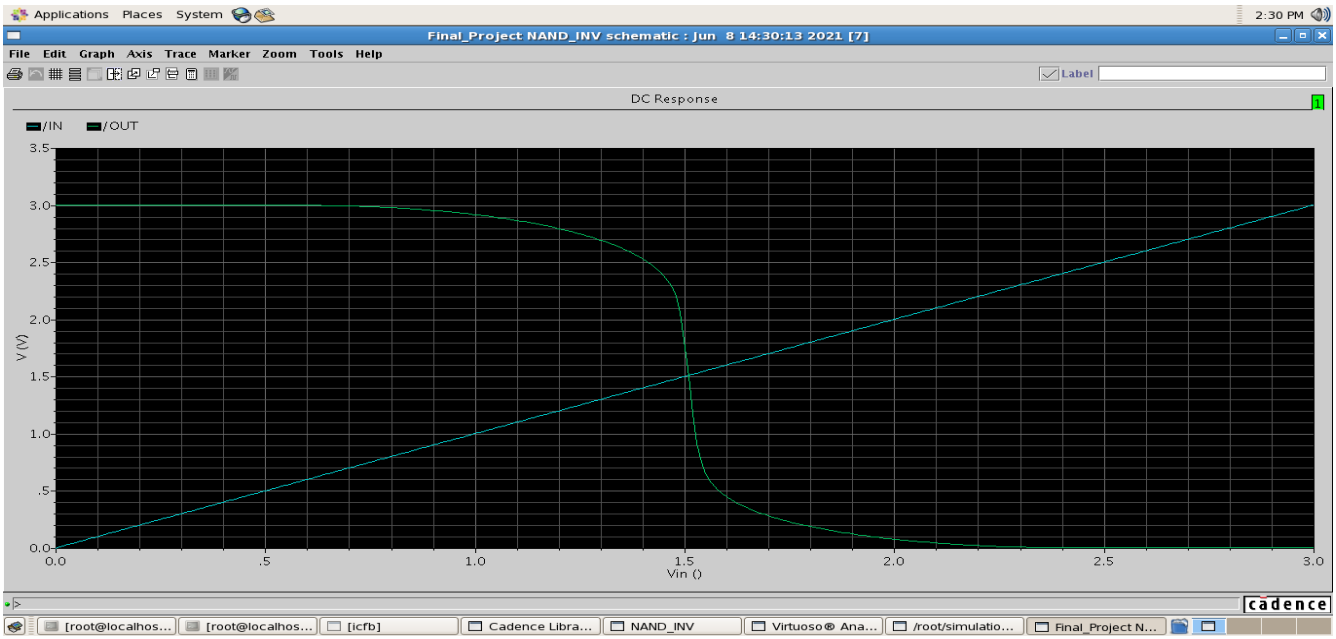
Symbol:



For Wp_Nand=Wp_Nand=600n & L_Nand=350n

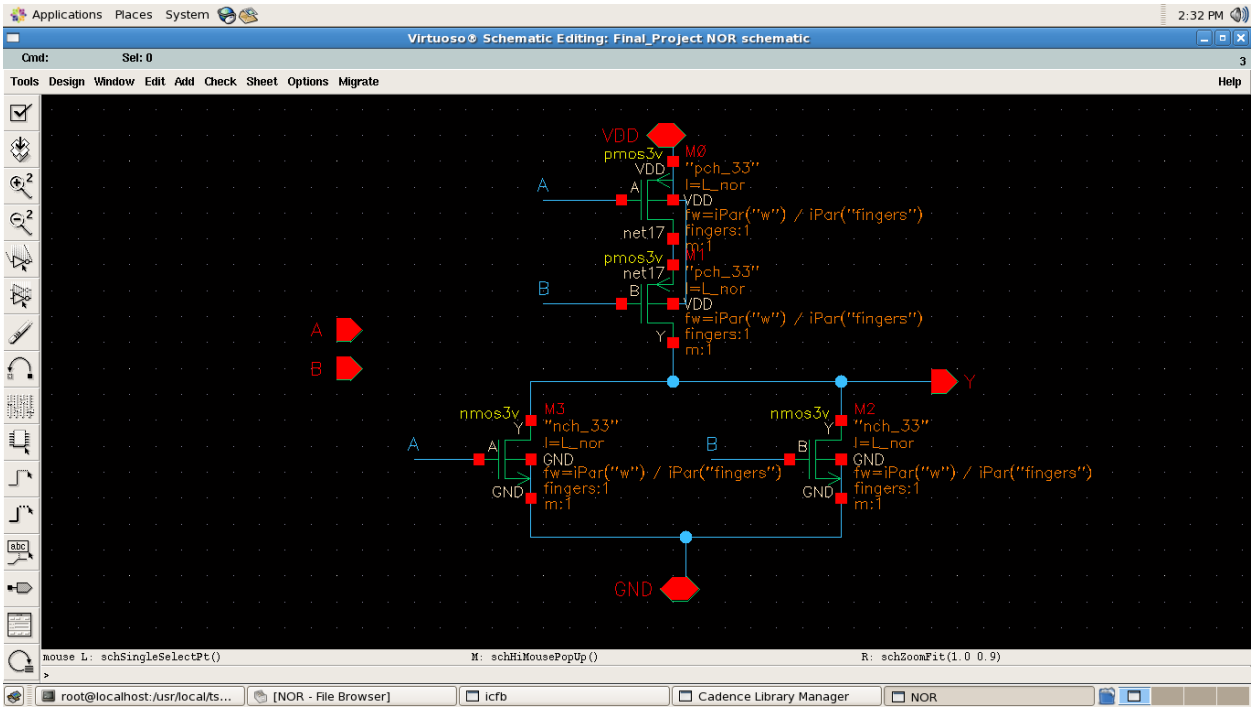

Applications Places System
2:25 PM
Virtuoso® Schematic Editing: Final_Project NAND_INV schematic
Cmd:
Sel: 0
Tools Design Window Edit Add Check Sheet Options Migrate
Help
gnd
VSRC
VDD
IN
V1
vdc=Vin
A
B
OUT
C0
c:1p
GND
gnd
gnd
mouse L: schSingleSelectPt()
M: schHiMousePopUp()
R: geScroll(nil "n" nil)
[root@localhost:/usr/l...
[root@localhost:/usr/l...
[icfb]
Cadence Library Man...
NAND_INV


Virtuoso® Analog Design Environment (2)
Status: Selecting outputs to be saved...
T=27 C Simulator: spectre 5
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Library Final_Project
Cell NAND_INV
View schematic
Analyses
Type Arguments Enable
1 dc t 0 3 10m yes
Design Variables
Name Value
1 Wp_nand 600n
2 Wn_nand 600n
3 Vin 1
4 L_nand 350n
Outputs
Name/Signal/Expr Value Plot Save March
1 OUT yes allv no
2 IN yes allv no
Plotting mode: Replace
> Select on Schematic Outputs to Be Saved

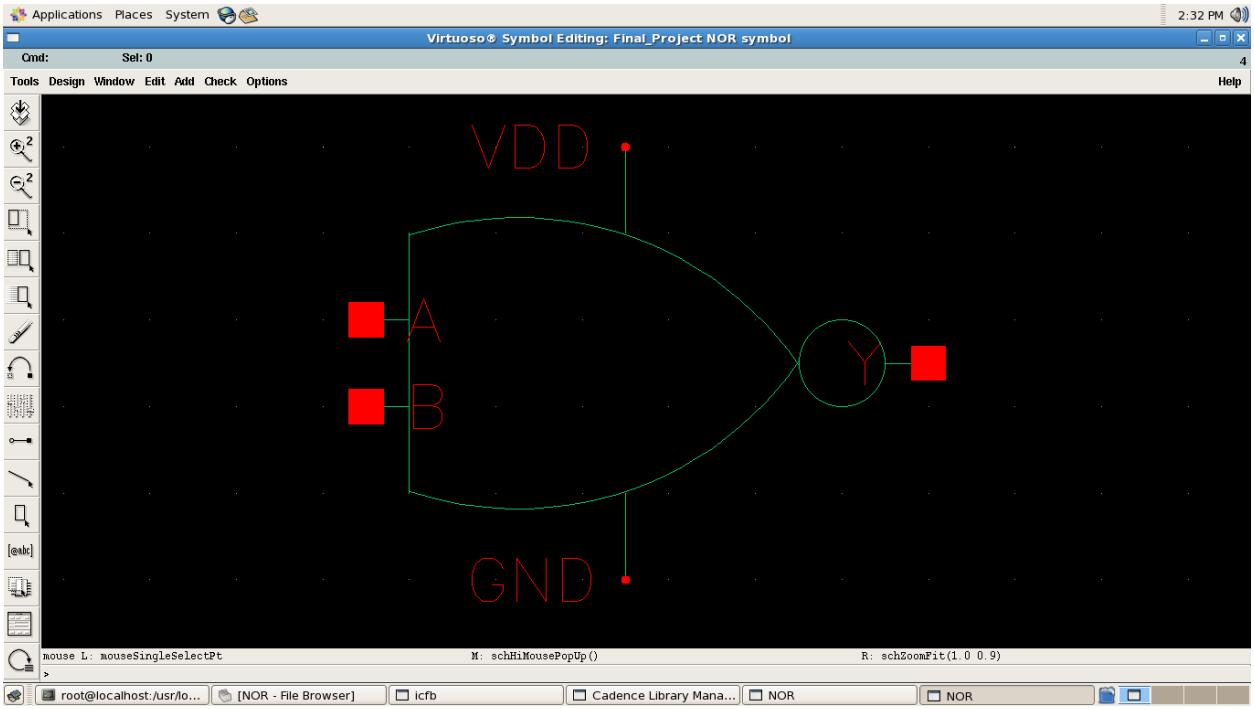

Applications Places System
2:30 PM
Final_Project NAND_INV schematic : Jun 8 14:30:13 2021 [7]
File Edit Graph Axis Trace Marker Zoom Tools Help
Label
DC Response
/IN
/OUT
3.5
3.0
2.5
2.0
1.5
1.0
.5
0.0
V (V)
0.0
.5
1.0
1.5
2.0
2.5
3.0
Vin ()
cadence
[root@localhos...
[root@localhos...
[icfb]
Cadence Libra...
NAND_INV
Virtuoso® Ana...
/root/simulatio...
Final_Project N...

NOR:

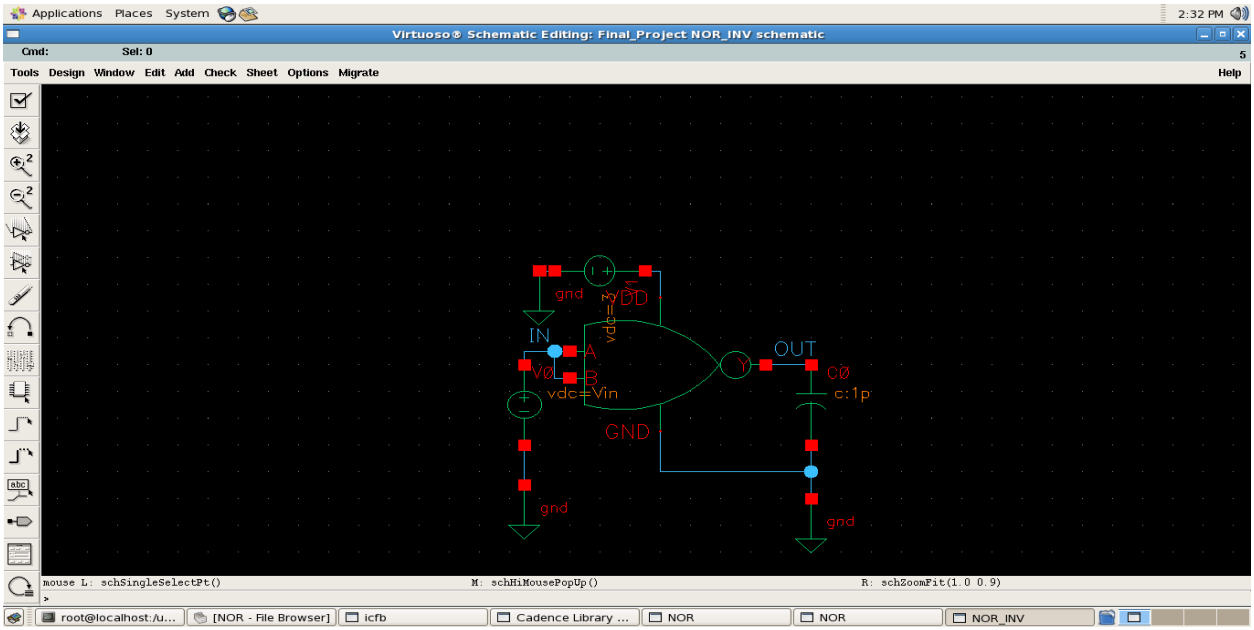
Schematic: Y=A+B

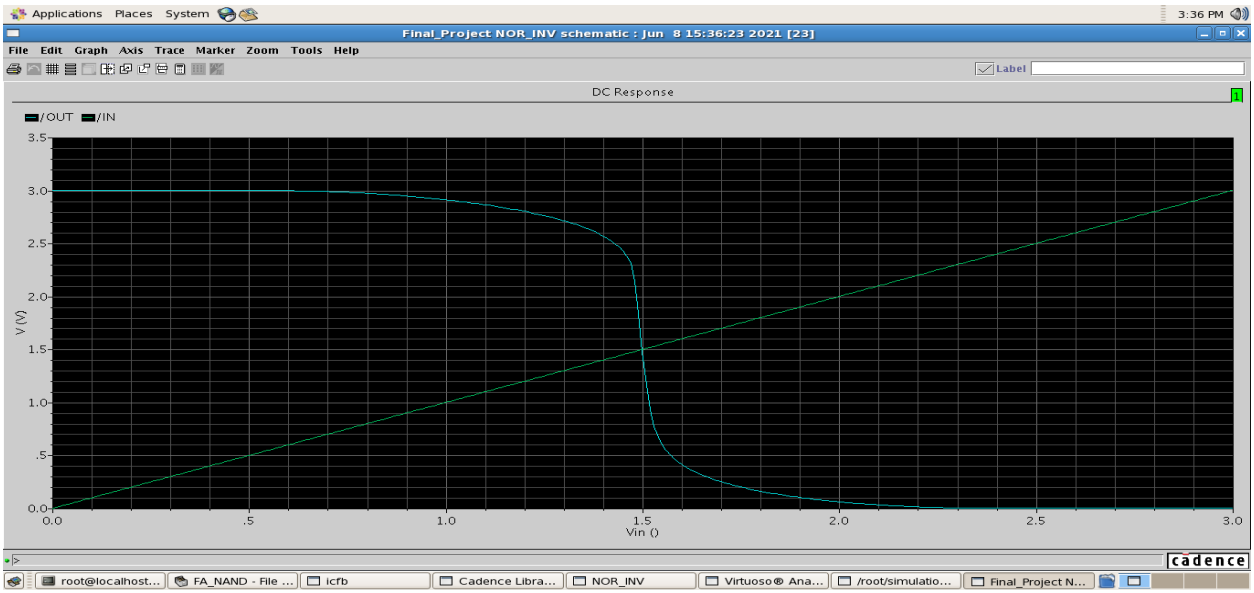


Symbol:



For Wp_Nor=7.5u ,Wp_Nor=600n & L_Nor=350n

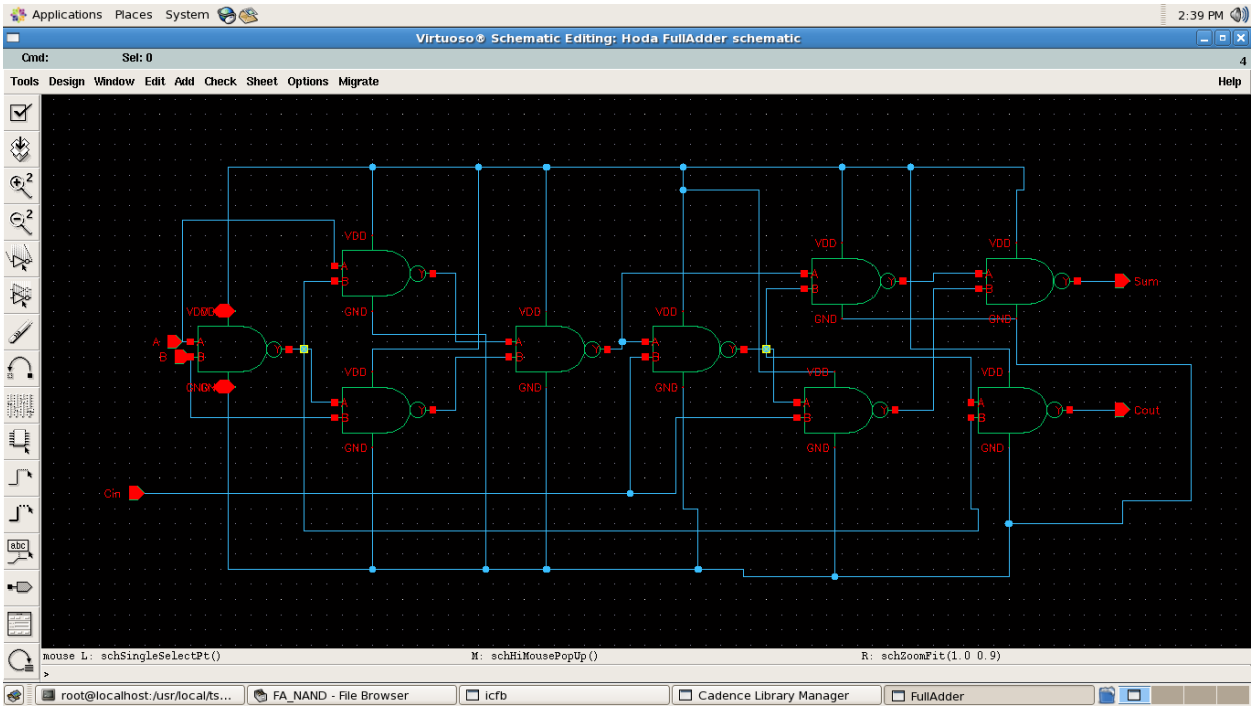




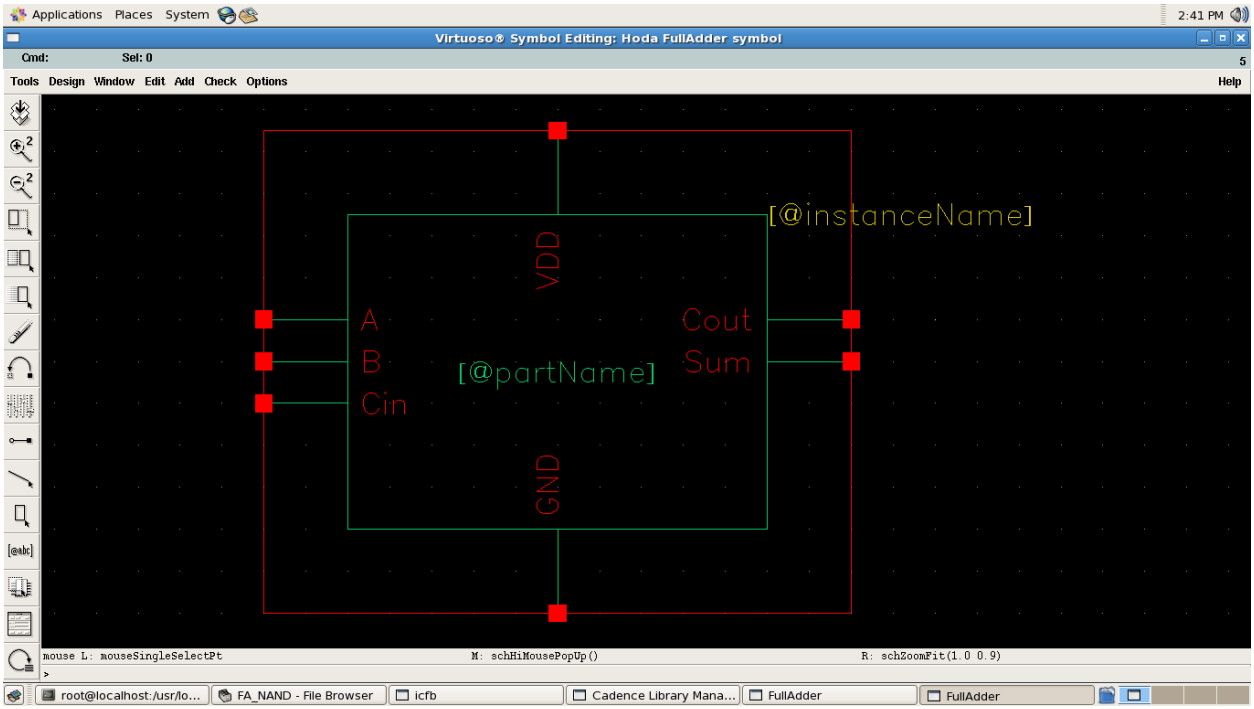
Second phase: the large circuit

Full Adder using NAND

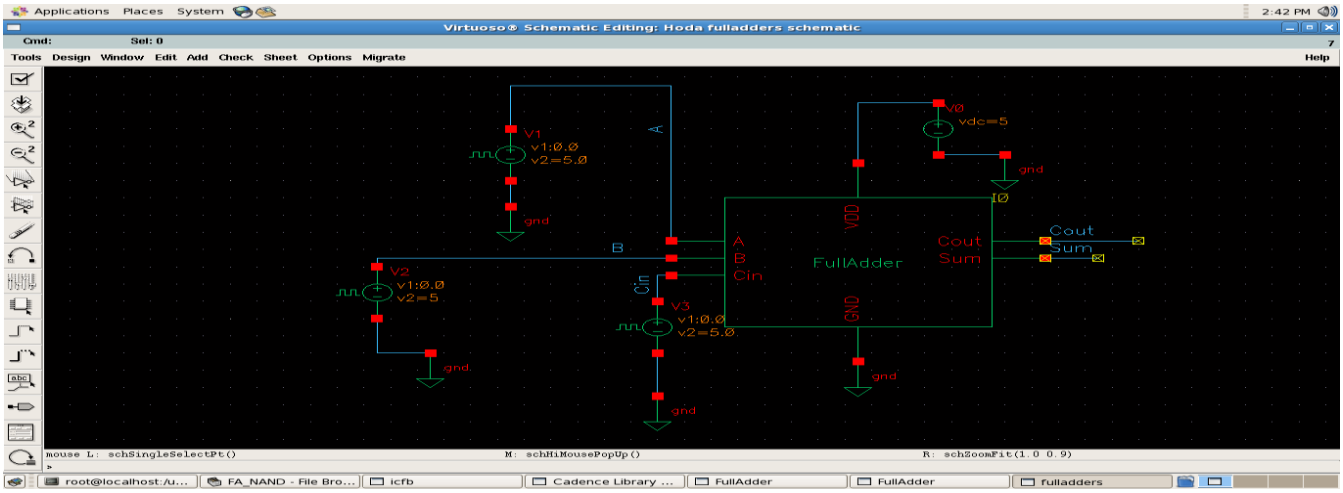
Schematic:

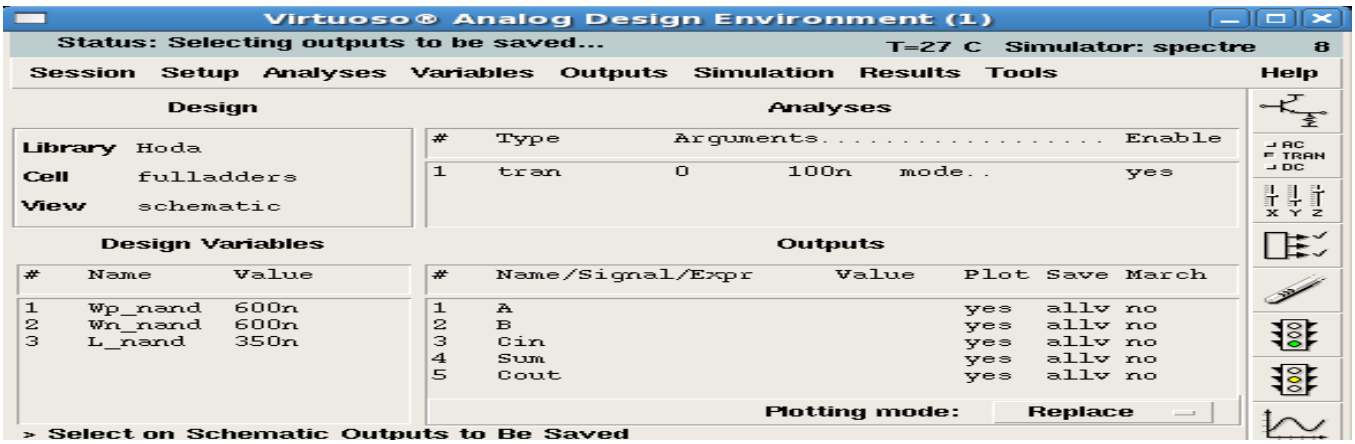


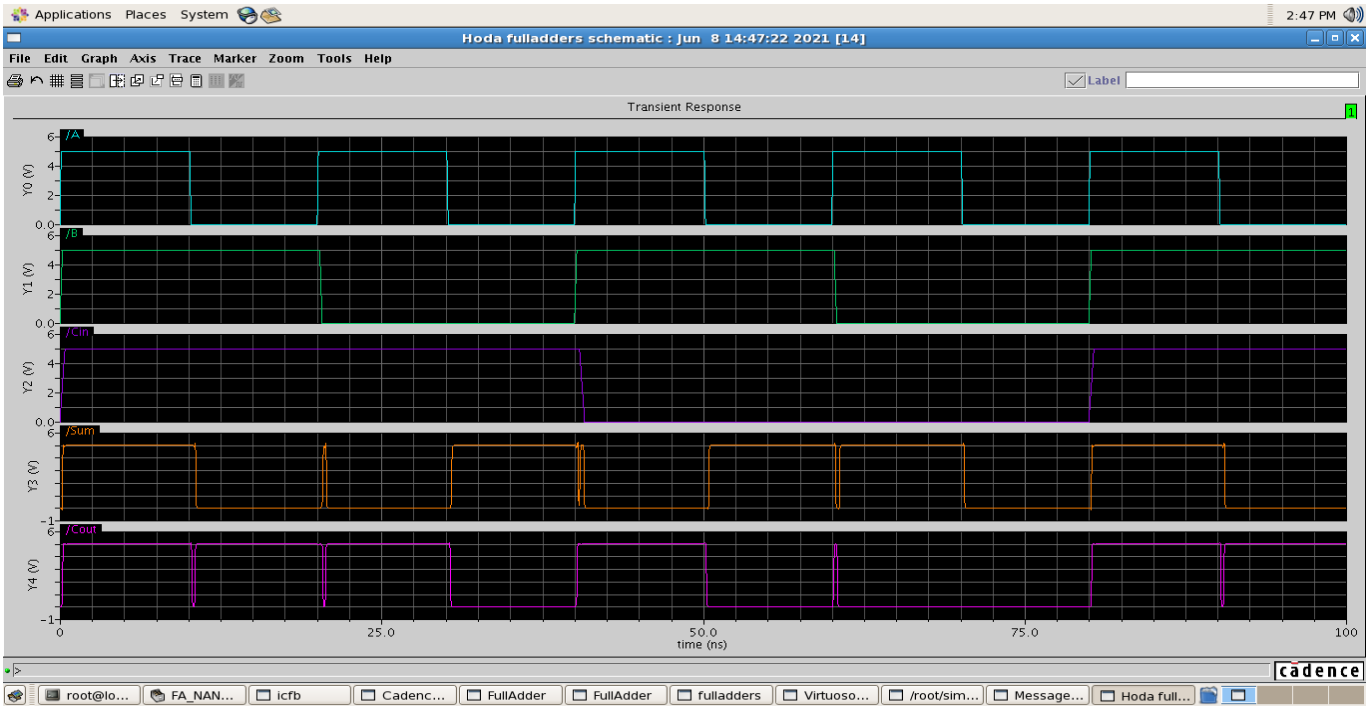
Symbol:



Full Adder operation:

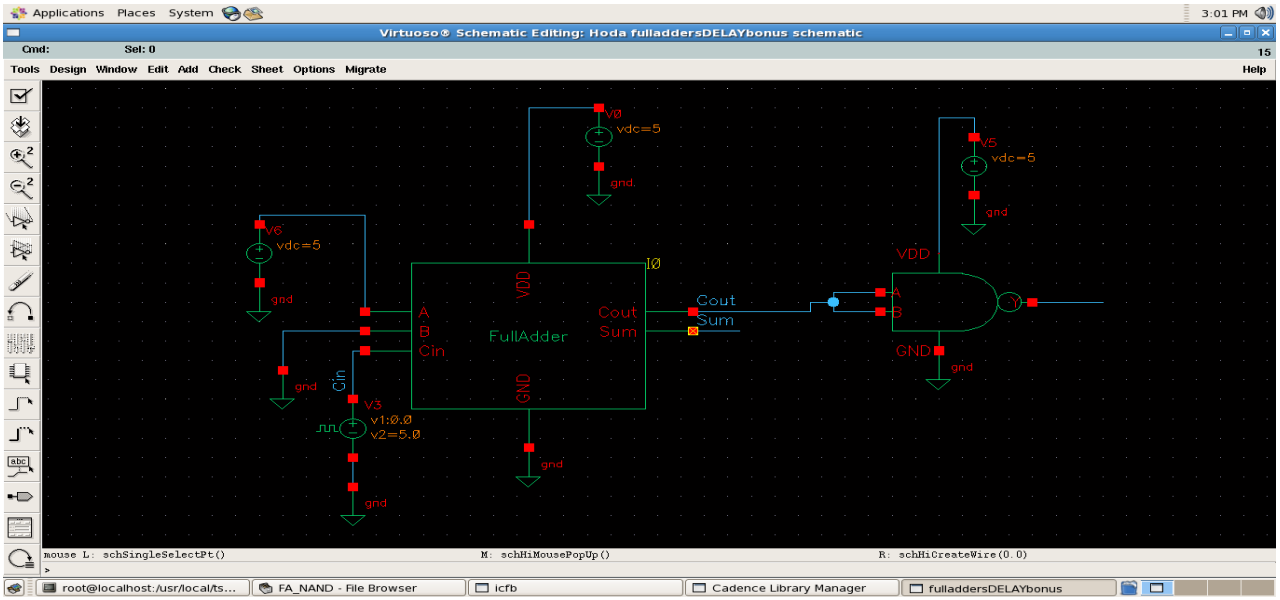


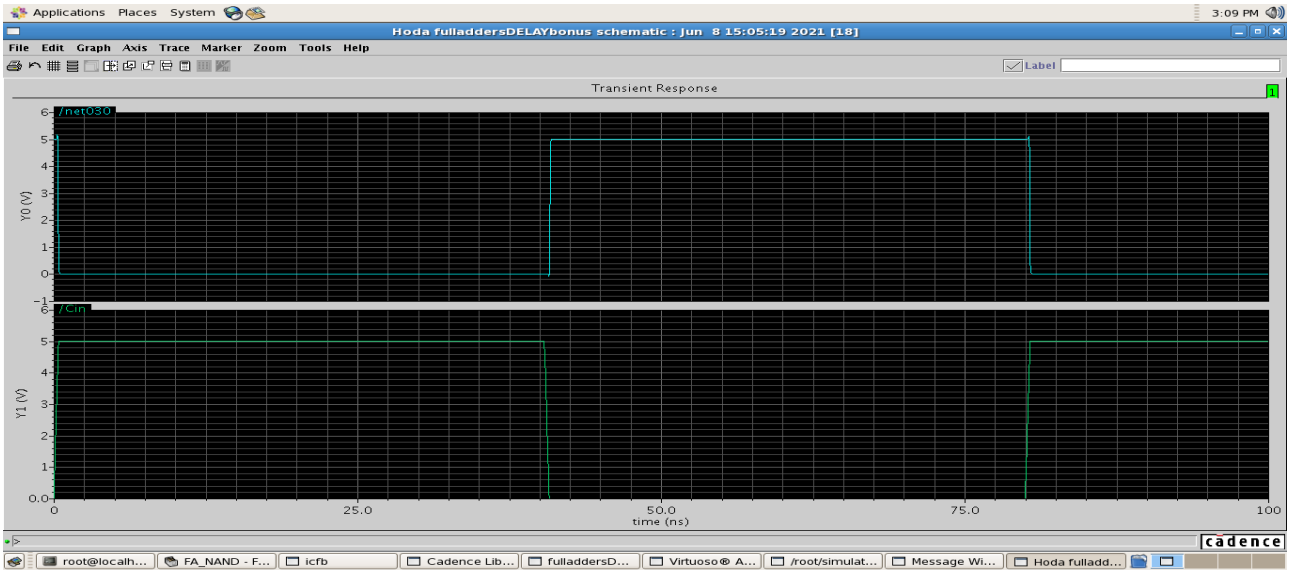


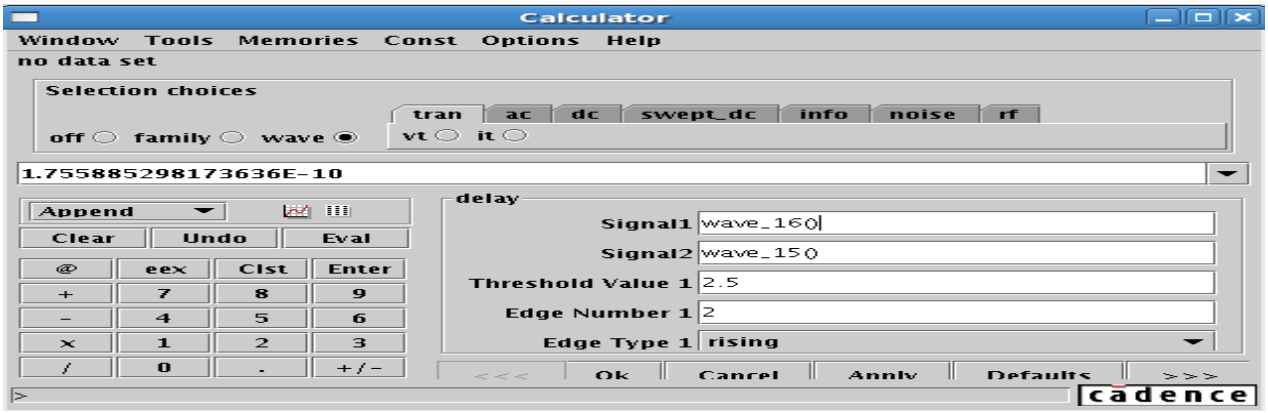


Calculating delay:

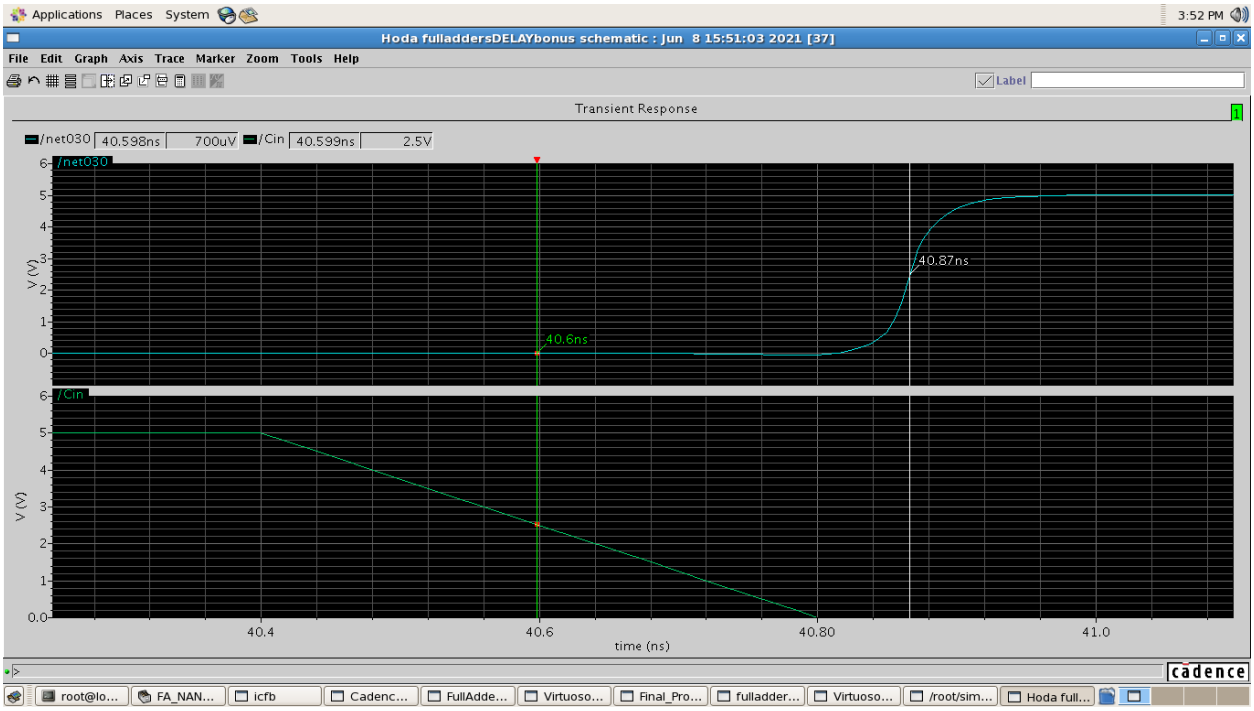
Schematic:







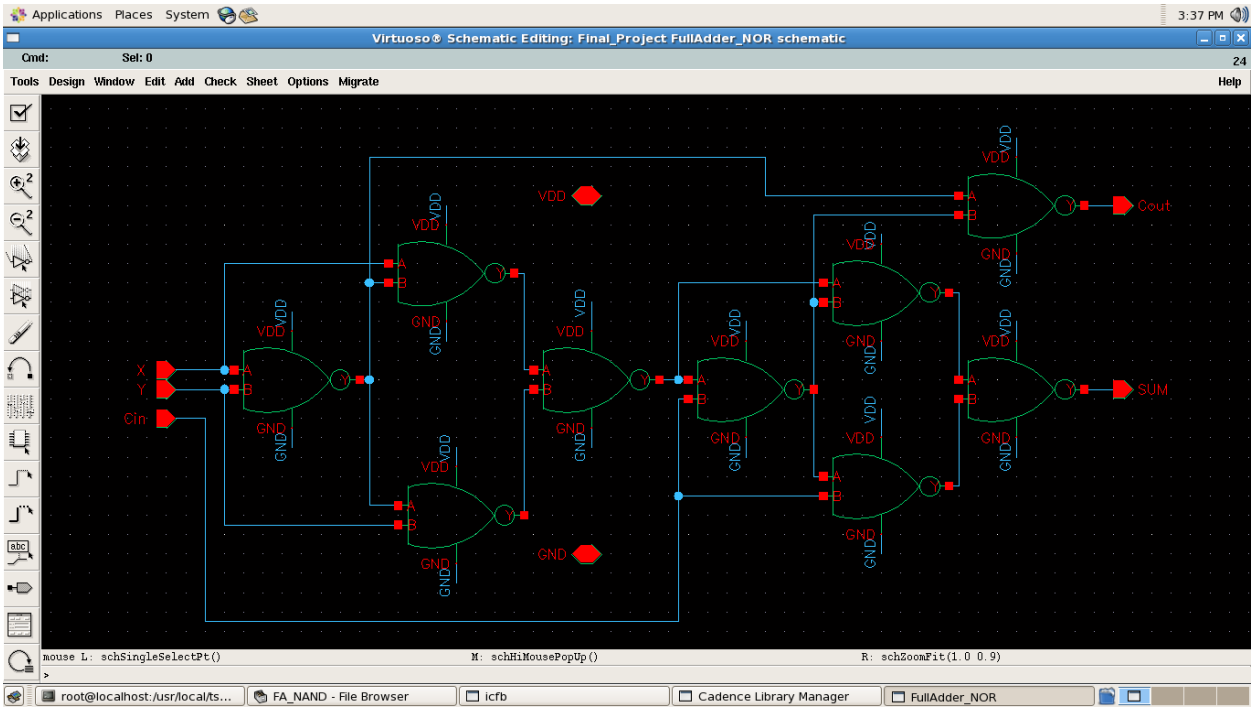
Delay = 0.1756ns



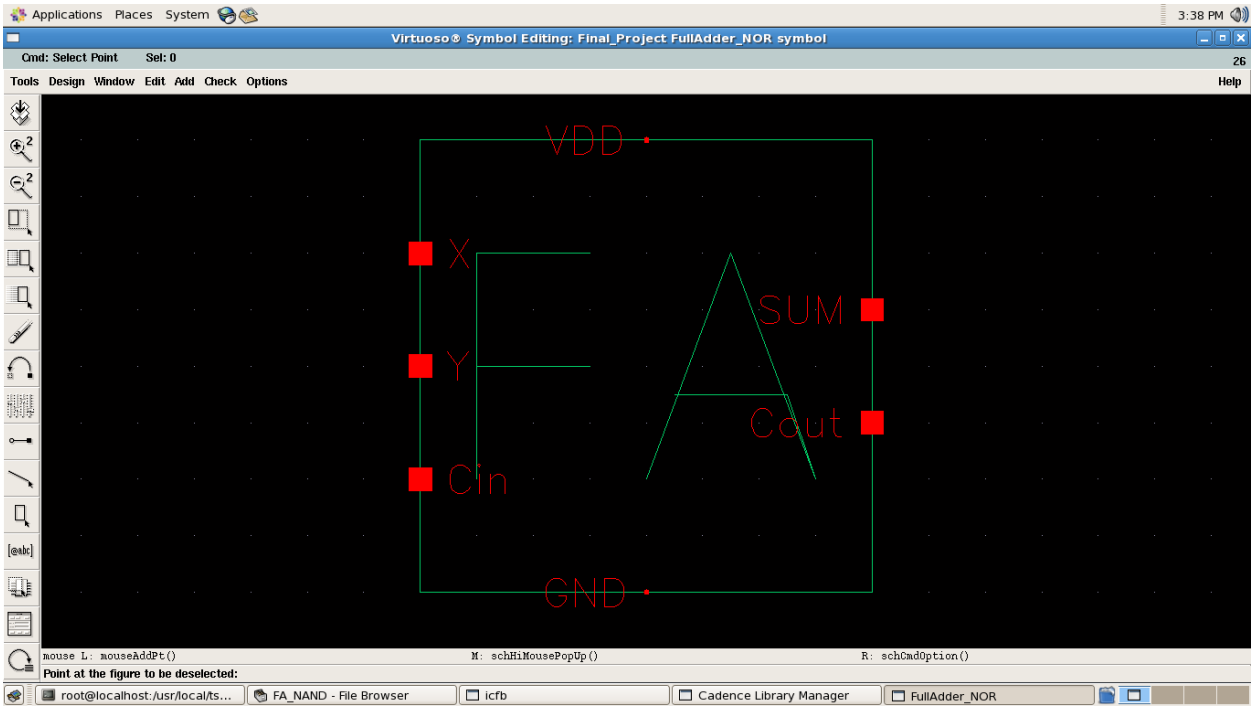
Delay=0.27ns

Full Adder using NOR

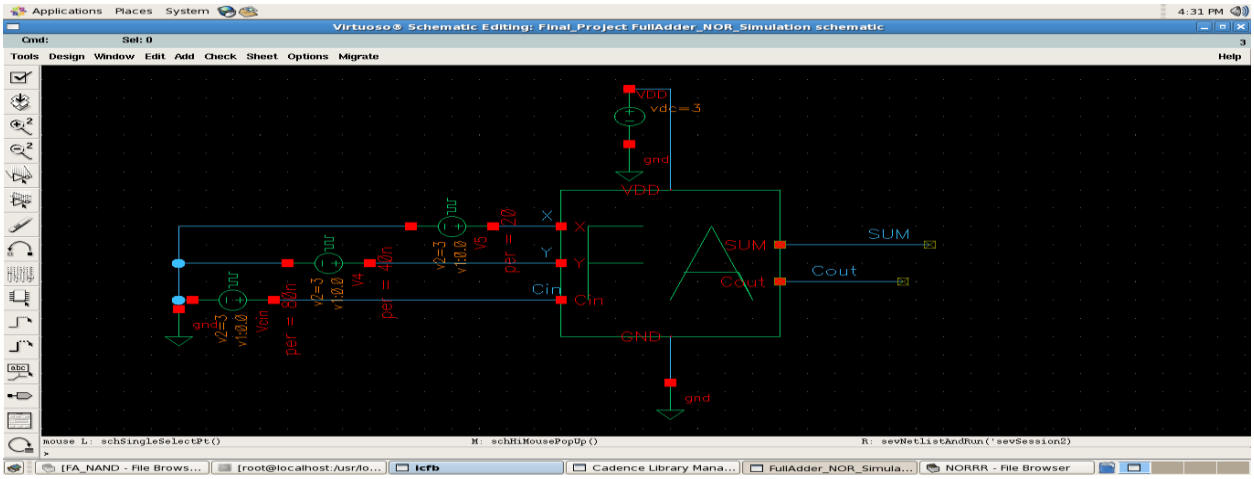
Schematic:

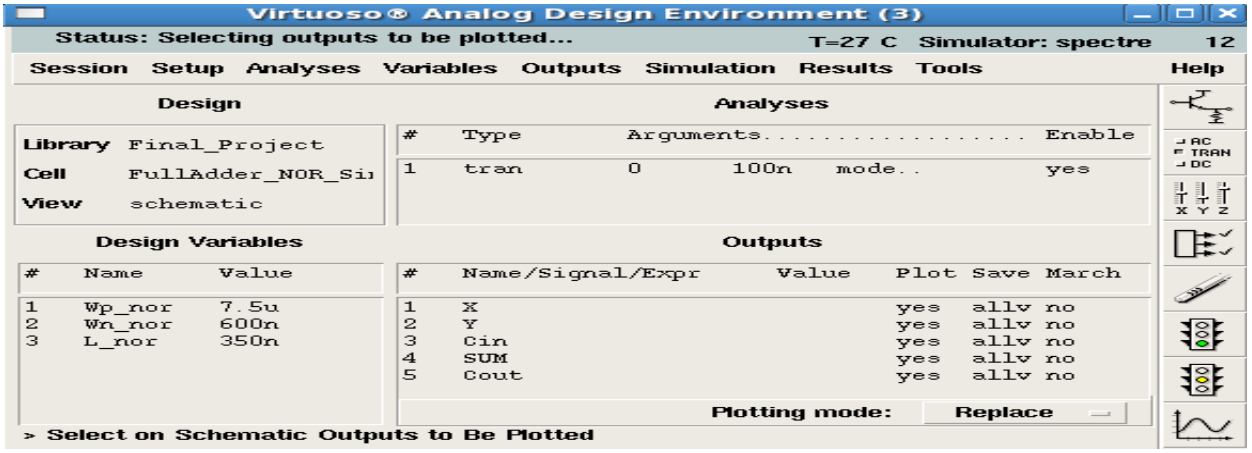


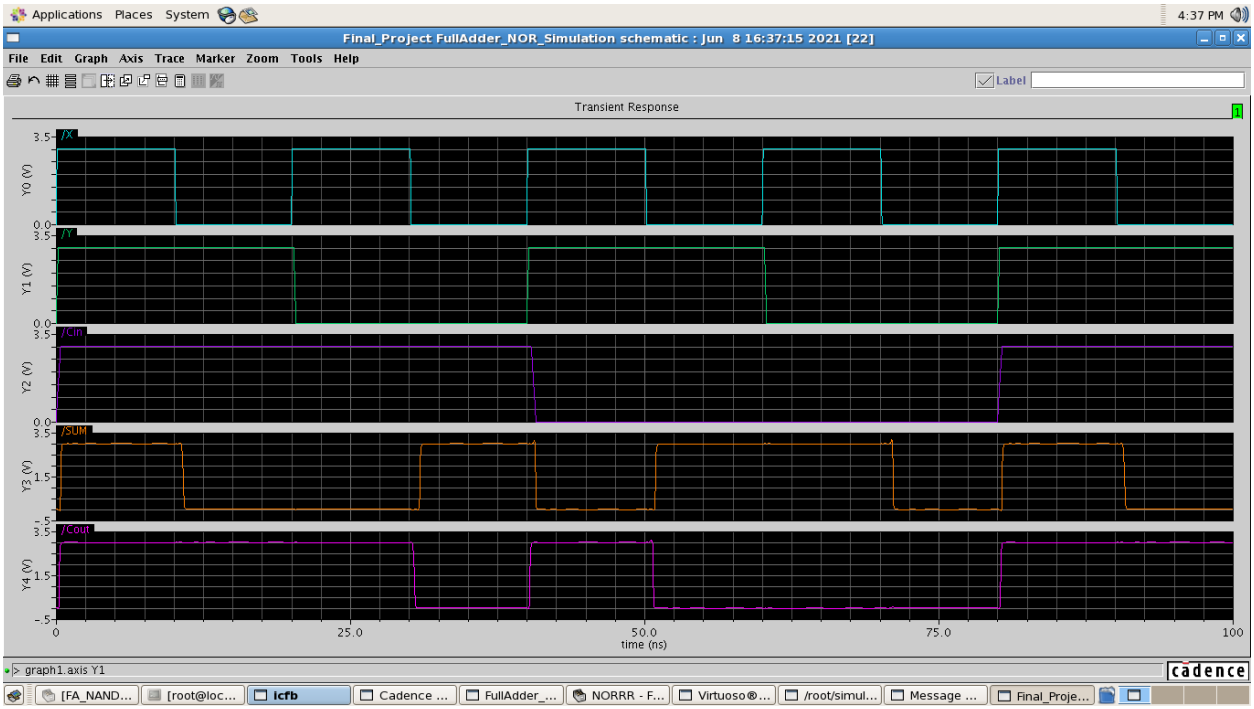
Symbol:



Operation:

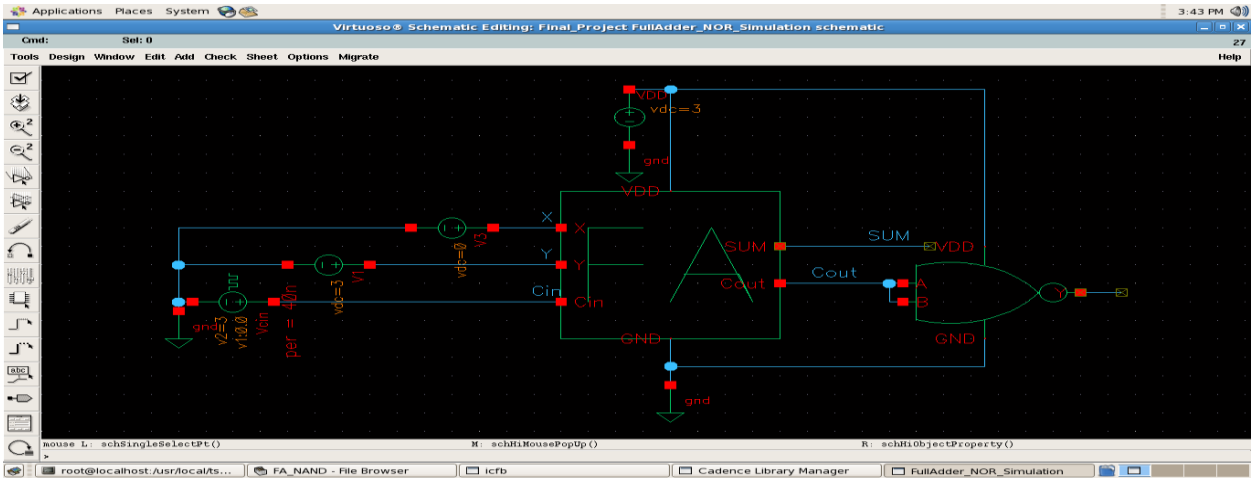

Virtuoso® Schematic Editing: Final_Project FullAdder_NOR_Simulation schematic
VDD
vdc=3
gnd
SUM
Cout
X
Y
Cin
GND

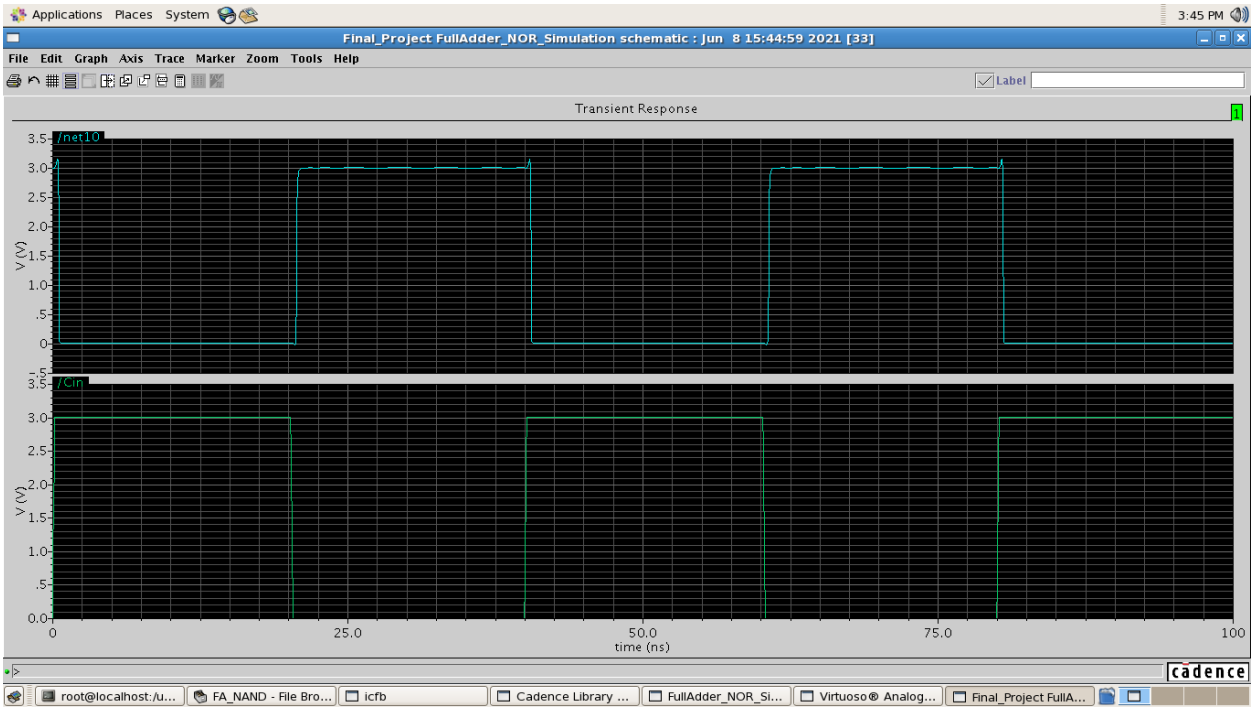

Virtuoso® Analog Design Environment (3)
Status: Selecting outputs to be plotted...
T=27 C
Simulator: spectre
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Library Final_Project
Cell FullAdder_NOR_Si
View schematic
Analyses
Type Arguments Enable
1 tran 0 100n mode yes
Design Variables
Name Value
1 Wp_nor 7.5u
2 Wn_nor 600n
3 L_nor 350n
Outputs
Name/Signal/Expr Value Plot Save March
1 X yes allv no
2 Y yes allv no
3 Cin yes allv no
4 SUM yes allv no
5 Cout yes allv no
Plotting mode: Replace
> Select on Schematic Outputs to Be Plotted

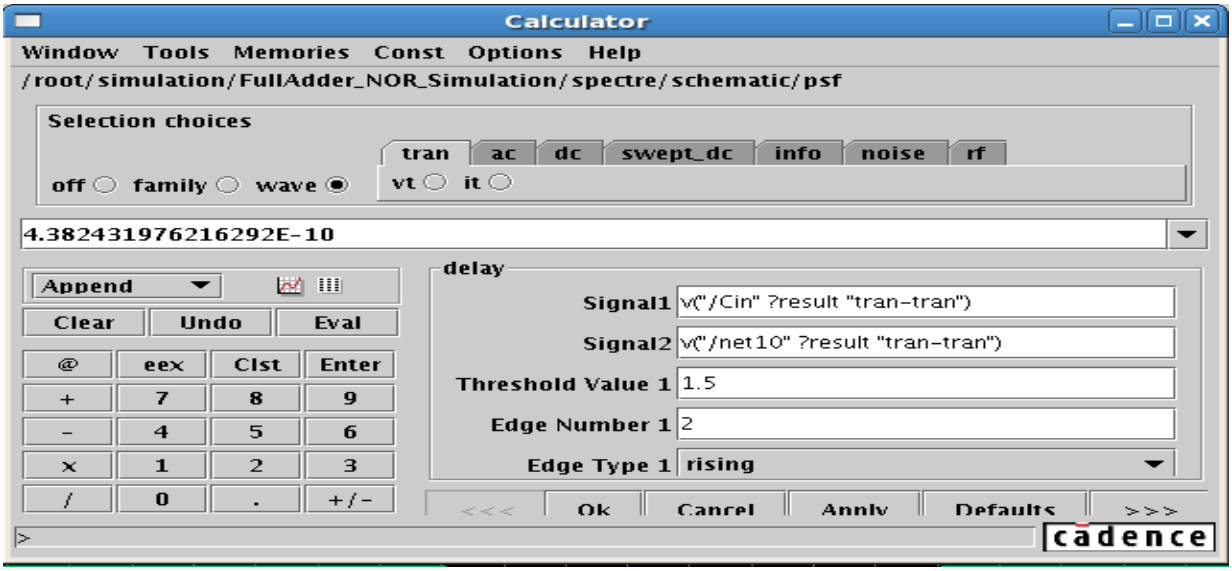

Final_Project FullAdder_NOR_Simulation schematic : Jun 8 16:37:15 2021 [22]
Transient Response
/X
/Y
/Cin
/SUM
/Cout
Y0 (V)
Y1 (V)
Y2 (V)
Y3 (V)
Y4 (V)
time (ns)
graph1.axis Y1

Calculating delay:

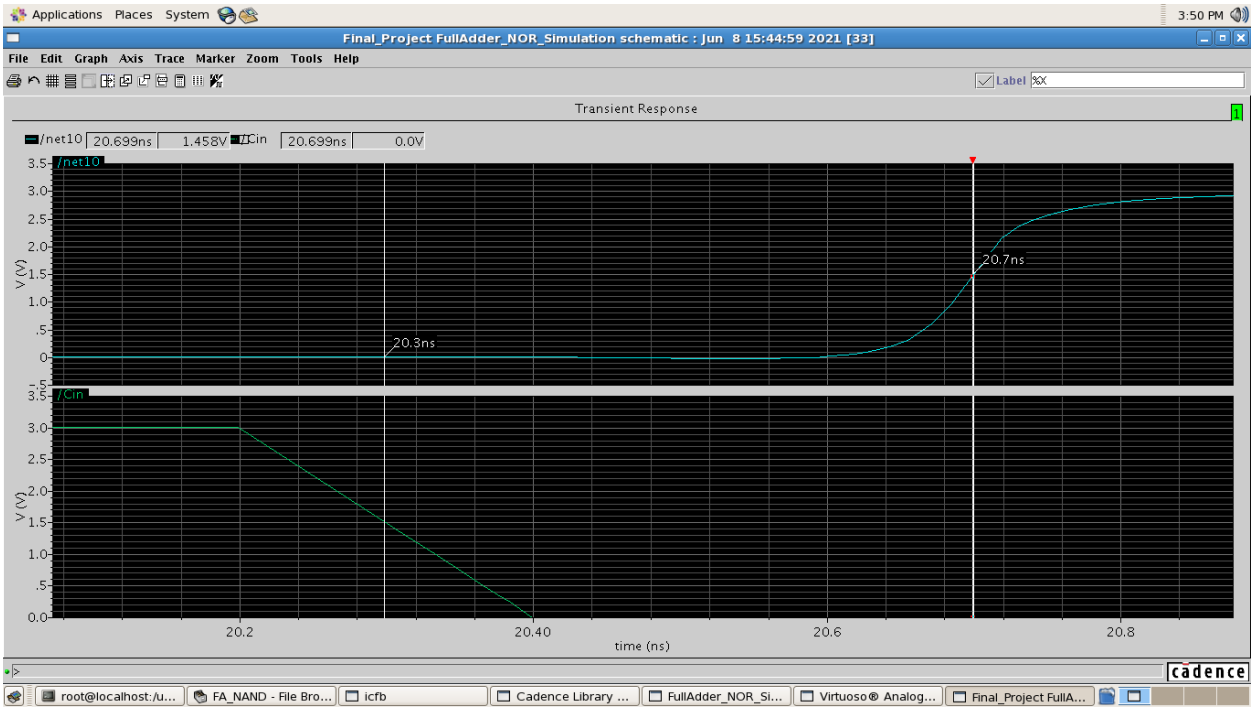
Schematic:







Delay= 0.438ns



Delay=0.5ns