VLSI project

1/Rules:

1. Team should be 8 to 10 students.
2. Team will make the project on cadence software used in the lab.
3. Copying between teams would be heavily penalized.
4. You need to be ready with the results **within one week.**
5. On the presentation day: not all students are required to be there. however, it is extremely advised that there should be 3 to 4 students to be on campus for discussion. These students have to be each group’s most brilliant individuals who made the most work and have a good understanding of VLSI and Digital ICs.
6. You will use transistors from library (tsmc13rf) used in the labs

2/project

You are required to design NAND and NOR gates and use them to create larger circuits.

**First phase: NAND and NOR cells.**

The NAND and NOR circuits have two inputs and one output, as well as pins for VDD and GND.

The circuits’ transistors should have their lengths and widths as variables (three variables for each circuit: L, Wn, Wp ).

Name the variables differently in NAND cell and in NOR cell (for example: L\_nand , L\_nor, etc.).

You are required to find the perfect ratio of each cell’s variables so that the threshold voltage Vm = VDD/2 and prove it by simulation (remember VTC curve and DC sweep (the crossing point simulation))

Save the final simulation results for the values that achieve the requirements.

**Second phase: the large circuit**

After designing your two cells, you will use them to make a **Full adder circuit**.

You must verify its function via simulation (transient). Use pulse source with periods that have ratio 1:2:4.

You must minimize the delay as possible, especially the delay of the carry output. A good measure is that the delay for the carry output should be **less than 9 ns** for the path from the carry input to the carry output.

You will use only these two cells to create the adder circuit.

Design a unique symbol for each of your cells.

For delay calculations: it’s the best way to have a NAND or a NOR cell (depends on how you built the circuit) and have its two inputs connected together to the carry out to act as an inverter. This will be considered your load on the output.

For delay calculations: put one of the inputs as 0 and the other as VDD to guarantee the worst-case delay.

(**Bonus**) if you could reach **less than 5 ns** for the path from the carry input to the carry output while applying the same conditions.

Grading:

The project without bonus: 10 marks

The project with bonus: up to 15 marks

Discussion:

Your team will be asked several questions on VLSI subject (Oral) in order to get the rest of your marks (up to 10 marks). You will also turn in your project and discuss the results you have reached.