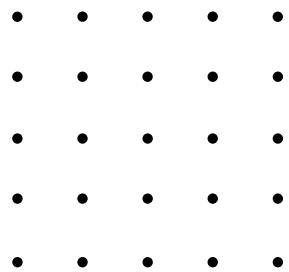


RISC-V Integrated With Cache Memory System From RTL TO GDS

Mahmoud S. Zahran

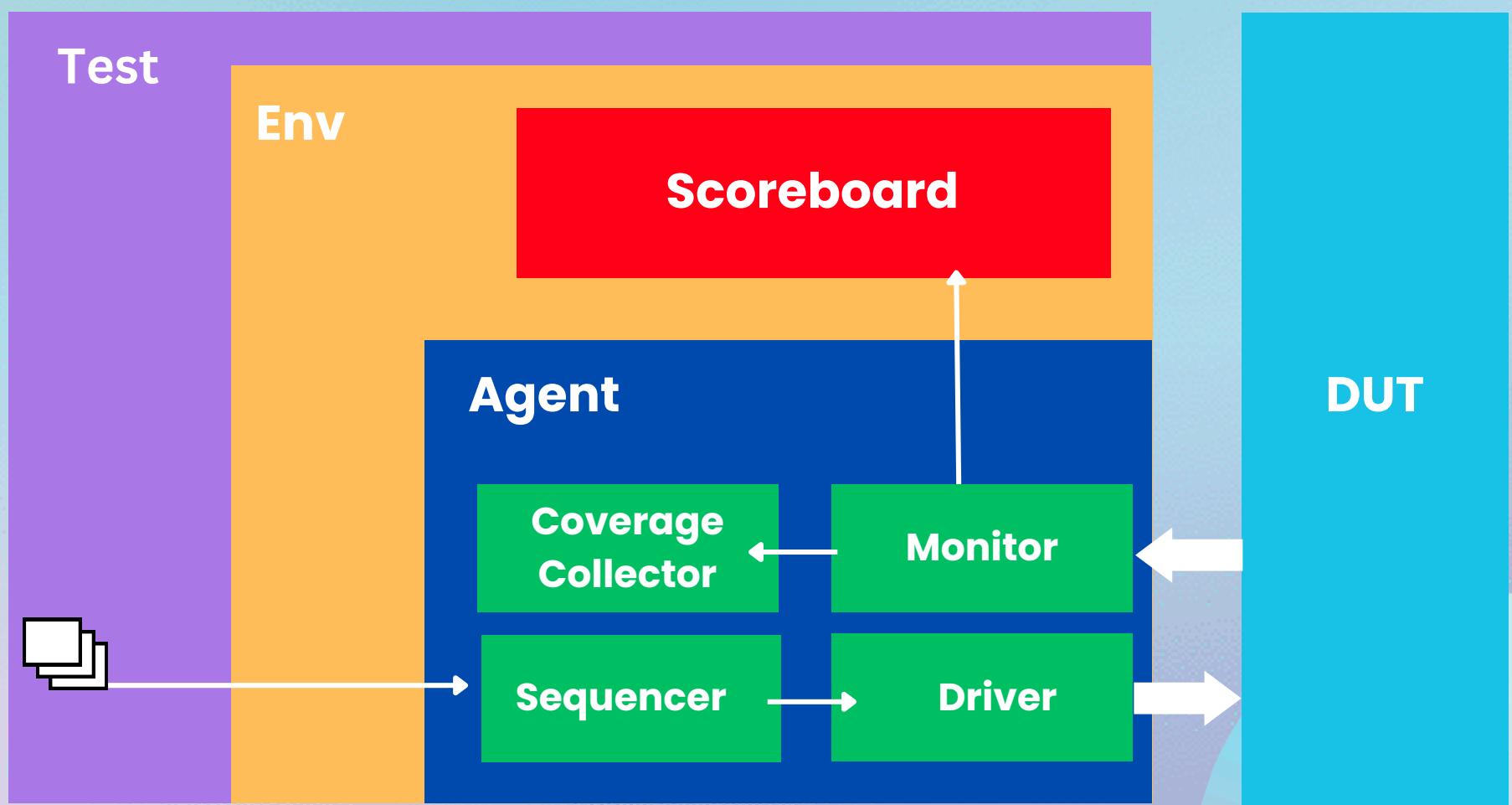
ASIC FLOW

1. Chip Specifications
2. RTL Design // Functional Verification
3. Synthesis
4. DFT Insertion
5. Floor Planning
6. Power Planning
7. Placement
8. Clock Tree Synthesis (CTS)
9. Routing
10. Chip Finishing

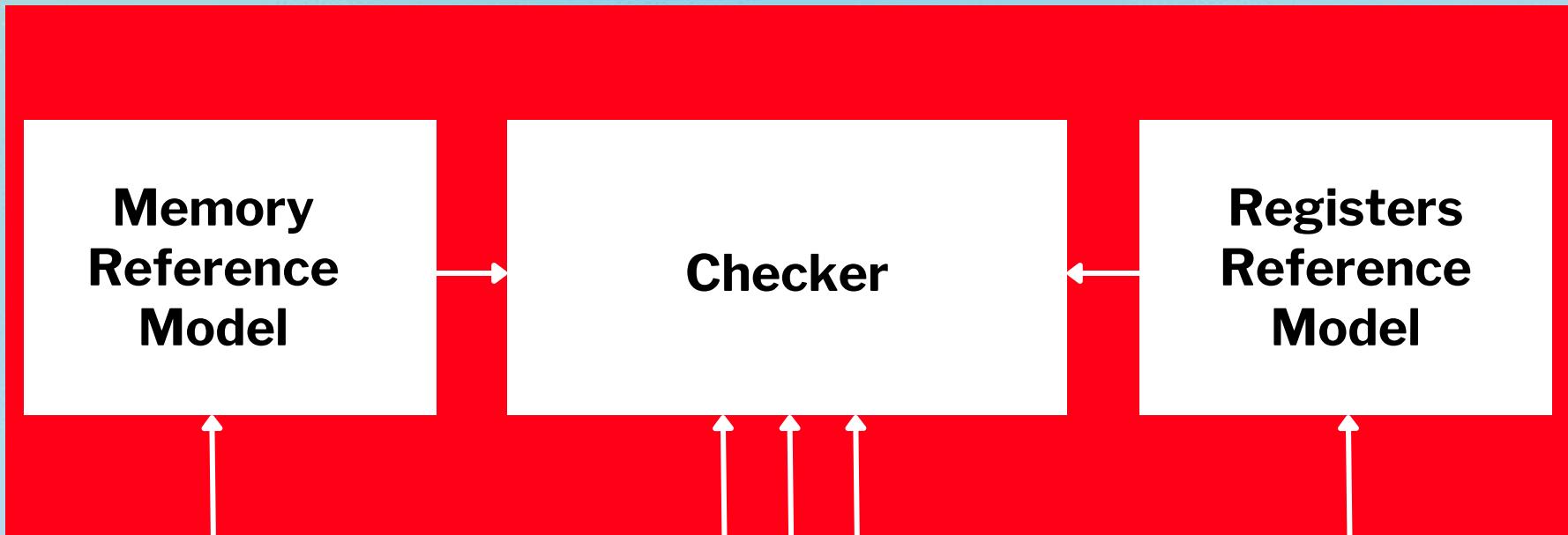


Functional Verification

Testbench Structure



Scoreboard



transaction data from monitor

Verification Plan

Name	test.expected	owner	at_least	weight	description	Score	Group
RISC_V_Verification_Plan	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
1 Basic	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
Measure_1						<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
RISCV_pkg::Coverage						<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
2 Advanced	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
2.1 Instructions	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
2.1.1 R_Type	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
Measure_1						<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
2.1.2 B_Type	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
Measure_1						<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
2.1.3 S_Type	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
Measure_1						<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
2.1.4 I_Type	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
Measure_1						<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
2.1.5 U_Type	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
Measure_1						<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
2.1.6 J_Type	0	Youssef	0	1		<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%
Measure_1						<div style="width: 100.0%; background-color: green;"></div> 100.0%	<div style="width: 100.0%; background-color: green;"></div> 100.0%

Code Coverage

Name	Score	Assert	Line	Toggle	FSM	Condition	Branch
AIW	96.78%		95.45%	100.00%		100.00%	91.67%
Cache_Ctrl	85.91%		87.23%	98.21%	66.67%	97.44%	80.00%
Cache_Memory	80.28%		100.00%	78.80%		57.69%	84.62%
Control_Unit	95.54%		98.55%	90.91%		95.35%	97.37%
DataMem	88.74%		100.00%	88.31%		66.67%	100.00%
Data_Memory_System	91.86%			91.86%			
ImmGen	90.08%		87.50%	97.01%			85.71%
Interface	98.60%			98.60%			
PC	99.75%		100.00%	99.24%			100.00%
RISCV	97.14%			99.10%		92.31%	100.00%
RISCV_Top	93.75%		87.50%	100.00%			
reg_file	96.16%		100.00%	84.64%		100.00%	100.00%
uvm_custom_install_rec...	30.91%			31.82%			30.00%
uvm_pkg							
vcs_paramclassrepository	100.00%	100.00%					

Functional Coverage

•	Cover Group Item	Score	Instances	U+C	U	C	X	Goal	Weight	AtLeast	PerInst	Overlap	AutoBin	Missing	Comment
	RISCV_pkg::C...	100.00%	100.00%	37	0	37	0	100%	1	1	1	1	64	64	
	CP B_Type	100.00%		6	0	6	0	100%	1	1		1	0		
	CP I_Type	100.00%		15	0	15	0	100%	1	1		1	0		
	CP J_Type	100.00%		1	0	1	0	100%	1	1		1	0		
	CP R_Type	100.00%		10	0	10	0	100%	1	1		1	0		
	CP S_Type	100.00%		3	0	3	0	100%	1	1		1	0		
	CP U_Type	100.00%		2	0	2	0	100%	1	1		1	0		

Functional Coverage

•	Status	Bin Name	Type	At Least	Size	Hit Count
	✓	BEQ	User	1	1	2895
	✓	BGE	User	1	1	2741
	✓	BGEU	User	1	1	2793
	✓	BLT	User	1	1	2816
	✓	BLTU	User	1	1	2783
	✓	BNO	User	1	1	2728

Functional Coverage

Cover Group Item	Score	Instances	U+C	U	C	X	Goal	Weight	AtLeast	PerInst	Overlap	AutoBin	Missing	Comment
Cg RISCV_pkg::C...	100.00%	100.00%	37	0	37	0	100%	1	1	1	1	64	64	
Cr B_Type	100.00%		6	0	6	0	100%	1	1		1	0		
Cr I_Type	100.00%		15	0	15	0	100%	1	1		1	0		
Cr J_Type	100.00%		1	0	1	0	100%	1	1		1	0		
Cr R_Type	100.00%		10	0	10	0	100%	1	1		1	0		
Cr S_Type	100.00%		3	0	3	0	100%	1	1		1	0		
Cr U_Type	100.00%		2	0	2	0	100%	1	1		1	0		

Status	Bin Name	Type	At Least	Size	Hit Count
✓	ADDI	User	1	1	2801
✓	ANDI	User	1	1	2660
✓	JALR	User	1	1	2628
✓	LB	User	1	1	41
✓	LBU	User	1	1	2713
✓	LH	User	1	1	16
✓	LHU	User	1	1	68
✓	LW	User	1	1	2633
✓	ORI	User	1	1	2680
✓	SLLI	User	1	1	27
✓	SLTI	User	1	1	2602
✓	SLTIU	User	1	1	2590
✓	SRAI	User	1	1	15
✓	SRLI	User	1	1	16
✓	XORI	User	1	1	2666

Functional Coverage

Functional Coverage

*	Cover Group Item	Score	Instances	U+C	U	C	X	Goal	Weight	AtLeast	PerInst	Overlap	AutoBin	Missing	Comment	
	Cg RISCV_pkg::C...	<div style="width: 100.00%;">100.00%</div>	<div style="width: 100.00%;">100.00%</div>	37	0	37	0	100%	1	1	1	1	64	64		
	Cp B_Type	<div style="width: 100.00%;">100.00%</div>		6	0	6	0	100%	1	1		1	0			
	Cp I_Type	<div style="width: 100.00%;">100.00%</div>		15	0	15	0	100%	1	1		1	0			
	Cp J_Type	<div style="width: 100.00%;">100.00%</div>		1	0	1	0	100%	1	1		1	0			
	Cp R_Type	<div style="width: 100.00%;">100.00%</div>		10	0	10	0	100%	1	1		1	0			
	Cp S_Type	<div style="width: 100.00%;">100.00%</div>		3	0	3	0	100%	1	1		1	0			
	Cp U_Type	<div style="width: 100.00%;">100.00%</div>		2	0	2	0	100%	1	1		1	0			

*	Status	Bin Name	Type	At Least	Size	Hit Count
	✓	SB	User	1	1	3600
	✓	SH	User	1	1	3445
	✓	SW	User	1	1	3187

Functional Coverage

Cover Group Item	Score	Instances	U+C	U	C	X	Goal	Weight	AtLeast	PerInst	Overlap	AutoBin	Missing	Comment
RISCV_pkg::C...	<div style="width: 100.00%; background-color: green;"></div> 100.00%	<div style="width: 100.00%; background-color: green;"></div> 100.00%	37	0	37	0	100%	1	1	1	1	64	64	
CP B_Type	<div style="width: 100.00%; background-color: green;"></div> 100.00%			6	0	6	0	100%	1	1		1	0	
CP I_Type	<div style="width: 100.00%; background-color: green;"></div> 100.00%			15	0	15	0	100%	1	1		1	0	
CP J_Type	<div style="width: 100.00%; background-color: green;"></div> 100.00%			1	0	1	0	100%	1	1		1	0	
CP R_Type	<div style="width: 100.00%; background-color: green;"></div> 100.00%			10	0	10	0	100%	1	1		1	0	
CP S_Type	<div style="width: 100.00%; background-color: green;"></div> 100.00%			3	0	3	0	100%	1	1		1	0	
CP U_Type	<div style="width: 100.00%; background-color: green;"></div> 100.00%			2	0	2	0	100%	1	1		1	0	

Status	Bin Name	Type	At Least	Size	Hit Count
<input checked="" type="checkbox"/>	AUIPC	User	1	1	21255
<input checked="" type="checkbox"/>	LUI	User	1	1	21452

Final Results

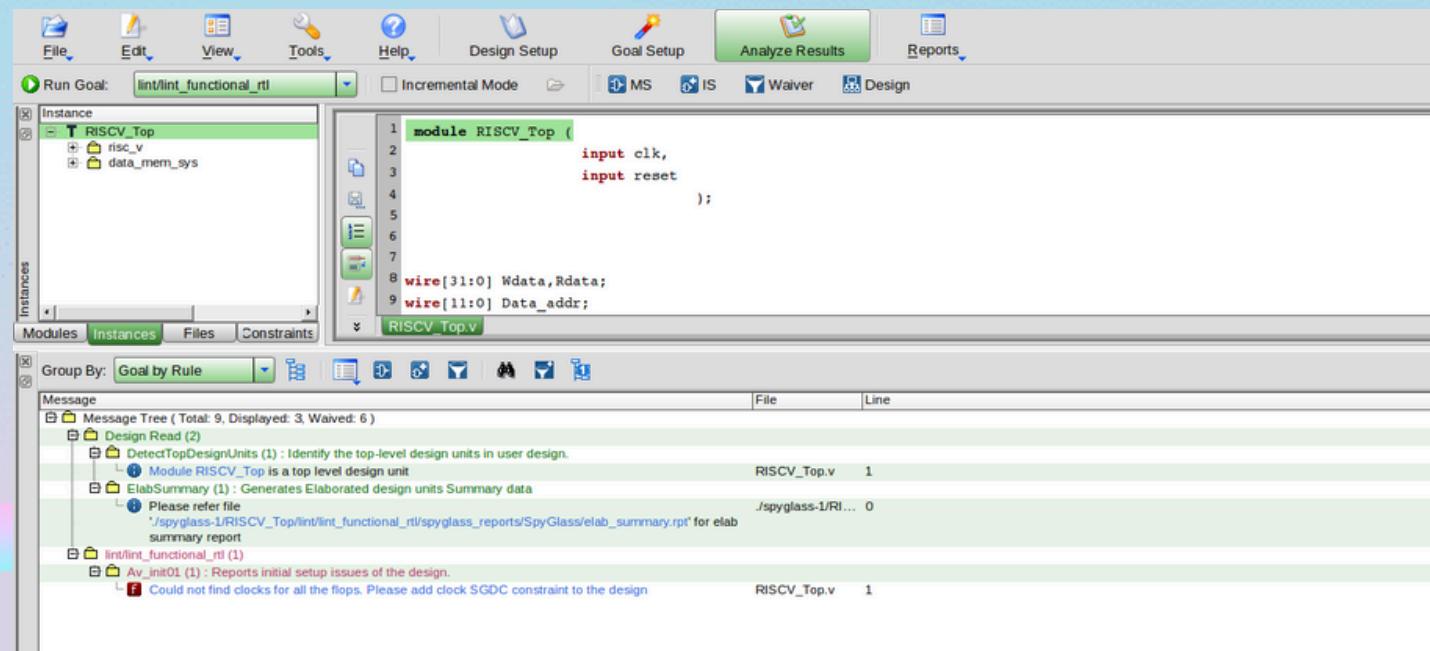
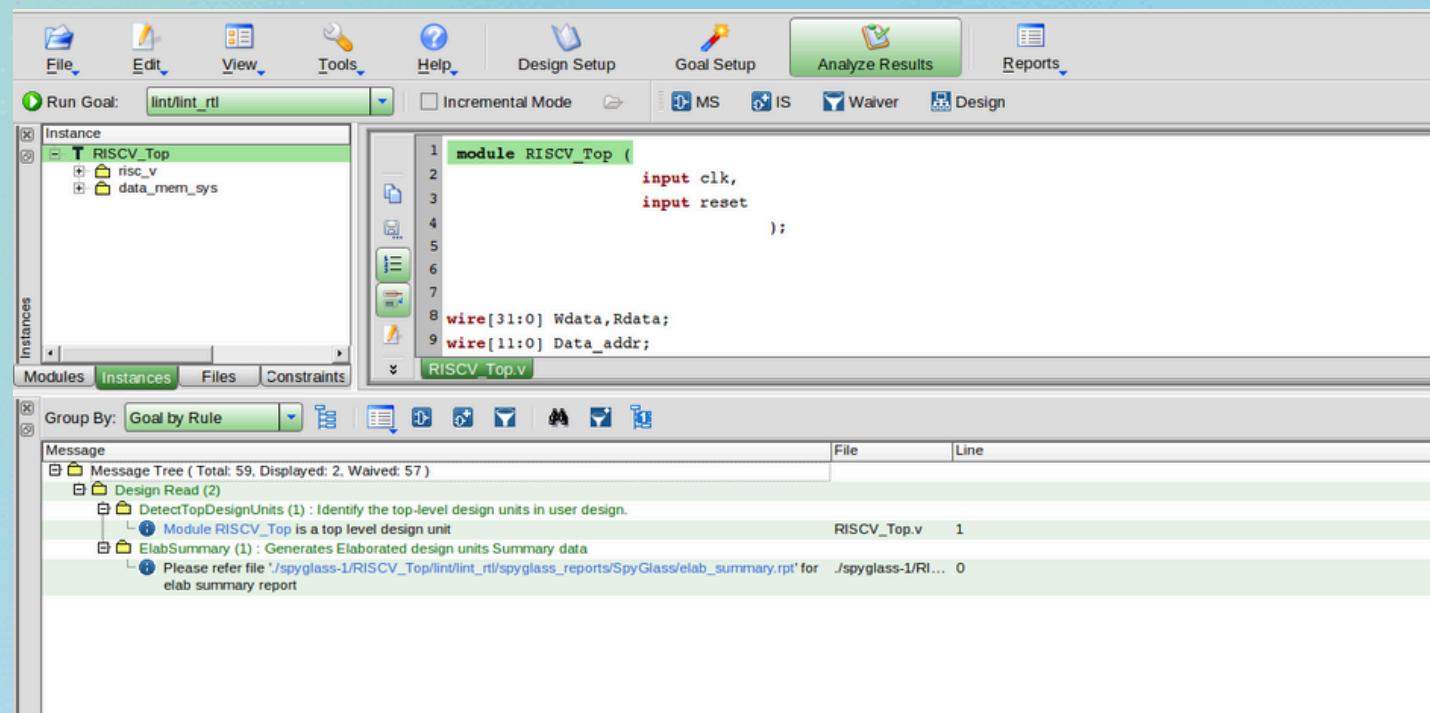
```
UVM_INFO Coverage_Collector.sv(178) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_coverage_collector [Coverage_Collector] Inside build phase of coverage collector Class
UVM_INFO Driver.sv(42) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_driver [Driver] Inside build phase of Driver Class
UVM_INFO Monitor.sv(50) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_monitor [Monitor] Inside build phase of Monitor Class
UVM_INFO Sequencer.sv(33) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_sequencer [Sequencer] Inside build phase of Sequencer Class
UVM_INFO Scoreboard.sv(41) @ 0: uvm_test_top.RISCV_environment.RISCV_Scoreboard [Scoreboard] Inside build phase of Scoreboard Class
UVM_INFO Coverage_Collector.sv(196) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_coverage_collector [Coverage_Collector] Inside connect phase of coverage collector Class
UVM_INFO Driver.sv(67) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_driver [Driver] Inside connect phase of Driver Class
UVM_INFO Monitor.sv(78) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_monitor [Monitor] Inside connect phase of Monitor Class
UVM_INFO Sequencer.sv(51) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_sequencer [Sequencer] Inside connect phase of Sequencer Class
UVM_INFO Agent.sv(67) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent [Agent] Inside connect phase of Agent Class
UVM_INFO Scoreboard.sv(66) @ 0: uvm_test_top.RISCV_environment.RISCV_Scoreboard [Scoreboard] Inside connect phase of Scoreboard Class
UVM_INFO Environment.sv(74) @ 0: uvm_test_top.RISCV_environment [Environment] Inside connect phase of Environment Class
UVM_INFO RISCV_Test.sv(74) @ 0: uvm_test_top [RISCV_Test] Inside connect phase of RISCV Test Class
UVM_INFO Coverage_Collector.sv(213) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_coverage_collector [Coverage_Collector] Inside run phase of coverage collector Class
UVM_INFO Driver.sv(84) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_driver [Driver] Inside run phase of Driver Class
UVM_INFO Monitor.sv(96) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_monitor [Monitor] Inside run phase of Monitor Class
UVM_INFO Sequencer.sv(68) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent.RISCV_sequencer [Sequencer] Inside run phase of Sequencer Class
UVM_INFO Agent.sv(88) @ 0: uvm_test_top.RISCV_environment.RISCV_Agent [Agent] Inside run phase of Agent Class
UVM_INFO Scoreboard.sv(79) @ 0: uvm_test_top.RISCV_environment.RISCV_Scoreboard [Scoreboard] Inside connect phase of Scoreboard Class
UVM_INFO Environment.sv(92) @ 0: uvm_test_top.RISCV_environment [Environment] Inside run phase of Environment Class
UVM_INFO RISCV_Test.sv(93) @ 0: uvm_test_top [RISCV_Test] Inside run phase of RISCV Test Class
UVM_INFO /home/synopsys/vcs-mx/0-2018.09-1/etc/uvm-1.2/base/uvm_objection.svh(1276) @ 6479400: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO Scoreboard.sv(112) @ 6479400: uvm_test_top.RISCV_environment.RISCV_Scoreboard [Scoreboard] Inside check phase of Scoreboard Class
UVM_INFO Scoreboard.sv(114) @ 6479400: uvm_test_top.RISCV_environment.RISCV_Scoreboard [Scoreboard] ##### The num of mismatching data = 0 #####
UVM_INFO /home/synopsys/vcs-mx/0-2018.09-1/etc/uvm-1.2/base/uvm_report_catcher.svh(705) @ 6479400: reporter [UVM/REPORT/CATCHER]
--- UVM Report catcher Summary ---
```

```
--- UVM Report Summary ---

** Report counts by severity
UVM_INFO : 38
UVM_WARNING : 0
UVM_ERROR : 0
UVM_FATAL : 0
** Report counts by id
[Agent] 4
[Coverage_Collector] 4
[Driver] 4
[Environment] 4
[Monitor] 4
[RISCV_Test] 4
[RNTST] 1
[Scoreboard] 6
[Sequencer] 4
[TEST_DONE] 1
[UVM/RELNOTES] 1
[UVM/REPORT/CATCHER] 1
```

```
$finish called from file "/home/synopsys/vcs-mx/0-2018.09-1/etc/uvm-1.2/base/uvm_root.svh", line 527.
$finish at simulation time 6479400.
```

Linting



File Edit View Tools Help Design Setup Goal Setup Analyze Results Reports

Run Goal: lint/lint_abstract

Instances

Module Instances Files Constraints

Group By: Goal by Rule

Message Tree (Total: 9, Displayed: 3, Waived: 6)

- Design Read (2)
 - DetectTopDesignUnits (1) : Identify the top-level design units in user design.
 - Module RISCV_Top is a top level design unit RISCV.Top.v 1
 - ElabSummary (1) : Generates Elaborated design units Summary data
 - Please refer file './spyglass-1/RISCV_Top/lint/lint_abstract/spyglass_reports/SpyGlass/elab_summary.rpt' for elab summary report ./spyglass-1/RI... 0
- lint/lint_abstract (1)
 - LINT_abstract01 (1) : Generates relevant base policy constraints for block abstraction
 - Abstract view for design RISCV_Top successfully created ./spyglass-1/RI... 0

File Edit View Tools Help Design Setup Goal Setup Analyze Results Reports

Run Goal: lint/lint_turbo_rtl

Instances

Module Instances Files Constraints

Group By: Goal by Rule

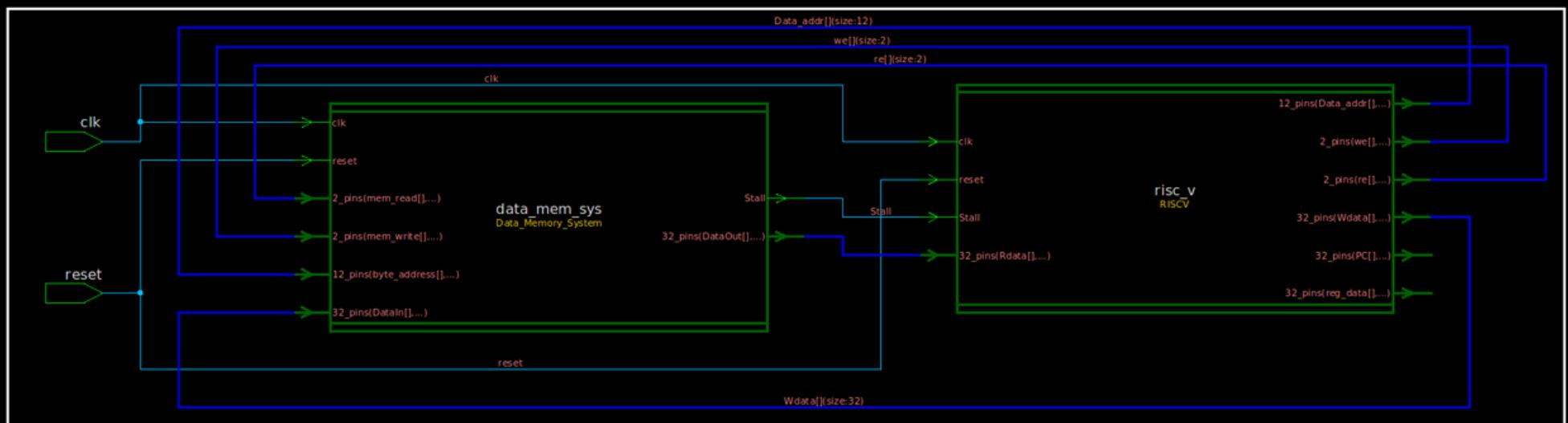
Message Tree (Total: 35, Displayed: 4, Waived: 68, Secondary Waived: 36)

- Design Read (3)
 - DetectTopDesignUnits (1) : Identify the top-level design units in user design.
 - Module RISCV_Top is a top level design unit RISCV.Top.v 1
 - ElabSummary (1) : Generates Elaborated design units Summary data
 - Please refer file './spyglass-1/RISCV_Top/lint/lint_turbo_rtl/spyglass_reports/SpyGlass/elab_summary.rpt' for elab summary report ./spyglass-1/RI... 0
 - TurboModeStatus (1) : Reports if turbo_struct license feature is successfully checked out or not.
 - Turbo-Mode is enabled in the current run as turbo_struct license feature successfully checked out N.A. 0
- lint/lint_turbo_rtl (1)
 - Av_init01 (1) : Reports initial setup issues of the design.
 - Could not find clocks for all the flops. Please add clock SGDC constraint to the design RISCV.Top.v 1

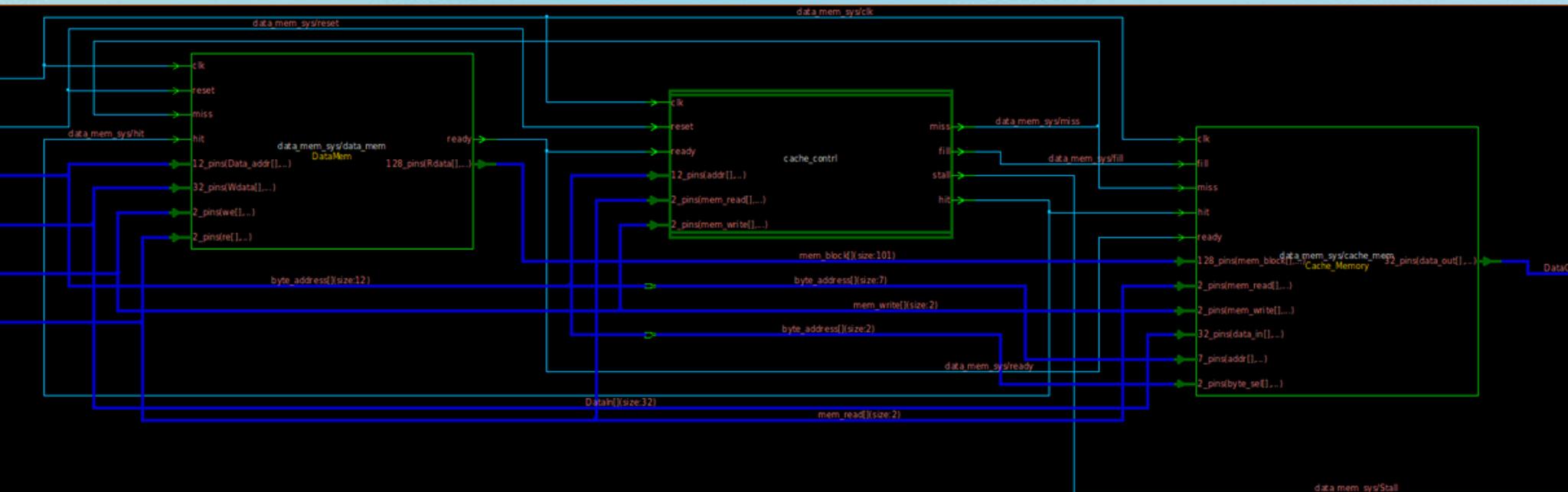


Synthesis

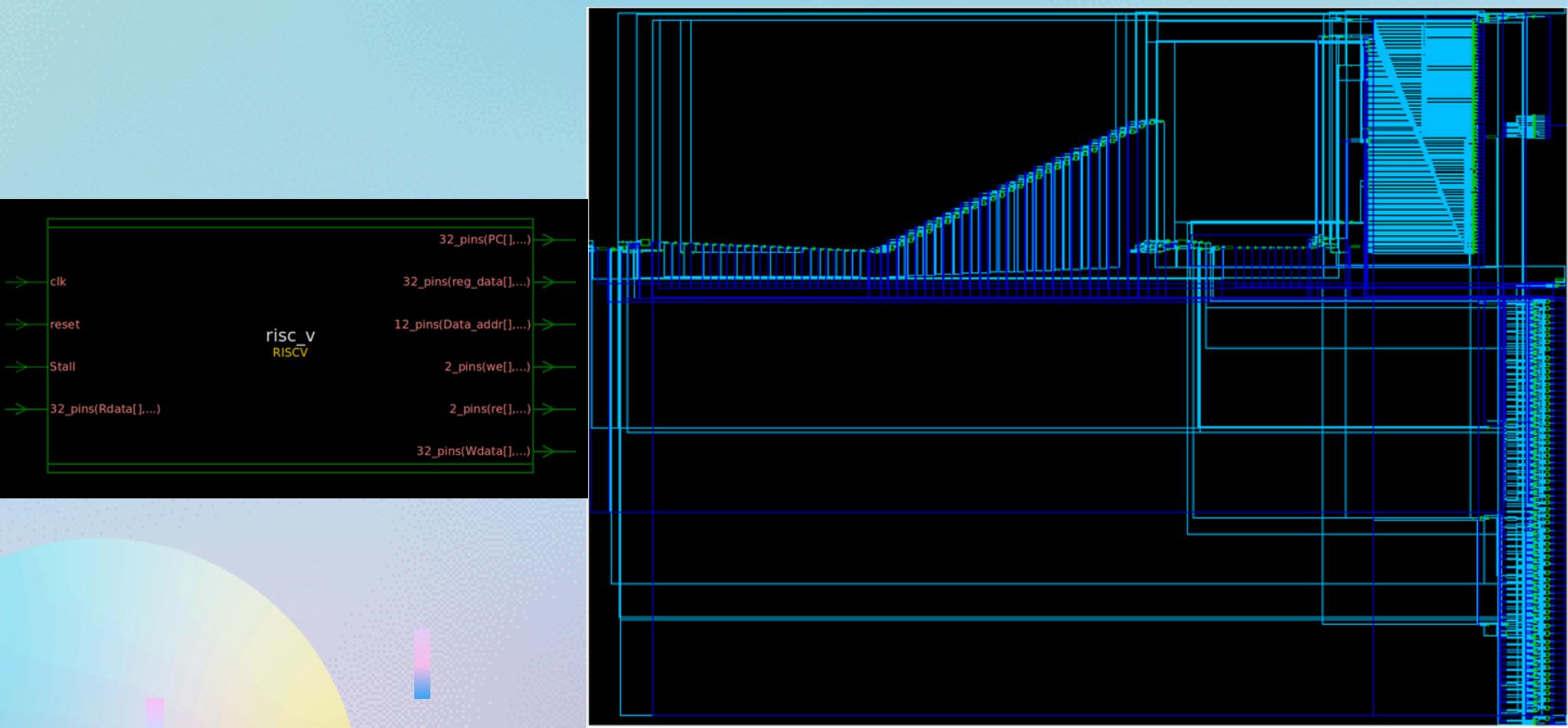
Schematic of Top Design



Schematic of Data Memory System



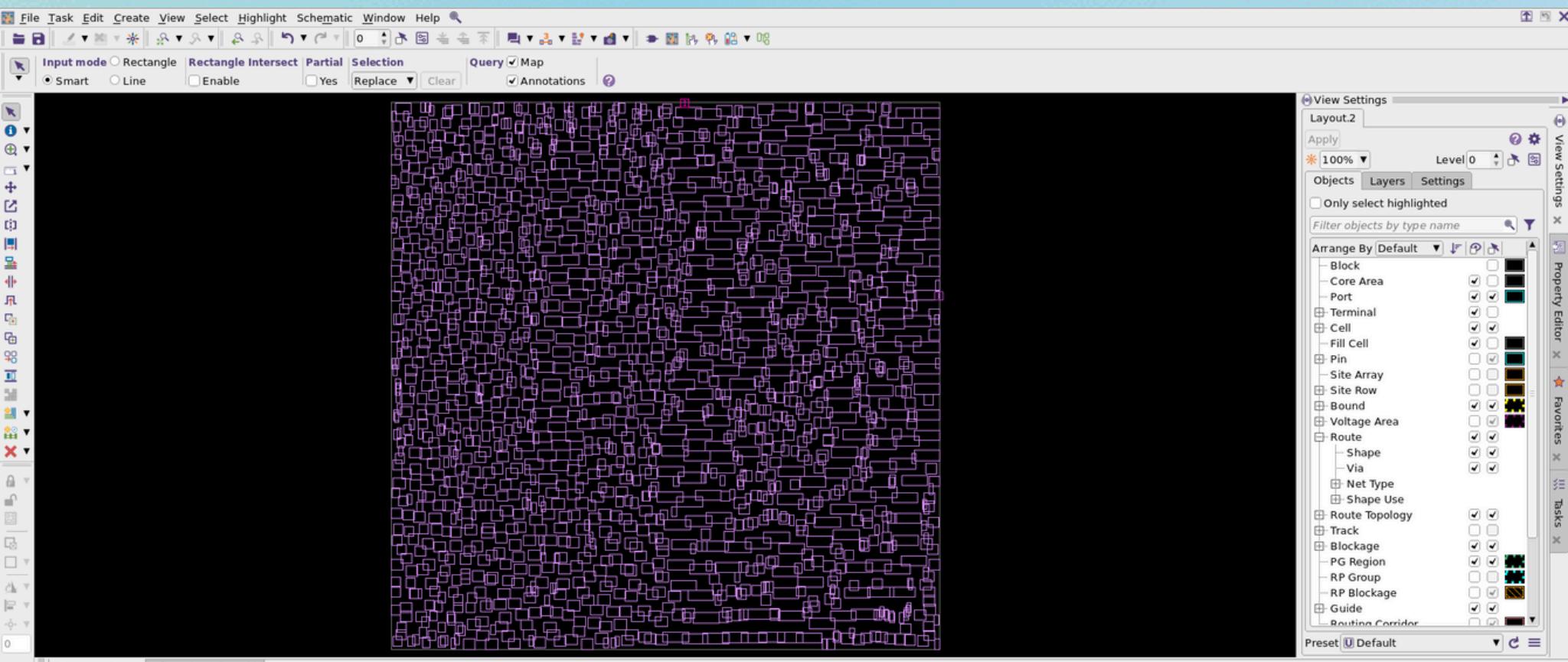
Schematic of RISC-V



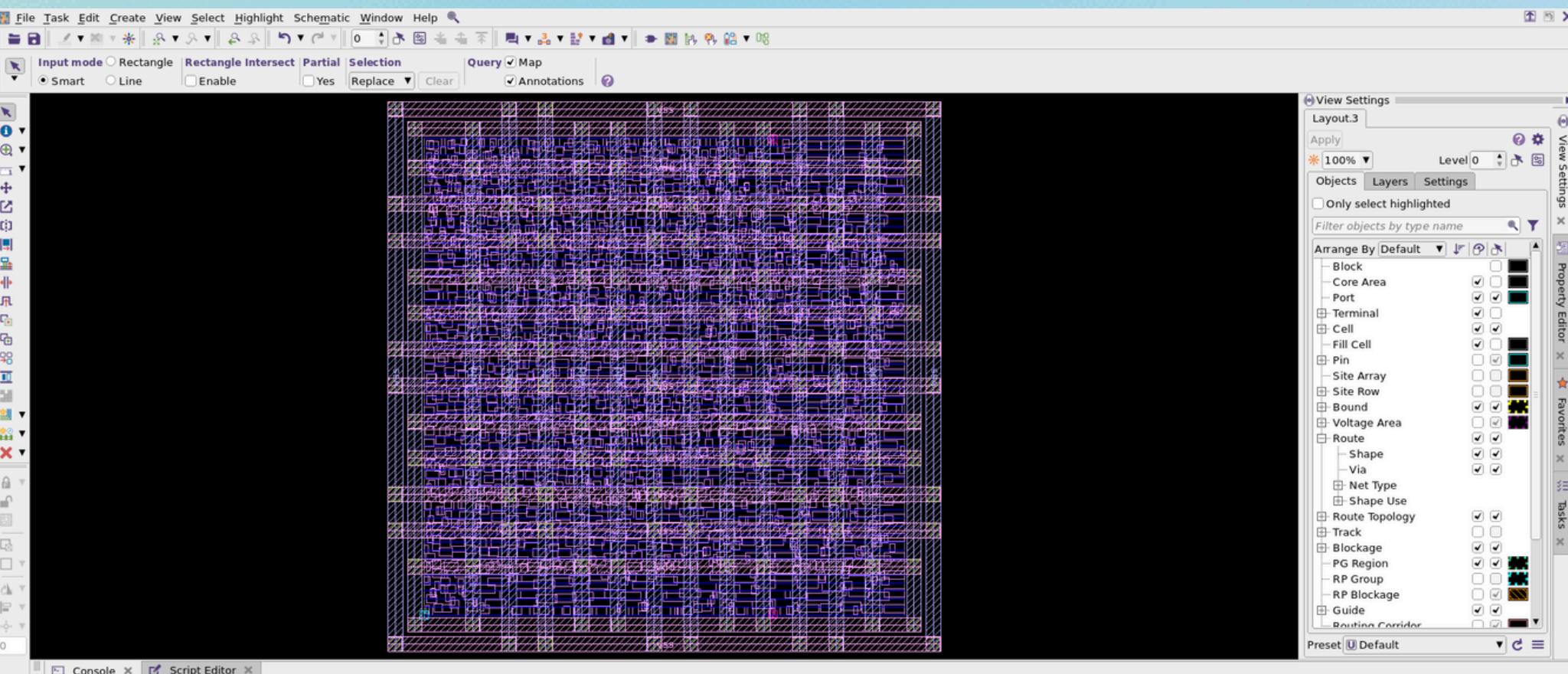


PNR

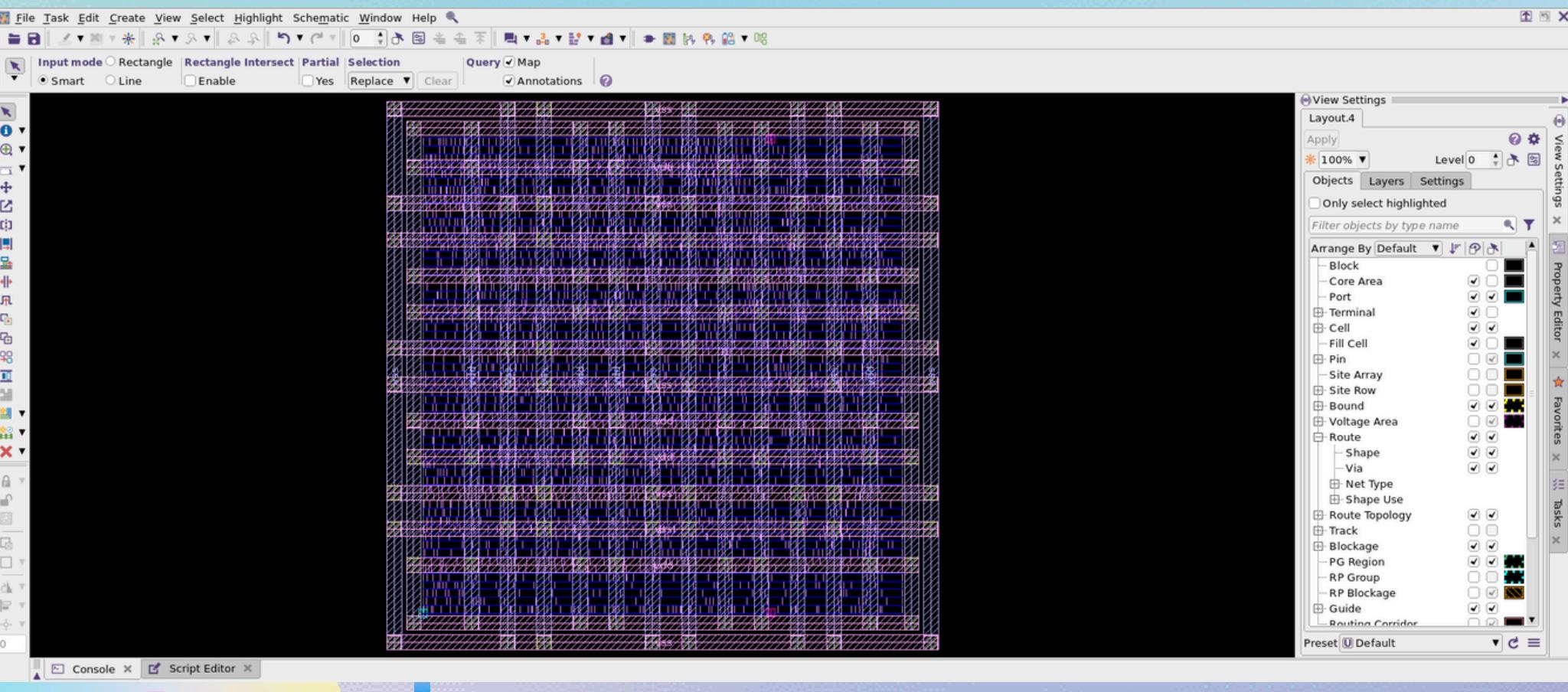
Floor Planning



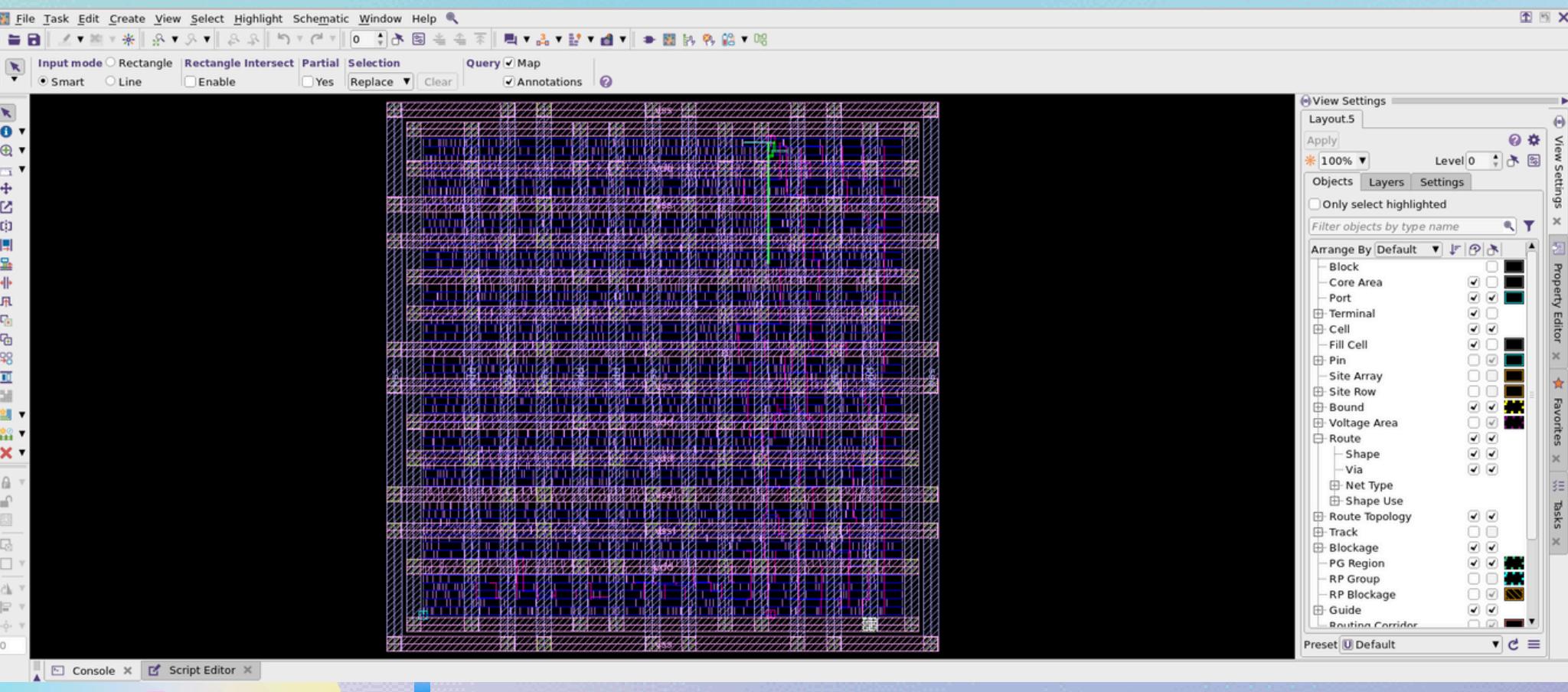
Power Planning



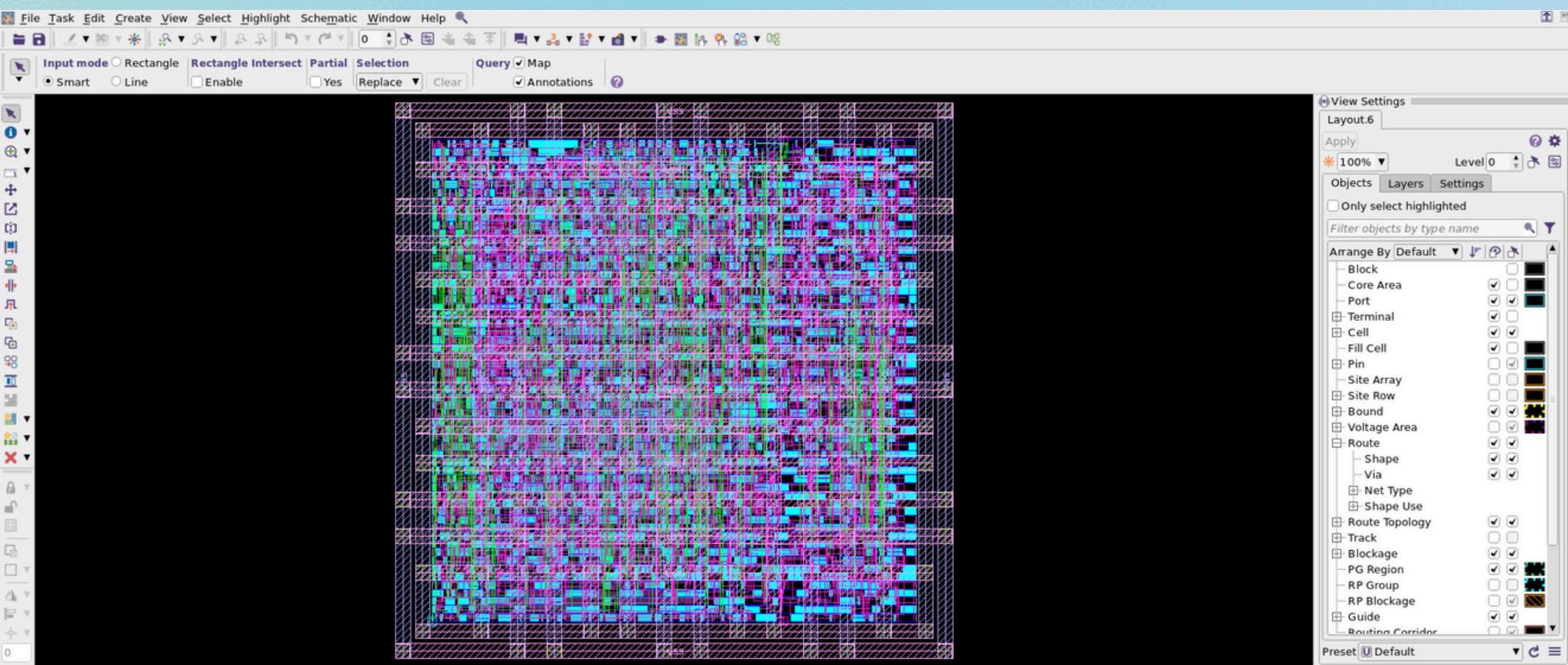
Placement



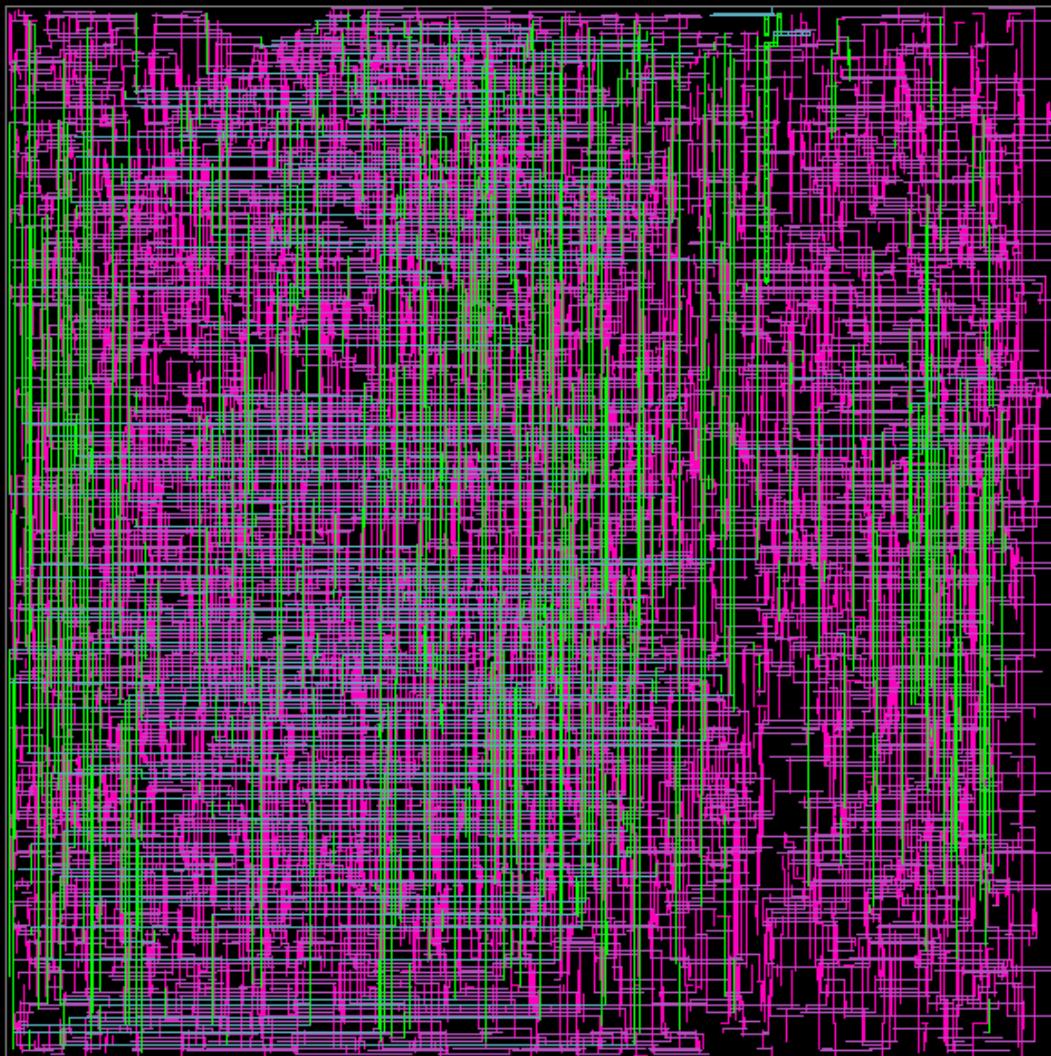
Clock Tree Synthesis



Routing

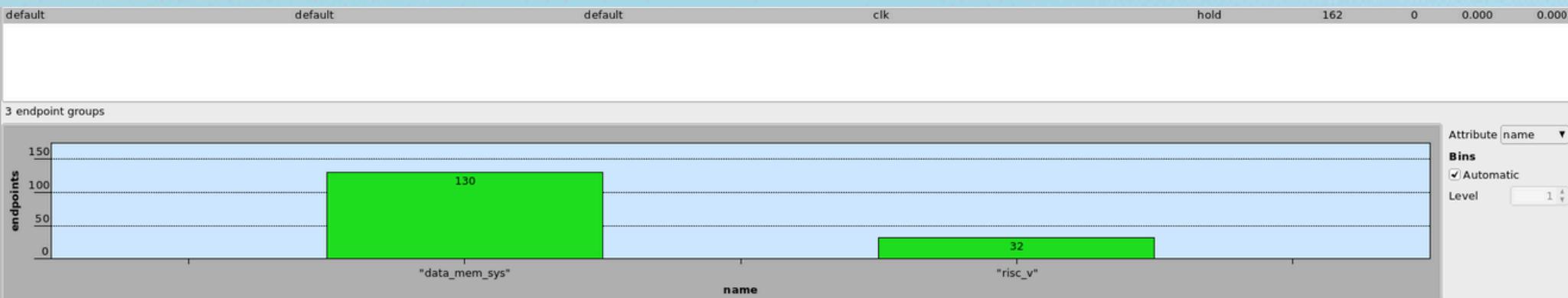


Routing Layers



Chip Finishing

Timing Paths

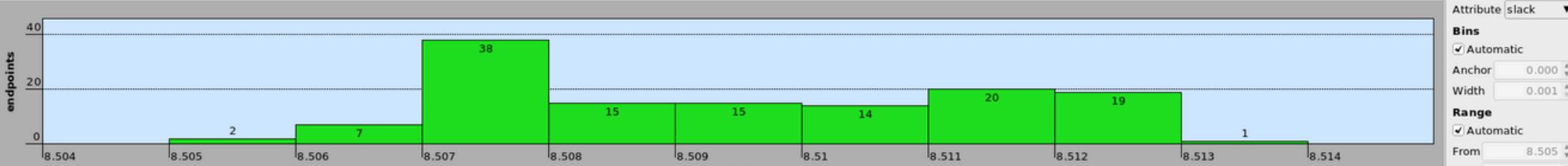


Setup Time Analysis

Histogram of Slack Values at Max TLU

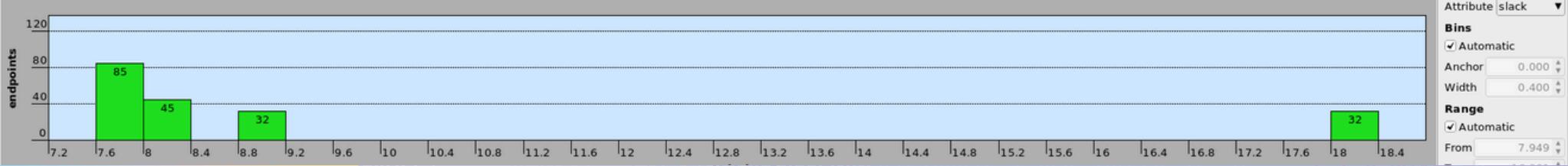
default	default	default	**async_default**	setup	131	0	0.000	0.000
default	default	default	clk	setup	194	0	0.000	0.000
default	default	default	clk	hold	162	0	0.000	0.000

3 endpoint groups



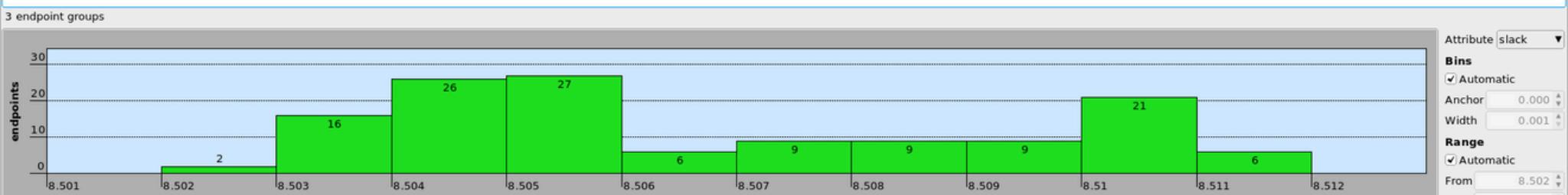
default	default	default	default	clk	setup	194	0	0.000	0.000
default	default	default	default	clk	hold	162	0	0.000	0.000

3 endpoint groups

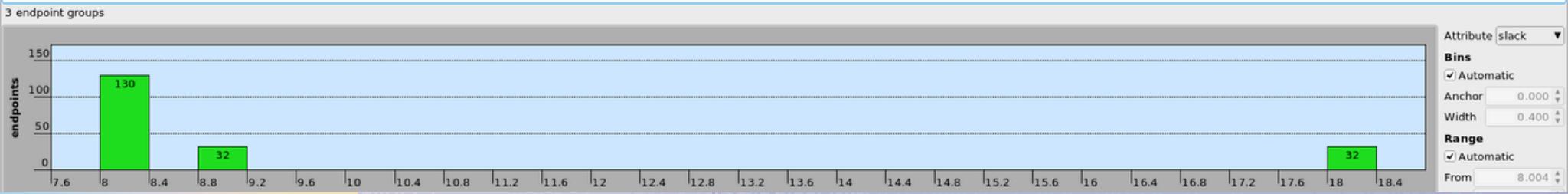


Histogram of Slack Values at Min TLU

default	default	default	**async_default**	setup	131	0	0.000	0.000
default	default	default	clk	setup	194	0	0.000	0.000
default	default	default	clk	hold	162	0	0.000	0.000



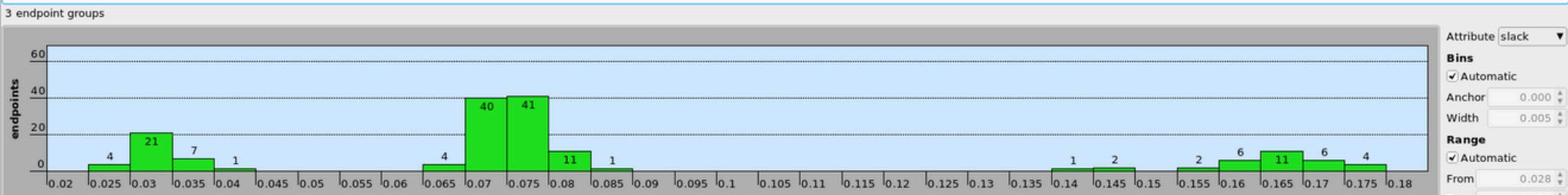
default	default	default	default	clk	setup	194	0	0.000	0.000
default	default	default	default	clk	hold	162	0	0.000	0.000



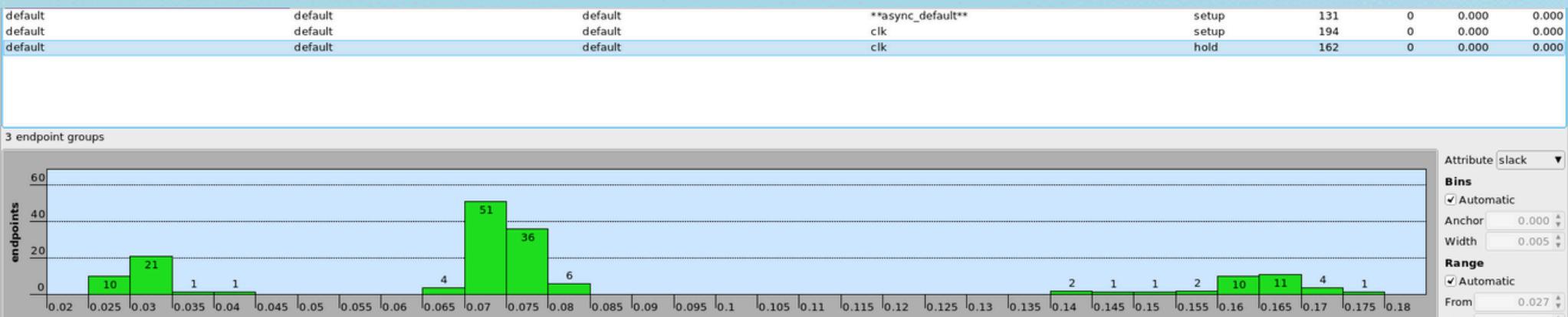
Hold Time Analysis

Histogram of Slack Values at Max TLU

default	default	default	**async_default**	setup	131	0	0.000	0.000
default	default	default	clk	setup	194	0	0.000	0.000
default	default	default	clk	hold	162	0	0.000	0.000



Histogram of Slack Values at Min TLU





Thank you!

