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# Low-power Content Addressable Memory (CAM) USING 9T SRAM Array for Mobile Devices.

Mahmoud Sublabn[1] · Yousef Hammad[2]

## Abstract

We present a circuit-level technique of designing a lower write-power along with variability-resistant 9-MOFTET static random-access memory cell. Our proposed bitcell exhibits lower write-power consumption owing to reduction of activity factor and breakup of feedback path between the cross-coupled inverters during write operation. It exhibits higher read static noise margin compared with standard 6T SRAM cell at minimum-area. These improvements are achieved due to breakup of feedback path during the process of writing a bit on to the storage node. The paper investigates in detail the influence of variation in process related parameters, environmental parameters such as supply voltage and temperature on most of the important design parameters of the bitcell and compares the obtained simulation results with conventional 6-MOSFET. It draws lower power from supply voltage while flipping of stored data during write mode compared with standard 9T SRAM cell iso-area. It also compares key design metrics of LP9T with those of few other 9T SRAM cells found in the literature.

## 1 Introduction

Static random-access memory consumers a vast area of a state-of-the-art microprocessor . In lP SRAM bitcell is used to make level-1 , level-2 and level- 3 caches. Future that is system-on-chip and that is network-on-chip will embed even bigger sized caches for bridging the gap between DRAM speed and the processor speed. The ITRS predicts, that the 90% of processor area will be occupied by cache memory in near future Semiconductor Industry Associa- tion . Dynamic or switching power dissipation in SRAM is the charging/discharging power of bitlines and power consumed by the peripheral circuits such as decoder and sense amplifier. PDYN owing to discharging/charging of bitlines accounts for 60% of the total PDYN because always at least one bitline discharges almost fully per write operation . “1” difficulties without write-assist method. Singh et al. proposed single-ended 6-MOSFET SRAM bitcell, which suffered from longer write time. Singh et al. proposed low-power 6-MOSFET SRAM bitcell could decrease access time and write- power. propose a low-dynamic power 9 transistor SRAM cell . The design metrics of the proposed LP9T are compared with those of standard 6T SRAM cell @ minimum-area for a given cratio and bratio mentioned in the following section. design parameters are also compared with those of standard 8T SRAM bitcell @ iso-area for a given cratio and bratio mentioned in the following section. also compares key design metrics of LP9T with those of other 9T SRAM cells found in the literature. also realizes the proposed bitcell with CNFET. The proposed cell utilizes different access devices for writing and reading and storage nodes are decoupled while reading. We have extensively simulated the LP9T bitcell in SPICE environment and verified the technique proposed in this work. We have used MOSFET’s parameters from 22-nm Predictive Technology Model Nanoscale Integration and Modeling .

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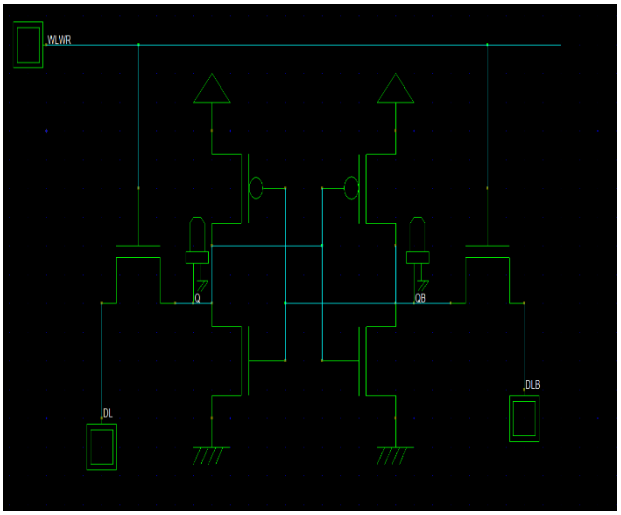



*Figure 1:Low-power 6-Transistor static random-access memory bitcell*

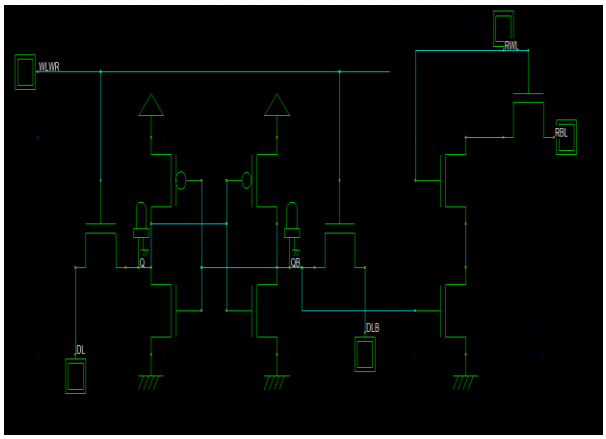



*Figure 2:Low-power 9-Transistor static random-access memory bitcell*

# 2 Literature Review

### 2.1 Content-Addressable Memory System Using a Nanoelectromechanical Memory Switch

Hyunju Kim , et.al [1] proposed a static-based architecture for a low-power, high-speed binary CAM (BCAM) and ternary CAM (TCAM), using a memory switch for non-volatile data storage on a 65 nm process node,to replace random-access memory devices because they are not suitable for high-capacity data processing in big data and artificial intelligence. Content-addressable memory (CAM) compares search data against all data stored in the data array simultaneously in parallel. CAMs have a significantly lower density than SRAMs or DRAMs. In this study, a NEM memory-switch device, utilizing a CMOS back-end-of-the-line (BEOL) process, is applied to a high-speed, low-power CAM device using a commercial65-nm process. By doing so, this study aims to improve the problems that have occurred. owing to the low density of a typical CMOS-based CAM. This study aims to improve the problems that have occurred when implementing high-capacity, low-power CAMs. We propose a CAM single-bit cell and 10 × 10 CAM array structure using a NEM memory switch, which utilizes the CMOS BEOL process. With conventional CMOS-based CAMs, BCAMs and TCAMs must be implemented with the same structure separately. On the other hand, with the NEM-based CAM proposed in this paper, both BCAMs and TCAMs can be implemented with the same structure. This design has up to 23% less propagation delay, three times less matching power, and 9.4 times less area than a conventional design.

# 3 Comparison of previous designs

Figure:2 shows a 1-bit cell 9T SRAM with 9 NMOS transistors. In order to write data into Q and QB. If DL and DLB were set to 1 and 0 respectively. then WLWR was set to 1. And in order to read data we set WLWR=0, RWL=1 and RBL=1 then we check the line between the 2 transistor if the line=1 then the result=1 else the result = 0.
On the other hand 6T Sram has only 6 NMOSs and works exactly like 9t but without RBL ,RWL. Making the read noise margine for 9t sram bigger than 6t but at a cost of a bigger size .

# 3 Proposed solution

## ➢ 3.1 Bit SRAM 9T

Figure:2 shows a 1-bit cell 9T SRAM with 9 NMOS transistors. In order to write data into Q and QB. If DL and DLB were set to 1 and 0 respectively. then WLWR was set to 1. And in order to read data we set WLWR=0, RWL=1 and RBL=1 then we check the line between the 2 transistor if the line=1 then the result=1 else the result = 0.

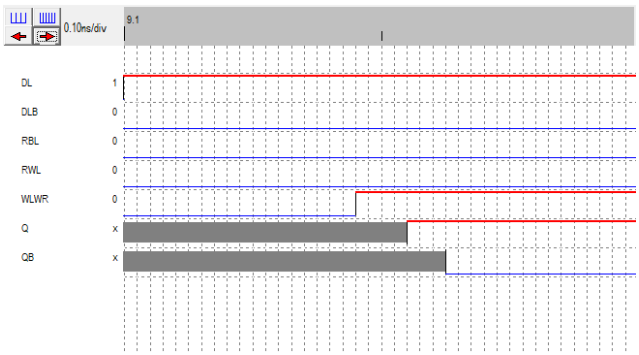
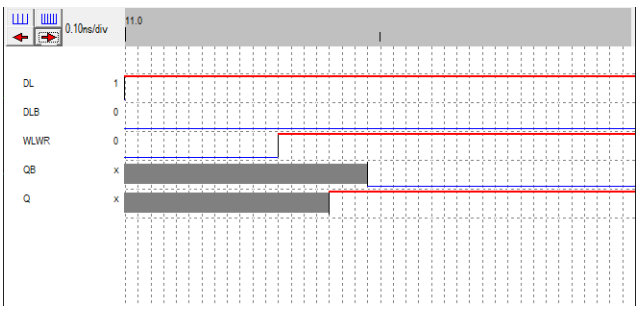



*Figure 3:Simulation of 9T Sram*

Discussion:
As we Q has a delay of 0.4ns to charge QB has a bigger delay because it waits for Q to charge then it will Discharge of0.3ns after Q is fully charged.

## 1 Bit SRAM 6T

As seen in Fig:1 is the 6t Sram with 9 NMOS transistors. In order to write data into Q and QB. If DL and DLB were set to 1 and 0 respectively. then WLWR was set to 1. And in order to read data we set WLWR=0 ,then we check the line between the 2 transistor if the line=1 then the result=1 else the result = 0.



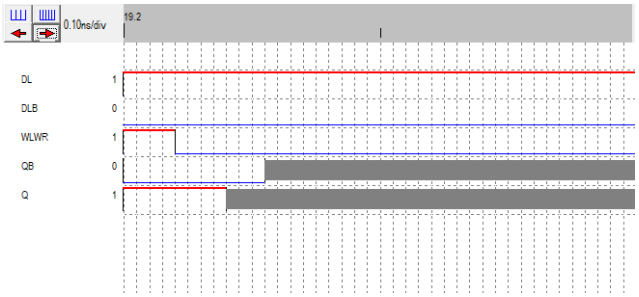




*Figure 4: 6T Simulation*

## ➢ 1 Bit SRAM with Comparison Circuit (1-bitCAM cell)

Figure 3 represents a 1-bit CAM cell, here we used XOR pass-gate to compare between CAM DATA and stored data. CAM cell checks if the match data=1 that means DL doesn't match CAM data. Else there's no difference between them.

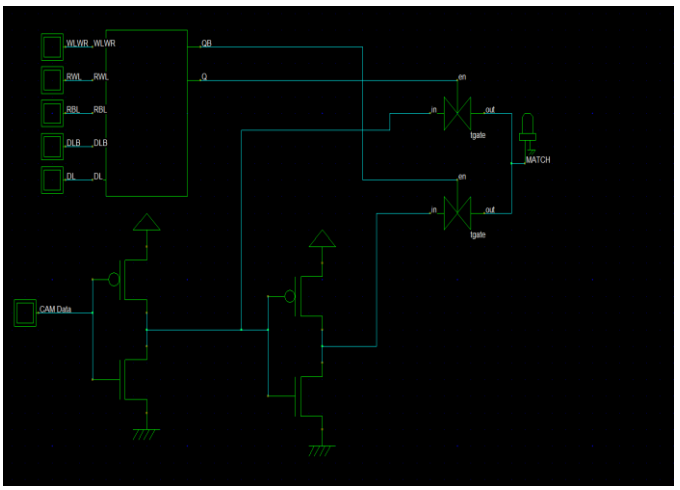



Figure 5: 1 bit cam cell DSCH design

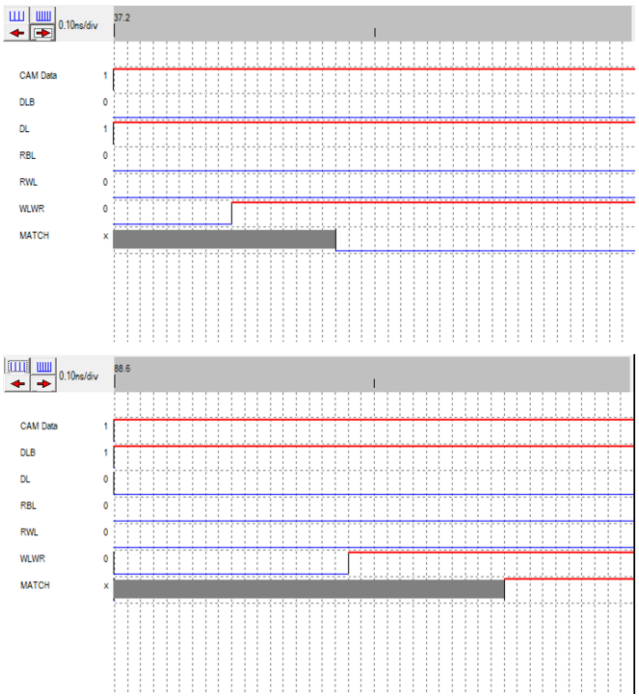



*Figure 6:1bit 9t CAM Cell*

➢ 4 Bit CAM Cell 9T

We used the 1-bit SRAM Comparison circuit from the previous circuit to build 4-bit CAM Cell, as shown in the figure below.

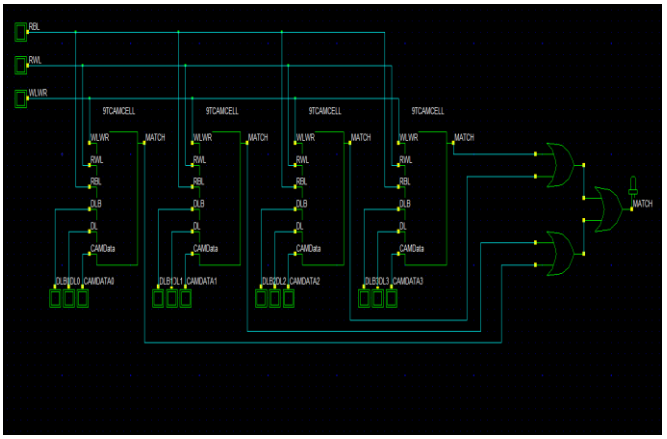



Figure 9: 4-bit cam cell DSCH design

➢ **1 Bit SRAM with Comparison Circuit (1-bitCAM cell)**

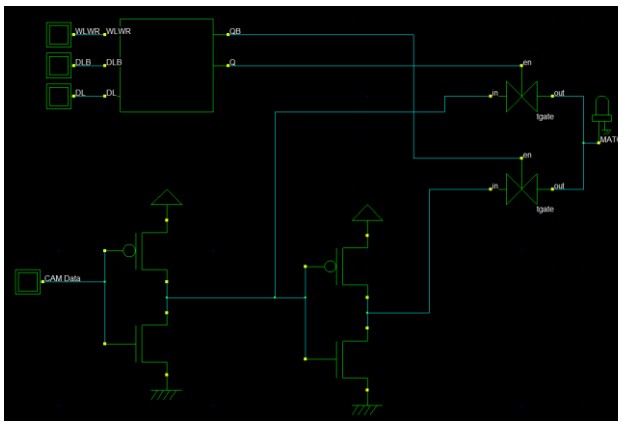



*Figure 7:1Bit Cam cell 6T*

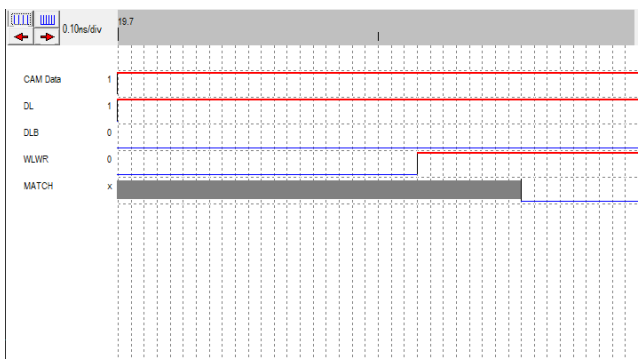



*Figure 8:simulation 1Bit 6t Cam*

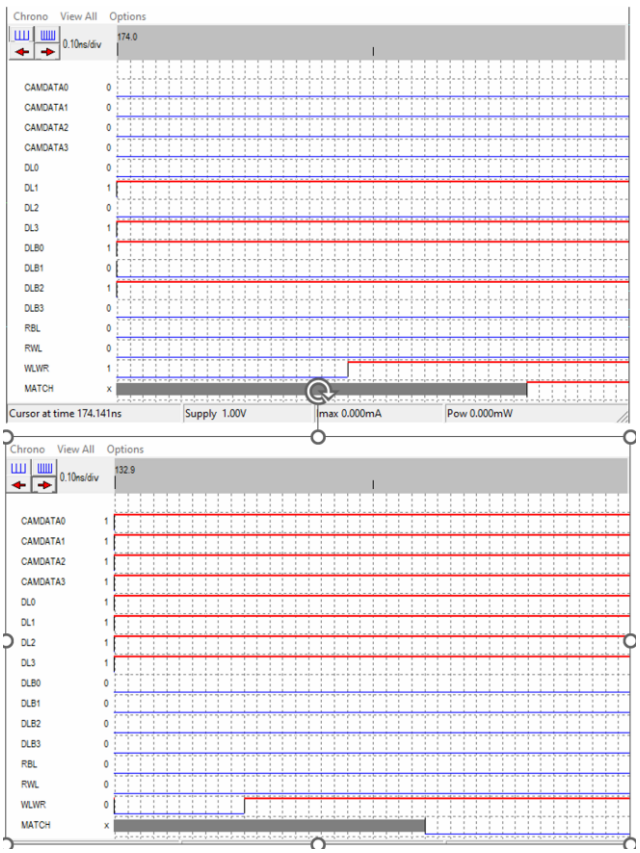



*Figure 10:Simulation 4Bit 9t Cam*

Delay in Charging match is 1.3ns discharge 1.5ns

## 4 Bit CAM Cell 6T

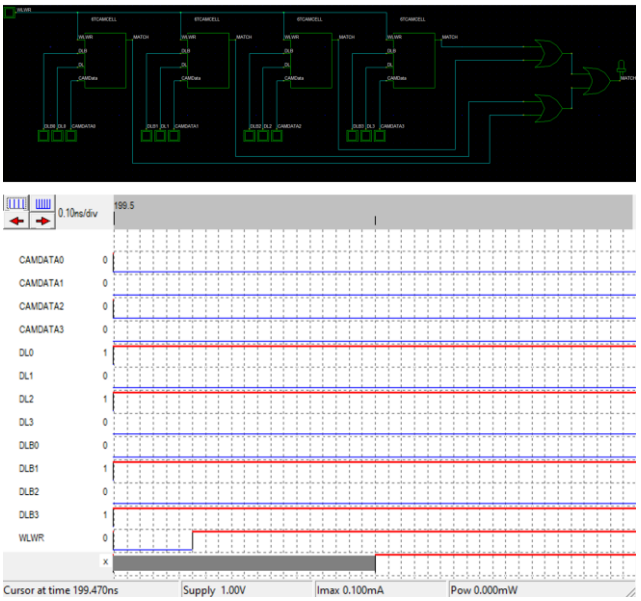



*Figure 11:6T 4 Bit Cam*

Discussion :

The Dealy in Charging the match point is 1.5ns and in dis is 1.8ns so it is higher than the 9t Sram As expected .

## ➢ Decoder

We used inverters and "AND" Gates to design the decoder.

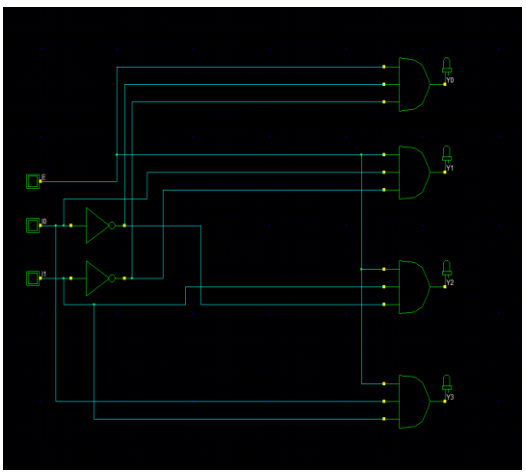


Figure 12: Decoder

## ➢ CAM Memory

We used four "4-bit CAM cells", to build a 4x4 table of data, and a decoder to decide which row to check for equality.

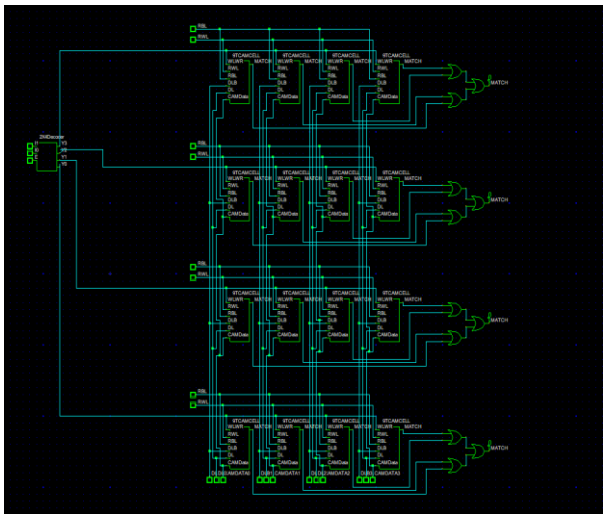


Figure 13: CAM Memory

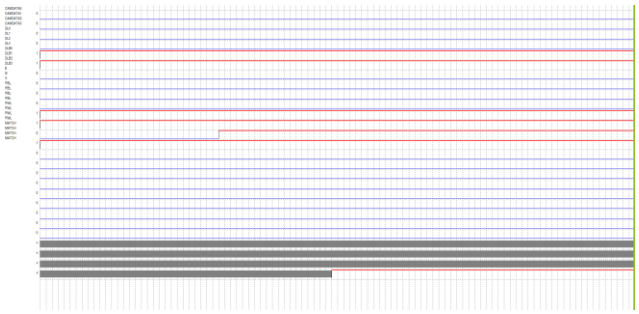


*Figure 14:16 bit 9t Cam Simulation*

## Layouts and

➢ 9T SRAM Layout

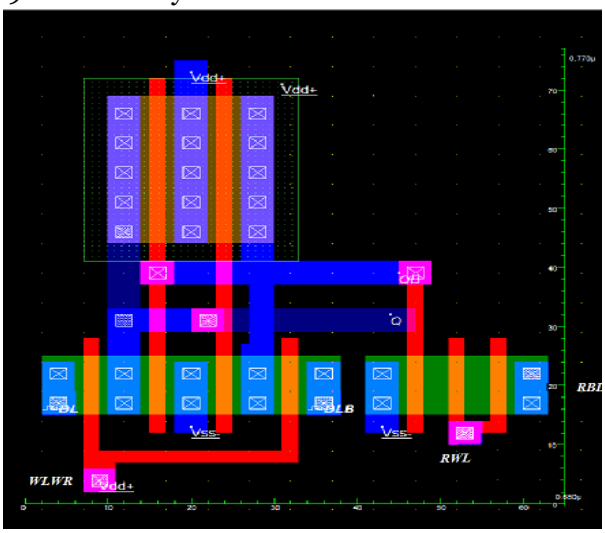



Figure 15: 9T SRAM

- 9T SRAM Simulation

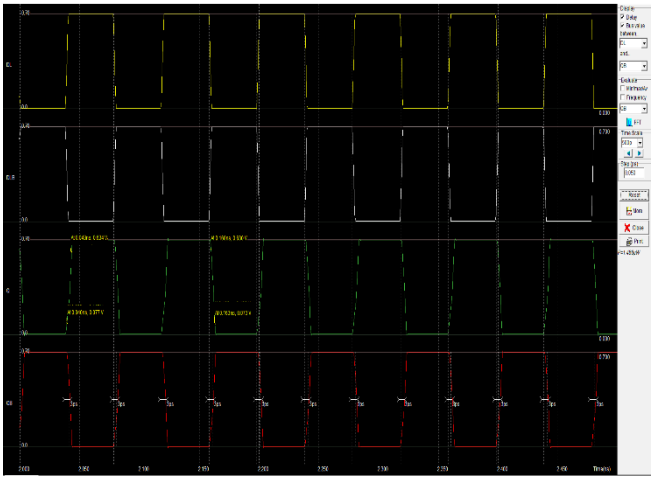


Figure 16: 9T SRAM Simulation

## Discussion:

Rise Time=0.003ns, Fall Time= 0.003ns, delay=3ps, the rise time and fall time were taken on 10% and 90% of the amplitude value.

**The Power Consumption:** switching the 9T SRAM data 12 times costs 1.486uwat then the power needed for 1 switch = 0.124 uwat.

**The Overall Area:** 0.770u * 0.65u.

- 1 bit cell CAM Layout 9T

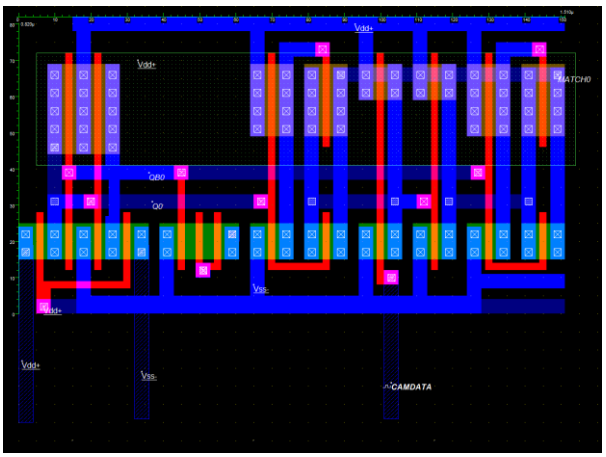


Figure 17: 1 bit cell CAM Layout

- 1 bit CAM cell Simulation

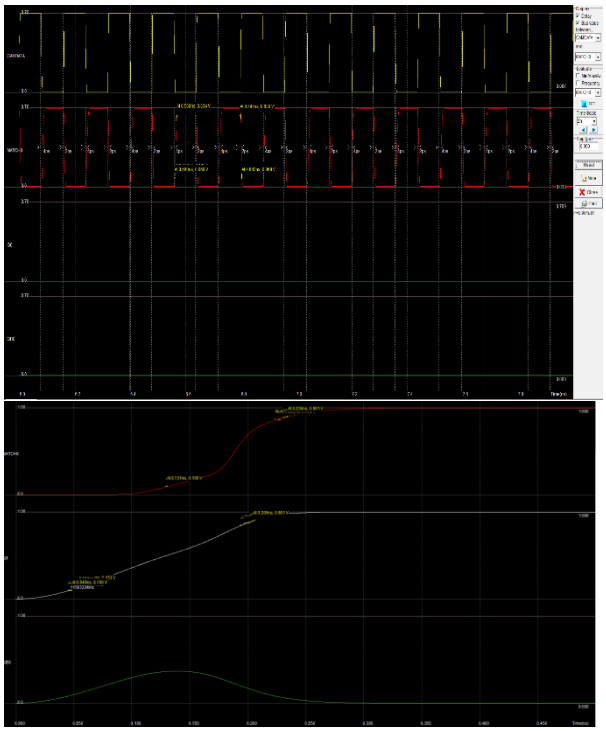


Figure 18: 1 bit CAM cell Simulation

## Discussion:

Rise Time = 0.008ns and Fall Time=0.006ns, delay = 4ps for the rise and 2ps for the fall.

**The Power Consumption:** switching the CAM data of the 9T CAM cell only effects the XOR passing circuit which means the power consumption will only be on the XOR. Switching the CAM data 25 times costs 0.981 uwat which means switching the CAM data once only costs 0.03924 uwat.

**The Overall Area:** 0.866u * 1.554u. (by adding 2 lambda to the top button left and right).

- 4 bit CAM Layout

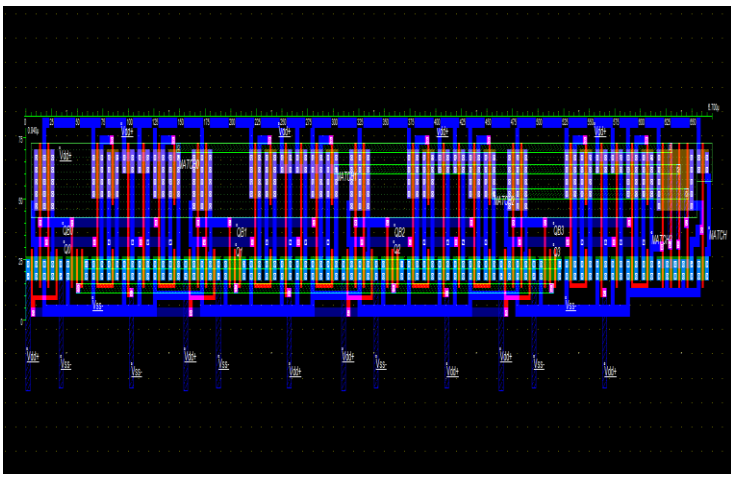
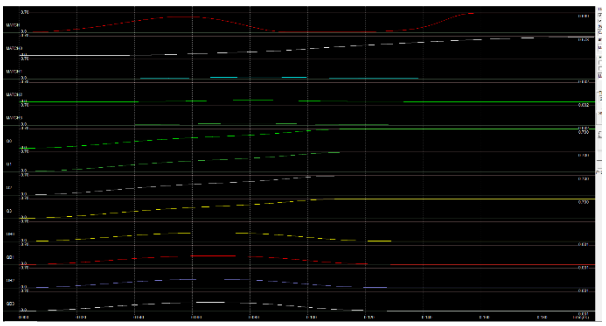


Figure 19: 4bit CAM Layout

## Discussion:

**The Power Consumption**: 1 switch costs 21.166 uwat.
**The Area**: 0.84*6.7

- 4 bit CAM Simulation Mismatch



4 bit CAM Simulation Match

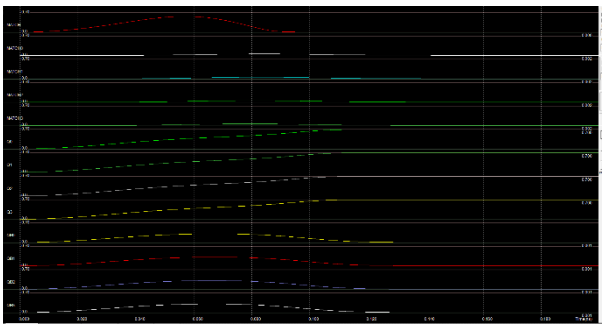


Figure 21: 4bit CAM Simulation Match

**Discussion:** when all the CAM data match all the data on the CAM's gets the match of all the row=0.

1Bit Cam Cell 6T

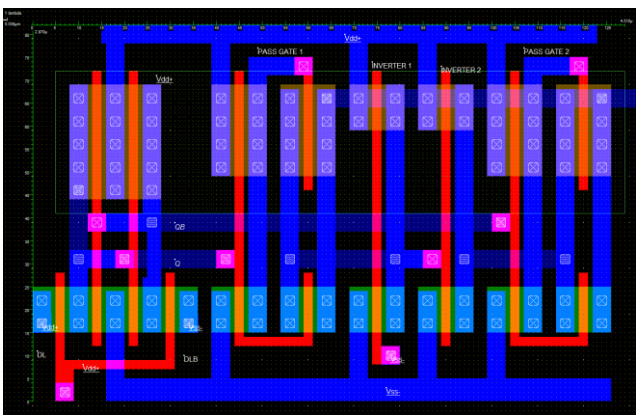



*Figure 22:1Bit Cam 6T*

Figure 20 4bit CAM Simulation Mismatch

**Discussion:** when one of the CAM data doesn't match the data on one of the CAM's gets the match of all the row=1.

## 1 Conclusion

In this work we propose a lower dynamic power and variation-resistant 9-transistor static random-access mem- ory bitcell. It reduces write power by decreasing activity factor. It studies the effect of variation in process, supply voltage and temperature on read time. Our simulation results exhibit significant improvement in important design parameters static random-access memory cell. We have

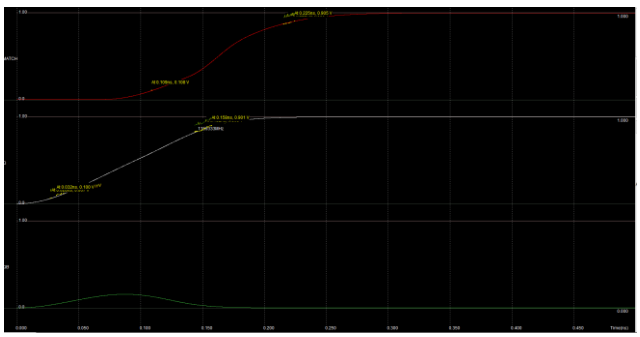


*Figure 23:Simulation 1bit Cam 6T*

References

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[5]: Different Types of RAM (Random Access Memory), geeks for geeks_