



CPCS-211

Digital Logic Design (10%)

Xerox machine

CS3 - Dr. Asaad Ahmed – CPCS-211

Student:

Mahmued Alardawi - 2135209

- Submission Date: 19/11/2022

Table of content

Input specification	4
Determination of System components	5
Determination of truth tables, state/characteristic tables, characteristic equations	6
4-bit 7-segment encoder	6
Truth table	6
4-bit 7-segment decoders	7
Truth table	7
4-bit comparator.....	8
Truth table	8
K-maps	8
2x1 multiplexer	9
Truth table	9
1x2 demultiplexer	9
Truth table	9
JK flip flop	10
Truth table	10
Characteristic table	10
Excitation table	10
K-maps	10
4x4 bit multiplier.....	11
Costume 2-digit 7-segment display encoders	11
Truth table	11
K-maps	11
Implementation of state diagrams, time tracing, timing diagrams	13
Implementation for the 3-bit KJ flip flop counter	13
State table.....	13

K-maps	13
State diagram.....	14
Time trace	14
Timing table	15
Output Specification	16
CONCLUSION	17
References	18

Input specification

- On/Off switch.
- 32-bit password inputted as 8 decimal numbers.
- Inputting 1 or 2 for both printing properties.
- Number of copies wanted.

Determination of System components

- (4) 1-bit input switches.
- (9) 4-bit 7-segment encoders.
- (8) 4-bit 7-segment decoders.
- (9) 4-bit comparators.
- (2) 2x1 multiplexer.
- (2) 1x2 demultiplexer.
- (3) JK flip flops.
- (1) Clock.
- 4x4 bit multiplier.
- Costume 2-digit 7-segment display encoders.

Determination of truth tables, state/characteristic tables, characteristic equations

4-bit 7-segment encoder

Truth table

N	a	b	c	d	e	f	g	b3	b2	b1	b0
0	1	1	1	1	1	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	1
2	1	1	0	1	1	0	1	0	0	1	0
3	1	1	1	1	0	0	1	0	0	1	1
4	0	1	1	0	0	1	1	0	1	0	0
5	1	0	1	1	0	1	1	0	1	0	1
6	1	0	1	1	1	1	1	0	1	1	0
7	1	1	1	0	0	0	0	0	1	1	1
8	1	1	1	1	1	1	1	1	0	0	0
9	1	1	1	1	0	1	1	1	0	0	1
10	x	x	x	x	x	x	x	x	x	x	x
11	x	x	x	x	x	x	x	x	x	x	x
12	x	x	x	x	x	x	x	x	x	x	x
13	x	x	x	x	x	x	x	x	x	x	x
14	x	x	x	x	x	x	x	x	x	x	x
15	x	x	x	x	x	x	x	x	x	x	x

4-bit 7-segment decoders

Truth table

N	b3	b2	b1	b0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	x	x	x	x	x	x	x	x	x	x	x
11	x	x	x	x	x	x	x	x	x	x	x
12	x	x	x	x	x	x	x	x	x	x	x
13	x	x	x	x	x	x	x	x	x	x	x
14	x	x	x	x	x	x	x	x	x	x	x
15	x	x	x	x	x	x	x	x	x	x	x

4-bit comparator

Truth table

A1	A0	B1	B0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

The truth should be for 4x4 comparator bit but doing that table will take 256 rows so I will do the truth table of 2x2 bit comparator.

K-maps

A>B	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

A=B	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

A<B	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

$$A > B = A1B1' + A0B1'B0' + A1A0B0'$$

$$A = B = (A1 (+) B1) (A0 (+) B0)$$

$$A < B = A1'B1 + A1'A0'B0 + A0'B1B0$$

2x1 multiplexer

Truth table

S	Y
0	I_0
1	I_1

1x2 demultiplexer

Truth table

S	Y0	Y1
0	1	0
1	0	1

JK flip flop

Truth table

CIK	J	K	Q _{n+1}
0	x	x	Q _n
1	0	0	Q _n
1	0	1	0
1	1	0	1
1	1	1	Q _n '

Characteristic table

Q _n	J	K	Q _{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation table

Q _n	Q _{n+1}	J	K
0	0	0	X
0	1	1	x
1	0	X	1
1	1	x	0

K-maps

J	0	1
0	0	1
1	x	x

$$J = Q_{n+1}$$

K	0	1
0	x	x
1	1	0

$$K = Q_n' + 1$$

Q _{n+1}	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$$Q_{n+1} = Q_n'J + Q_nK'$$

4x4 bit multiplier

Is not included in the lectures but I used it. 🧐

Costume 2-digit 7-segment display encoders

Truth table

Hex	A	B	C	D	d1	a1	b1	c1	d1	e1	f1	g1	d2	a2	b2	c2	d2	e2	f2	g2	N
00	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	00
01	0	0	0	1	0	1	1	1	1	1	1	0	1	0	1	1	0	0	0	0	01
02	0	0	1	0	0	1	1	1	1	1	1	0	2	1	1	0	1	1	0	1	02
03	0	0	1	1	0	1	1	1	1	1	1	0	3	1	1	1	1	0	0	1	03
04	0	1	0	0	0	1	1	1	1	1	1	0	4	0	1	1	0	0	1	1	04
05	0	1	0	1	0	1	1	1	1	1	1	0	5	1	0	1	1	0	1	1	05
06	0	1	1	0	0	1	1	1	1	1	1	0	6	1	0	1	1	1	1	1	06
07	0	1	1	1	0	1	1	1	1	1	1	0	7	1	1	1	0	0	0	0	07
08	1	0	0	0	0	1	1	1	1	1	1	0	8	1	1	1	1	1	1	1	08
09	1	0	0	1	0	1	1	1	1	1	1	0	9	1	1	1	1	0	1	1	09
10	1	0	1	0	1	0	1	1	0	0	0	0	0	1	1	1	1	1	1	0	10
11	1	0	1	1	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	11
12	1	1	0	0	1	0	1	1	0	0	0	0	2	1	1	0	1	1	0	1	12
13	1	1	0	1	1	0	1	1	0	0	0	0	3	1	1	1	1	0	0	1	13
14	1	1	1	0	1	0	1	1	0	0	0	0	4	0	1	1	0	0	1	1	14
15	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	15

K-maps

a1	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	x	0
10	1	1	0	0

$$a1 = A' + AB'C'$$

b1	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	x	1
10	1	1	1	1

$$b1 = A' + A$$

c1	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	x	1
10	1	1	1	1

$$c1 = A' + A$$

d1	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	x	0
10	1	1	0	0

$$d1 = A' + AB'C'$$

e1	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	x	0
10	1	1	0	0

$$e1 = A' + AB'C'$$

f1	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	x	0
10	1	1	0	0

$$f1 = A' + AB'C'$$

g1	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	x	0
10	0	0	0	0

$$g1 = 0$$

a2	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	1	1	x	0
10	1	1	0	1

$$a2 = AC' + A'C + BD + B'D'$$

b2	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	1	1	x	1
10	1	1	1	1

$$b2 = A'B' + A + C'D' + CD$$

c2	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	0	1	x	1
10	1	1	1	1

$$c2 = A'C' + CD + A'B + AB' + BC + AD$$

d2	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	1	1	x	0
10	1	1	0	1

$$d2 = A'B'C + AC' + BC'D + A'CD' + B'D'$$

e2	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	1	0	x	0
10	1	0	0	1

$$e2 = AC'D' + A'CD' + B'D'$$

f2	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	0	0	x	1
10	1	1	0	1

$$f2 = A'C'D' + AB'C' + BCD' + A'BC' + AB'D'$$

g2	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	1	1	x	1
10	1	1	0	0

$$g2 = BC' + A'B'C + BCD' + AC'$$

Implementation of state diagrams, time tracing, timing diagrams

Implementation for the 3-bit KJ flip flop counter

State table

A	B	C	A*	B*	C*	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	0	0	0	x	1	x	1	x	1

K-maps

J _A	00	01	11	10
0	0	0	1	0
1	x	x	x	x

$$J_A = BC$$

K _A	00	01	11	10
0	x	x	x	x
1	0	0	1	0

$$K_A = BC$$

J _B	00	01	11	10
0	0	1	x	x
1	0	1	x	x

$$J_B = C$$

K _B	00	01	11	10
0	x	x	1	0
1	x	x	1	0

$$K_B = C$$

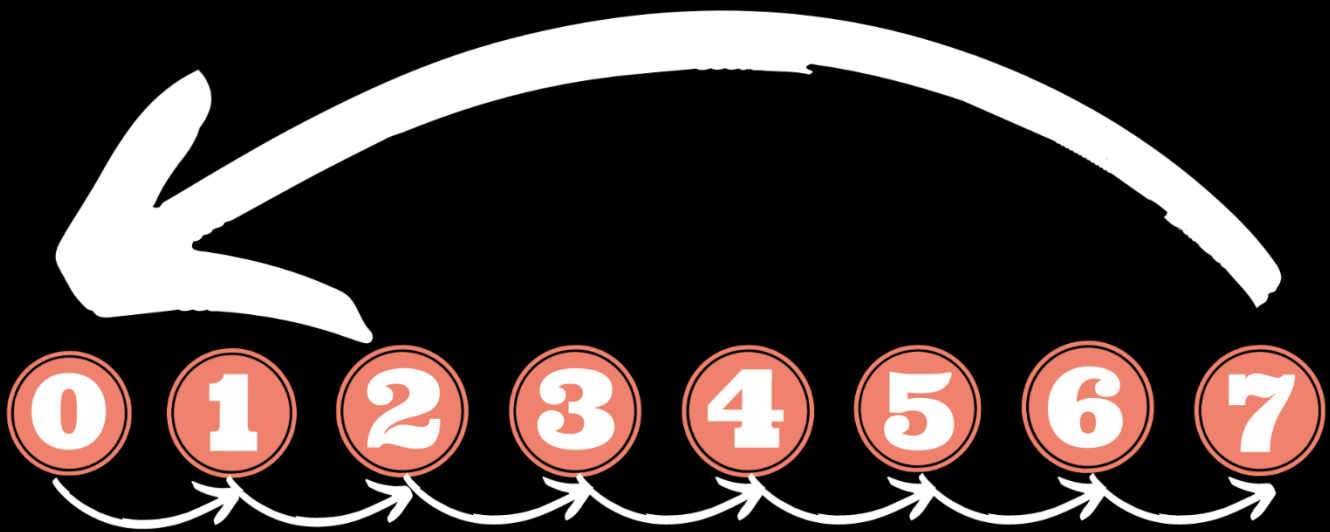
J _C	00	01	11	10
0	1	x	x	1
1	1	x	x	1

$$J_C = 1$$

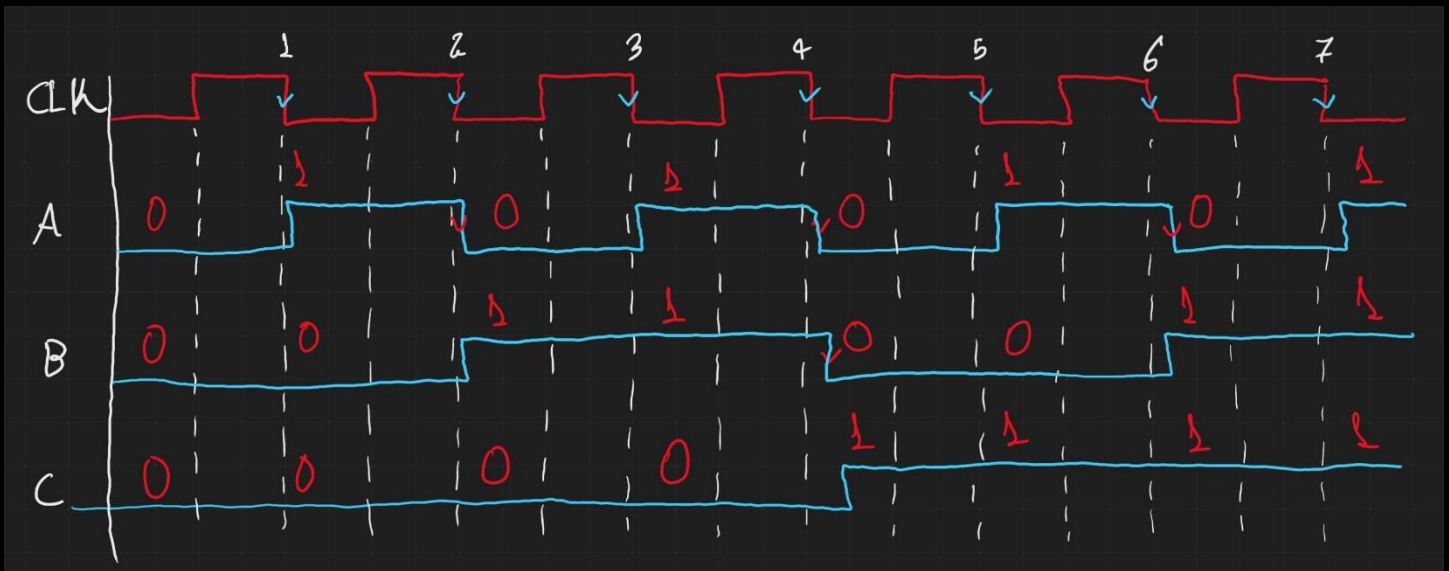
k _C	00	01	11	10
0	x	1	1	x
1	x	1	1	x

$$K_C = 1$$

State diagram



Time trace



Timing table

Clock	C	B	A	Decimal Eq
Initially	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7

Output Specification

- LED lamps
- (8) 4-bit 7-segment decoders.
- Costume 2-digit 7-segment display encoders.

CONCLUSION

From this project I learnt a lot about combinational and sequential circuits and how to implement what I studies in real life. I will harness that new experience to something great In Shaa Allah.

Extra: there might be malfunction in the 2-digit 7-segment display and due to the shortage of time I was not unable to fix it so sorry for that. 😊

References

- https://youtu.be/s1DSZEaCX_g (Neso Academy)