ECE 506/ section 001 – Machine Problem 2 report

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1. Varying Cache Size: 256KB, 512KB, 1MB, 2MB for each protocol

Varying Cache Size: 256KB, 512KB, 1MB, 2MB

Associativity: 8

Block size: 64B

Numer of processors: 4

Protocol: MSI, MESI, Dragon

Trace file: canneal.04t.longTrace

The following table is the running average results (11 requested statistics) of 4 processor caches when using different cache coherency protocol under varying cache size in each protocol.

MSI	256KB	512KB	1MB	2MB
01. number of reads	112964.25	112964.25	112964.25	112964.25
02. number of read misses	5791	5775.25	5768.75	5767.25
03. number of writes	12035.75	12035.75	12035.75	12035.75
04. number of write misses	40.25	40.25	40.25	40.25
05. total miss rate	4.67%	4.65%	4.65%	4.65%
06. number of writebacks	250.25	184	167	159.25
07. number of cache-to-cache transfers	0	0	0	0
08. number of memory transactions	6755	6673	6649.5	6640.25
09. number of interventions	64.75	65.75	66.25	66.25
10. number of invalidations	2019	2019	2019	2019
11. number of flushes	103.25	104.25	104.75	104.75

Table 1. MSI smp average results under Varying Cache Size

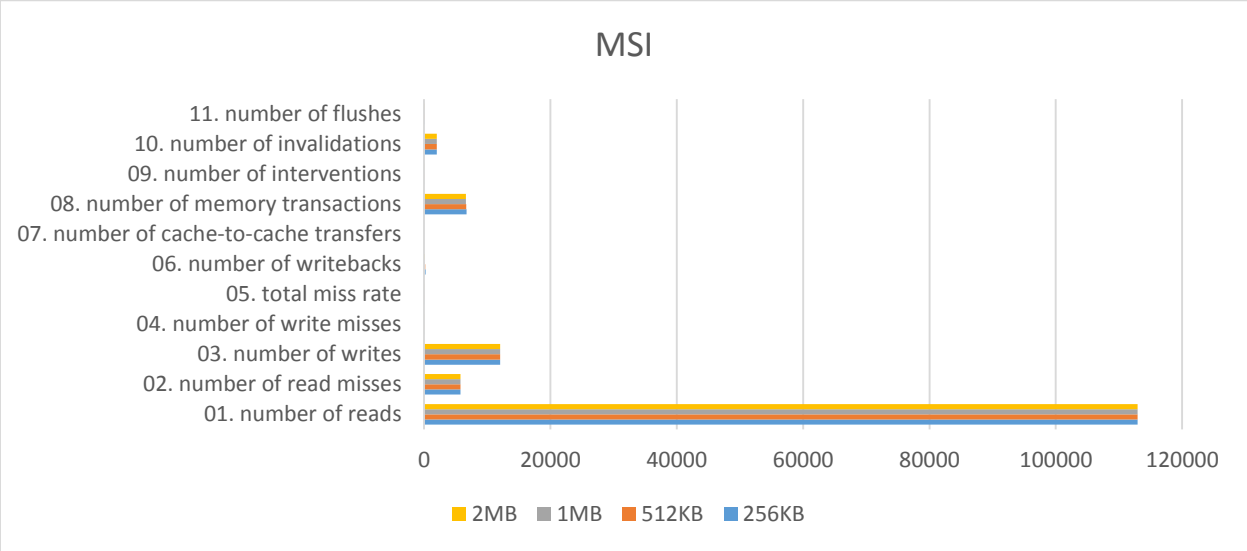
MESI	256KB	512KB	1MB	2MB
01. number of reads	112964.25	112964.25	112964.25	112964.25
02. number of read misses	5791	5775.25	5768.75	5767.25
03. number of writes	12035.75	12035.75	12035.75	12035.75
04. number of write misses	40.25	40.25	40.25	40.25
05. total miss rate	4.67%	4.65%	4.65%	4.65%
06. number of writebacks	250.25	184	167	159.25
07. number of cache-to-cache transfers	4415.75	4404.75	4399.75	4398.25
08. number of memory transactions	1665.75	1594.75	1576.25	1568.5
09. number of interventions	1462	1458.5	1457.5	1457.5
10. number of invalidations	2019	2019	2019	2019
11. number of flushes	103.25	104.25	104.75	104.75

Table 2. MESI smp average results under Varying Cache Size

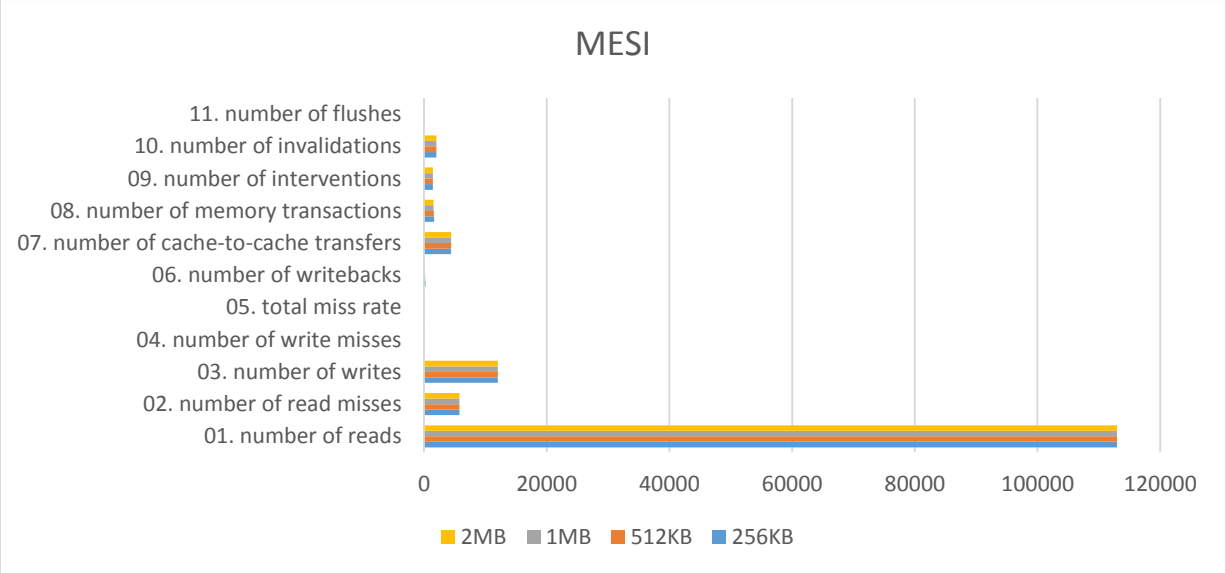
Dragon	256KB	512KB	1MB	2MB
01. number of reads	112964.25	112964.25	112964.25	112964.25
02. number of read misses	5644.25	5609.5	5603.5	5600.75
03. number of writes	12035.75	12035.75	12035.75	12035.75
04. number of write misses	1.75	1.75	1.75	1.75
05. total miss rate	4.52%	4.49%	4.48%	4.48%
06. number of writebacks	24050.00%	13875.00%	11725.00%	11250.00%
07. number of cache-to-cache transfers	0	0	0	0
08. number of memory transactions	5886.5	5750	5722.5	5715
09. number of interventions	1407.25	1398.75	1397.25	1396.5
10. number of invalidations	0	0	0	0
11. number of flushes	6.75	6	6	6

Table 3. Dragon smp average results under Varying Cache Size

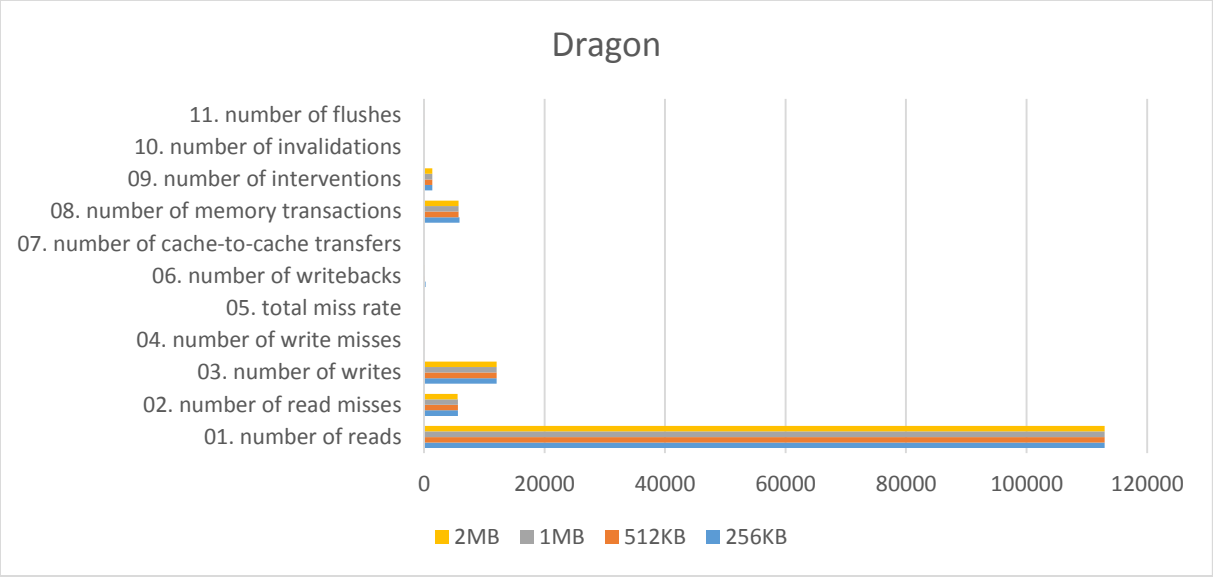
According the above result, I draw the bar graph for the average cache results in three Protocols (MSI, MESI, Dragon) under Varying Cache Size. The three bar graphs are as following:



Graph 1. MSI average cache results under Varying Cache Size



Graph 2. MESI average cache results under Varying Cache Size



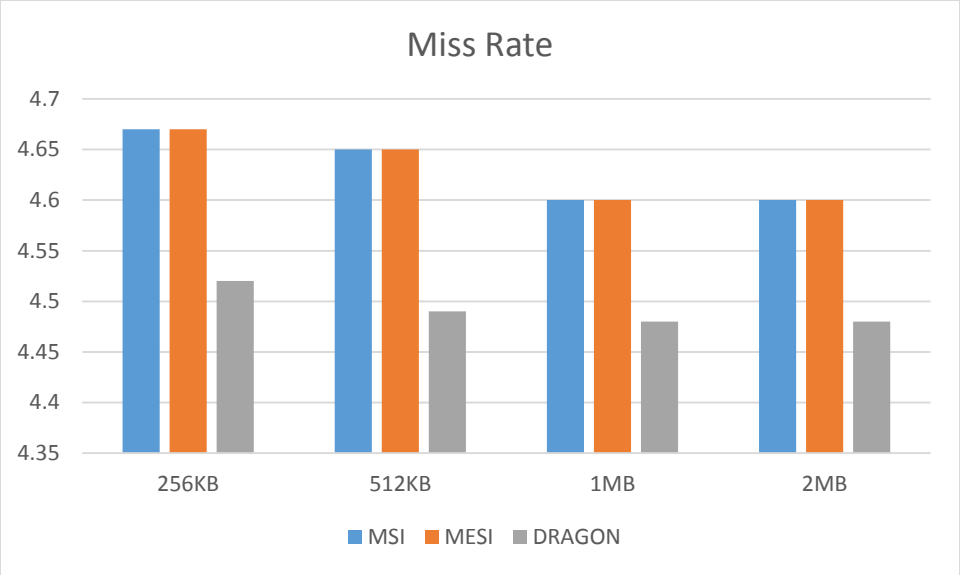
Graph 3. Dragon average cache results under Varying Cache Size

Effect of Change in Cache Size on Cache Miss Rate:

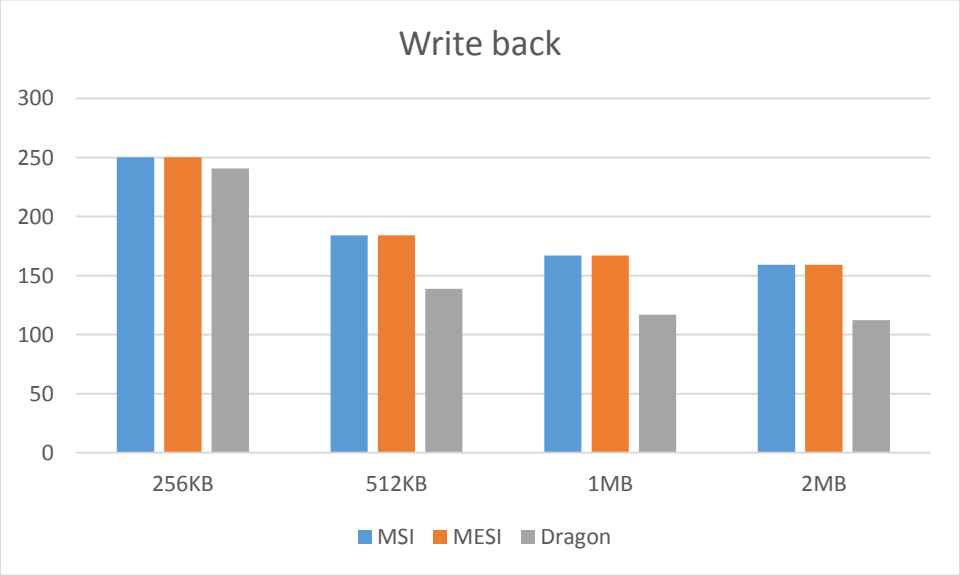
As the three graph showing above, we can get that the most obvious changed statistics is the number of write backs and the miss rates. There is obvious decrease of them with the increasing cache size. There are two bar graphs for the number of write backs and the miss rates. For better analysis and chart plotting, we take an average of the Miss Rate on all the four caches.

Average	**256KB**	**512KB**	**1MB**	**2MB**
MSI	4.67	4.65	4.60	4.60
MESI	4.67	4.65	4.60	4.60
DRAGON	4.52	4.49	4.48	4.48

Table 4. Miss rate under Varying Cache Size



Graph 4. Miss rate under Varying Cache Size



Graph 5. Number of write backs under Varying Cache Size

The reason for this decrease of misses is that the capacity of cache would be increased if we increase the cache size. So the cache capacity miss would be decreased if the capacity of cache increases. That is the reason of why the miss rates would be decreased.
The reason for this decrease of write backs is that the evicting probability of one block will be decreased when the cache size increasing. So we can see clearly that the number of write backs will decrease quickly when the cache size increases.

Totally, as cache size increases, the miss rate decreases to a minimum value as the number of capacity misses are reduced. The rest of the misses are compulsory misses.
Dragon protocol shows better performance in terms of misses as compared to MSI and MESI.

2. Varying Cache Associativity: 4,8,16 for each protocol

Cache Size: 1MB

Associativity: 4,8,16

Block size: 64B

Num_processors:4

Protocol: for each protocol, such as MSI, MESI, Dragon

Trace file: canneal.04t.longTrace

The following table is the running average results (11 requested statistics) of 4 processor caches when using different cache coherency protocol under varying cache associativity in each protocol.

MSI	4	8	16
01. number of reads	112964.25	112964.25	112964.25
02. number of read misses	5782.5	5768.75	5758.5
03. number of writes	12035.75	12035.75	12035.75
04. number of write misses	40.25	40.25	40.25
05. total miss rate	4.66%	4.65%	4.64%
06. number of writebacks	228.25	167	112.25
07. number of cache-to-cache transfers	0	0	0
08. number of memory transactions	6724.5	6649.5	6584.5
09. number of interventions	65	66.25	66.5
10. number of invalidations	2019	2019	2019
11. number of flushes	103.5	104.75	105

Table 5. MSI smp average results under Varying Cache Associativity

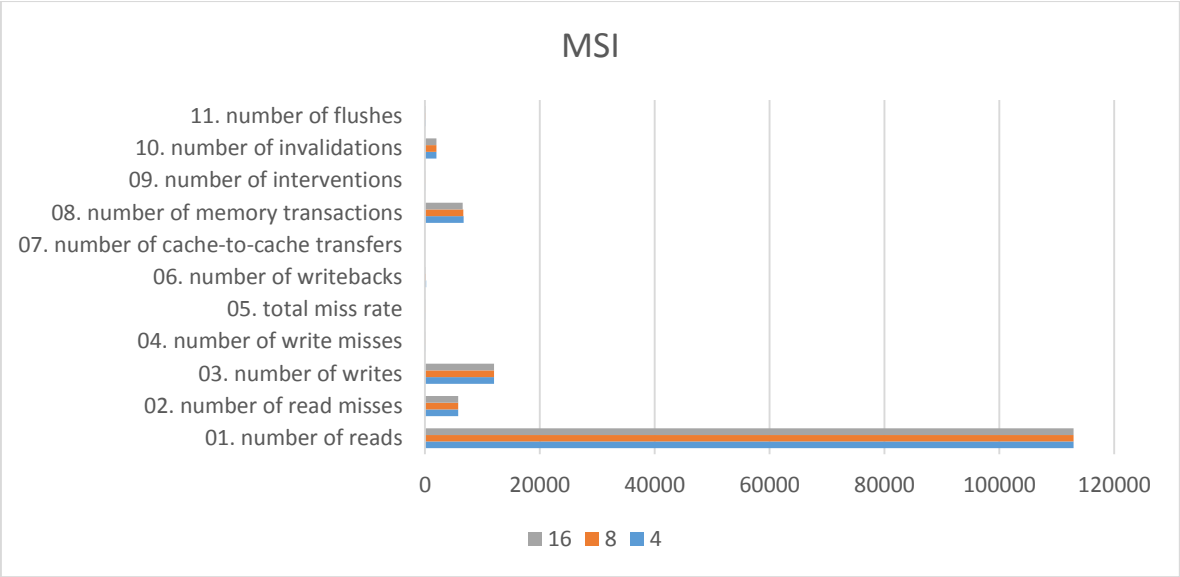
MESI	4	8	16
01. number of reads	112964.25	112964.25	111937.25
02. number of read misses	5782.5	5768.75	5766.25
03. number of writes	12035.75	12035.75	11867.5
04. number of write misses	40.25	40.25	40
05. total miss rate	4.66%	4.65%	4.69%
06. number of writebacks	228.25	167	105
07. number of cache-to-cache transfers	105	4399.75	4398.75
08. number of memory transactions	1641.5	1576.25	1512.5
09. number of interventions	1460.25	1457.5	1447
10. number of invalidations	2019	2019	2025.5
11. number of flushes	103.5	104.75	97.75

Table 6. MESI smp average results under Varying Cache Associativity

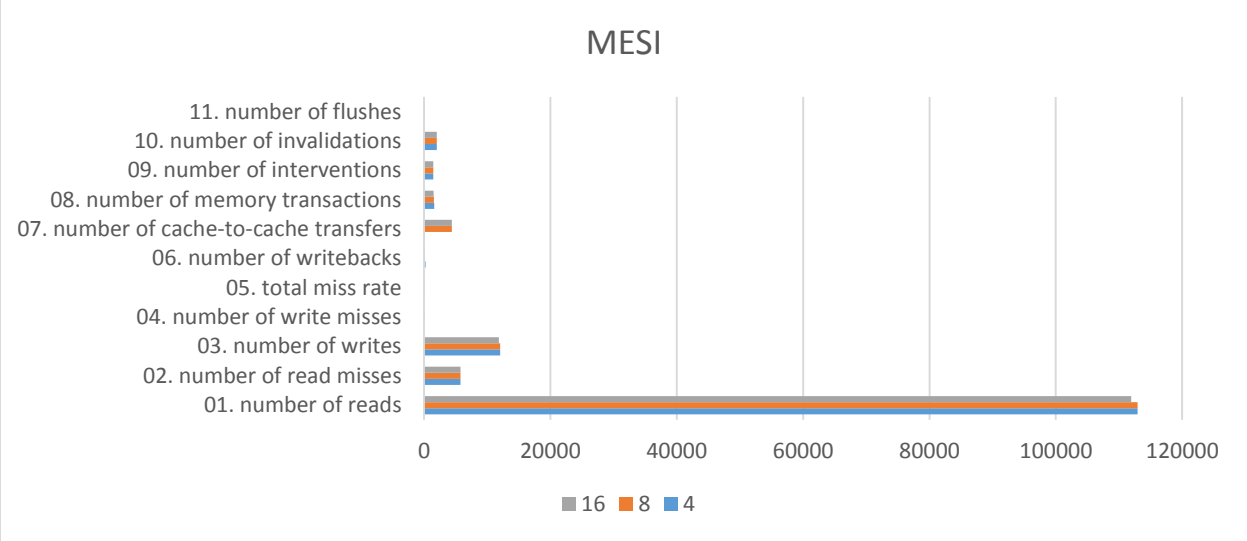
Dragon	4	8	16
01. number of reads	112964.25	112964.25	112964.25
02. number of read misses	5618.25	5603.5	5585.25
03. number of writes	12035.75	12035.75	12035.75
04. number of write misses	1.75	1.75	1.75
05. total miss rate	4.50%	4.48%	4.47%
06. number of writebacks	155.25	117.25	58.25
07. number of cache-to-cache transfers	0	0	0
08. number of memory transactions	5775.25	5722.5	5645.25
09. number of interventions	1401	1397.25	1392.75
10. number of invalidations	0	0	0
11. number of flushes	6	6	6

Table 7. Dragon smp average results under Varying Cache Associativity

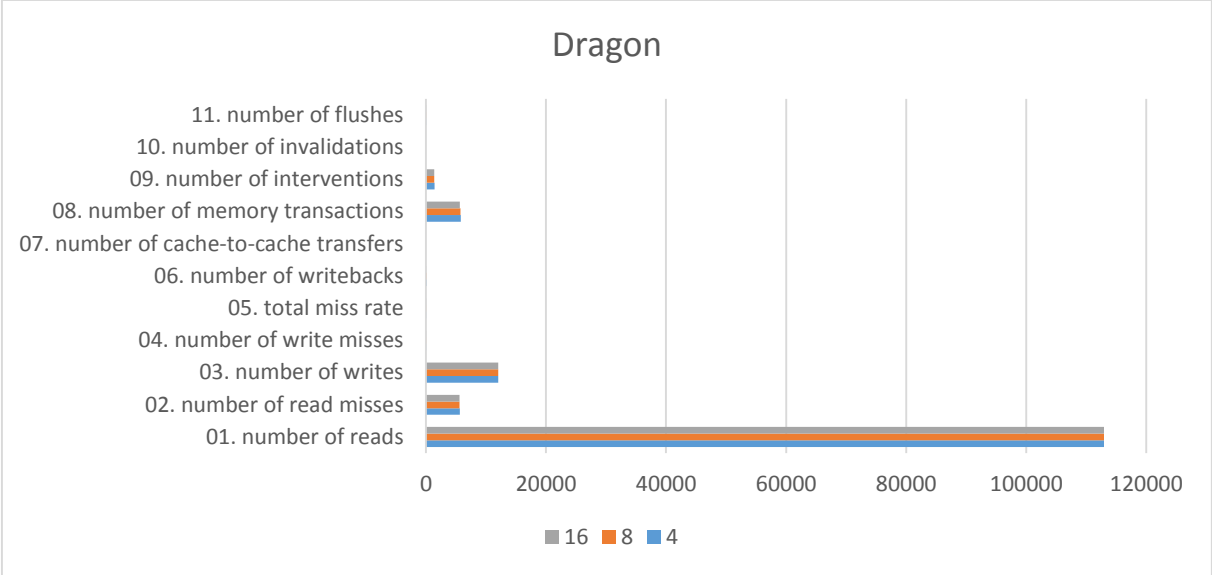
According the above result, I draw the bar graph for the average caches result in three Protocols (MSI, MESI, Dragon) under Varying Cache Associativity. The three bar graphs are as following:



Graph 6. MSI average cache results under Varying Cache Associativity



Graph 7. MESI average cache results under Varying Cache Associativity



Graph 8. Drogan average cache results under Varying Cache Associativity

Effect of Change in Associativity on Cache Miss Rate:

For better analysis and chart plotting, we take an average of the Miss Rate on all the three associativities. As the three graphs showing above, we can get that the most obvious changed statistics is the number of write backs and the miss rates. There is obvious decrease of them with the increasing cache associativity. There are two bar graphs for the number of write backs and the miss rates.

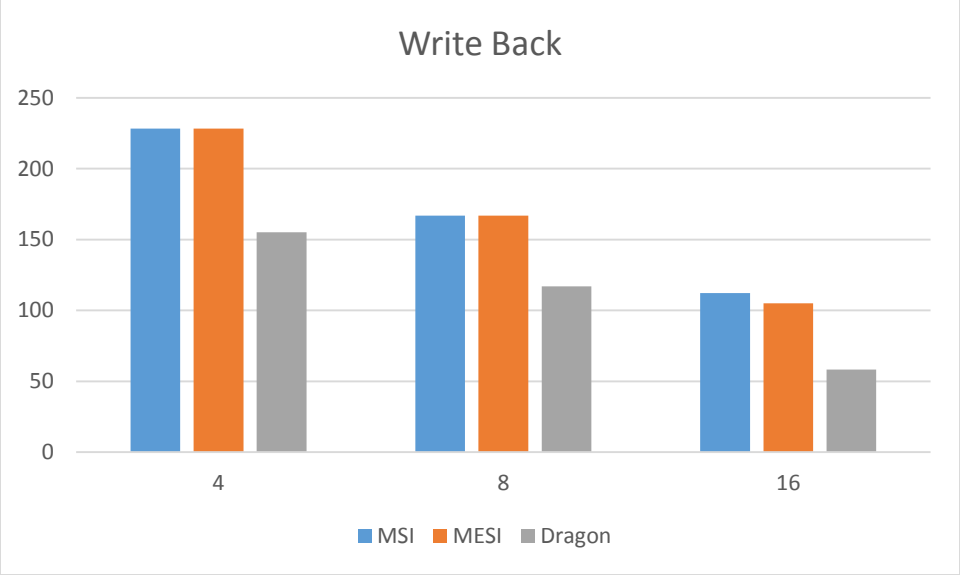
The cache conflict miss would be decreased if the associativity of cache increases. So the read and write miss number will decrease if the cache conflict miss is decreased.

That is the reason of why the read and write misses would be decreased. The reason for this decrease of write backs is that the evicting probability of one block will be decreased when the cache associativity increasing. So we can see clearly that the number of write backs will decrease quickly when the cache associativity increases.

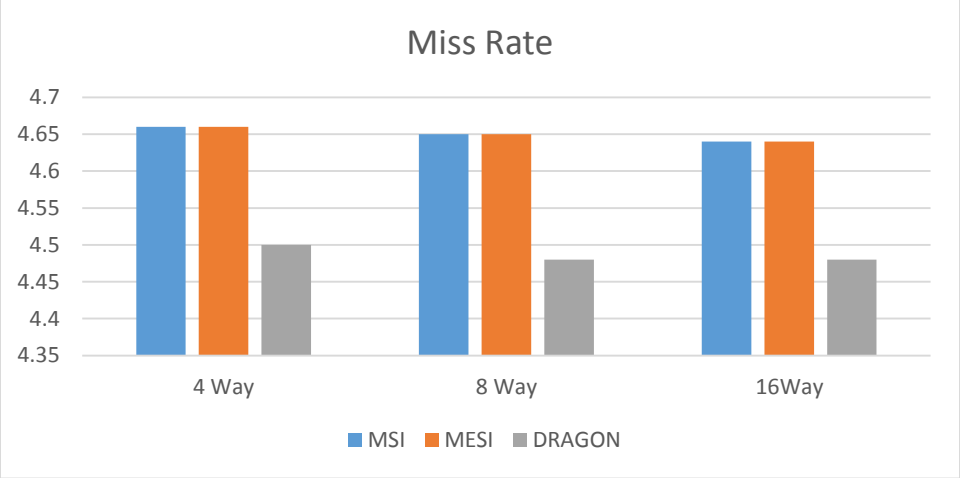
Average	**4 Way**	**8 Way**	**16Way**
MSI	4.66	4.65	4.64
MESI	4.66	4.65	4.64
DRAGON	4.5	4.48	4.48

Table 8. Miss rate under Varying Cache Associativity

Totally, as associativity increases, the miss rate decreases as the number of conflict misses are reduced. The capacity & compulsory misses remain constant.
Dragon protocol shows better performance in terms of misses as compared to MSI and MESI.



Graph 9. Number of write backs under Varying Cache Associativity



Graph 10. Miss Rate under Varying Cache Associativity

3. Varying Block Size: 64B, 128B, 256B for each protocol

Cache Size: 1MB

Associativity: 8

Block size: 64B, 128B, 256B

Number of processors: 4

Protocol: MSI, MESI, Dragon

Trace file: canneal.04t.longTrace

The following table is the running average results (11 requested statistics) of 4 processor caches when using different cache coherency protocol under varying block size in each protocol.

MSI	64KB	128KB	256KB
01. number of reads	112964.25	112964.25	112964.25
02. number of read misses	5768.75	5362.75	5045.25
03. number of writes	12035.75	12035.75	12035.75
04. number of write misses	40.25	40	40
05. total miss rate	4.65%	4.33%	4.07%
06. number of writebacks	167	269.25	355
07. number of cache-to-cache transfers	0	0	0
08. number of memory transactions	6649.5	6361.5	6152.5
09. number of interventions	66.25	110	159
10. number of invalidations	2019	2069	2136
11. number of flushes	104.75	148.5	197.5

Table 9. MSI smp average results under Varying Block Size

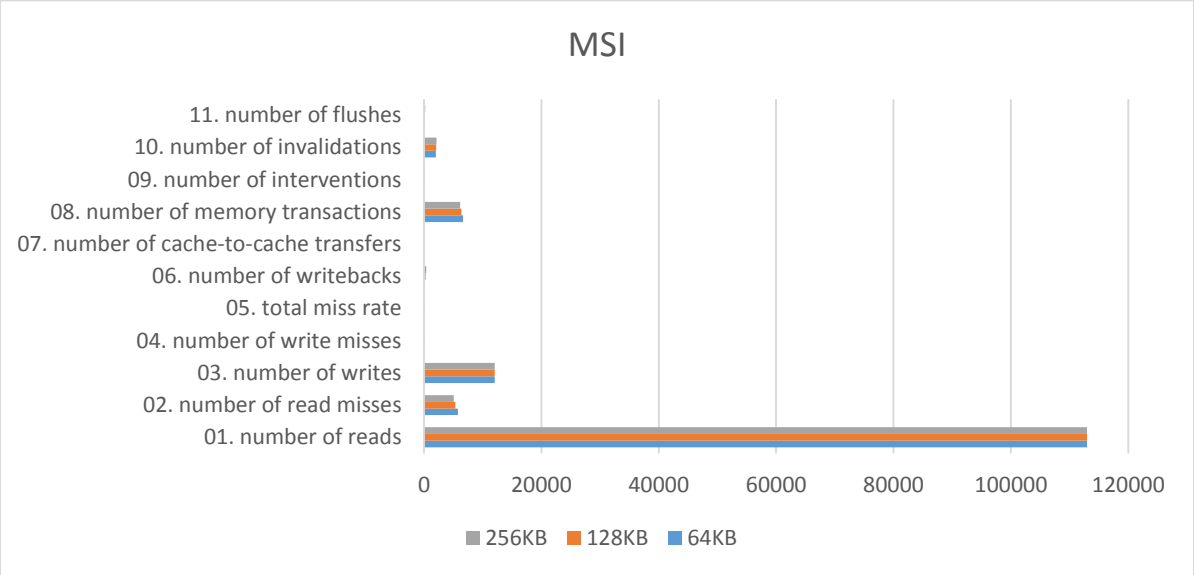
MESI	64KB	128KB	256KB
01. number of reads	112964.25	112964.25	112964.25
02. number of read misses	5768.75	5362.75	5045.25
03. number of writes	12035.75	12035.75	12035.75
04. number of write misses	40.25	40	40
05. total miss rate	4.65%	4.33%	4.07%
06. number of writebacks	167	269.25	355
07. number of cache-to-cache transfers	4399.75	4129.75	3930.75
08. number of memory transactions	1576.25	1542.25	1509.5
09. number of interventions	1457.5	1366.5	1299.25
10. number of invalidations	2019	2069	2136
11. number of flushes	104.75	148.5	197.5

Table 10. MESI smp average results under Varying Block Size

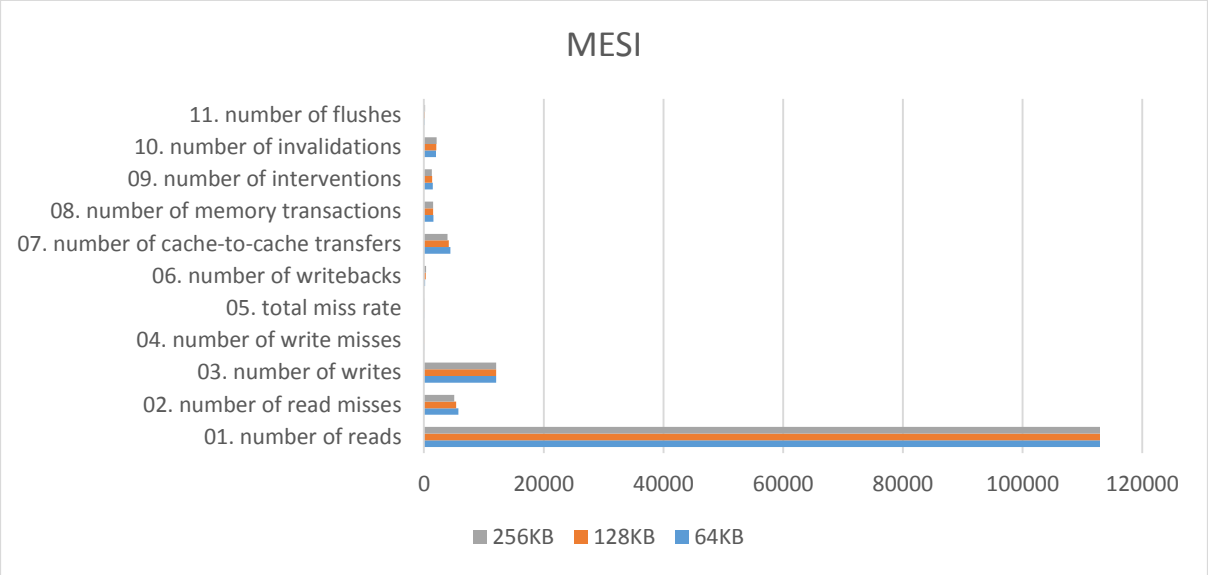
Dragon	64KB	128KB	256KB
01. number of reads	112964.25	112964.25	112964.25
02. number of read misses	5603.5	5078.75	4632.75
03. number of writes	12035.75	12035.75	12035.75
04. number of write misses	1.75	1.5	1.5
05. total miss rate	4.48%	4.07%	3.71%
06. number of writebacks	117.25	156.5	202.75
07. number of cache-to-cache transfers	0	0	0
08. number of memory transactions	5722.5	5236.75	4837
09. number of interventions	1397.25	1266.5	1154.75
10. number of invalidations	0	0	0
11. number of flushes	6	6.75	8

Table 11. Dragon smp average results under Varying Block Size

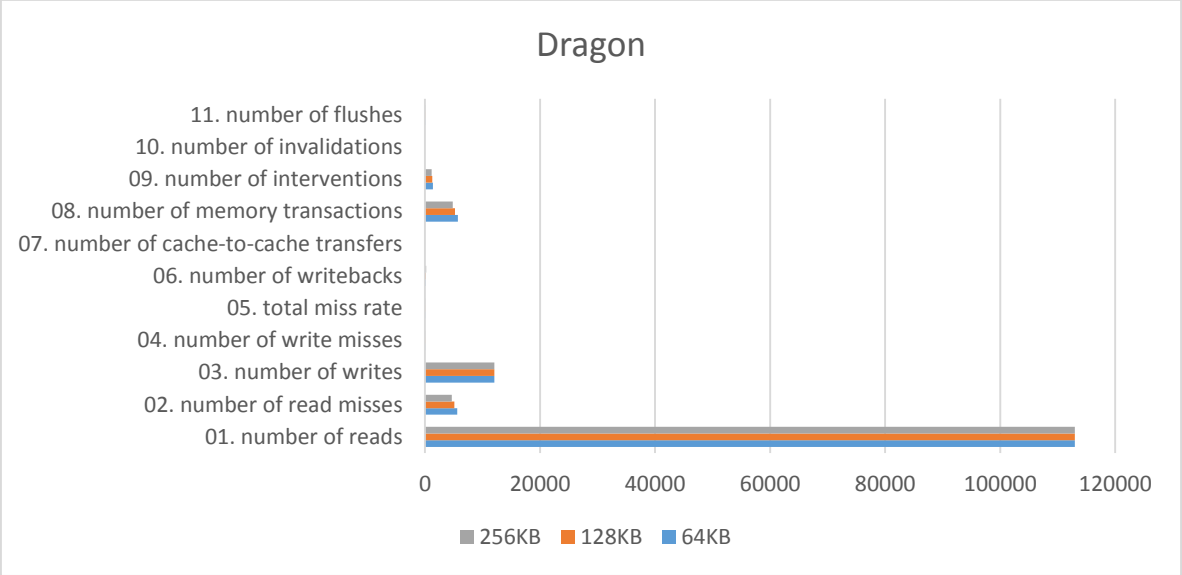
According the above result, I draw the bar graph for the average caches result in three Protocols (MSI, MESI, Dragon) under Varying Block Size.. The three bar graphs are as following:



Graph 11. MSI average cache results under Varying Block Size



Graph 12. MESI average cache results under Varying Block Size



Graph 13. Dragon average cache results under Varying Block Size

Effect of Change in Block Size on Cache Miss Rate:

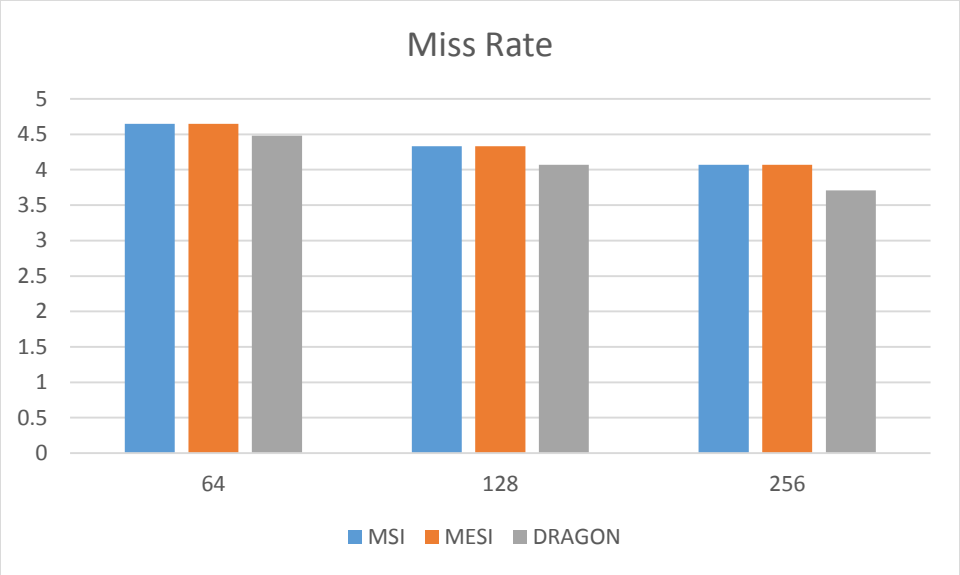
For better analysis and chart plotting, we take an average of the Miss Rate on all the three block sizes. As the six graphs showing above, we can get that the most obvious changed statistics is the number of write misses and the number of read miss. There is obvious decrease of them with the increasing block size. There is a bar graph for the miss rates as following. When the processor firstly access one data, there will be a miss in cache. This cache miss is called cache compulsory miss. The cache compulsory miss would be decreased if the block size of cache increases. So the read miss number and write misses number will decrease if the cache compulsory miss is decreased. That is the reason of why the read misses and write misses would be decreased.

Average	**64**	**128**	**256**
MSI	4.65	4.33	4.07
MESI	4.65	4.33	4.07
DRAGON	4.48	4.07	3.71

Table 12. Miss rate under Varying Cache Block Size

As block size increases, the miss rate decreases as the number of compulsory misses are reduced. This is due to the fact that increasing block size helps enable more available space for spatial locality. It should be noted that this available space can be exploited to a certain point after which it may cause cache pollution.

Dragon protocol shows better performance in terms of misses as compared to MSI and MESI.



Graph 14. Miss Rates under Varying Cache Block Size

4. Varying coherency protocol: MSI, MESI, Dragon discussion

Cache Size: 1MB

Associativity: 8

Block size: 64B

Num_processors: 4

Protocol: for each protocol, such as MSI, MESI, Dragon

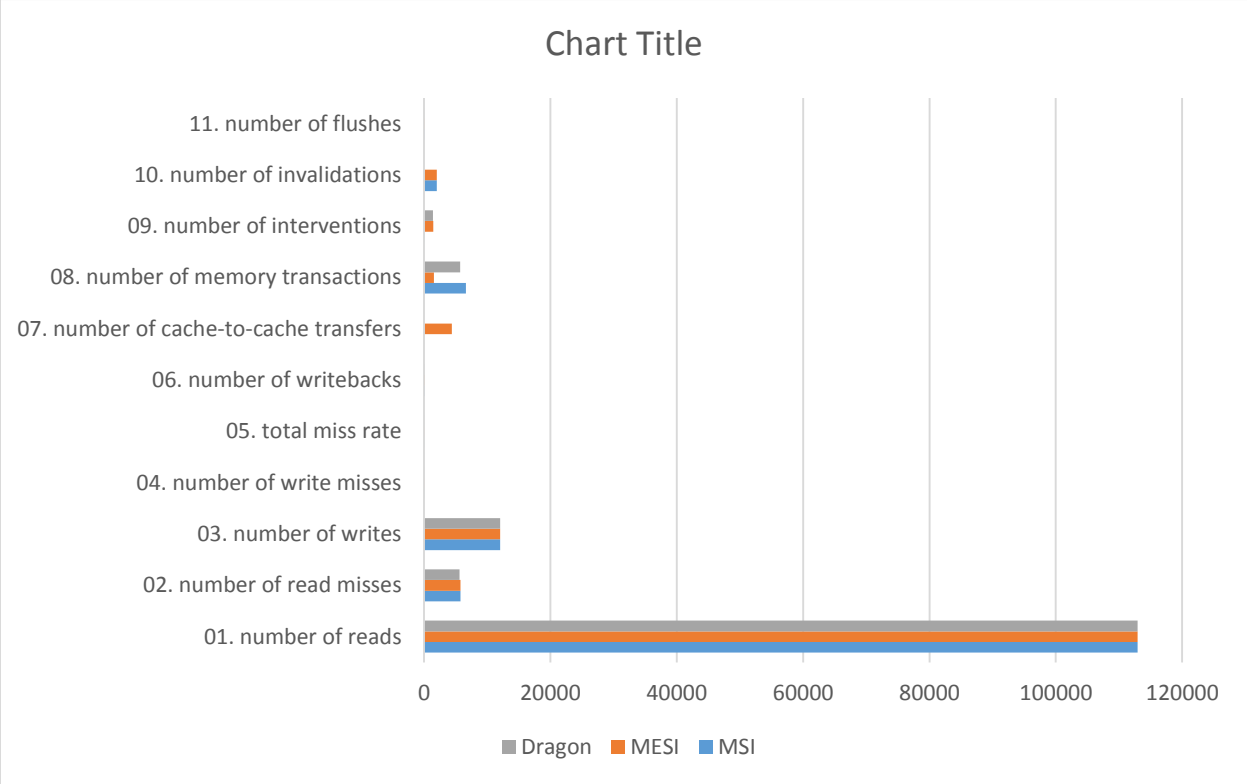
Trace file: canneal.04t.longTrace

The following table is the total running result of all cache when using the three protocols.

Cache size= 1MB, assoc 8, block_size=64			
	MSI	MESI	Dragon
01. number of reads	112964.25	112964.25	112964.25
02. number of read misses	5768.75	5768.75	5603.5
03. number of writes	12035.75	12035.75	12035.75
04. number of write misses	40.25	40.25	1.75
05. total miss rate	4.65%	4.65%	4.48%
06. number of writebacks	167	167	117
07. number of cache-to-cache transfers	0	4399.75	0
08. number of memory transactions	6649.5	1576.25	5722.25
09. number of interventions	66.25	1457.5	1397.25
10. number of invalidations	2019	2019	0
11. number of flushes	104.75	104.75	6

Table 13. The average of all cache results under different protocols for a single configuration

According the above result, I draw the bar graph for the average result in three Protocols (MSI, MESI, Dragon). The three bar graphs are as following:



Graph 15. The average of all cache results under different protocols for a single configuration

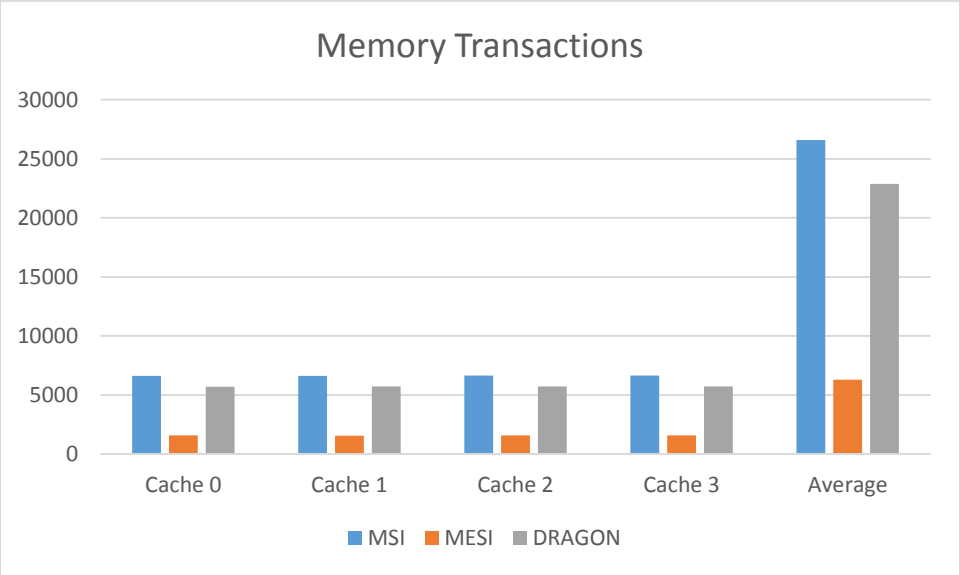
As the bar graph showing above, we can get that the most obvious changed statistics are the number of memory transactions and the number of flushes.
We can clearly see that MESI will get the most number of cache to cache transfers. And the MSI and Dragon get the least number of cache to cache transfers. That is because the processor always need to access memory to get data. However, in the MESI, the data always come from the other cache instead of memory. So the number of cache to cache transfers will increase in MESI protocol.
Also we can see that on average miss rate in Dragon is the least and in the MSI and MESI protocols are the same.

Effect of Coherence Protocol on Memory Transactions:

We can clearly see that MSI will get the most number of memory transactions. And the MESI gets the least number of memory transactions.

	Cache 0	Cache 1	Cache 2	Cache 3	Average
MSI	6638	6636	6663	6661	26598
MESI	1572	1555	1587	1591	6305
DRAGON	5708	5725	5717	5740	22890

Table 14. Number of Memory transaction under Varying Coherent Protocol



Graph 16. Number of Memory transaction under Varying Coherent Protocol

Since MESI exploits redundant bus transactions irrespective of the location of the stored block, it has least number of memory transactions.

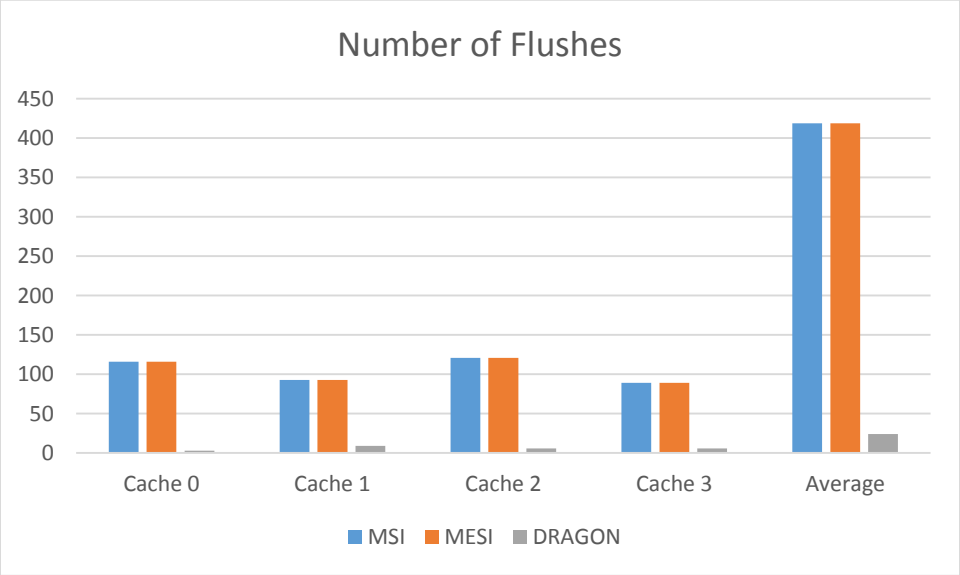
As observed in the first three test cases, Dragon protocol has less miss rate that MSI and hence it has less memory transactions than MSI.

Since Dragon protocol's implementation tries to keep all caches and memory updated with the most recent value it causes heavy bus traffic and hence high number of memory transactions.

Effect of Coherence Protocol on Flushes:

	Cache 0	Cache 1	Cache 2	Cache 3	Average
MSI	116	93	121	89	419
MESI	116	93	121	89	419
DRAGON	3	9	6	6	24

Table 15. Number of Flushes under Varying Coherent Protocol



Graph 17. Number of Flushes under Varying Coherent Protocol

We can also find that the Dragon gets the least number of flushes and the number of flushes MSI and MESI protocols are equal. Theoretically, the Dragon decrease the flush number comparing to MESI and MSI.