NC State University

Department of Electrical and Computer Engineering

ECE 463/521: Fall 2014

Project #1: Cache Design, Memory Hierarchy Design

by

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Project #1 Part2 .. Created 10/9/14.

9.1.1 Explore the effect of following parameters on overall performance of cache

1. L1 Cache size vs. miss rate (For different associativities) [Without L2]
2. Associativity vs. miss rate

L1 cache exploration: SIZE and ASSOC

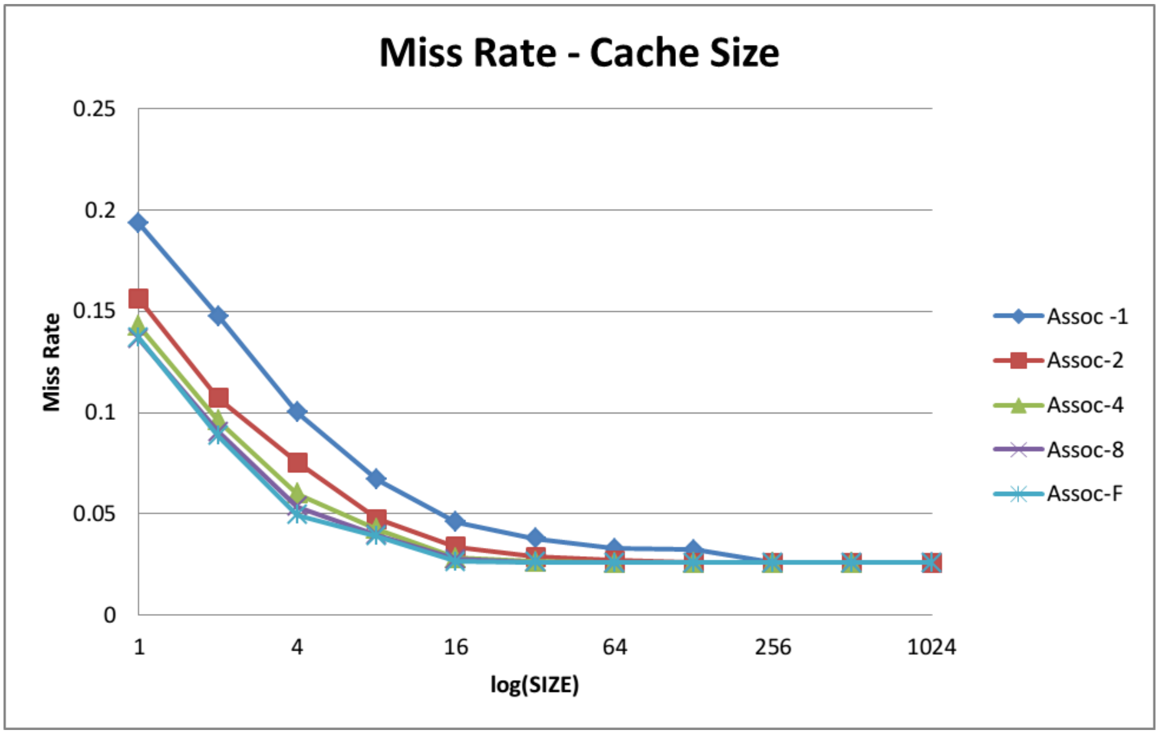


Figure 1

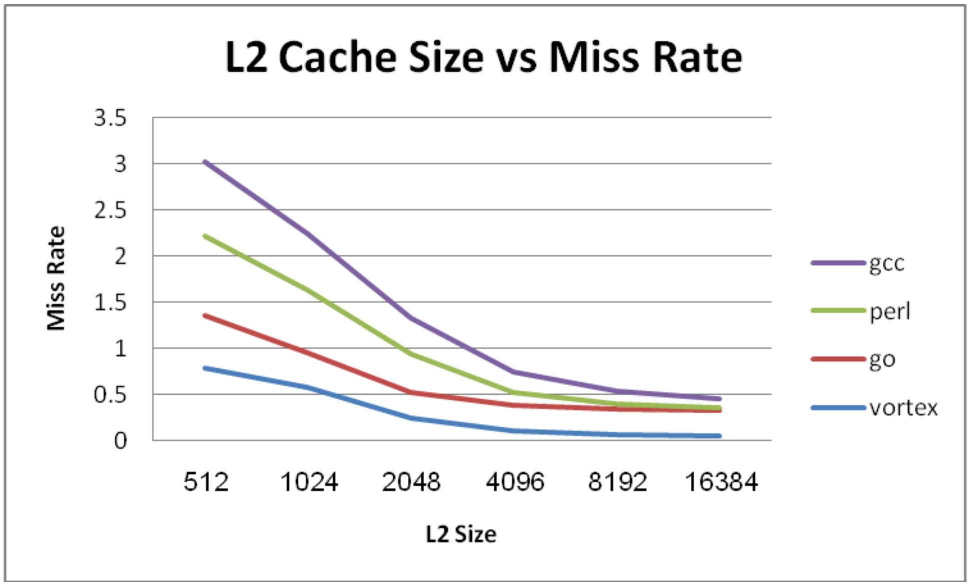
Discussion:

There are two conclusions we can deduce from observing this graph, first as we increase associativity we can see a decrease in miss rate (this is due to the reduction of conflict misses in our cache), also the increasing of cache size decreases the capacity misses while conflict misses remain the same hence also decreasing total misstate.

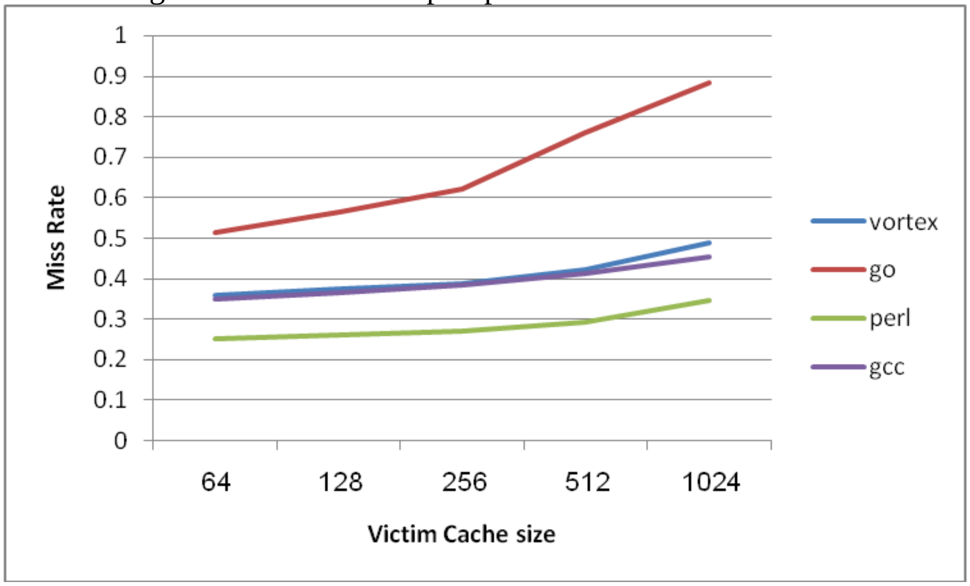
We can also see the having a fully associative cache in comparison to 4 or 8 associative give diminishing return in terms of miss-rates. Also this happens as we increase the cache size this due to other factors to include like the behavior of the workload and other types of misses.

We Estimate the compulsory miss rate from the graph.by noticing the point at which that miss rate stabilize, were the increasing of associativity and cache size has no effect on it (miss rate).

3. L2 Cache size vs. miss rate (keep L1 size constant)
Vortex had the lowest miss rate(shown as blue). gcc had the highest miss rate. The result is as following:



4. Vary size of victim cache vs miss rate (Keep L1 ,L2 constant)
Go provided the highest miss rate while perl provides lowest miss rate.



9.1.2 Thoroughly explore the design space and discuss noteworthy trends
9.1.3 Find best memory hierarchy configuration

L1 cache exploration: SIZE and BLOCKSIZE

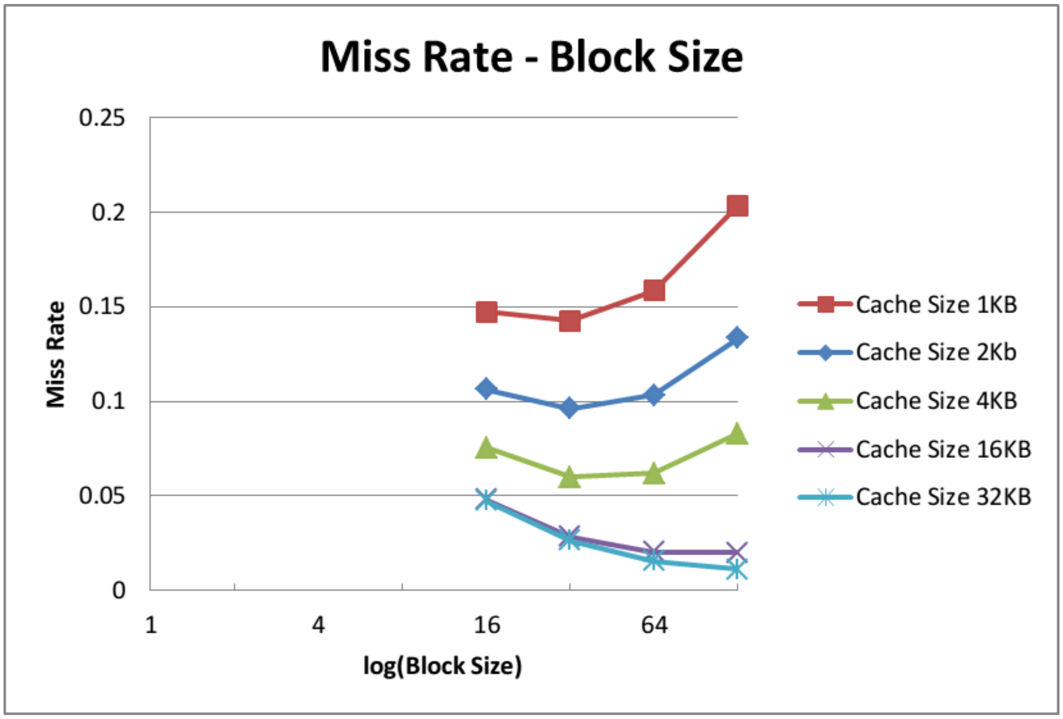


Figure 2

From this graph we can see that the evident mark of increasing block size on cache pollution and miss rate increase, but as we go down further and increase cache size especially at the 16KB and 32KB caches, we see that there is a beneficiary outcomes coming from the increase of cache sizes.
But small caches (1, 2, 4) seem to be affected more by cache pollution since bigger blocks means less space available for the workload. Hence we have to be more picky and thrifty in picking our data. Since picking unnecessary data seems to affect other instruction fetching their own data and conflicting or missing from previous requests.

L1 with L2 co-exploration

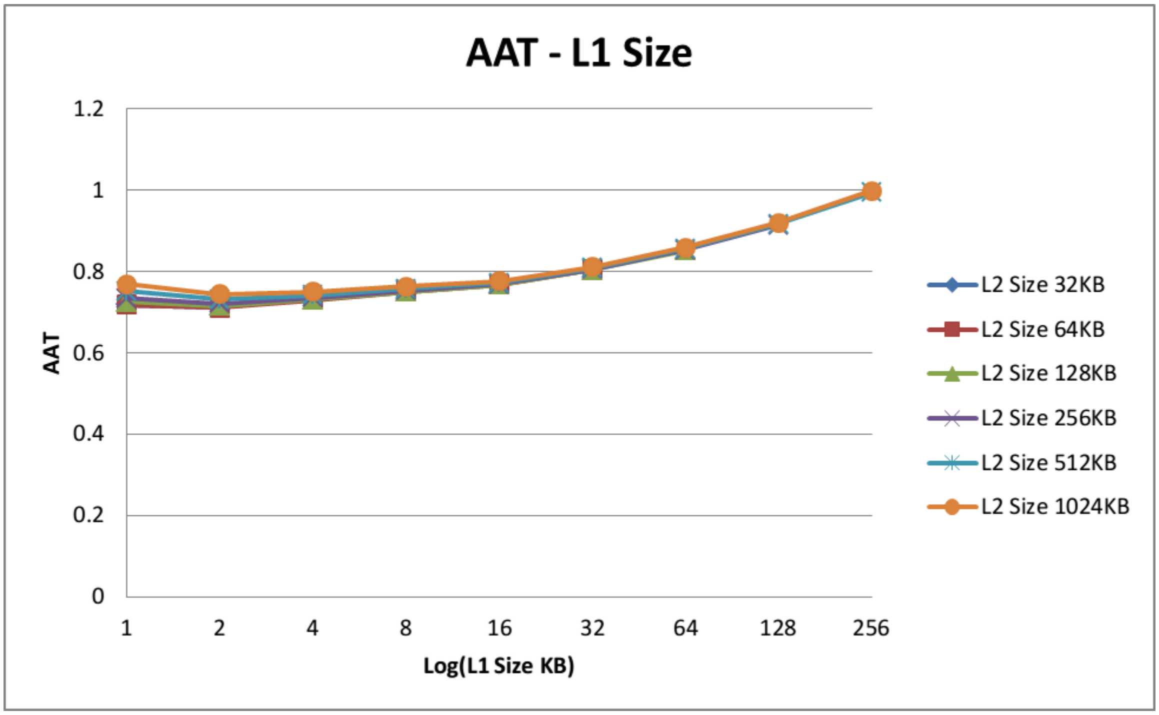


Figure 3

memory hierarchy configuration yields the best (i.e., lowest) AAT

Block Size	L1 Associativity	L2 Associativity	AAT (ns)	L1 Size	l2 Size
32	4	8	0.710306	2	64