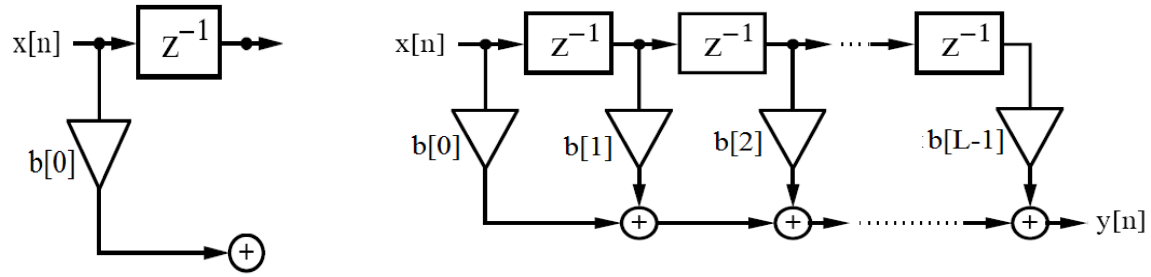
The finite impulse response (FIR) filter is common component in many digital signal processing (DSP) systems. This implementation shows the basic FIR filter diagram with *L* length. The result of delays operates on input samples.

Block Diagram:

For each integer *n*, the output is the values in the delay line scaled by *b*[0], b[1], …, *b*(*L-1)*.



Process Map:

The FIR Filter implemented using three digital hardware elements including a Latch, a Multiplier and an Adder. The latch updates (Y) output using the value of the input (X).