



Input or output	Signal name	addi	R-format	lw	sw	beq	jump
Inputs of control	Op5	0	0	1	1	0	1
	Op4	0	0	0	0	0	1
	Op3	0	0	0	1	0	1
	Op2	0	0	0	0	1	1
	Op1	0	0	1	1	0	1
	Op0	1	0	1	1	0	1
Outputs of control	RegDst	0	1	0	X	X	X
	ALUSrc	1	0	1	1	0	X
	MemtoReg	0	0	1	X	X	X
	RegWrite	1	1	1	0	0	X
	MemRead	0	0	1	0	0	X
	MemWrite	0	0	0	1	0	X
	Branch	0	0	0	0	1	0
	ALUOp1	1	1	0	0	0	X
	ALUOp0	0	0	0	0	1	X

ALUOp		Func						ctrlalu	OP	instruction
ALUOp1	ALUOp0	F5	F4	F3	F2	F1	F0			
0	0	X	X	X	X	X	X	0010	100011	LW
0	1	X	X	X	X	X	X	0110	101011	SW
1	0	1	0	0	0	0	0	0010	000000	ADD
1	0	1	0	0	0	1	0	0110	000000	SUB
1	0	1	0	0	1	0	0	0000	000000	AND
1	0	1	0	0	1	0	1	0001	000000	OR
X	X	X	X	X	X	X	X	0010	000001	addi
X	X	X	X	X	X	X	X	XXXX	000100	beq
X	X	X	X	X	X	X	X	XXXX	111111	jump

inst						
instruction	op	rs	rt	rd	shift	func
add / 32'd3	000000	00011	00010	00001	00000	100000
sub / 32'd4	000000	00011	00010	00001	00000	100010
and / 32'd5	000000	00011	00010	00001	00000	100100
or / 32'd6	000000	00011	00010	00001	00000	100101

inst				
instruction	op	rs	rt	datai
LW / 32'd0	100011	00011	00010	000010000000000000
SW / 32'd1	101011	00011	00010	000010000000000000
beq / 32'd2	000100	00011	00011	000110000000000000
addi / 32'd7	000001	00011	00010	0000100000100000

inst		
instruction	op	jump
jump / 32'd8	111111	00011000100000100000100000