LAB1:UART

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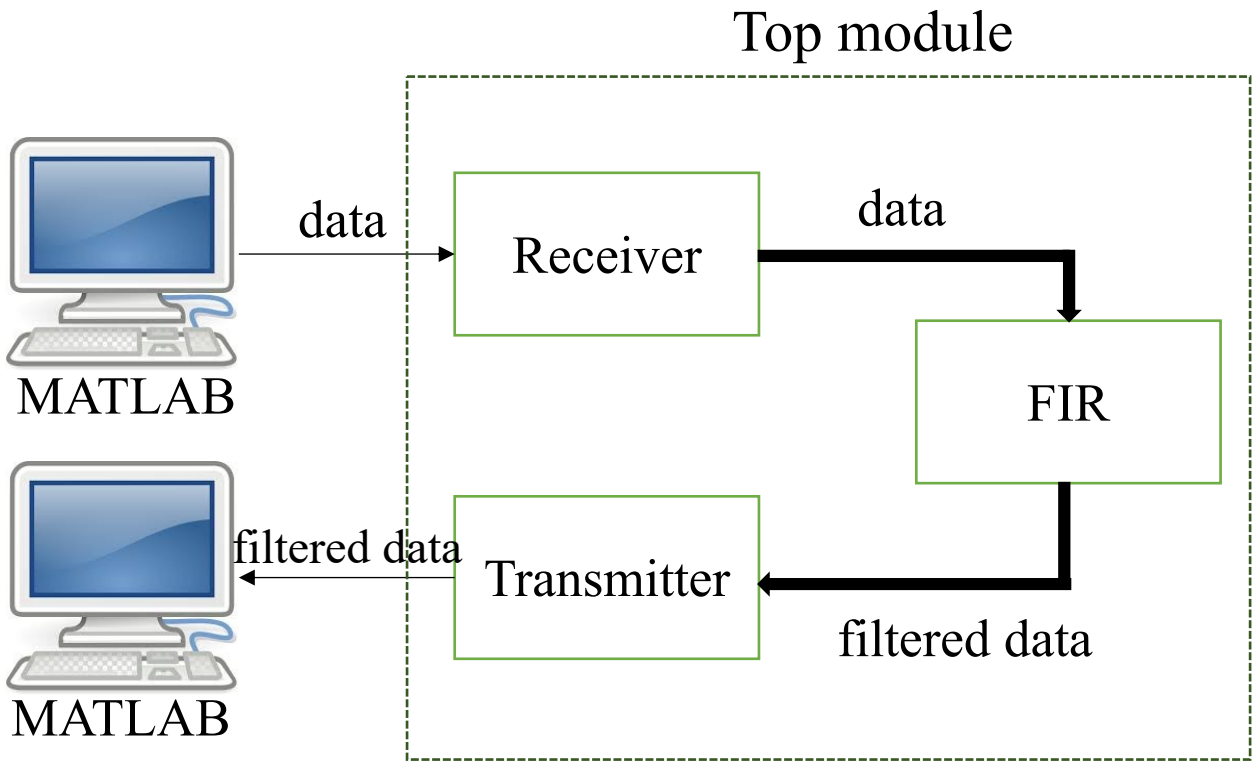
15 October 2022

FPGA-based Embedded System Design

School of Electrical and Computer Engineering, College of Engineering
University of Tehran

Design, Verification & Debugging of
Embedded Systems LAB

DVDES


Top module
data
Receiver
data
FIR
MATLAB
filtered data
Transmitter
filtered data
MATLAB

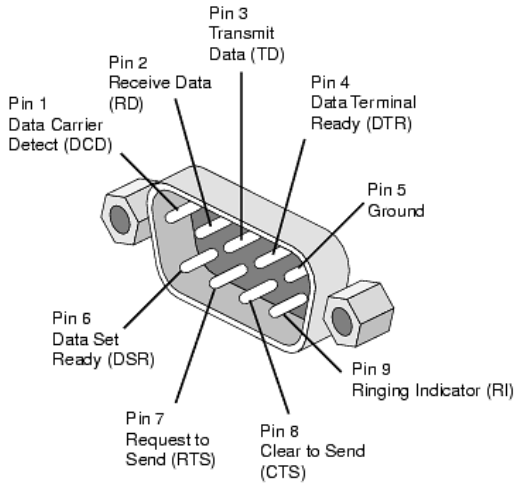
UART

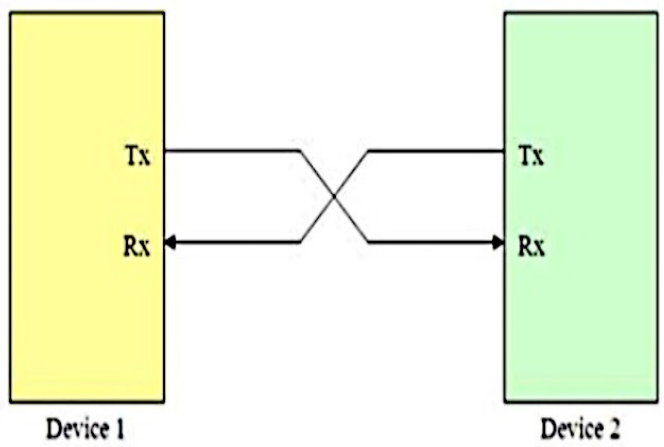
- Universal Asynchronous Receiver Transmitter
- The circuit sends parallel data through a serial line

- Serial communication without external clock signal
- Very cheap communication
  - Needs one wire for serial communicate

UART

DE9 connector





DVDES

Device Driver

- Computer program
- Operates or controls a particular type of device that is attached to a computer

- Program device driver for serial connections based on RS232 protocol
- Using asynchronous UART communication

UART character transmission

Idle bus ⟹ Data frame ⟹ Idle bus

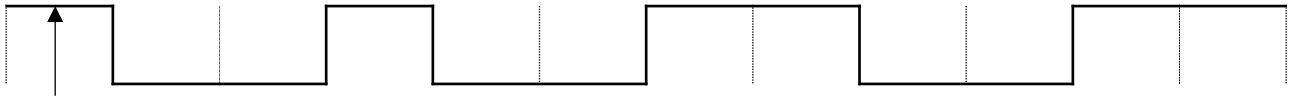
Data frame:
start bit ⟹ Data ⟹ parity (if needed) ⟹ stop bit

Idle state: bus in high voltage (*logic 1*)
Start bit: *logic 0*
Data
Parity: check for transmission error
Stop bit: *logic 1*

UART character transmission

Idle bus ⇢ Data frame ⇢ Idle bus

Start bit: 1 bit
Data: 5, 6, 7 or 8 bits
Parity: none, odd, or even
Stop bit: 1, 1.5 or 2 bits

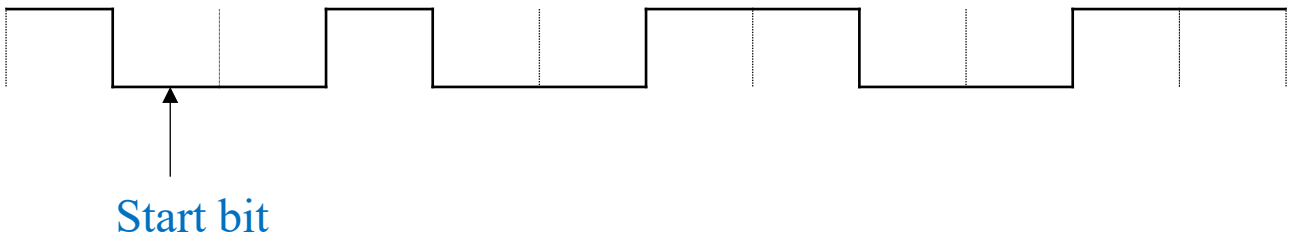


Idle bus

UART character transmission

Idle bus ⇢ Data frame ⇢ Idle bus

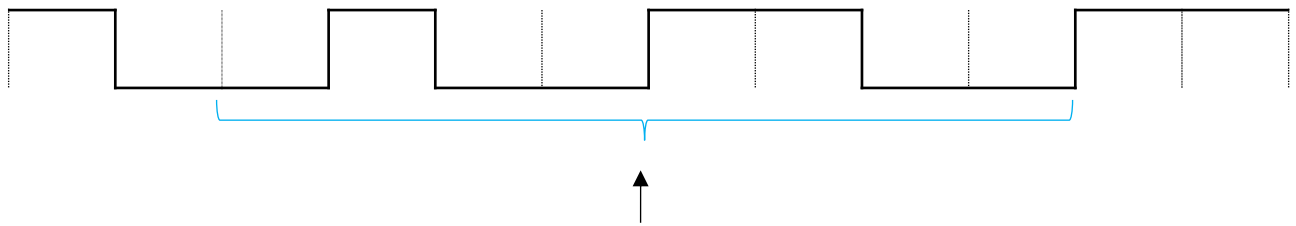
Start bit: 1 bit
Data: 8 bits
Parity: even
Stop bit: 1 bit



UART character transmission

Idle bus ⇢ Data frame ⇢ Idle bus

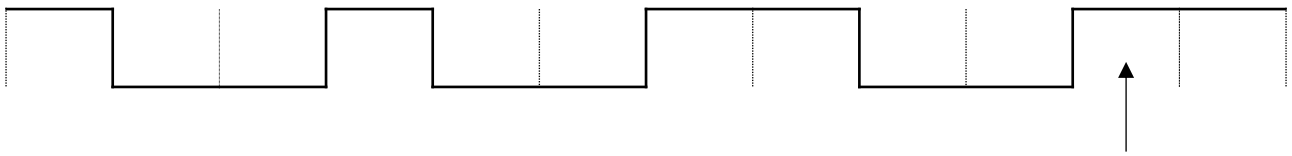
Start bit: 1 bit
Data: 8 bits (from LSB to MSB)
Parity: even
Stop bit: 1 bit



UART character transmission

Idle bus ⇢ Data frame ⇢ Idle bus

Start bit: 1 bit
Data: 8 bits
Parity: even
Stop bit: 1 bit

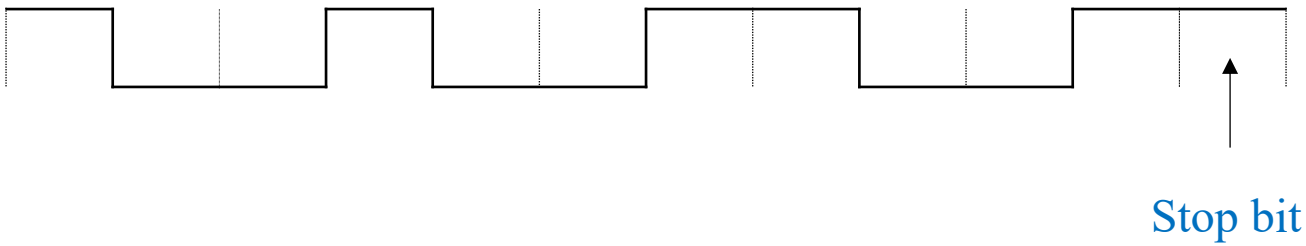


Even parity

UART character transmission

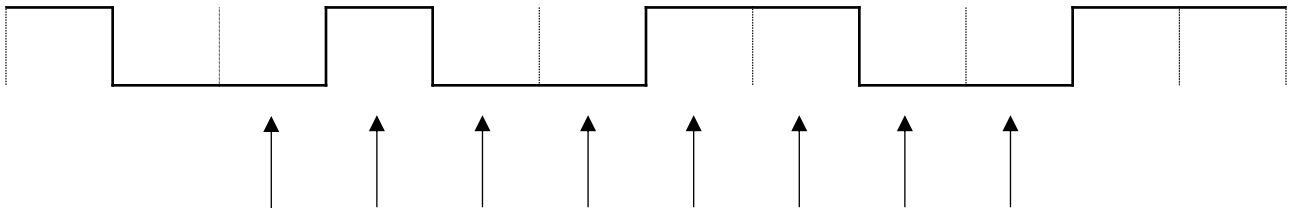
Idle bus ⇢ Data frame ⇢ Idle bus

Start bit: 1 bit
Data: 8 bits
Parity: even
Stop bit: 1 bit



UART character transmission

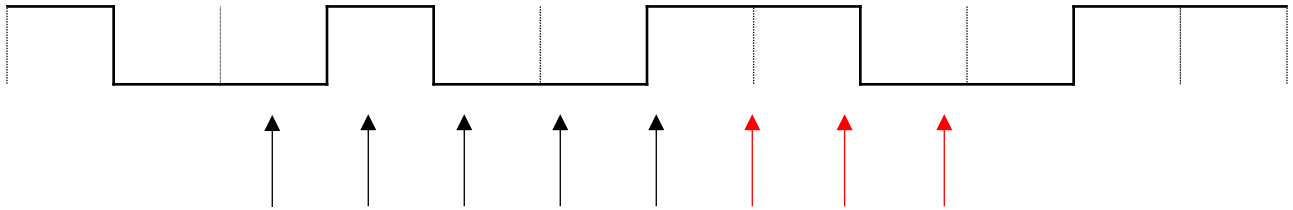
- Receiver should sample in middle of bits



- ✓ Transmitter and receiver agree on the same baud rate

UART character transmission

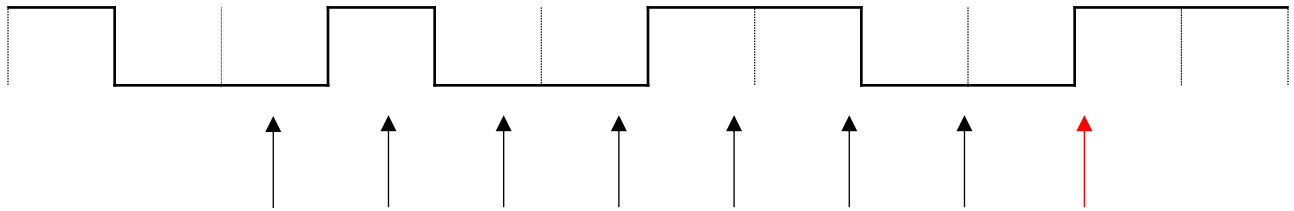
➢ Receiver samples quickly:



✗ Receiver receives wrong data

UART character transmission

➢ Receiver samples slowly:



✗ Receiver receives wrong data

Basics of serial communication

- **Bit rate:**
  Number of bits sent every second (BPS)
- **Baud rate:**
  Number of symbols sent every second

Standard bit rates:
100, 200, 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200 bps.

Basics of serial communication

➢ Example:
- 9600 baud rate
- 10MHz clock frequency

In one seconds clock signal has 10^7 cycles
We have 9600 symbol every second
Baud tick should clock every $10^7/9600=1041.66$ cycle

Clock divided by 1041

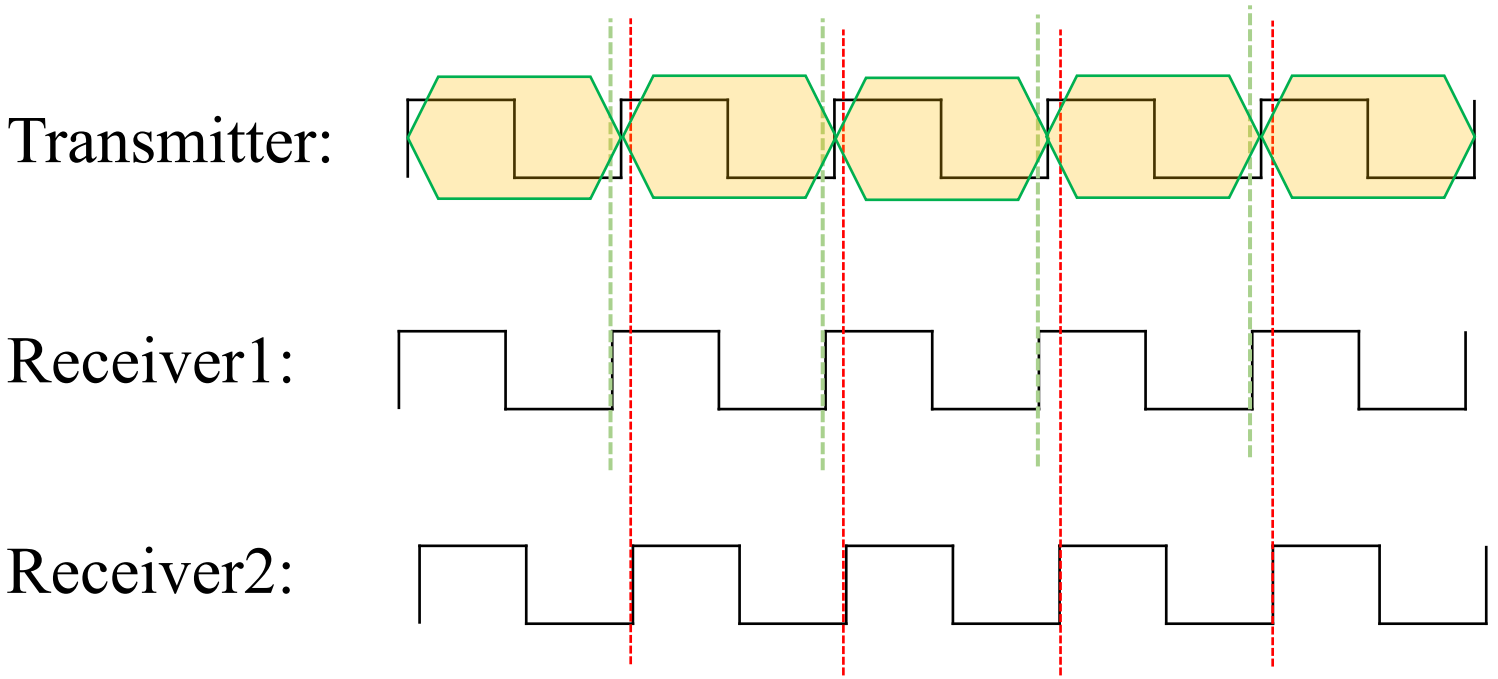
Basics of serial communication

- Example:
- 9600 baud rate
- 10MHz clock frequency

New baud rate = 10MHz/1041 = 9606.147

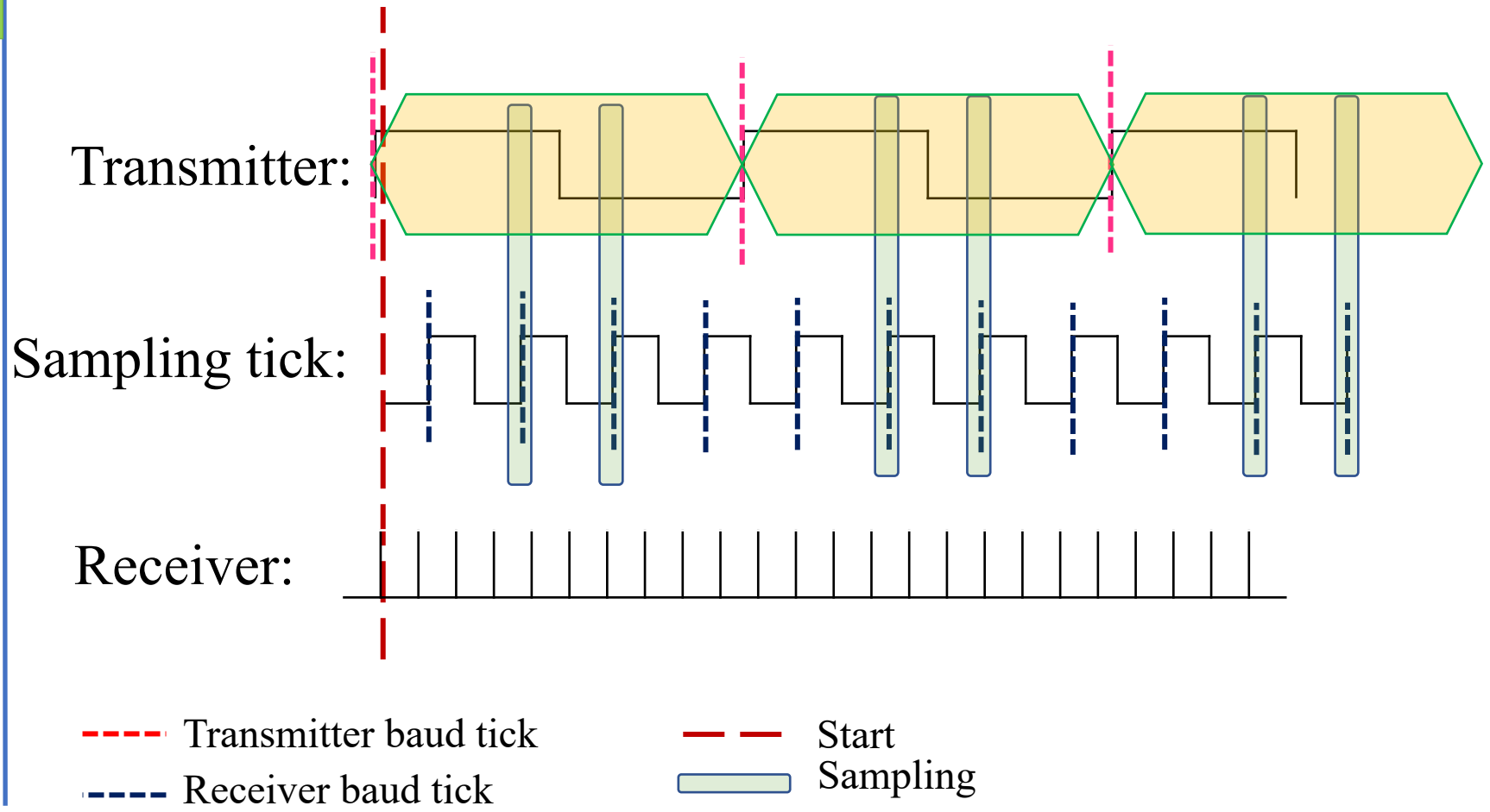
Error = (9606-9600)/9600 * 100 = 0.06% ≤ 0.3% ✓

UART character transmission



Oversampling helps receiver get correct data

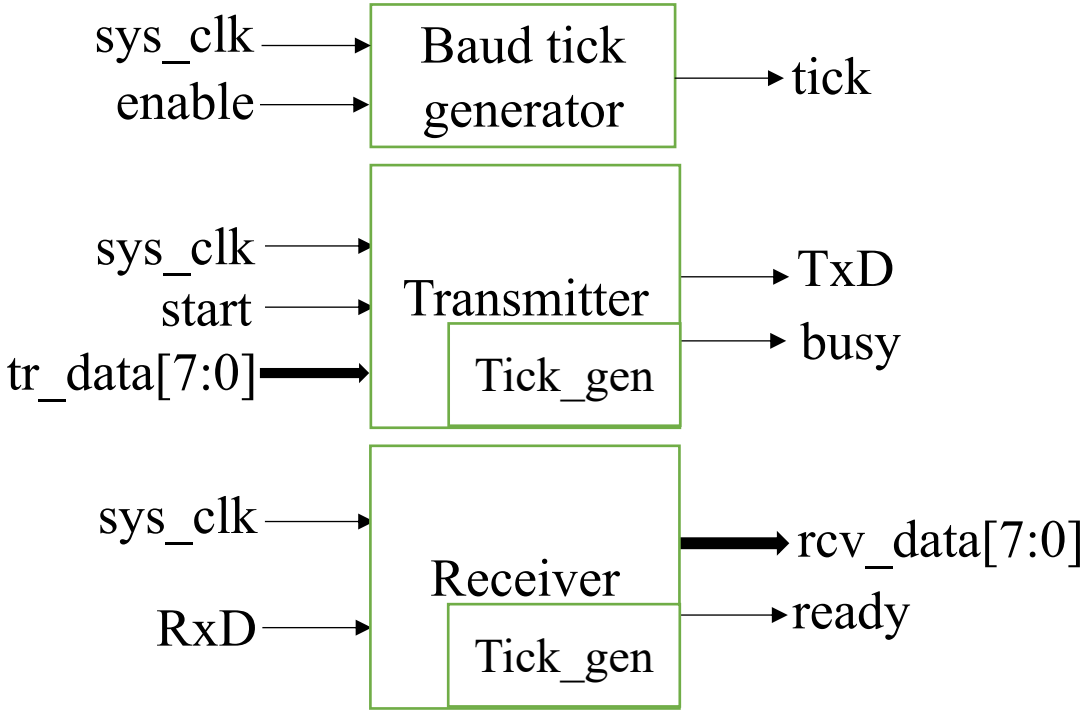
UART character transmission



LAB1

Required modules

1. Baud tick generator
2. Transmitter
3. Receiver

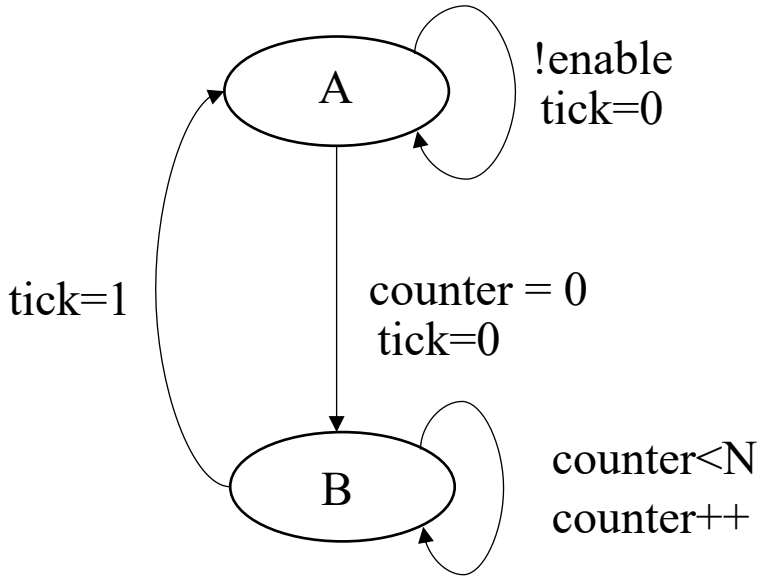


Baud tick generator

Baud tick generator

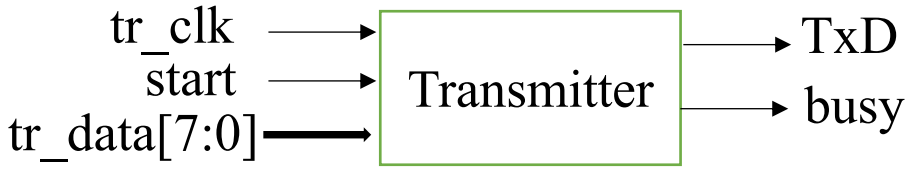
1. Calculate division factor (N)
   - clock frequency
   - baud-rate
   - oversampling
2. Use up-counter counting to N
3. Tick every N cycle

Baud tick generator

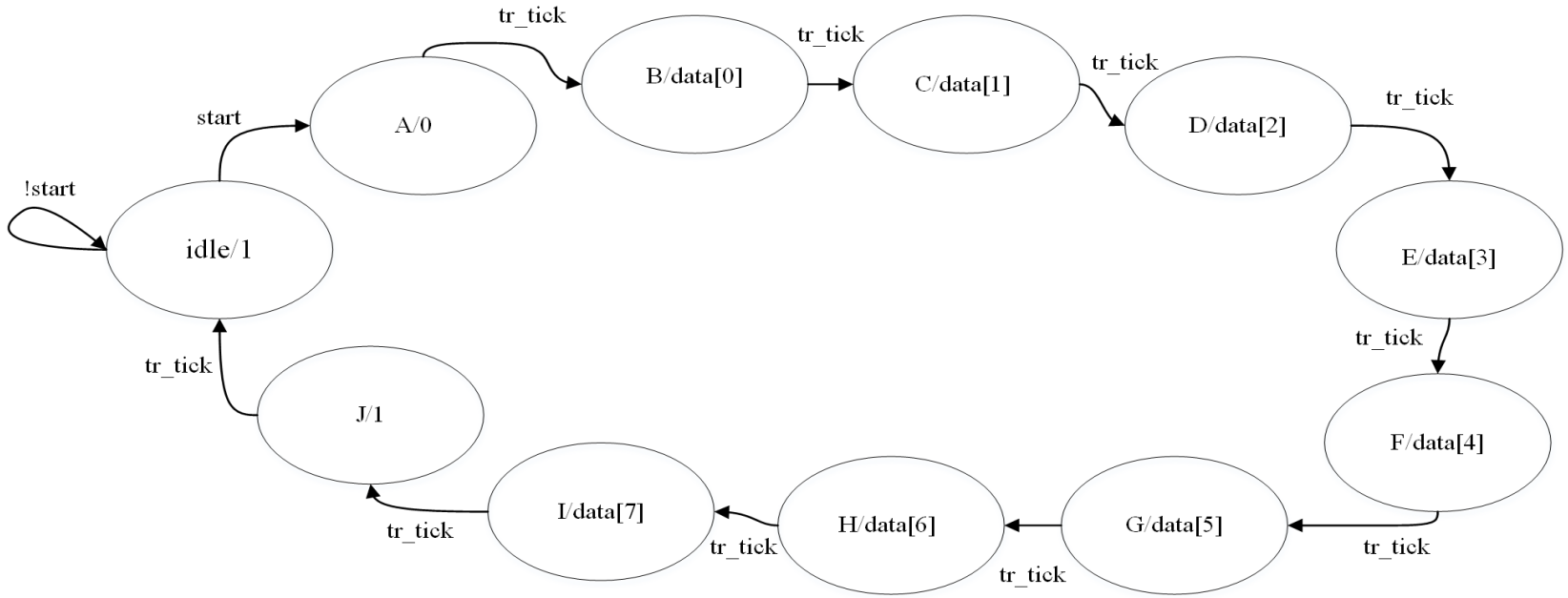


Transmitter

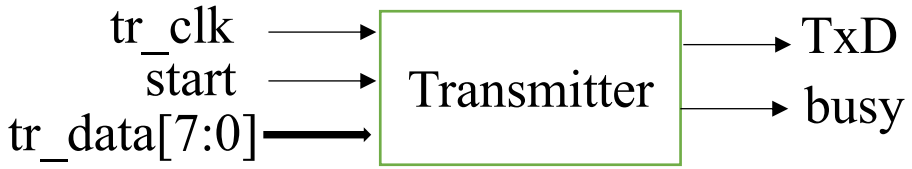
Transmitter



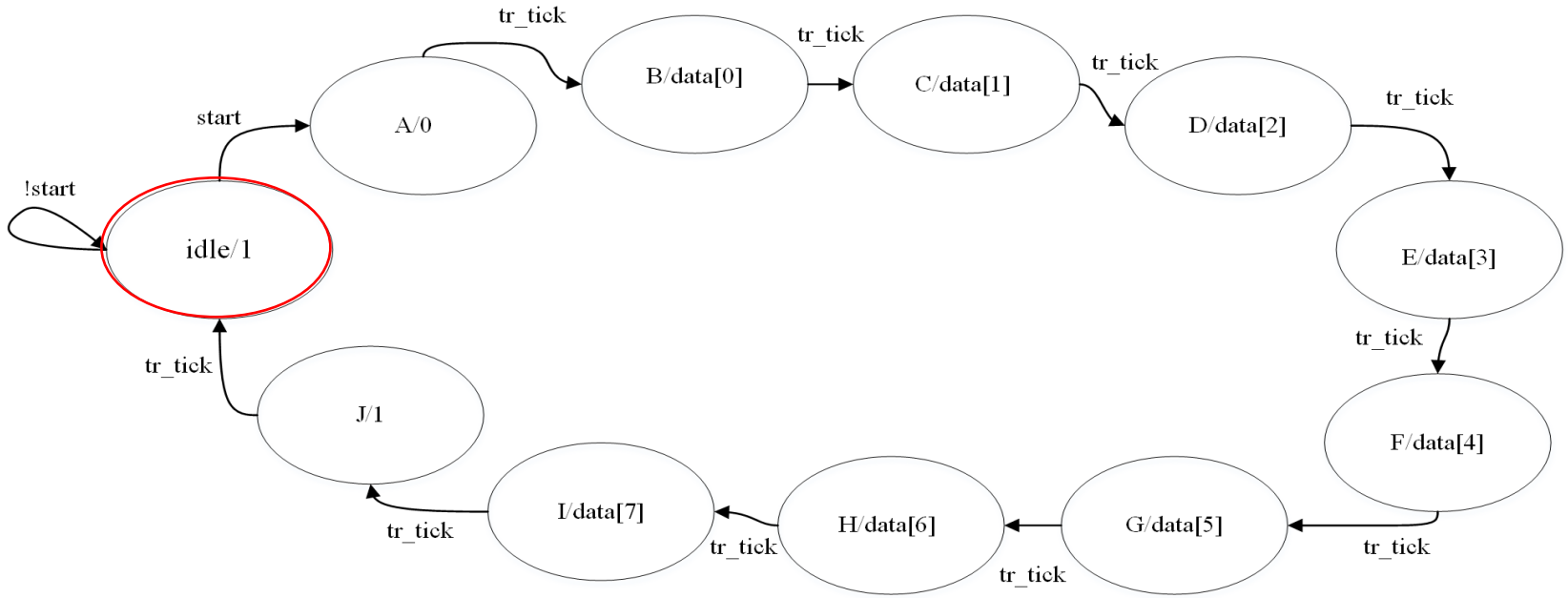
8n1 = 8 bit data, No parity, 1 stop bit



Transmitter



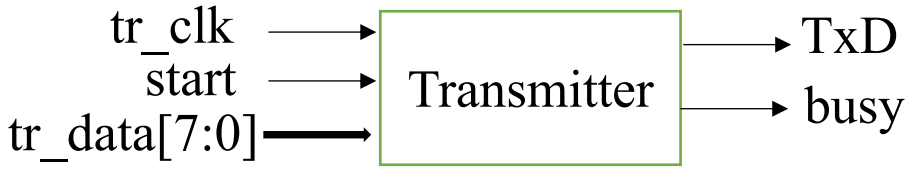
8n1 = 8 bit data, No parity, 1 stop bit



TxD: idle bit = 1

DVDES

Transmitter



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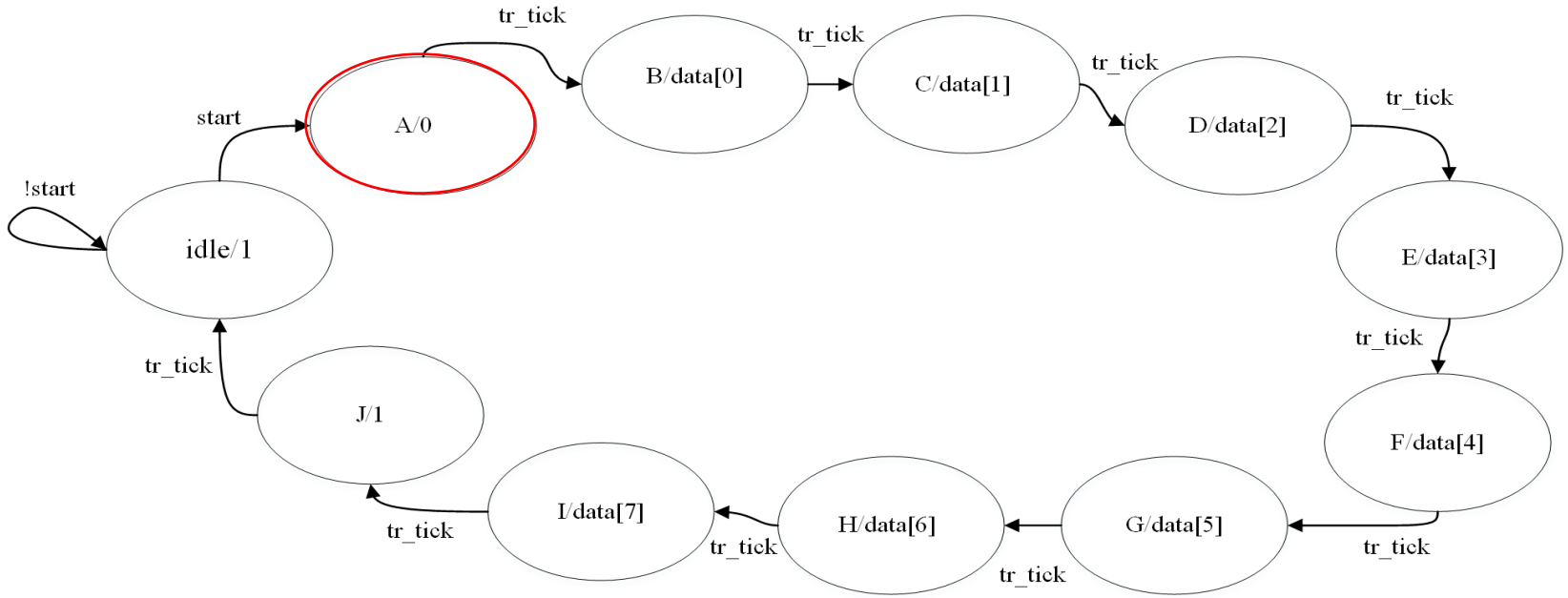
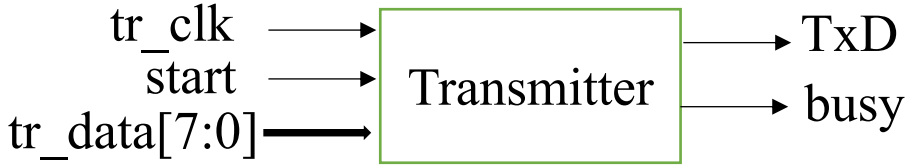


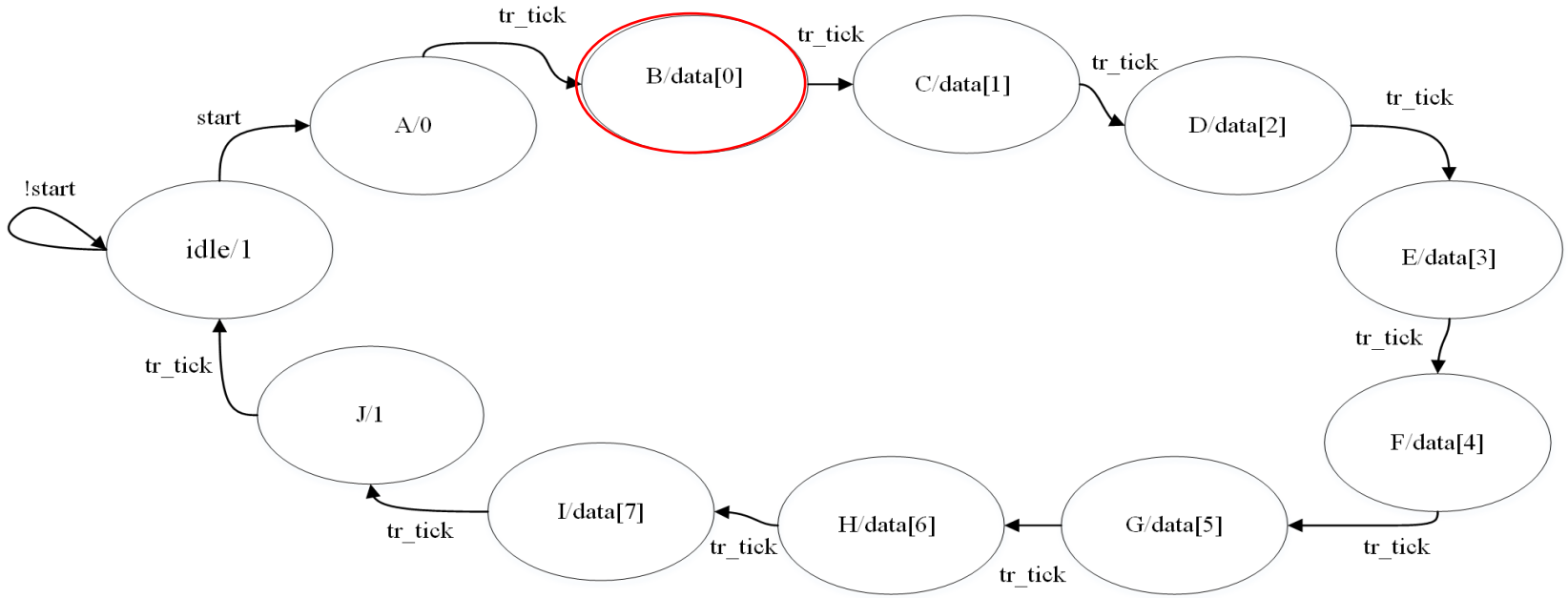
TxD: start bit = 0

DVDES

Transmitter



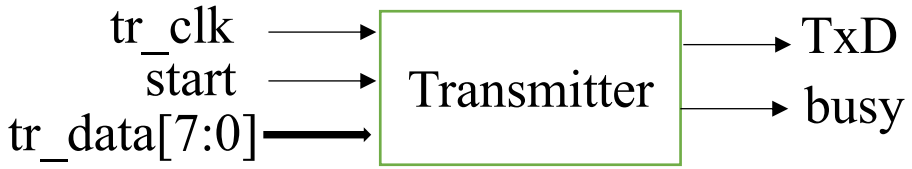
8n1 = 8 bit data, No parity, 1 stop bit



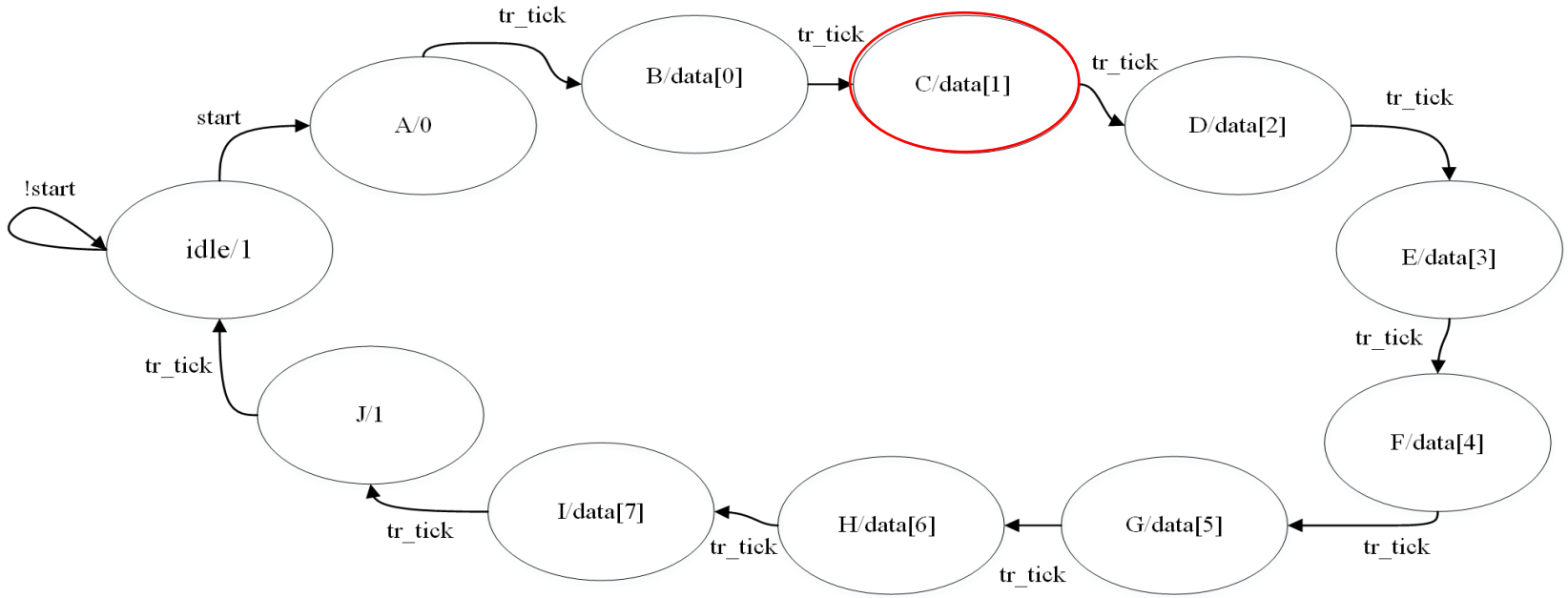
TxD: data[0]

DVDES

Transmitter



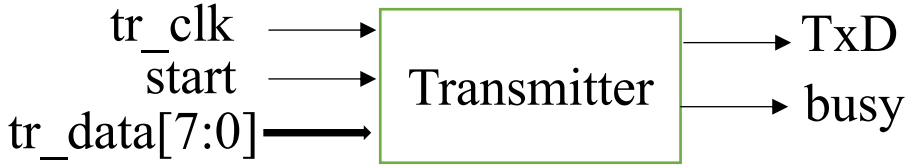
8n1 = 8 bit data, No parity, 1 stop bit



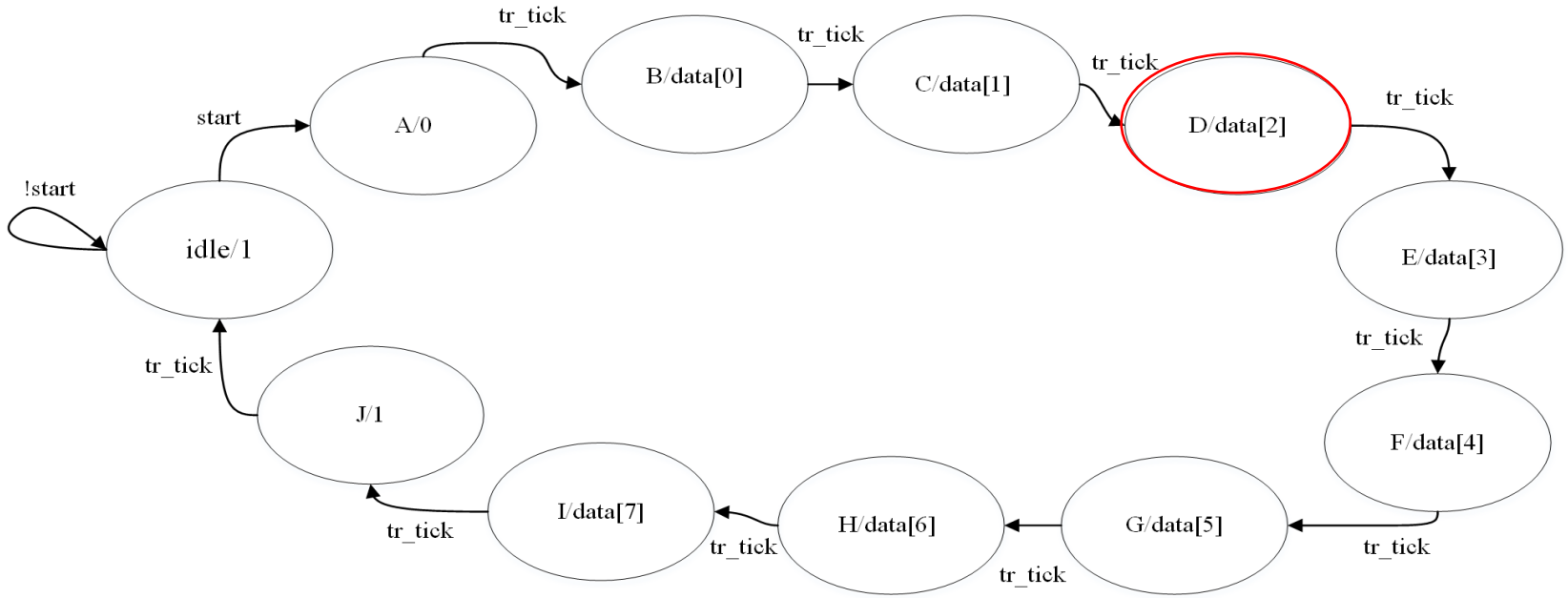
TxD: data[1]

DVDES

Transmitter



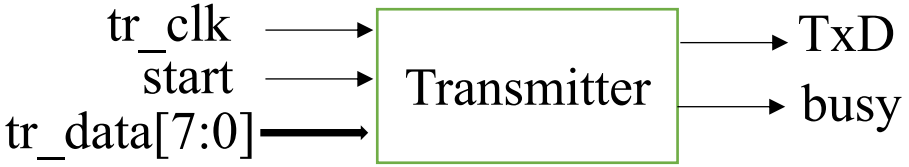
8n1 = 8 bit data, No parity, 1 stop bit



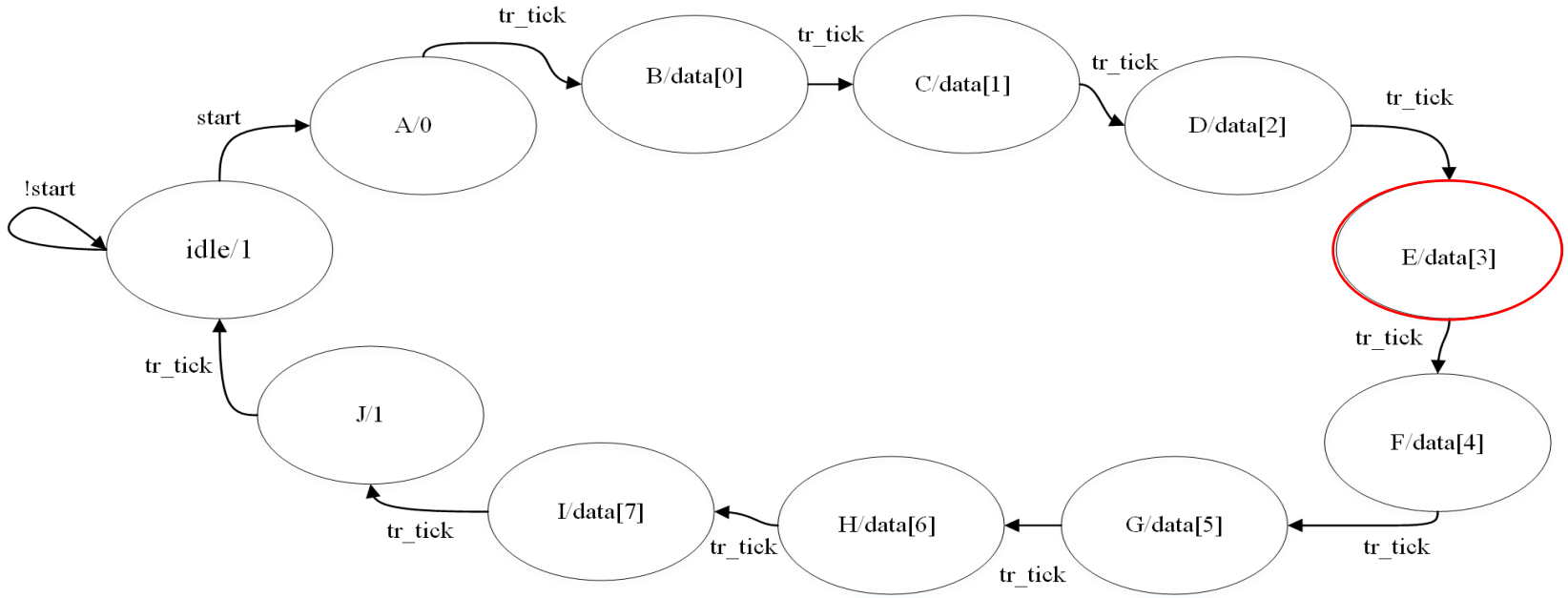
TxD: data[2]

DVDES

Transmitter



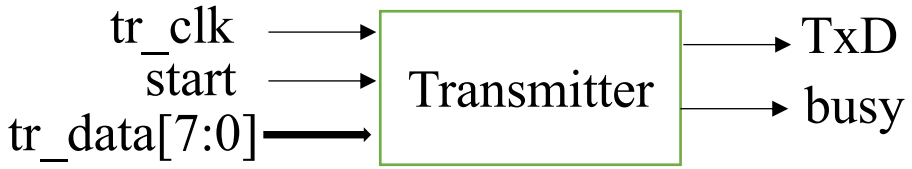
8n1 = 8 bit data, No parity, 1 stop bit



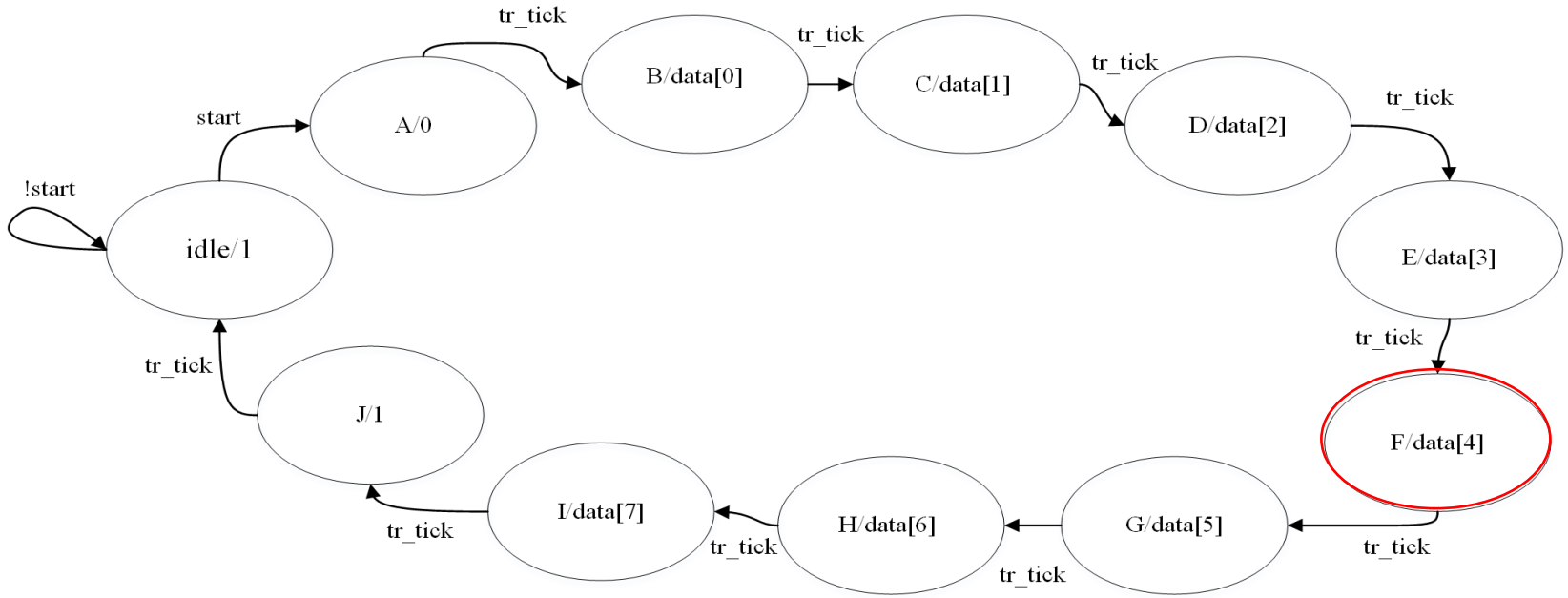
TxD: data[3]

DVDES

Transmitter



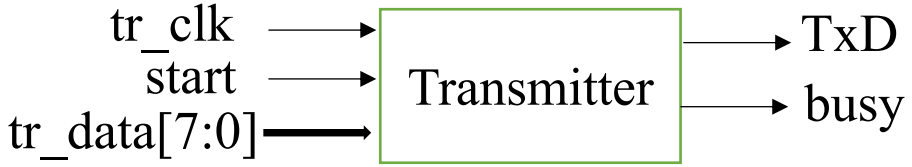
8n1 = 8 bit data, No parity, 1 stop bit



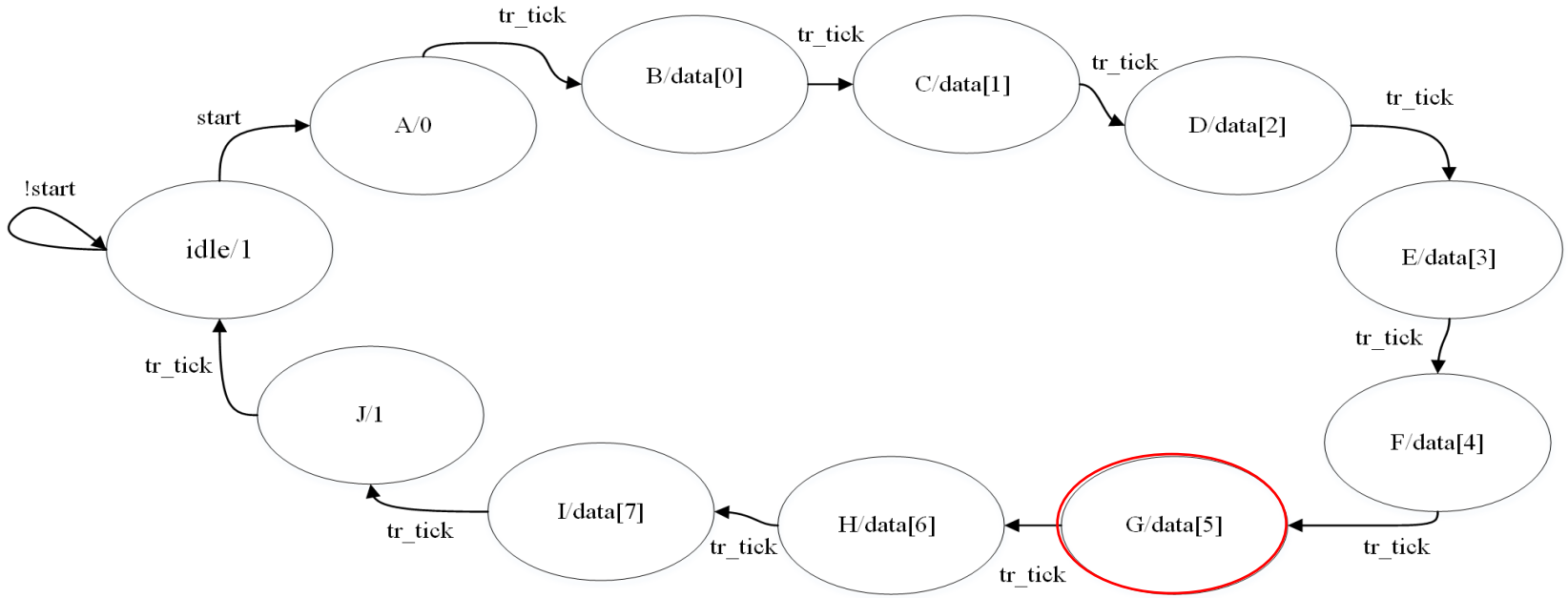
TxD: data[4]

DVDES

Transmitter



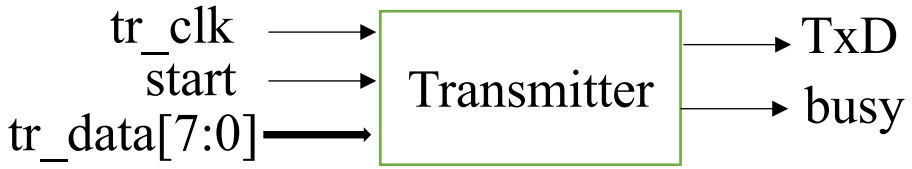
8n1 = 8 bit data, No parity, 1 stop bit



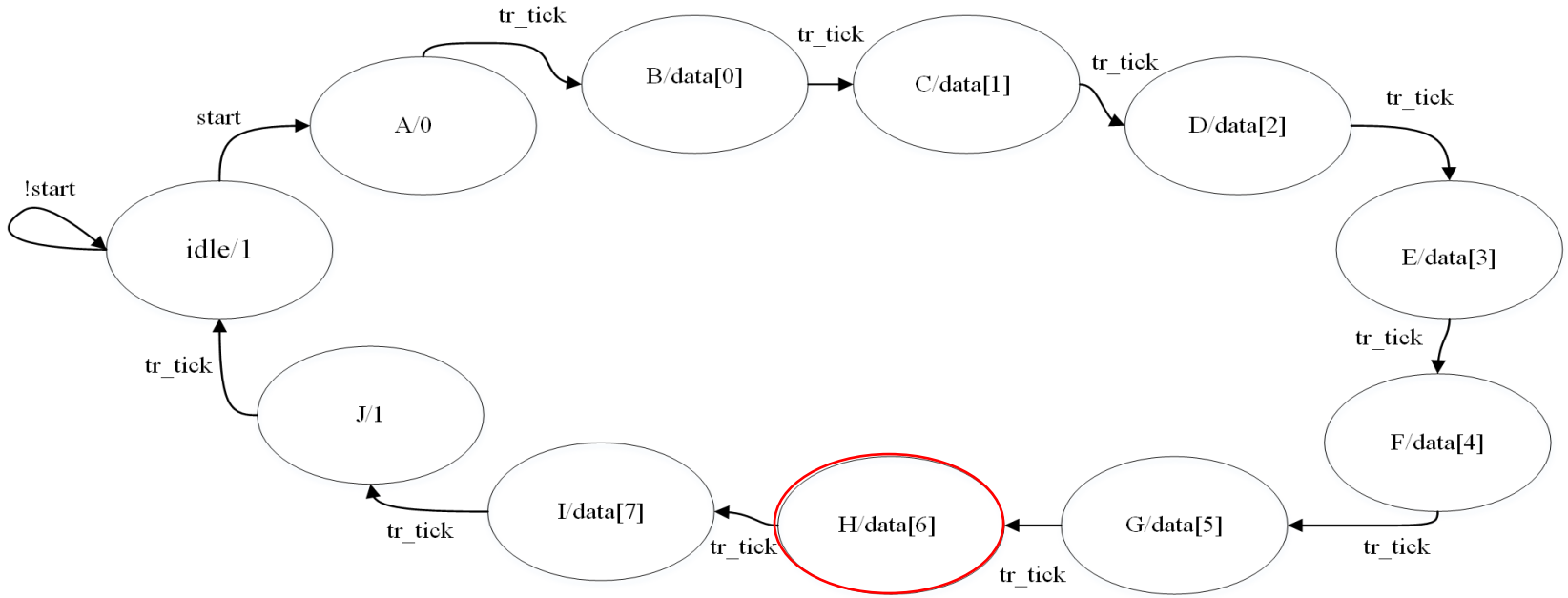
TxD: data[5]

DVDES

Transmitter



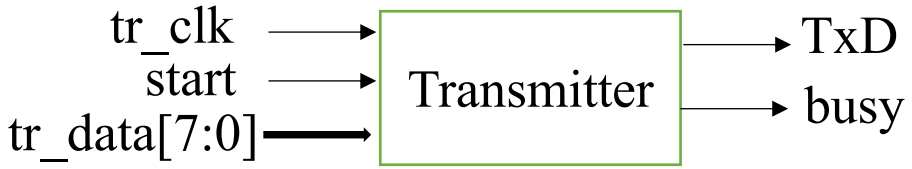
8n1 = 8 bit data, No parity, 1 stop bit



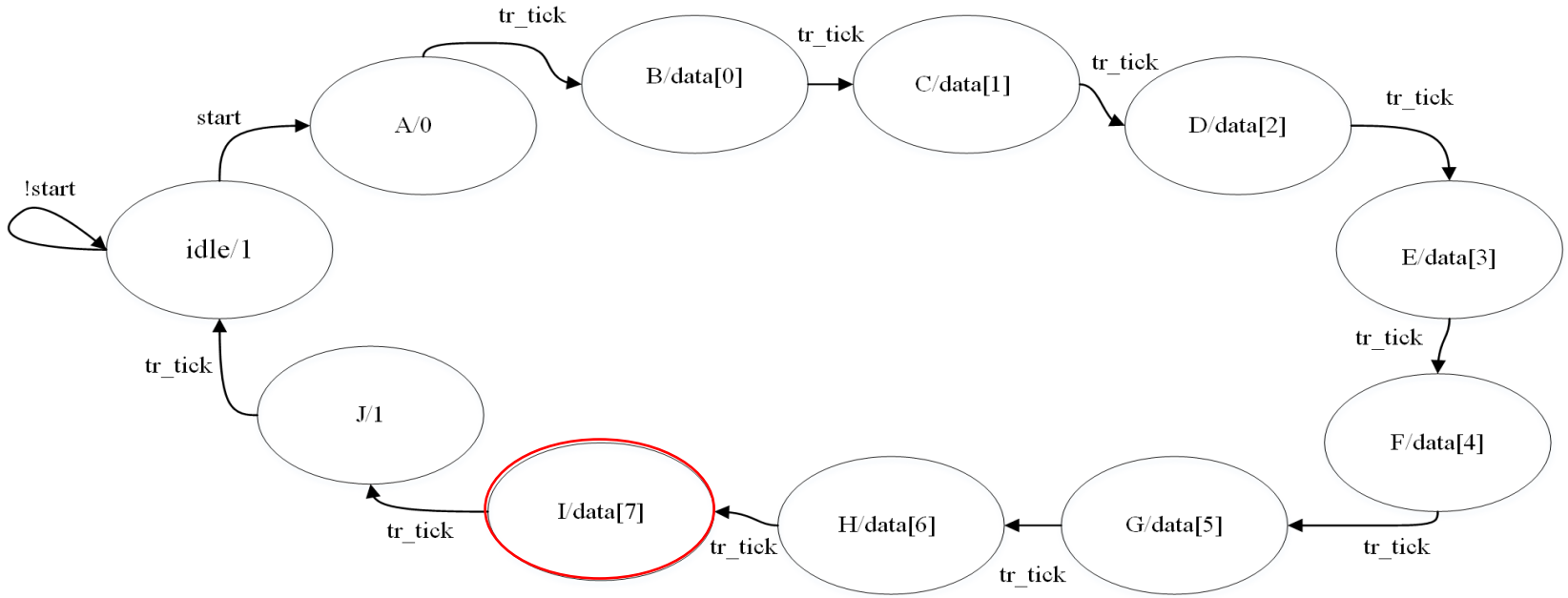
TxD: data[6]

DVDES

Transmitter



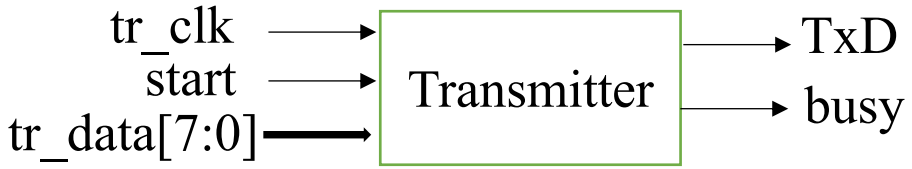
8n1 = 8 bit data, No parity, 1 stop bit



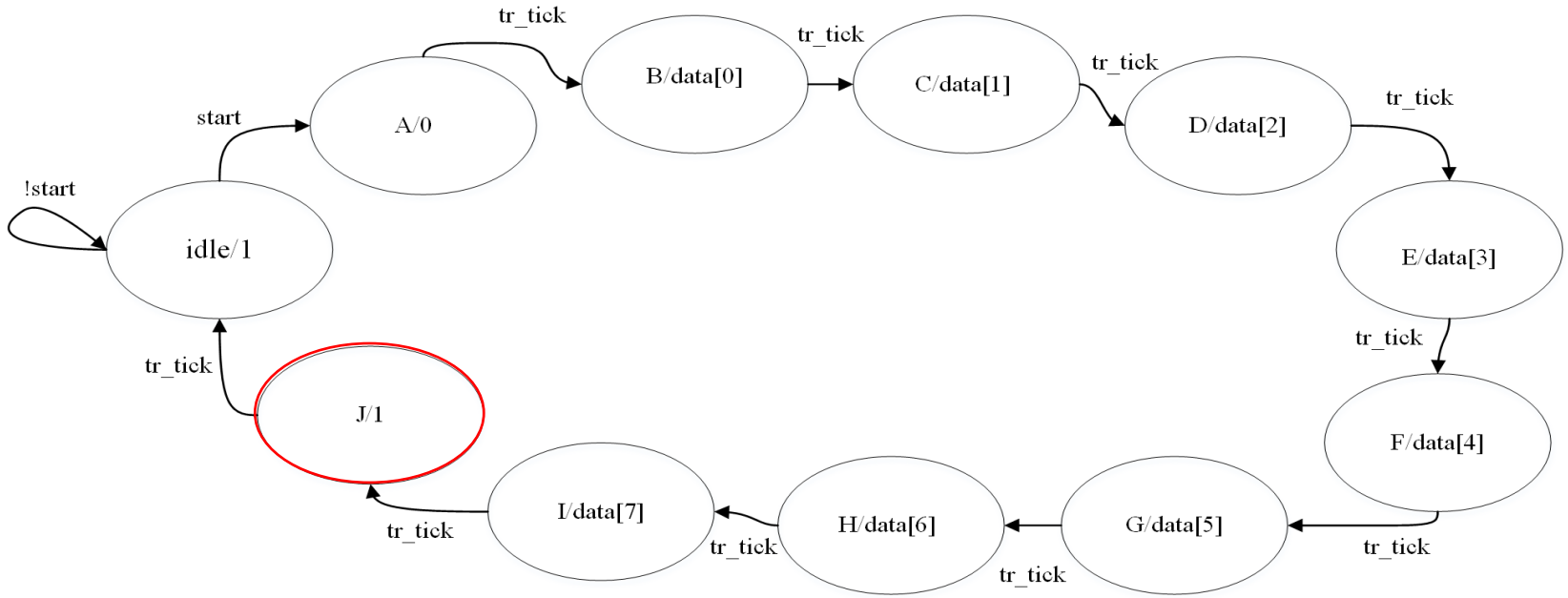
TxD: data[7]

DVDES

Transmitter



8n1 = 8 bit data, No parity, 1 stop bit



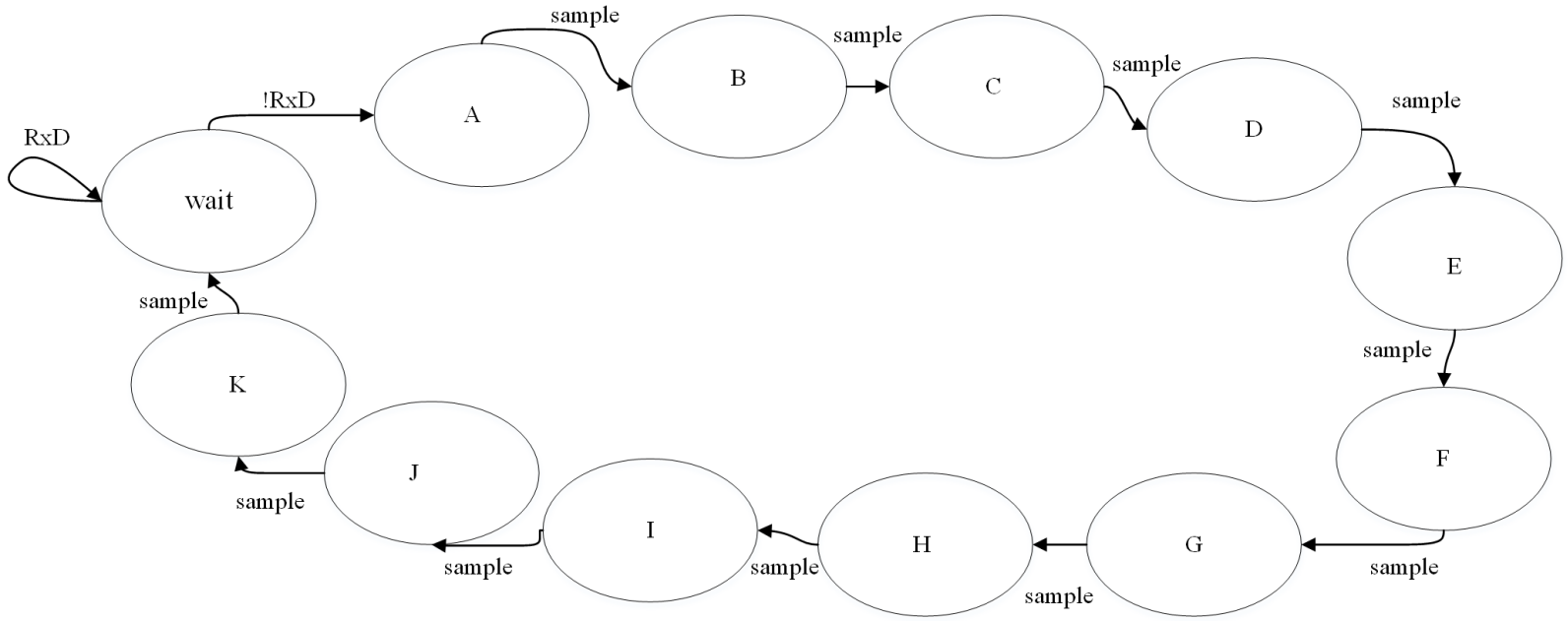
TxD: stop bit = 1

DVDES

Receiver

Receiver

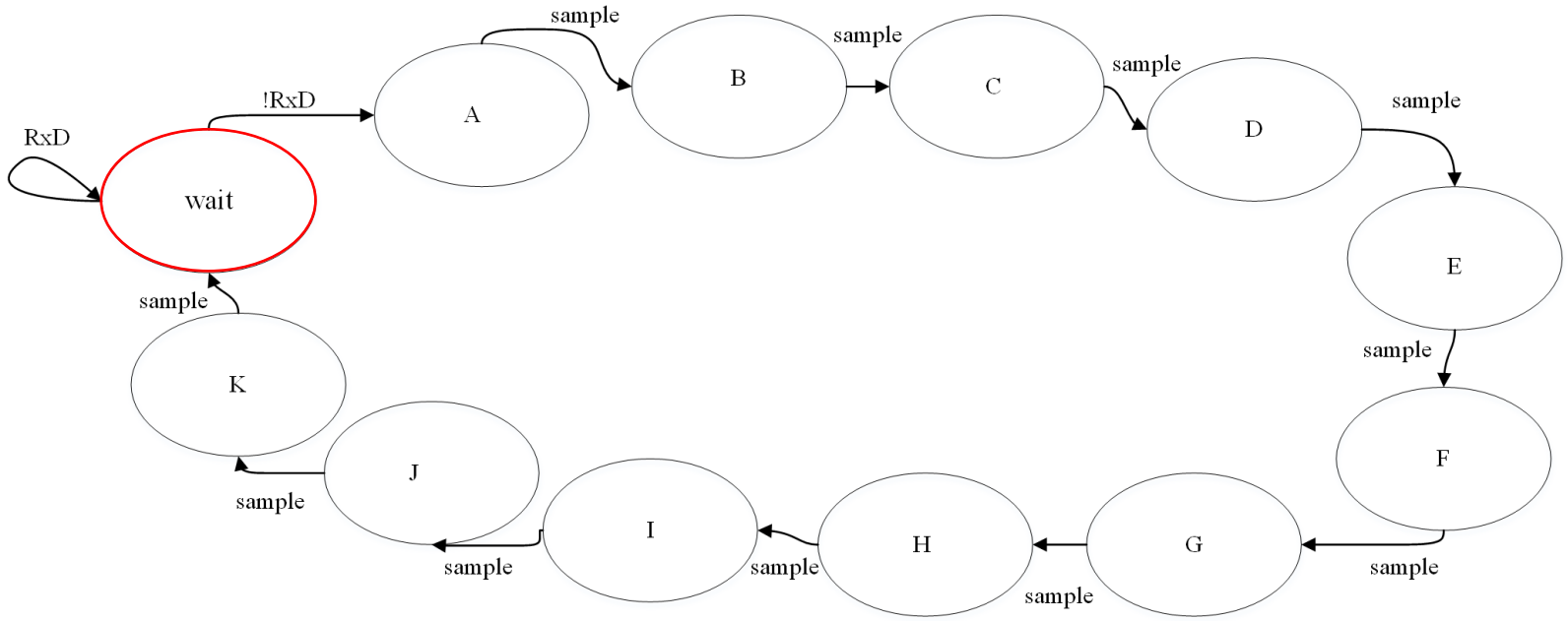
8n1 = 8 bit data, No parity, 1 stop bit



DVDES

Receiver

8n1 = 8 bit data, No parity, 1 stop bit

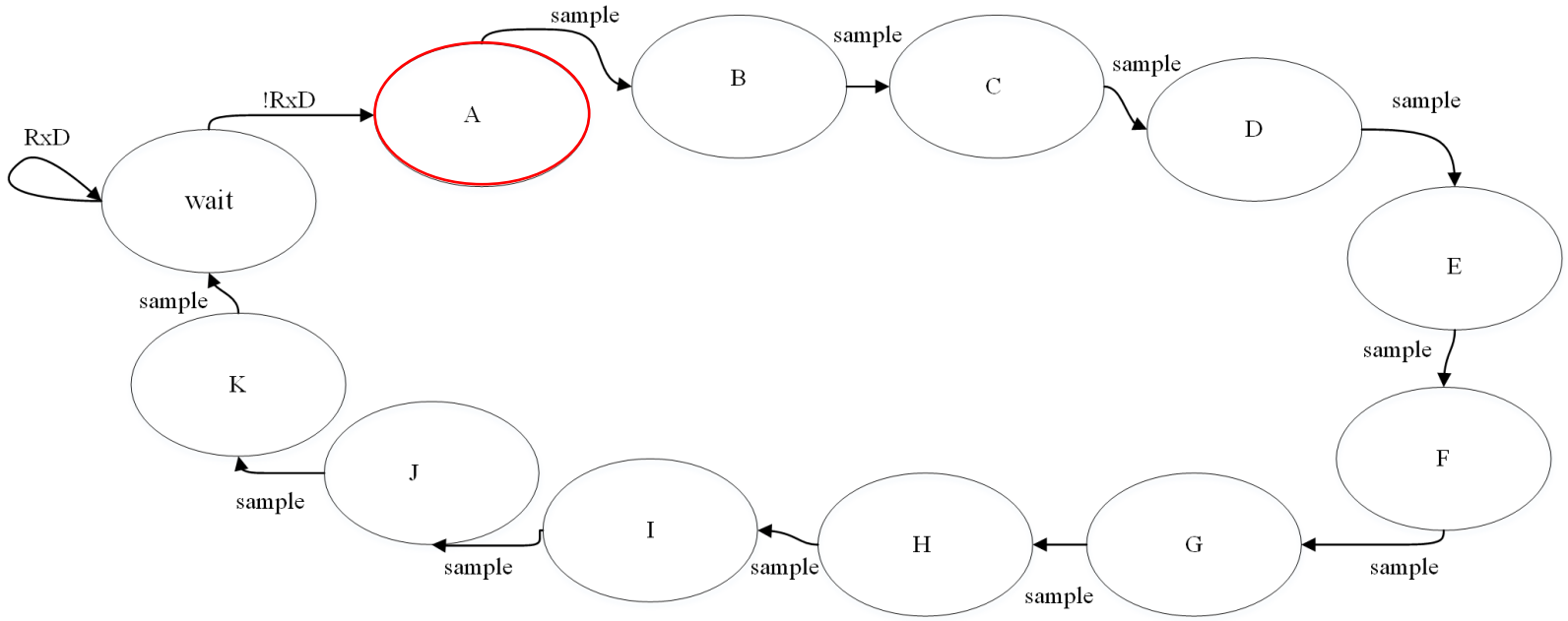


RxD: idle bus = 1

DVDES

Receiver

8n1 = 8 bit data, No parity, 1 stop bit

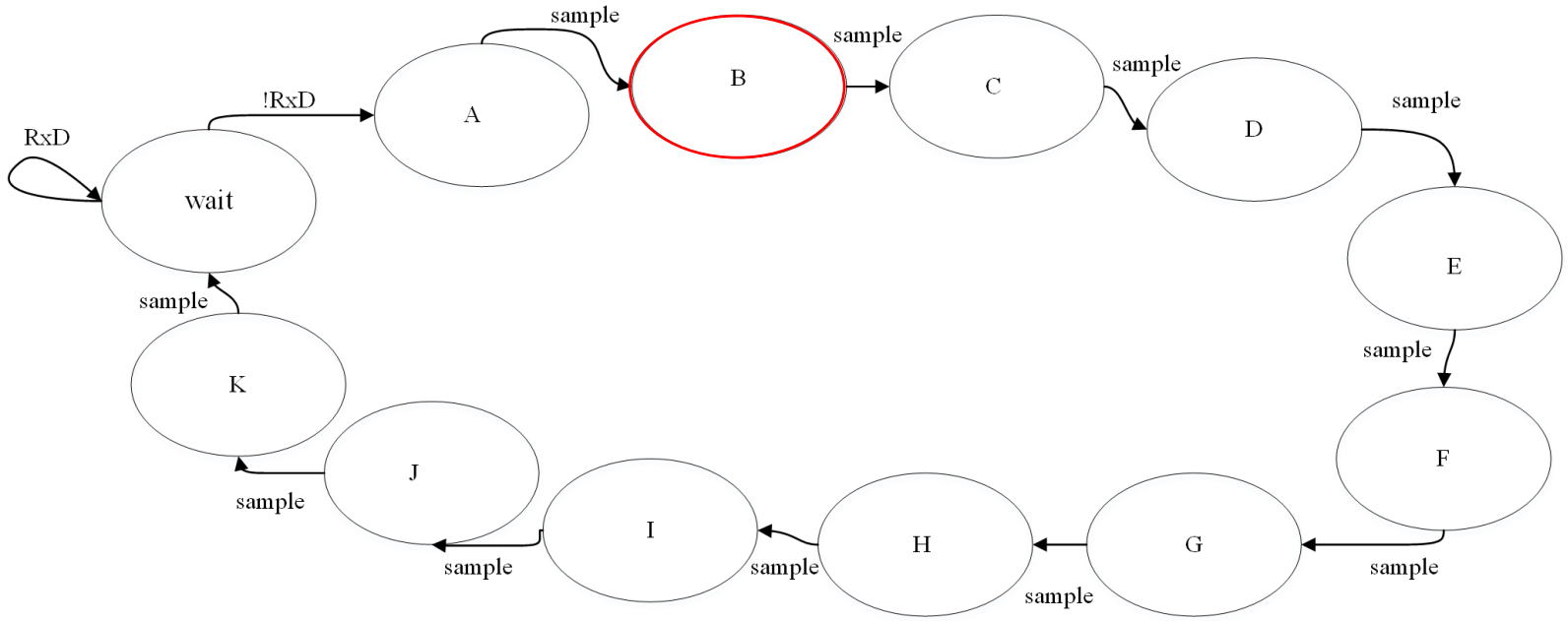


RxD: start bit = 0

DVDES

Receiver

8n1 = 8 bit data, No parity, 1 stop bit

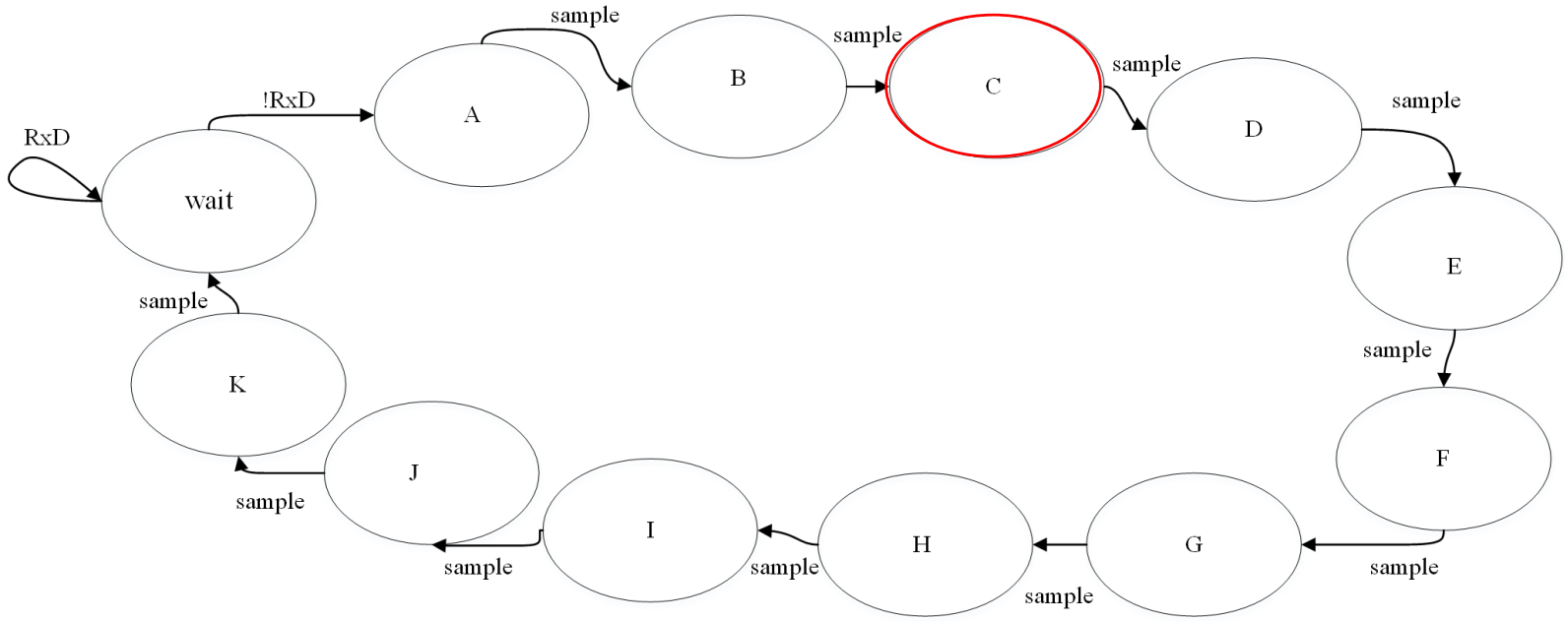


RxD: start bit = 0

DVDES

Receiver

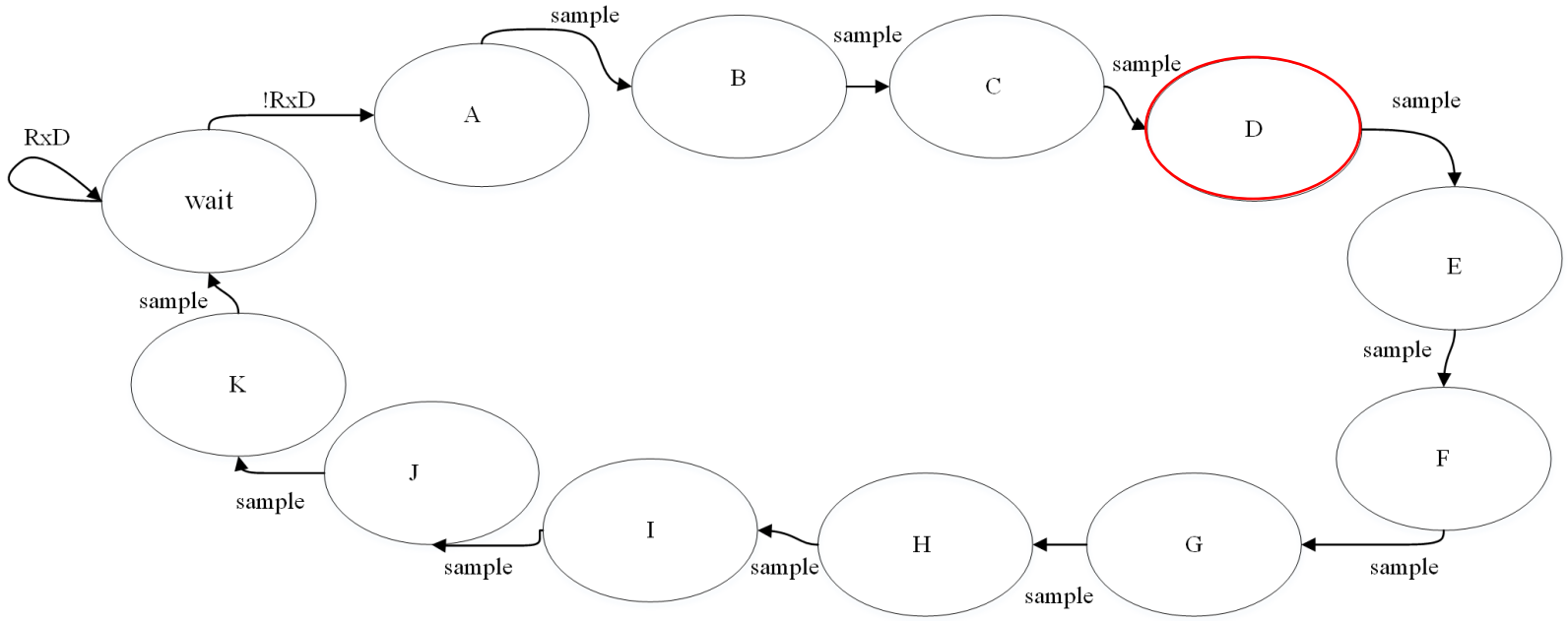
8n1 = 8 bit data, No parity, 1 stop bit



RxD: data[0]

Receiver

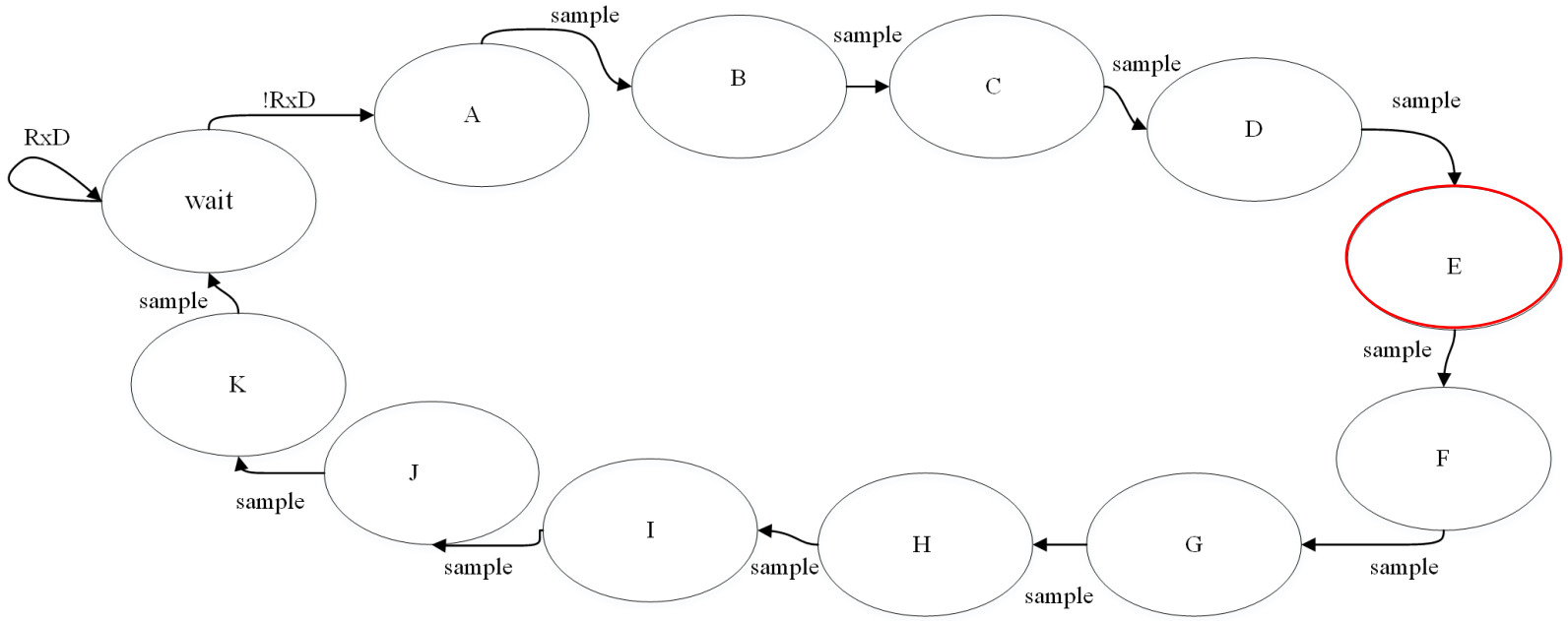
8n1 = 8 bit data, No parity, 1 stop bit



RxD: data[1]

Receiver

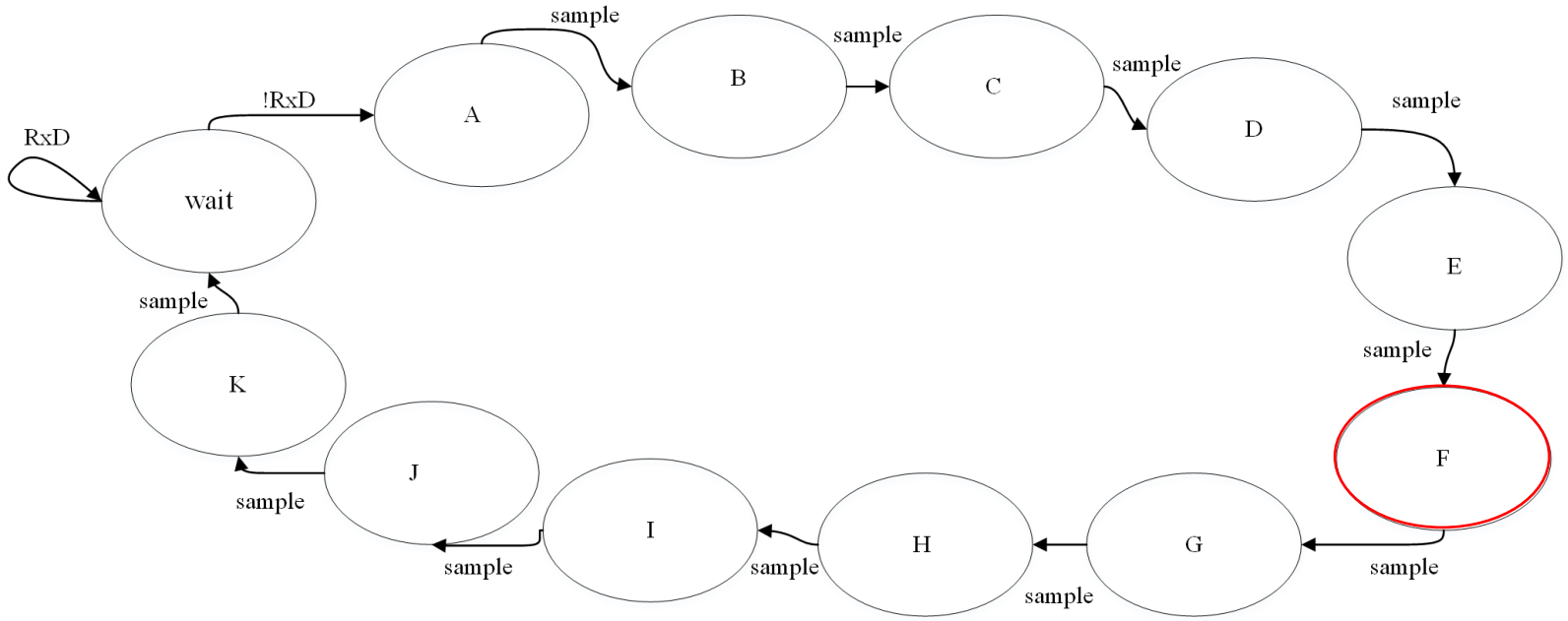
8n1 = 8 bit data, No parity, 1 stop bit



RxD: data[2]

Receiver

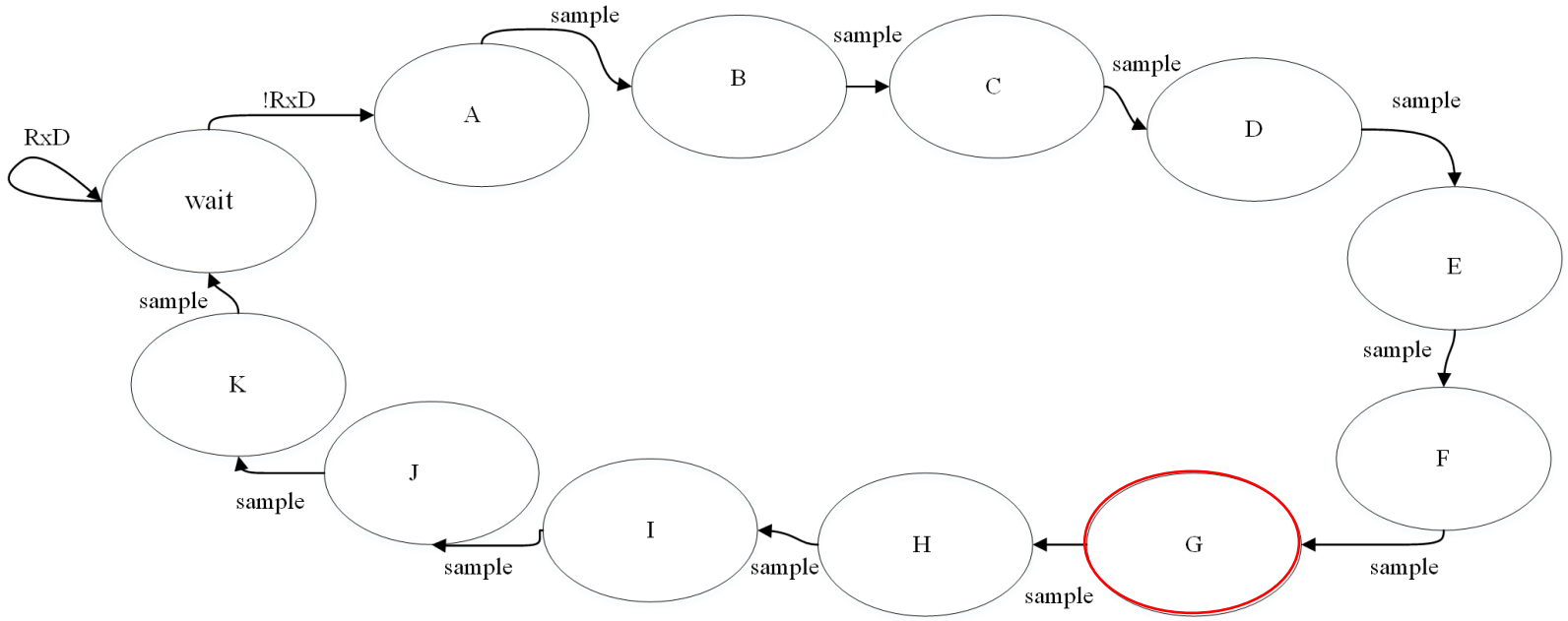
8n1 = 8 bit data, No parity, 1 stop bit



RxD: data[3]

Receiver

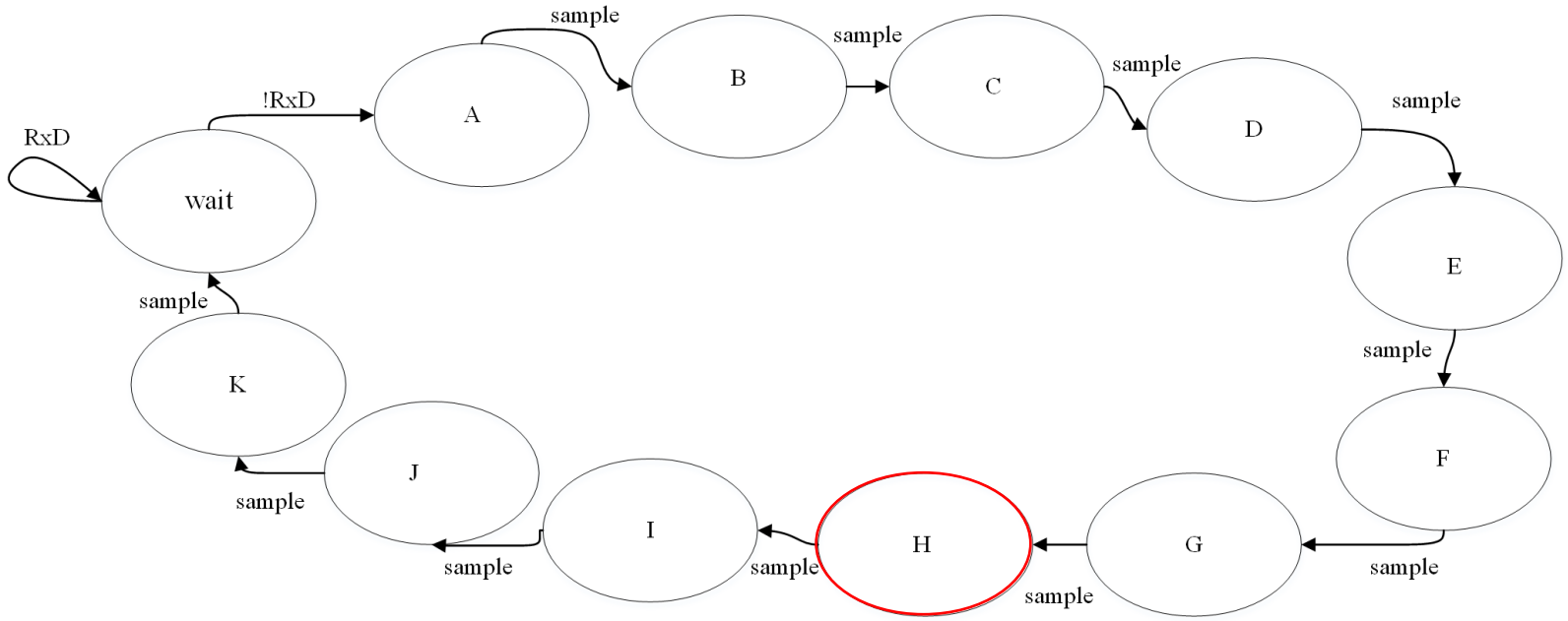
8n1 = 8 bit data, No parity, 1 stop bit



RxD: data[4]

Receiver

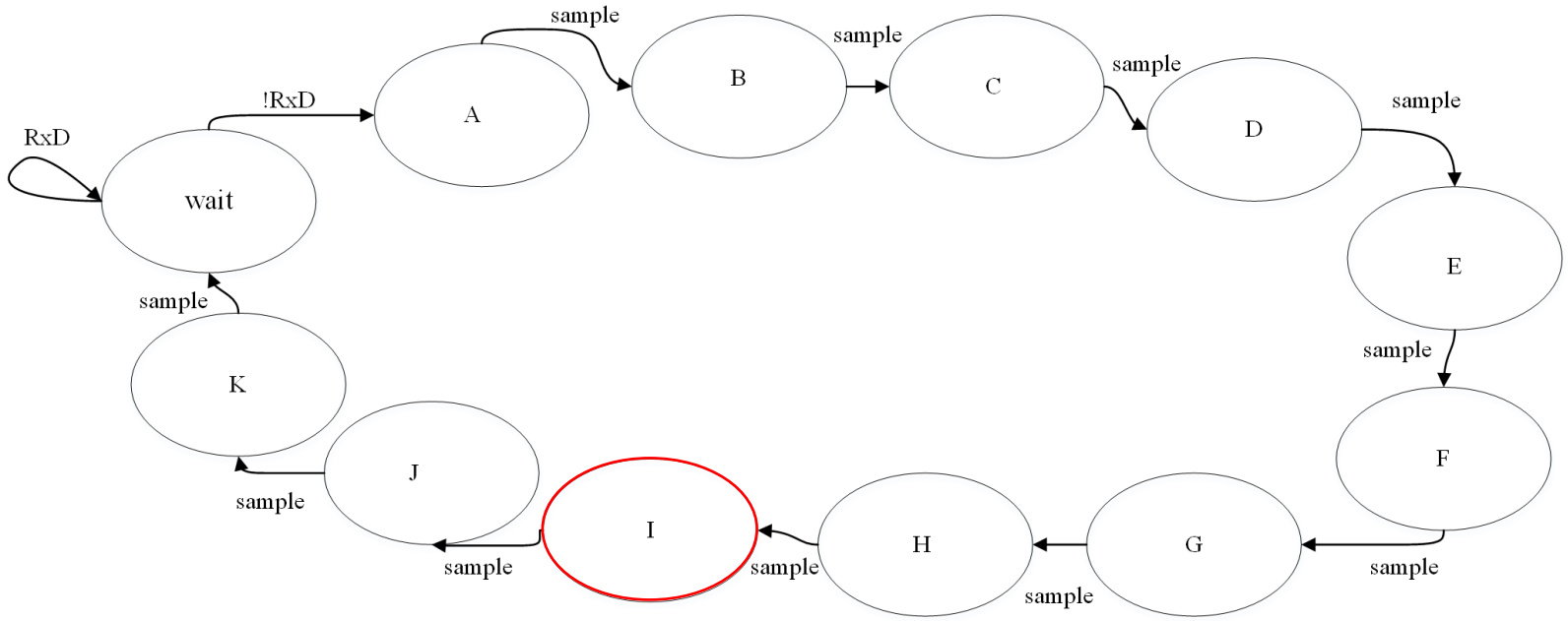
8n1 = 8 bit data, No parity, 1 stop bit



RxD: data[5]

Receiver

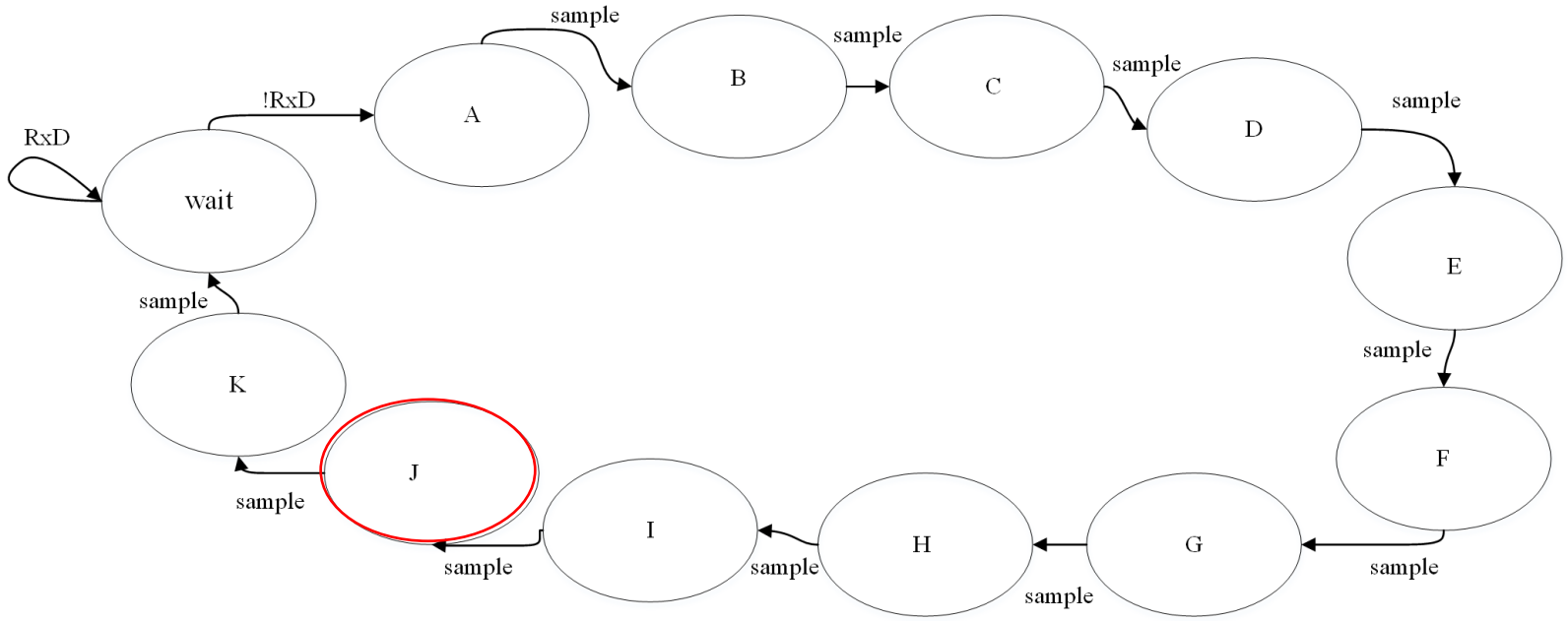
8n1 = 8 bit data, No parity, 1 stop bit



RxD: data[6]

Receiver

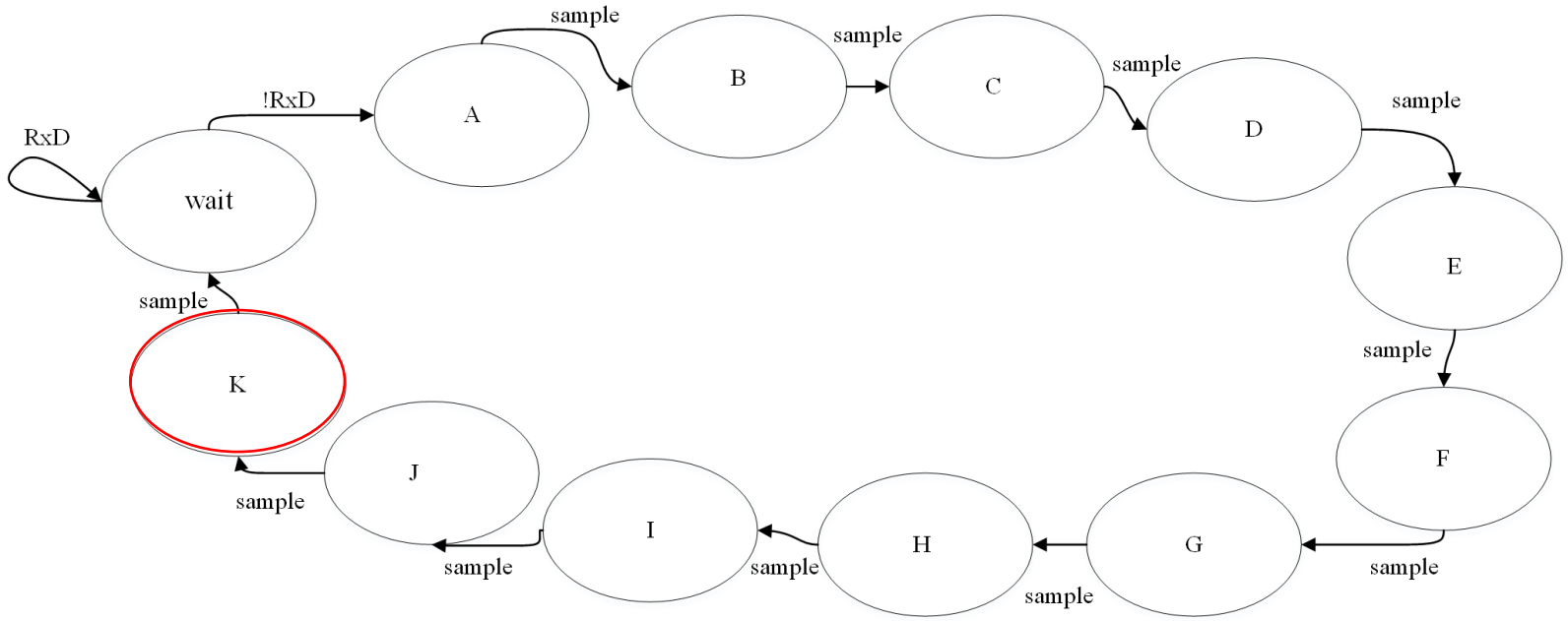
8n1 = 8 bit data, No parity, 1 stop bit



RxD: data[7]

Receiver

8n1 = 8 bit data, No parity, 1 stop bit

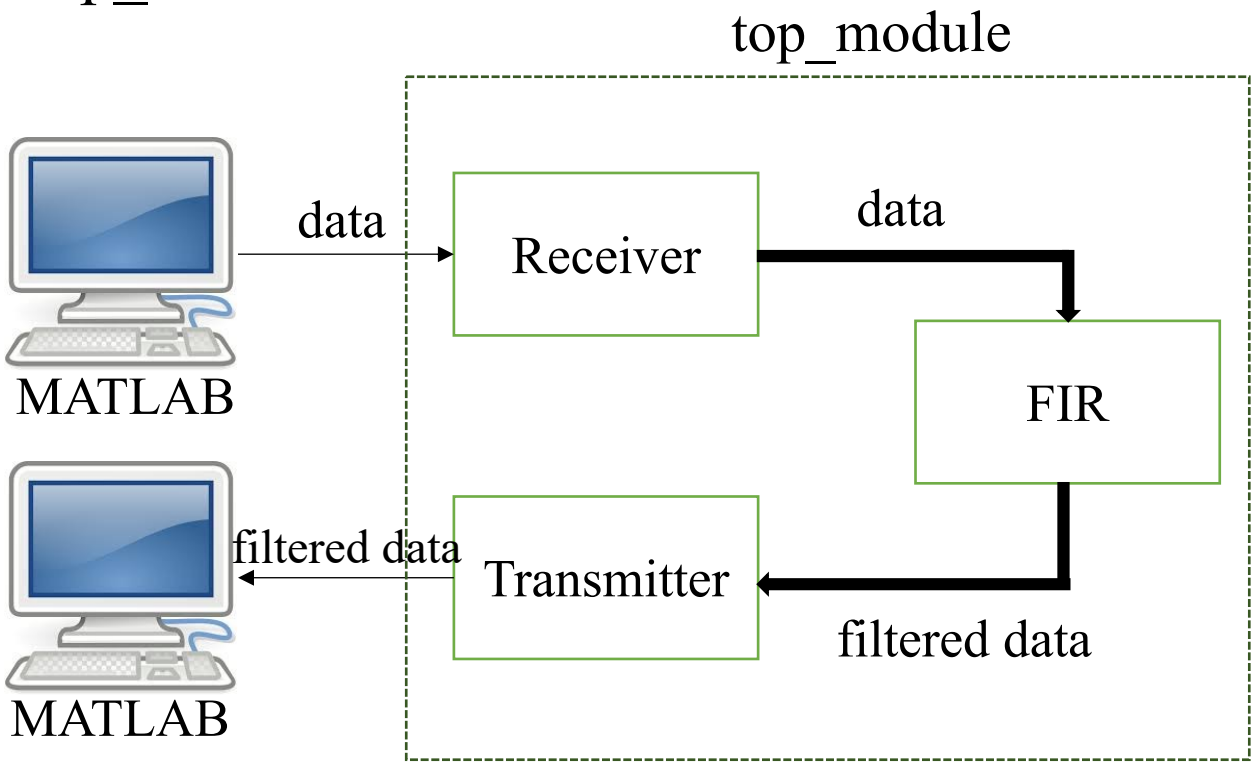


RxD: stop bit = 1

DVDES

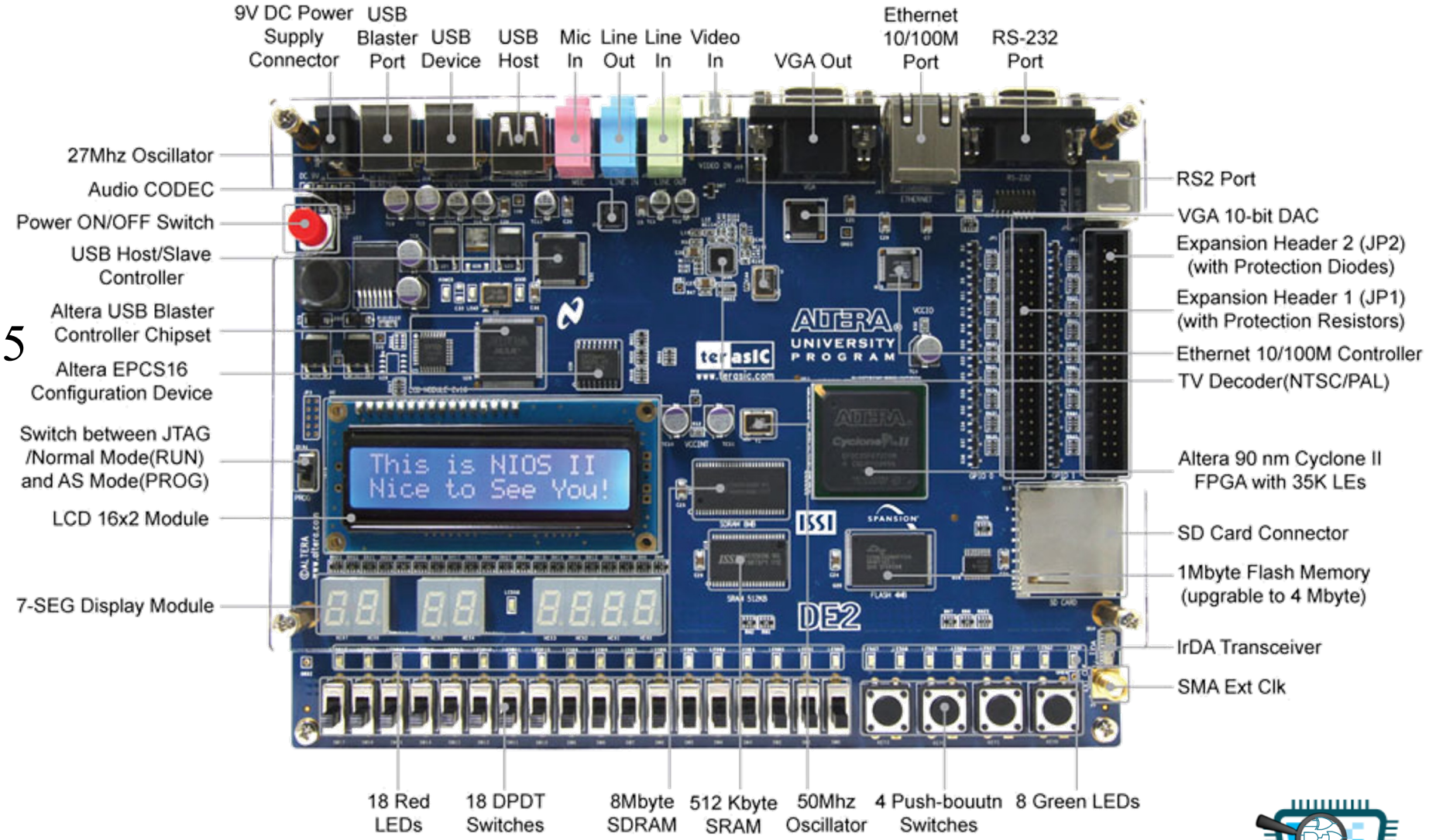
Lab1

Write top_module code



Lab1

DE2
Cyclone II 2C35



DVDES

Quartus II - C:/altera/81/quartus/lab1-1/lab1-1 - lab1-1 - [Pin Planner]

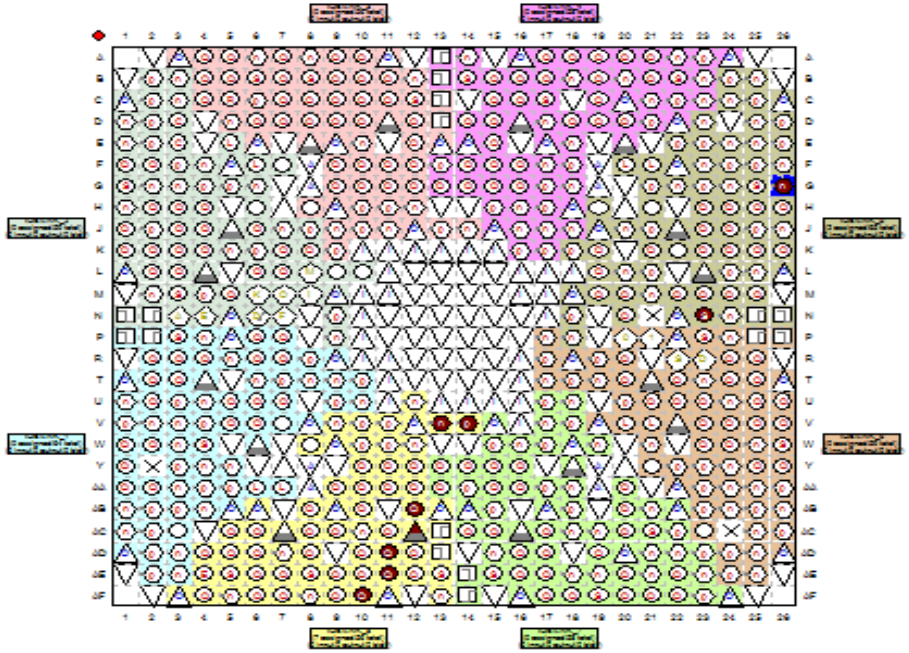
File Edit View Processing Tools Window

Groups

Named:

Node Name	Di
<<new node>>	

Top View - Wire Bond
Cyclone II - EP2C35F672C6



Named: Edit: PIN_G26 Filter: Pins: all

	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard
1	button1_input	Input	PIN_N23	5	B5_N1	3.3-V LVTTL (default)
2	button0_input	Input	PIN_G26	5	B5_N0	3.3-V LVTTL (default)
3	digit0_bottom	Unknown	PIN_AD11	8	B8_N0	3.3-V LVTTL (default)
4	a	Unknown	PIN_AF10	8	B8_N0	3.3-V LVTTL (default)
5	b	Unknown	PIN_AB12	8	B8_N0	3.3-V LVTTL (default)
6	c	Unknown	PIN_AC12	8	B8_N0	3.3-V LVTTL (default)
7	e	Unknown	PIN_AE11	8	B8_N0	3.3-V LVTTL (default)
8	f	Unknown	PIN_V14	8	B8_N0	3.3-V LVTTL (default)
9	g	Unknown	PIN_V13	8	B8_N0	3.3-V LVTTL (default)
10	<<new node>>					

All Pins

For Help, press F1 NUM

Project Navigator Entity Cyclone II: lab1-1

Tasks Flow: Compilatio Task

Message:

For Help, press F

Locate

Thanks for your attention