CS-235

COMPUTER ORGANIZATION AND ASSEMBLY LANGUAGE

ASSIGNMENT # 1

Name:

Mahum Samar

CMS ID:

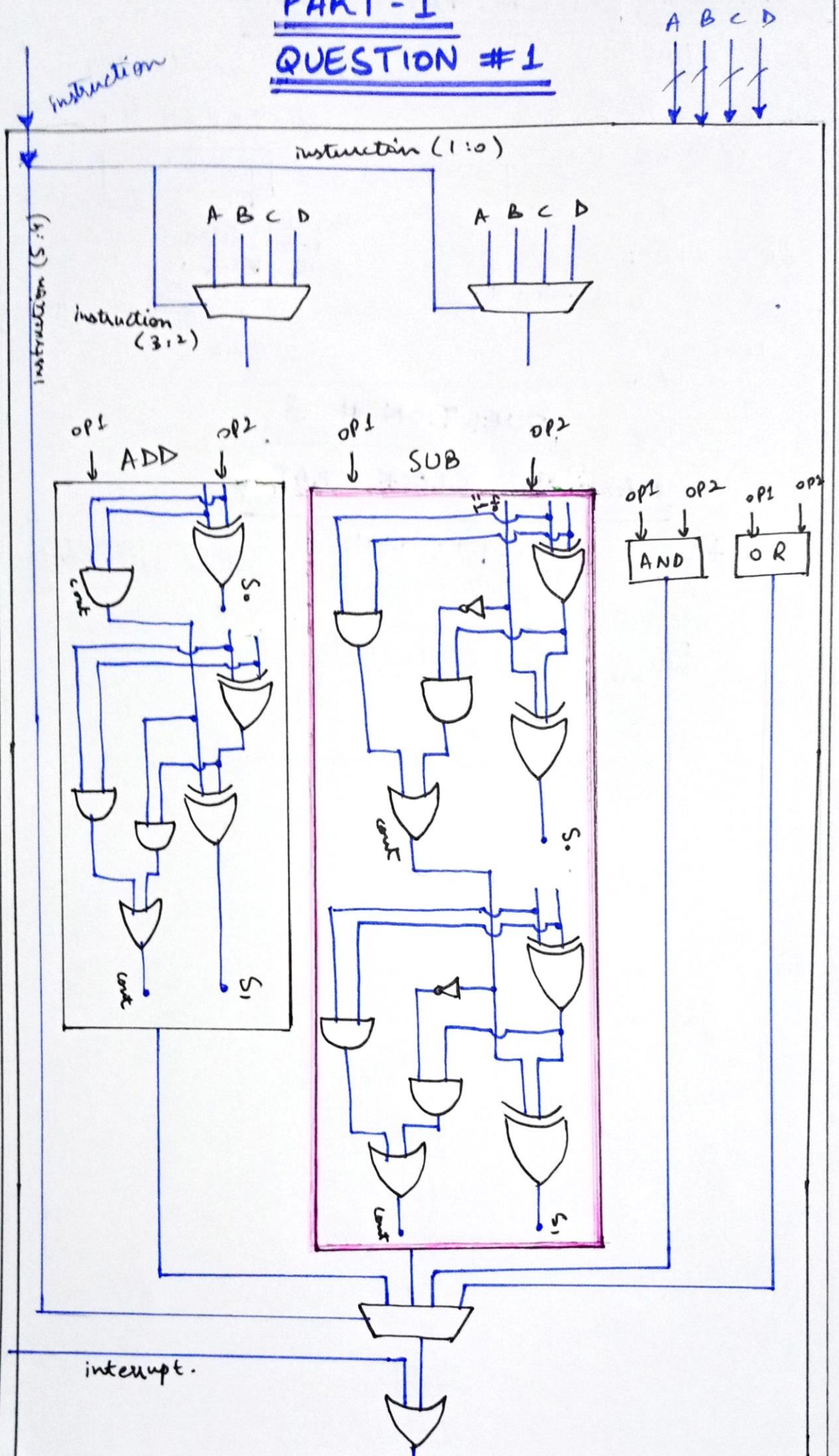
290647

submitted to:

Professor Mohammad Imran

PART - I

QUESTION #1



QUESTION #2 CRITICAL PATH DELAY

FOR ADDER:

$= 0.5 + 4 + 6 + 4 + 2 + 0.3$

$= 16.8$ ns

FOR AND:

$= 0.5 + 2 + 0.3 + 4 + 4 + 2$

$= 12.8$ ns

FOR Subtractor:

$= 0.5 + 4 + 12 + 4 + 2 + 0.3$

$= \boxed{22.8 \text{ ns}}$

Hence, this is critical path delay.

FOR FOR:

$= 0.5 + 0.2 + 0.3 + 4 + 4 + 2$

$= 2.8$ ns

QUESTION # 3

MAXIMUM CLOCK RATE

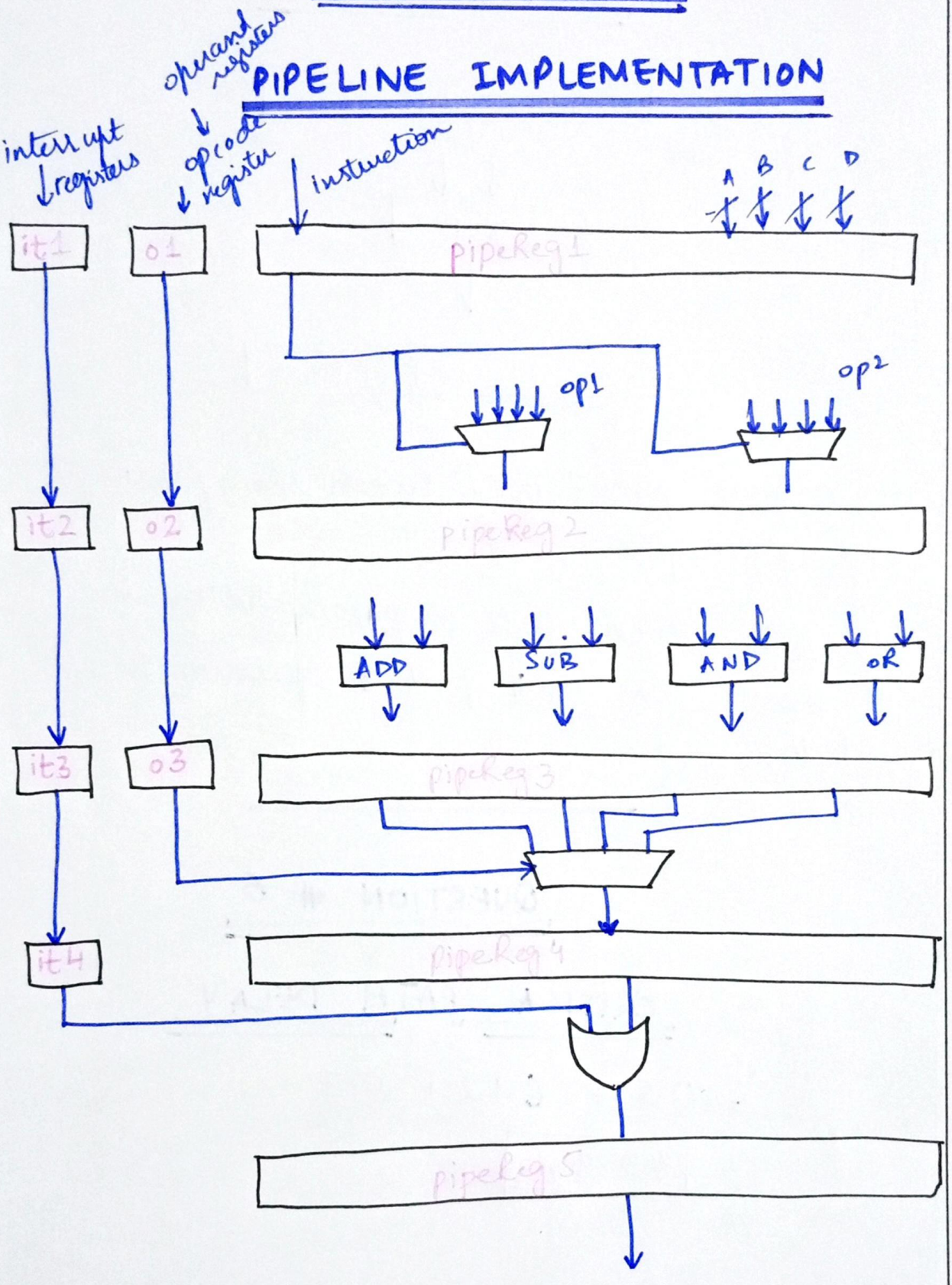
$$f_{clk_{Max}} = \frac{1}{22.8} \text{ Hz} = \frac{1}{\text{critical path delay}}$$

$$f_{clk_{max}} = 43.8596 \text{ MHz}.$$

PART # 2

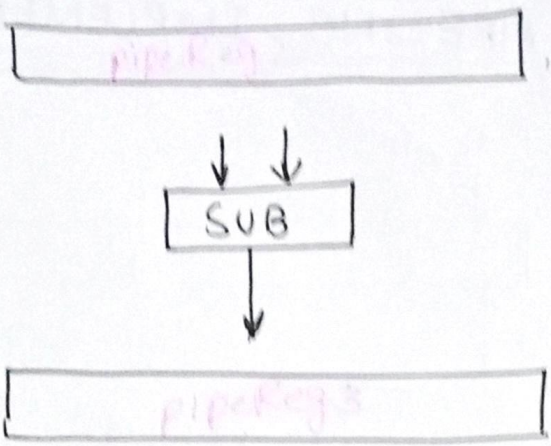
QUESTION # 4

PIPELINE IMPLEMENTATION



QUESTION # 5

CRITICAL PATH



critical path is between the pipeReg 2 and pipeReg 3.

SUB block full implementation is shown in Q # part I question 1 sub block.

QUESTION # 6

CRITICAL PATH DELAY

$= 0.5 + 12 + 0.3$

$= \boxed{12.8 \text{ ns}}$

MAXIMUM CLOCK RATE

$$t_{clk_{MAX}} = \frac{1}{\text{critical path delay}}$$

$$= \frac{1}{12.8}$$

$$t_{clk_{MAX}} = 78.125 \text{ MHz}$$

QUESTION #7

(i)

MACHINE CODE

1. ADD B,C:

00 01 10

2. OR A,D:

11 00 11

3. SUB D,C:

01 11 10

4. AND C,D:

11 11 11 ⇒ bug because interrupt 1

(ii)

BINARY CONTENTS OF REGISTERS

PIPELINE INTERRUPT REGISTER

clock cycle	it1 1-bit	it2 1-bit	it 3 1-bit	it 4 1-bit
1	0			
2	0	0		
3	0	0	0	
4	1	0	0	0
5		1	0	0
6			1	0
7				1

PIPELINE OPERATOR REGISTERS

clock cycle	2-bit 01	2-bit 02	2-bit 03
1	00		
2	11	00	
3	01	11	00
4	10	01	11
5		10	01
6			10

PIPELINE OPERAND REGISTERS

	4-bit	4-bit	8-bit	2-bit	2-bit
clock cycle	pipeReg1	pipeReg2	pipeReg3	pipeReg4	pipeReg5
1	01 10				
2	00 11	01 10			
3	11 10	00 11	11 01 00 11		
4	10 11	11 10	11 01 00 11	11	
5		10 11	01 01 10 11	11	11
6			01 01 10 11	01	01
7				10	11
8					11