CAZENAVE Maïté CS472

<u>Computer Architecture Projet 1 :</u> MIPS Disassembler

All Output \$

sub \$17, \$13, \$21 7A060 lw \$19, 24(\$23) 7A064 beq \$21, \$7 7A068 7A07C 7A06C add \$19, \$8, \$19 7A070 sw \$19, 24(\$12) 7A074 and \$19, \$9, \$15 7A078 sw \$15, -12(\$12) add \$12, \$12, \$12 7A07C or \$21, \$4, \$21 7A080 7A084 bne \$12, \$15 7A060 7A088 lw \$25, -16(\$18)