Computer Architecture Project 3 :
Pipeline

```
CYCLE 1
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 103
$4 : 104
$5 : 105
$6 : 106
$7 : 107
$8 : 108
$9 : 109
$10 : 10A
$11 : 10B
$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 118
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D
$30 : 11E
$31 : 11F


IF/ID Pipeline Write Version:
Inst = A1020000

IF/ID Pipeline Read Version:
Inst = 0


ID/EX Pipeline Write Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0,
MemToReg=0, RegWrite=1 []
ReadReg1Value = 0
ReadReg2Value = 0
SEOffset = 0
WriteReg_20_16 = 0
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WriteReg_15_11 = 0
Function = 0

ID/EX Pipeline Read Version:
Control: RegDst=0, ALUSrc=0, ALUOp=0, MemRead=0, MemWrite=0,
MemToReg=0, RegWrite=0 []
ReadReg1Value = 0
ReadReg2Value = 0
SEOffset = 0
WriteReg_20_16 = 0
WriteReg_15_11 = 0
Function = 0

EX/MEM Pipeline Write Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 []
ALUResult = 0
SBValue = 0
WriteRegNum = 0

EX/MEM Pipeline Read Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 []
ALUResult = 0
SBValue = 0
WriteRegNum = 0

MEM/WB Pipeline Write Version:
Control: MemToReg=0, RegWrite=0 []
ALUResult = 0
LBValue = 0 @ 0
WriteRegNum = 0

MEM/WB Pipeline Read Version:
Control: MemToReg=0, RegWrite=0 []
ALUResult = 0
LBValue = 0 @ 0
WriteRegNum= 0

CYCLE 2
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 103
$4 : 104
$5 : 105
$6 : 106
$7 : 107
$8 : 108
$9 : 109
$10 : 10A
$11 : 10B

$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 118
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D
$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 810AFFFC

IF/ID Pipeline Read Version:
Inst = A1020000

ID/EX Pipeline Write Version:
Control: RegDst=1, ALUSrc=1, ALUOp=0, MemRead=0, MemWrite=1,
MemToReg=0, RegWrite=0 [sb]
ReadReg1Value = 108
ReadReg2Value = 102
SEOffset = 0
WriteReg_20_16 = 2
WriteReg_15_11 = 0
Function = 28

ID/EX Pipeline Read Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0,
MemToReg=0, RegWrite=1 []
ReadReg1Value = 0
ReadReg2Value = 0
SEOffset = 0
WriteReg_20_16 = 0
WriteReg_15_11 = 0
Function = 0

EX/MEM Pipeline Write Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 []
ALUResult = 0
SBValue = 0

```
WriteRegNum = 0

EX/MEM Pipeline Read Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 []
ALUResult = 0
SBValue = 0
WriteRegNum = 0


MEM/WB Pipeline Write Version:
Control: MemToReg=0, RegWrite=0 []
ALUResult = 0
LBValue = 0 @ 0
WriteRegNum = 0

MEM/WB Pipeline Read Version:
Control: MemToReg=0, RegWrite=0 []
ALUResult = 0
LBValue = 0 @ 0
WriteRegNum= 0


CYCLE 3
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 103
$4 : 104
$5 : 105
$6 : 106
$7 : 107
$8 : 108
$9 : 109
$10 : 10A
$11 : 10B
$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 118
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D
```

$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 831820

IF/ID Pipeline Read Version:
Inst = 810AFFFC

ID/EX Pipeline Write Version:
Control: RegDst=0, ALUSrc=1, ALUOp=0, MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ReadReg1Value = 108
ReadReg2Value = 10A
SEOffset = FFFC
WriteReg_20_16 = 10
WriteReg_15_11 = 31
Function = 20

ID/EX Pipeline Read Version:
Control: RegDst=1, ALUSrc=1, ALUOp=0, MemRead=0, MemWrite=1, MemToReg=0, RegWrite=0 [sb]
ReadReg1Value = 108
ReadReg2Value = 102
SEOffset = 0
WriteReg_20_16 = 2
WriteReg_15_11 = 0
Function = 28

EX/MEM Pipeline Write Version:
Control: MemRead=0, MemWrite=1, MemToReg=0, RegWrite=0 [sb]
ALUResult = 108
SBValue = 102
WriteRegNum = 0

EX/MEM Pipeline Read Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 []
ALUResult = 0
SBValue = 0
WriteRegNum = 0

MEM/WB Pipeline Write Version:
Control: MemToReg=0, RegWrite=1 []
ALUResult = 0
LBValue = 0 @ 0
WriteRegNum = 0

MEM/WB Pipeline Read Version:
Control: MemToReg=0, RegWrite=0 []
ALUResult = 0

LBValue = 0 @ 0
WriteRegNum= 0

CYCLE 4
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 103
$4 : 104
$5 : 105
$6 : 106
$7 : 107
$8 : 108
$9 : 109
$10 : 10A
$11 : 10B
$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 118
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D
$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 1263820

IF/ID Pipeline Read Version:
Inst = 831820

ID/EX Pipeline Write Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0,
MemToReg=0, RegWrite=1 [add]
ReadReg1Value = 104
ReadReg2Value = 103
SEOffset = FFFC
WriteReg_20_16 = 3

WriteReg_15_11 = 3
Function = 20

ID/EX Pipeline Read Version:
Control: RegDst=0, ALUSrc=1, ALUOp=0, MemRead=1, MemWrite=0,
MemToReg=1, RegWrite=1 [lb]
ReadReg1Value = 108
ReadReg2Value = 10A
SEOffset = FFFC
WriteReg_20_16 = 10
WriteReg_15_11 = 31
Function = 20

EX/MEM Pipeline Write Version:
Control: MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ALUResult = 104
SBValue = 102
WriteRegNum = 10

EX/MEM Pipeline Read Version:
Control: MemRead=0, MemWrite=1, MemToReg=0, RegWrite=0 [sb]
ALUResult = 108
SBValue = 102
WriteRegNum = 0

MEM/WB Pipeline Write Version:
Control: MemToReg=0, RegWrite=0 [sb]
ALUResult = 108
LBValue = 0 @ 108
WriteRegNum = 0

MEM/WB Pipeline Read Version:
Control: MemToReg=0, RegWrite=1 []
ALUResult = 0
LBValue = 0 @ 0
WriteRegNum= 0

CYCLE 5
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 103
$4 : 104
$5 : 105
$6 : 106
$7 : 107
$8 : 108
$9 : 109
$10 : 10A
$11 : 10B

$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 118
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D
$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 1224820

IF/ID Pipeline Read Version:
Inst = 1263820

ID/EX Pipeline Write Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ReadReg1Value = 109
ReadReg2Value = 106
SEOffset = FFFC
WriteReg_20_16 = 6
WriteReg_15_11 = 7
Function = 20

ID/EX Pipeline Read Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ReadReg1Value = 104
ReadReg2Value = 103
SEOffset = FFFC
WriteReg_20_16 = 3
WriteReg_15_11 = 3
Function = 20

EX/MEM Pipeline Write Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ALUResult = 207
SBValue = 102

WriteRegNum = 3

EX/MEM Pipeline Read Version:
Control: MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ALUResult = 104
SBValue = 102
WriteRegNum = 10

MEM/WB Pipeline Write Version:
Control: MemToReg=1, RegWrite=1 [lb]
ALUResult = 104
LBValue = 4 @ 104
WriteRegNum = 10

MEM/WB Pipeline Read Version:
Control: MemToReg=0, RegWrite=0 [sb]
ALUResult = 108
LBValue = 0 @ 108
WriteRegNum= 10

CYCLE 6
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 103
$4 : 104
$5 : 105
$6 : 106
$7 : 107
$8 : 108
$9 : 109
$10 : 4
$11 : 10B
$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 118
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D

$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 81180000

IF/ID Pipeline Read Version:
Inst = 1224820

ID/EX Pipeline Write Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ReadReg1Value = 109
ReadReg2Value = 102
SEOffset = FFFC
WriteReg_20_16 = 2
WriteReg_15_11 = 9
Function = 20

ID/EX Pipeline Read Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ReadReg1Value = 109
ReadReg2Value = 106
SEOffset = FFFC
WriteReg_20_16 = 6
WriteReg_15_11 = 7
Function = 20

EX/MEM Pipeline Write Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ALUResult = 20F
SBValue = 102
WriteRegNum = 7

EX/MEM Pipeline Read Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ALUResult = 207
SBValue = 102
WriteRegNum = 3

MEM/WB Pipeline Write Version:
Control: MemToReg=0, RegWrite=1 [add]
ALUResult = 207
LBValue = 4 @ 207
WriteRegNum = 3

MEM/WB Pipeline Read Version:
Control: MemToReg=1, RegWrite=1 [lb]
ALUResult = 104

LBValue = 4 @ 104
WriteRegNum= 3

CYCLE 7
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 207
$4 : 104
$5 : 105
$6 : 106
$7 : 107
$8 : 108
$9 : 109
$10 : 4
$11 : 10B
$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 118
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D
$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 81510010

IF/ID Pipeline Read Version:
Inst = 81180000

ID/EX Pipeline Write Version:
Control: RegDst=0, ALUSrc=1, ALUOp=0, MemRead=1, MemWrite=0,
MemToReg=1, RegWrite=1 [lb]
ReadReg1Value = 108
ReadReg2Value = 118
SEOffset = 0
WriteReg_20_16 = 24

WriteReg_15_11 = 0
Function = 20

ID/EX Pipeline Read Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0,
MemToReg=0, RegWrite=1 [add]
ReadReg1Value = 109
ReadReg2Value = 102
SEOffset = FFFC
WriteReg_20_16 = 2
WriteReg_15_11 = 9
Function = 20

EX/MEM Pipeline Write Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ALUResult = 20B
SBValue = 102
WriteRegNum = 9

EX/MEM Pipeline Read Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ALUResult = 20F
SBValue = 102
WriteRegNum = 7

MEM/WB Pipeline Write Version:
Control: MemToReg=0, RegWrite=1 [add]
ALUResult = 20F
LBValue = 4 @ 20F
WriteRegNum = 7

MEM/WB Pipeline Read Version:
Control: MemToReg=0, RegWrite=1 [add]
ALUResult = 207
LBValue = 4 @ 207
WriteRegNum= 7

CYCLE 8
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 207
$4 : 104
$5 : 105
$6 : 106
$7 : 20F
$8 : 108
$9 : 109
$10 : 4
$11 : 10B

$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 118
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D
$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 624022

IF/ID Pipeline Read Version:
Inst = 81510010

ID/EX Pipeline Write Version:
Control: RegDst=0, ALUSrc=1, ALUOp=0, MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ReadReg1Value = 4
ReadReg2Value = 111
SEOffset = 10
WriteReg_20_16 = 17
WriteReg_15_11 = 0
Function = 20

ID/EX Pipeline Read Version:
Control: RegDst=0, ALUSrc=1, ALUOp=0, MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ReadReg1Value = 108
ReadReg2Value = 118
SEOffset = 0
WriteReg_20_16 = 24
WriteReg_15_11 = 0
Function = 20

EX/MEM Pipeline Write Version:
Control: MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ALUResult = 108
SBValue = 102

WriteRegNum = 24

EX/MEM Pipeline Read Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [add]
ALUResult = 20B
SBValue = 102
WriteRegNum = 9

MEM/WB Pipeline Write Version:
Control: MemToReg=0, RegWrite=1 [add]
ALUResult = 20B
LBValue = 4 @ 20B
WriteRegNum = 9

MEM/WB Pipeline Read Version:
Control: MemToReg=0, RegWrite=1 [add]
ALUResult = 20F
LBValue = 4 @ 20F
WriteRegNum= 9

CYCLE 9
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 207
$4 : 104
$5 : 105
$6 : 106
$7 : 20F
$8 : 108
$9 : 20B
$10 : 4
$11 : 10B
$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 118
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D

$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 0

IF/ID Pipeline Read Version:
Inst = 624022

ID/EX Pipeline Write Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [sub]
ReadReg1Value = 207
ReadReg2Value = 102
SEOffset = 10
WriteReg_20_16 = 2
WriteReg_15_11 = 8
Function = 22

ID/EX Pipeline Read Version:
Control: RegDst=0, ALUSrc=1, ALUOp=0, MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ReadReg1Value = 4
ReadReg2Value = 111
SEOffset = 10
WriteReg_20_16 = 17
WriteReg_15_11 = 0
Function = 20

EX/MEM Pipeline Write Version:
Control: MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ALUResult = 14
SBValue = 102
WriteRegNum = 17

EX/MEM Pipeline Read Version:
Control: MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ALUResult = 108
SBValue = 102
WriteRegNum = 24

MEM/WB Pipeline Write Version:
Control: MemToReg=1, RegWrite=1 [lb]
ALUResult = 108
LBValue = 102 @ 108
WriteRegNum = 24

MEM/WB Pipeline Read Version:
Control: MemToReg=0, RegWrite=1 [add]
ALUResult = 20B

LBValue = 4 @ 20B
WriteRegNum= 24

CYCLE 10
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 207
$4 : 104
$5 : 105
$6 : 106
$7 : 20F
$8 : 108
$9 : 20B
$10 : 4
$11 : 10B
$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 111
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 102
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D
$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 0

IF/ID Pipeline Read Version:
Inst = 0

ID/EX Pipeline Write Version:
Control: RegDst=0, ALUSrc=0, ALUOp=0, MemRead=0, MemWrite=0,
MemToReg=0, RegWrite=0 [NOP]
ReadReg1Value = 0
ReadReg2Value = 0
SEOffset = 0
WriteReg_20_16 = 0

WriteReg_15_11 = 0
Function = 0

ID/EX Pipeline Read Version:
Control: RegDst=1, ALUSrc=0, ALUOp=A, MemRead=0, MemWrite=0,
MemToReg=0, RegWrite=1 [sub]
ReadReg1Value = 207
ReadReg2Value = 102
SEOffset = 10
WriteReg_20_16 = 2
WriteReg_15_11 = 8
Function = 22

EX/MEM Pipeline Write Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [sub]
ALUResult = 105
SBValue = 102
WriteRegNum = 8

EX/MEM Pipeline Read Version:
Control: MemRead=1, MemWrite=0, MemToReg=1, RegWrite=1 [lb]
ALUResult = 14
SBValue = 102
WriteRegNum = 17

MEM/WB Pipeline Write Version:
Control: MemToReg=1, RegWrite=1 [lb]
ALUResult = 14
LBValue = 14 @ 14
WriteRegNum = 17

MEM/WB Pipeline Read Version:
Control: MemToReg=1, RegWrite=1 [lb]
ALUResult = 108
LBValue = 102 @ 108
WriteRegNum= 17

CYCLE 11
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 207
$4 : 104
$5 : 105
$6 : 106
$7 : 20F
$8 : 108
$9 : 20B
$10 : 4
$11 : 10B

$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 14
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 102
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D
$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 0

IF/ID Pipeline Read Version:
Inst = 0

ID/EX Pipeline Write Version:
Control: RegDst=0, ALUSrc=0, ALUOp=0, MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 [NOP]
ReadReg1Value = 0
ReadReg2Value = 0
SEOffset = 0
WriteReg_20_16 = 0
WriteReg_15_11 = 0
Function = 0

ID/EX Pipeline Read Version:
Control: RegDst=0, ALUSrc=0, ALUOp=0, MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 [NOP]
ReadReg1Value = 0
ReadReg2Value = 0
SEOffset = 0
WriteReg_20_16 = 0
WriteReg_15_11 = 0
Function = 0

EX/MEM Pipeline Write Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 [NOP]
ALUResult = 0
SBValue = 0

WriteRegNum = 0

EX/MEM Pipeline Read Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=1 [sub]
ALUResult = 105
SBValue = 102
WriteRegNum = 8

MEM/WB Pipeline Write Version:
Control: MemToReg=0, RegWrite=1 [sub]
ALUResult = 105
LBValue = 14 @ 105
WriteRegNum = 8

MEM/WB Pipeline Read Version:
Control: MemToReg=1, RegWrite=1 [lb]
ALUResult = 14
LBValue = 14 @ 14
WriteRegNum= 8

CYCLE 12
Registers
$0 : 0
$1 : 101
$2 : 102
$3 : 207
$4 : 104
$5 : 105
$6 : 106
$7 : 20F
$8 : 105
$9 : 20B
$10 : 4
$11 : 10B
$12 : 10C
$13 : 10D
$14 : 10E
$15 : 10F
$16 : 110
$17 : 14
$18 : 112
$19 : 113
$20 : 114
$21 : 115
$22 : 116
$23 : 117
$24 : 102
$25 : 119
$26 : 11A
$27 : 11B
$28 : 11C
$29 : 11D

$30 : 11E
$31 : 11F

IF/ID Pipeline Write Version:
Inst = 0

IF/ID Pipeline Read Version:
Inst = 0

ID/EX Pipeline Write Version:
Control: RegDst=0, ALUSrc=0, ALUOp=0, MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 [NOP]
ReadReg1Value = 0
ReadReg2Value = 0
SEOffset = 0
WriteReg_20_16 = 0
WriteReg_15_11 = 0
Function = 0

ID/EX Pipeline Read Version:
Control: RegDst=0, ALUSrc=0, ALUOp=0, MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 [NOP]
ReadReg1Value = 0
ReadReg2Value = 0
SEOffset = 0
WriteReg_20_16 = 0
WriteReg_15_11 = 0
Function = 0

EX/MEM Pipeline Write Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 [NOP]
ALUResult = 0
SBValue = 0
WriteRegNum = 0

EX/MEM Pipeline Read Version:
Control: MemRead=0, MemWrite=0, MemToReg=0, RegWrite=0 [NOP]
ALUResult = 0
SBValue = 0
WriteRegNum = 0

MEM/WB Pipeline Write Version:
Control: MemToReg=0, RegWrite=0 [NOP]
ALUResult = 0
LBValue = 0 @ 0
WriteRegNum = 0

MEM/WB Pipeline Read Version:
Control: MemToReg=0, RegWrite=1 [sub]
ALUResult = 105

LBValue = 14 @ 105
WriteRegNum= 0