小任务解析

这个任务最终是实现一个模60计数器，即每60个时钟周期为一次循环。

文件导入后`Vivado`会根据代码包含的例化关系自动构建出项目结构。

```
count60.v
|--count10.v
|--count6.v
```

下面是比较规范的代码写法和注释（via第二组）

希望大家能够根据我发的教程，完全理解`wire、reg、连续赋值、过程赋值`的含义，这在下一步的实验中非常重要。

```
// count10.v
module count_10(
    input wire rst,
    input wire clk,
    input wire en,
    output reg [3:0] count,
    output reg co
);
    always @ (posedge clk) begin
        if (rst) begin
            count <= 4'b0;
            co <= 1'b0;
        end
        else if (en) begin
            if (count == 4'd9) begin
                count <= 4'b0;
                co <=1'b0;
            end
            else if(count == 4'd8) begin
                count <= count + 1'b1;
                co <= 1'b1;
            end
            else begin
                count <= count + 1'b1;
                co <= 1'b0;
            end
        end
    end
endmodule
```

```
// count6.v
module count_6(
    input wire rst,
    input wire clk,
    input wire en,
    output reg [3:0] count,
```

```
    output reg co
);
    always @ (posedge clk) begin
        if (rst) begin
            count <= 4'b0;
            co <= 1'b0;
        end
        else if (en) begin
            if (count == 4'd5) begin
                count <= 4'b0;
                co <=1'b0;
            end
            else if(count == 4'd4)begin
                co <= 1'b1;
                count <=count + 1'b1;
            end
            else begin
                count <= count + 1'b1;
                co <= 1'b0;
            end
        end
    end
endmodule
```

```
// count60.v
module count_60(
    input wire rst,
    input wire clk,
    input wire en,
    output wire [7:0] count,
    output wire co
);
    wire co10,co6,co10_j;
    wire [3:0] count10, count6;
    count_10 u_count_10(
        .rst   (rst     ),
        .clk   (clk     ),
        .en    (en      ),
        .count (count10 ),
        .co    (co10_j  )
    );// 引入模10计数器
    wire en_6;
    assign en_6=co10_j&en;// 模10计数器进位时模6计数器才会自增
    count_6 u_count_6(
        .rst   (rst    ),
        .clk   (clk    ),
        .en    (en_6   ),
        .count (count6 ),
        .co    (co6    )
    );// 引入模6计数器
    assign co=en_6&co6;// 模6计数器完成一次循环 即模60
    assign count= {count6,count10};
endmodule
```

```v
// count60_tb.v
module count60_tb(

    );
    reg rst;
    reg clk;
    reg en;
    wire [7:0] count;
    wire co;
    initial begin
        rst = 0;
        clk = 0;
        en = 0;
        #100
        rst = 1;
        #40
        rst = 0;
        en = 1;
    end

    always #2 clk = ~clk;
    count_60 count60(rst,clk,en,count,co);
endmodule
```