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Paper Code : CS-403

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) The main memory of a computer has 2 cm blocks while the cache has 2c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set; then block k of the main memory maps to the set

   a) (k mod m) of the cache

   b) (k mod c) of the cache

   c) (k mod $2m$) of the cache

   d) (k mod $2c$) of the cache.

ii) Suppose the time delay of the four stages of a pipeline are t1 = 60 ns, t2 = 50 ns, t3 = 90 ns, t4 = 80 ns respectively and the interface latch has a delay t1 = 10 ns, then the maximum clock frequency for the pipeline is

a) 100 ns b) 90 ns

c) 190 ns d) 30 ns.

iii) As the bus in a multiprocessor is a shared resource, so there must be some mechanism to resolve the conflict. The ..... algorithm form the below mentioned is not a conflict resolution technique.

a) State priority Algorithm

b) FIFO Algorithm

c) LRU Algorithm

d) Daisy Chaining Algorithm.

iv) Dynamic pipeline allows

a) Multiple functions to evaluate

b) Only streamline connection

c) Perform fixed function

d) None of the above.

v) A computer with cache access time of 100 ns, a main memory access time of 1000 ns and a hit ratio of 0·9 produces an average access time of

a) 250 ns b) 200 ns

c) 190 ns d) 80 ns.

vi) The number of cycles required to complete n tasks in a k stage pipeline is

a) $k+n-1$ b) $nk+1$

c) k d) None of these.

vii) The prefetching technique is a solution for

a) Data hazard

b) Structural Hazard

c) Control Hazard

d) Enhancing the speed of pipeline.

viii) In general an n input Omega network requires ..... stages of 2 * 2 switches.

a) 2 b) 4

c) 8 d) 16.

ix) Which of the following has no practical usage ?

a) SISD b) SIMD

c) MISD d) MIMD.

x) The expression for Amdahl's law is

a) $S(n) = 1/f$ where $n \to \infty$

b) $S(n) = f$ where $n \to \infty$

c) $S(n) = 1/T$ where $n \to \infty$

d) None of these.

GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. If there are no stalls (waits) then prove that the speedup is equal to the pipeline depth i.e. the number of pipeline stages.

OR

Show that the maximum speedup of a pipeline is equal to its stages.

3. Draw pipeline execution diagram during the execution of the following instructions :

MUL R1, R2, R3

ADD R2, R3, R4

INC R4

SUB R6, R3, R7

Find out the delay in pipeline execution due to data dependency of the above instructions. 3 + 2

4. How "Reservation Table" helps to study the performance of pipeline.

5. What do you mean cache coherence problem ? Describe one method to remove this problem and its limitations.

1 + 4

6. Consider the execution of a program of 15000 instructions by linear pipeline processor. The clock rate of pipeline is 25 MHz. Pipeline has five stages and one instruction is issued per clock cycle. Neglect pipelines due to branch instructions and out of sequence execution :

   (i) Calculate the speedup program execution by pipeline as compared with that by non-pipelined processor.

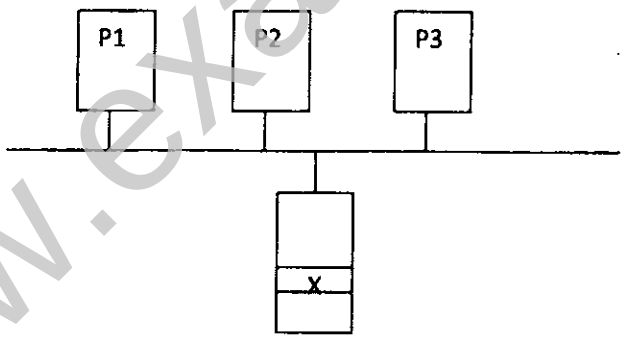
   (ii) What are the efficiency and throughput of the pipeline processor. 3 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. What is the difference between broadcast and invalidate protocols ? Explain MESI protocol. What is the difference between centralized shared memory and distributed shared memory ? Explain superscalar, super-pipelined and VLIW processors.



The value of X (shared memory) is 50. P1 and P3 want to read X and store in their cache memories. At t1 time P1 wants to write on X for three times. After that P3 wants to read for two times. After that first P3 writes on X and then P2 wants to read.

Explain the above mentioned scenario using Write through update, Write back update, Write through invalidate. Write back invalidate protocols.

2 + 4 + 2 + 4 + 3

8. Explain Flynn's classification. What are the differences between loosely coupled system and tightly coupled system ? Construct a multiport network where three processing elements want to connect with three memory modules. Design a network where 25 inputs want to connect with 9 outputs. What is the difference between omega network and delta network ? Construct an omega network for $N = 8$ where N represent no. of processors.

4 + 2 + 2 + 4 + 1 + 2

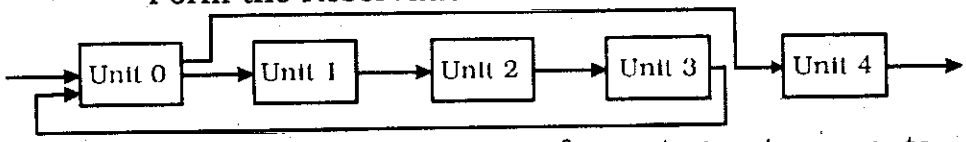
9. a) Consider the following pipeline reservation table.

	1	2	3	4	5	6	7	8
S1	X				X		X	
S2		X		X				
S3			X		X		X	

b) What are the forbidden latencies ?
c) Draw the state transition diagram.
d) List all the simple cycles and greedy cycles.
e) Determine the optimal constant latency cycle and the minimal average latency.
f) Let the pipeline clock period be $\tau = 20$ ns. Determine the throughput of the pipeline.

2 + 2 + 3 + 5 + 3

10. a) Consider the following block diagram of a circuit. Form the Reservation table.



b) An instruction requires four stages to execute : Stage 1 (instruction fetch) requires 30 ns, stage 2 (instruction decode) = 9 ns, stage 3 (instruction execute) = 20 ns and stage 4 (store results) = 10 ns. An instruction must proceed through the stages in sequence. What is the minimum asynchronous time for any single instruction to complete ?

c) We want to set this up as a pipelined operation. How many stages should we have and at what rate should we clock the pipeline ? 5 + 5 + (2 + 2 + 1)

11. a) With the use of Amdhl's law, conclude, among the given options which possible improvement is the best one.

Instruction type	Frequency	CPI
ALU	40%	1
Branch	20%	4
Load	30%	2
Store	10%	3

Possible improvements :

1. Branch CPI can be decreased from 4 to 3.
2. Increase clock frequency from 2 to 2·3 GHz
3. Store CPI can be decreased from 3 to 2.

b) What do you mean by memory fragmentation ? What is the advantage of using Paging ? Explain Virtual memory concept with an example where logical address space is 8 kb, physical address space is 4 kb, page size is 1 kb. Explain page fault with FIFO and LRU Algorithm. 4 + (2 + 2 + 4 + 3).