Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech/CSE/NEW/SEM-4/CS-403/2013

2013

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) The performance of a pipelined processor suffers if

      a) the pipeline stages have different delays

      b) consecutive instructions are dependent on each other

      c) the pipeline stages share hardware resources

      d) all of these.

   ii) What will be the speed up for a 4 segment linear pipeline when the number of instruction $n = 64$?

      a) 4·5 b) 3·82

      c) 8·16 d) 2·95.

iii) In which type of memory mapping there will be conflict miss ?

a) Direct mapping

b) Set associative mapping

c) Associative mapping

d) Both (a) & (b).

iv) Example of a recirculating network is

a) 3 cube network

b) ring network

c) tree network

d) mess connected Illiac network.

v) Array process is present in

a) MIMD b) MISD

c) SISD d) SIMB.

vi) Which type of data hazard is not possible ?

a) WAR b) RAW

c) RAR d) WAW.

vii) In general 64 input Omega network requires ..... stages of 2 × 2 switches.

a) 6 b) 64

c) 8 d) 7.

viii) Virtual address space can be divided into some fixed size

a) segments b) blocks

c) pages d) none of these.

ix) MIPS means

a) Multiple Instruction Per Second

b) Millions of Instruction Per Second

c) Multi-Instruction Performed System

d) None of these.

x) Which is not the property of a memory module ?

a) Inclusion b) Consistency

c) Capability d) Locality.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. For the code segment given below, explain how delayed branching can help :

I1.	LOAD	R1, A
I2.	Dec	R3, 1
I3.	BrZero	R3, 15
I4.	Add	R2, R4
I5.	Sub	R5, R6
I6.	Store	R5, B

3. A certain program generates the following sequence of word addresses :

4, 5, 12, 8, 10, 28, 6, 10

A page has four words; the number of page frames in main memory is 3. How many page faults are generated if optimum page replacement policy is used ?

4. Draw data flow graph to represent the following computations :

   1. $A = P + Q$
   2. $B = A / Q$
   3. $C = P * A$
   4. $D = C - B$
   5. $E = C * A$
   6. $F = D + E$

5. For the following code show how loop unrolling can help improve instruction level parallelism (ILP) performance :

```
Loop1 : I1 :  Load R0, A (R1 )
                    ;   A is the starting address of
                        array location
                    ;   R1 holds the initial address of
                        the element
      I2  Add R0, R2    ;   R0 ← R0 + R2, R2 is a scalar
      I3  Store R0, A (R1 )
      I4  Add R1, - 8   ;   go to next word in Array of
                            doubles
                    ;   whose address is 8 bytes
                        earlier.
      I5  BNE     R1, Loop1
```

6. What is a fundamental difference in interprocessor coordination mechanism between multiprocessor & multicomputer systems ? Explain with reference to their architectural differences.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) What do you mean by cache coherence problem ? Describe one method to remove this problem and indicate its limitations. 5

   b) What do you mean by Program Flow Mechanism ? Compare between Control-Flow, Data-Flow and Demand-Driven mechanism. 1 + 4

   c) Explain in brief with neat diagrams the Flynn's classifications of computers. 5

8. a) What do you mean by loosely coupled and tightly coupled multiprocessors ? 5

   b) Compare & contrast between UMA & NUMA with examples. What is Dumb memory ? 4 + 1

   c) What are the major differences between segmentation and Paging ? Why is the page size is usually a power of 2 ? 3 + 2

9. a) An address space is specified by 28 bits and corresponding memory space of 26 bits. If a page consists of 4K words

   i) How many pages and blocks are there in the system ?

   ii) The associative memory page-table contains the following entries.

Page	Block
0	0
1	1
5	2
6	3

Make a list of all virtual addresses (in decimal and in binary), that will cause a page fault. 2 + 3

b) Briefly explain the two write policies : write through and write back with advantages and disadvantages. 5

c) What are the different types of vector operations ? Give different fields in a vector instructions. What is pipeline chaining ? 3 + 1 + 1

10. a) A system has 48 bit virtual address, 36 bit physical address and 128 MB main memory address. If the system has 4096 bytes pages, how many virtual and physical pages can have address support ? How many page frames of main memory are there ? 2 + 2 + 1

b) Describe the different types of interconnection networks in computer systems. What is multistage switching networks ? 4 + 1

c) What do you understand by instruction pipelining and arithmetic pipelining ? Why pipeline scheduling is necessary and how it is done ? 2 + 2 + 1

11. a) Describe different access methods of the memory system ? What will be the maximum capacity of a memory, which uses an address bus of size 8 bit ? 1 + 4

b) What is the objective of OPT page replacement algorithm policy of virtual memory ? Using LRU, show the page-fault rate for the reference string

7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. 1 + 4

c) Define pipelining technique. Assume a 4 stage pipeline :

Fetch : Read the instruction from the memory

Decode : Decode the instruction

Execute : Execute the instruction

Write : Store the result in destination location

Draw the space-time diagram for pipelining. 1 + 4