MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : CS-403

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) CPI of super scalar pipeline is

a) less than 1 b) more than 1

c) 1 d) none of these.

ii) Pipelining uses

a) data parallelism b) temporal parallelism

c) spatial parallelism d) none of these.

iii) Utilization pattern of successive stages of a synchronous pipeline are specified by

a) Truth table b) Excitation time

c) Reservation table d) Periodic table.

iv) Dynamic pipeline allows

a) multiple functions to evaluate

b) only streamline connection

c) perform fixed function

d) none of these.

v) the equations for Amdahl's law is

a) $S(n) = 1/f$ where $n \rightarrow \infty$

b) $S(n) = f$ where $n \rightarrow \infty$

c) $S(n) = 1/T$ where $n \rightarrow \infty$

d) none of these.

vi) Array Processors are put under which one of the following categories ?

a) SISD b) SIMD

c) MISD d) MIMD.

vii) The number of cycles required to complete n tasks in a k stage pipeline is

a) $k + n - 1$ b) $nk - 1$

c) k d) none of these.

viii) an n-dimensional hypercube has

a) n^n nodes b) n^{-n} nodes

c) 2^n nodes d) none of these.

ix) Which of the following is a recursive network ?

a) Benes network

b) Baseline network

c) Cross bar network

d) None of these.

x) The compiler optimization technique is used to reduce

a) cache miss penalty

b) cache miss rate

c) cache hit time

d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following $3 \times 5 = 15$

2. "Instruction execution throughput increases in proportion with the number of pipeline stages". Is it true ? Justify your statement.

3. a) Write down Amdhal's law of parallel processing.

   b) Suppose, you have a program that has 10% code portion which must be executed sequentially. Now further suppose that we are to employ parallel programming to achieve a speedup. How many parallel processors must be there to achieve an overall speedup of 5 in the program execution time ?

4. What is branch hazard ? Briefly discuss two methods to handle branch hazards.

5. What do you mean by cache coherence problem ? Describe one method to remove this problem and its limitations.

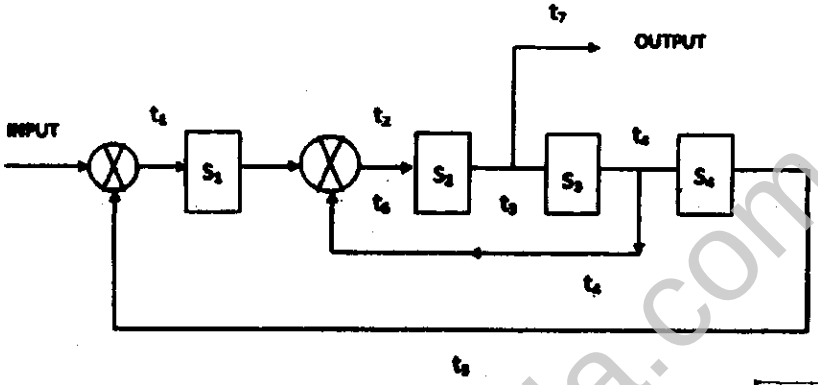
6. What is the drawback of direct mapped cache ? How is it resolved in set associative cache ?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. Consider the following pipeline processor :



where, S = number of stages & T = clock cycles
S_i is number of stages and T_i is clock cycle.

	1	2	3	4	5	6
S_1	X				X	
S_2		X				X
S_3			X			
S_4				X		

a) Specify the reservation table for this pipeline with six columns and four rows.

b) List the set of forbidden latencies between task initiations.

c) Draw the state diagram which shows all possible latency cycles.

d) List all greedy cycles from the state diagram

e) What is the value of minimal average latency ?

f) What is the maximal throughput of this pipeline ?

2 + 2 + 6 + 2 + 2 + 1

8. a) A computer has 512kB cache memory and 2MB main memory. If the block size is 64 bytes then find subfield for

   i) associative memory

   ii) direct mapping

   iii) set-associative mapping.

   b) How does cache memory increase the speed of processing ? Explain. 10 + 5

9. a) Explain different types of addressing modes ?

   b) What are the advantages of Relative addressing mode over Direct addressing mode ?

   c) Differentiate between Vectored and Non-vectored interrupts. 5 + 5 + 5

10. a) With the help of a neat diagram show the structure of a typical arithmetic pipeline performing (A*B+C).

    b) A hierarchical cache main memory sub-system has the following specifications :

    Cache access time : 50 ns.

    Main memory access time : 500 ns.

    80% of memory request for read

    Hit ratio : 0.9 for read access and write through scheme is used.

    i) Calculate the average access time of the memory system considering only memory read cycle.

    ii) Calculate the average access time of memory system both for read and write cycle. 7 + 8