



A modified high step-up non-isolated DC-DC converter for PV application

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Abstract

A non-isolated high voltage gain DC-DC converter has been presented in this paper. The boost, SEPIC and modified SEPIC converters were analyzed and their performance was compared with the proposed converter. The proposed converter has been designed for the input voltage of 15 V and an output voltage of 150 V with 100 W output power. The efficiency of the converter obtained was 92.5%, which is higher than that of the other converter models which were analyzed. Also, the proposed converter utilizes reduced input current and shows low switching voltage stress. The time response analysis conveys that the proposed converter settles to the steady state voltage and current faster than the other compared converters.

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Keywords: Boost converter; SEPIC; Photovoltaic; DC-DC power conversion

1. Introduction

Nowadays, the use of electricity has increased and hence the demand increases a lot. Power generation by means of conventional sources, such as coal and oil, results in increasing the greenhouse effect and environmental pollution issues in the world. The shortage of energy generation and pollution issues has been a main obstacle for industrial growth. These issues make the researchers concentrate on the clean energy resources such as photovoltaic (Li, Haskew, Li, & Hu, 2011), wind (Kesraoui, Korichi, & Belkadi, 2011) and fuel cell. The generation of electricity from renewable sources is important to reduce global warming and energy demand in the future as their use does not produce pollution and also the resources are abundantly available in nature.

Among the renewable energy sources, the photovoltaic (PV) one is one of the most outstanding in the world, because it is reliable, eco-friendly, low-maintenance and because of its low operational cost (Figueres, Garcerá, Sandia, Gonzalez-Espin, & Rubio, 2009; Li & Wolfs, 2008). PV-based standalone

and grid-connected systems are fast developing power generation areas in recent days in all over the world. Generating power from PV is reduced because of partial shading and mismatch condition in town areas (Scarpa, Buso, & Spiazzi, 2009). Another disadvantage of PV systems is their low conversion efficiency with the current technology which makes the PV systems an expensive technology. Because of these reasons, research work on this field has been carried out in recent years.

In the PV system maximum power point tracking algorithms are used to increase the energy harvesting facility and to improve the efficiency (Saravanan & Babu, 2016; Subudhi & Pradhan, 2013). The design of PV cells for study is considered with the rating of $P_{MPP} = 100$ W and $V_{MPP} = 15$ V. Also, to increase the performance of the system, high step up DC-DC converters are used to convert from low voltage to high voltage for required applications. The difficulties occurring regarding the DC-DC converter's efficiency is due to the low input voltage, high inrush current and static gain. The boost converter is the conventional non-isolated step up DC-DC converter with limited static gain and high switching voltage stress were used in literature (Kjaer, Pedersen, & Blaabjerg, 2005; Li & He, 2011; Meneses, Blaabjerg, Garcia, & Cobos, 2013).

The conventional boost converter is used for high step up applications with high current ripples for power system which causes conduction losses. Most of the high step up converter is affected with high input current because of the inductance

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values (Al-Saffar & Ismail, 2015; Hsieh, Chen, Liang, & Yang, 2013; Kim & Moon, 2015; Saravanan & Babu, 2015). To reduce that, the switching frequency has to be increased and hence it reduces the voltage stress occurring in the switches (Fardoun & Ismail, 2010; Wai, Lin, Duan, & Chang, 2007). Moreover, soft-switching is needed to reduce the switching loss and to improve the performance.

Various researchers use the SEPIC converter (Chiang, Shieh, & Chen, 2009; Kim, Choi, Jang, Lee, & Won, 2005; Park, Moon, & Youn, 2010; Pazhampilly, Saravanan, & Babu, 2015) and the modified SEPIC converter (Park, Seong, Kim, Moon, & Youn, 2008; Song, Oh, & Kang, 2012) for high static gain applications. The modified SEPIC converter has twice the static gain (De Melo, Gules, Romaneli, & Annunziato, 2010) value when compared with the conventional boost converter and also the switching voltage is half of the output voltage is value occurred (Yang, Liang, & Chen, 2009). In this paper, a converter with high static gain with reduced switching stress is proposed based on the SEPIC converter design. Compared with other converters, the proposed method gives reduced input inrush current for inductor, with faster settling time and less peak time of output voltage.

This paper is organized as follows: Section 2 describes the DC-DC converters operation and compares the boost and SEPIC with its merits and demerits. Section 3 presents the design of the proposed converter and its operation along with the chosen parameters. In Section 4 the analysis and results for the various DC-DC converters along with the proposed converter are explained briefly. The paper concludes the performance merits of the proposed converter in Section 5.

2. DC-DC converter

The converter is used to convert variable dc voltage to the fixed dc voltage for many DC applications. The main advantage of the high step up DC converter is the generation of the high voltage, i.e., from the input it is possible to generate ten times greater output using a single power semiconductor switch. The boost converter is a conventional high step up converter used in high voltage applications. The boost converter is based on the stepup principle used for output voltage which is greater than the input voltage and its circuit model (Gules, Dos Santos, Dos Reis, Romaneli, & Badin, 2014; Park & Kim, 2012; Santos, Antunes, Chehab, & Cruz, 2006), as shown in Fig. 1. To improve the efficiency of the boost converter it is connected with both coupled inductor and switched capacitor (Li & He, 2011). During high step up operation, current ripple is larger in the power devices and causes conduction loss which turns off the current.

For high voltage application, the switching voltage is almost equal to the output voltage of the converter. To improve the efficiency of the boost converter, it is upgraded to the conventional interleaved boost converter (Nejabatkhah, Danyali, Hosseini, Sabahi, & Niapour, 2012; Lee, Lee, Cheng, & Liu, 2000; Huang et al., 2004; Yao, Chen, & He, 2007). It consists of two switches to reduce the current ripple but a reverse recovery problem occurs in the diode.

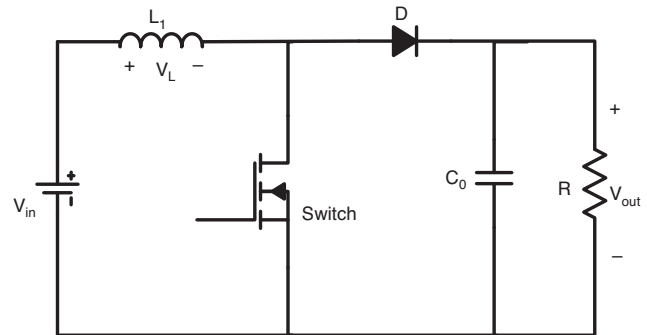


Fig. 1. Boost converter circuit.

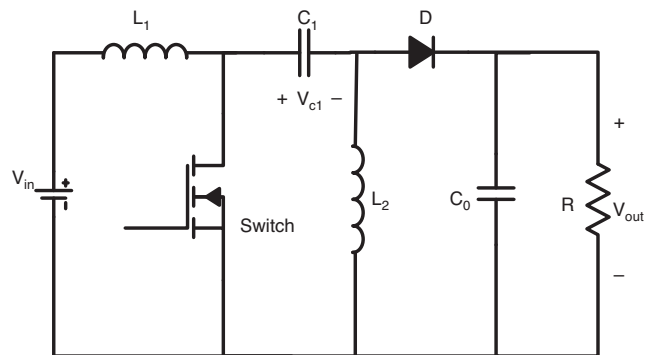


Fig. 2. SEPIC converter circuit.

The single-ended primary inductor converter (SEPIC) follows both the step-up and step-down principles. It consists of two inductors for buck or boost operation of the input voltage for output with no polarity reversal, as shown in Fig. 2. It transfers energy through capacitor C_1 and inductor L_1 ; because of that, the switching voltage is higher than the boost converter. The static gain of the converter used for wide input voltage application. The voltage flow in the switch is almost equal to the sum of both input and output voltages. The inrush input current is low when compared to the boost converter but the voltage stress is high.

The conventional SEPIC converter is modified using diode D_M and capacitor C_M is (Gules et al., 2014) added in the converter circuit as in Fig. 3. It is the combination of the SEPIC and boost converter which improves the static gain. The static gain is enhanced by charging the C_M capacitor using the conventional

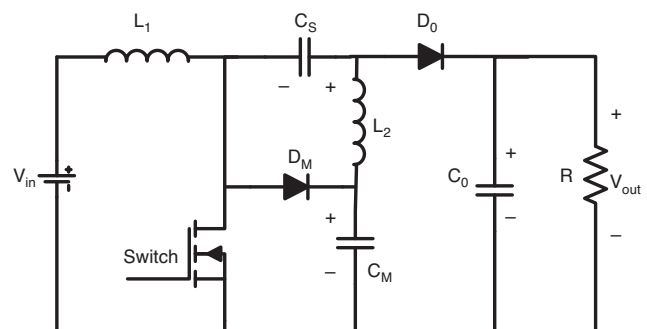


Fig. 3. Modified SEPIC converter circuit.

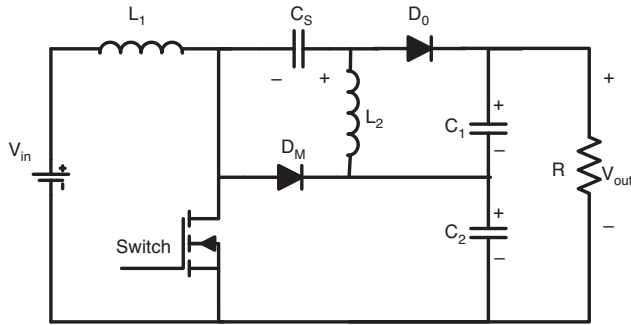


Fig. 4. Proposed converter circuit.

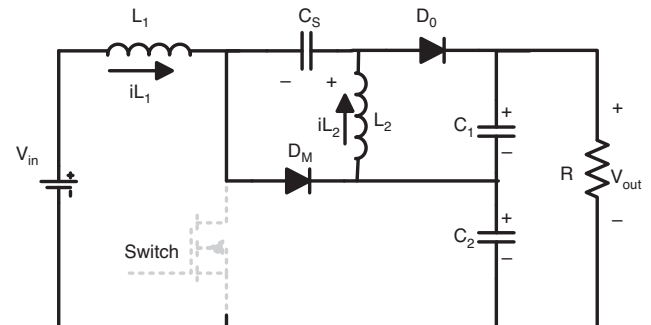


Fig. 6. Proposed converter switched OFF condition circuit.

boost converter's output voltage. The static gain is doubled and the switching voltage is reduced to half of the value than that of the boost converter. In this, high startup inrush current flows through the inductor L_1 , and to reduce that, a large input inductor is required. It consists of soft switching operation for turn ON and turn OFF condition for all low input voltages.

3. Proposed converter

The proposed converter is shown in Fig. 4, with modification on the SEPIC converter to improve the performance and to reduce the inrush current of inductor. It also works in the combination of both boost and SEPIC mode but the connection of output capacitor is slightly modified. The proposed converter reduces the inrush current for inductor L_1 and improves the operation of the converter faster than other converters.

It also reduces the stress and utilizes the low voltage for switching in the converter for high voltage conversion. It consists of one switch S , two inductors L_1 and L_2 , two diodes D_0 and D_M , and three capacitors C_1 , C_2 and C_S . The sum of the C_1 and C_2 capacitor's voltages is equal to the output voltage of the converter.

When the switch is on, the diode D_0 and D_M are reversed biased and the charges are stored in inductors L_1 and L_2 , as shown in Fig. 5. The input voltage flows through inductor L_1 to the inductor L_2 through C_S and C_2 . The capacitor voltage V_{C2} is equal to the switching voltage.

When the switch is off, the diode D_0 and D_M are in forward biased condition and stored energy from inductor L_1 starts discharging, as shown in Fig. 6. The output flows through C_S and

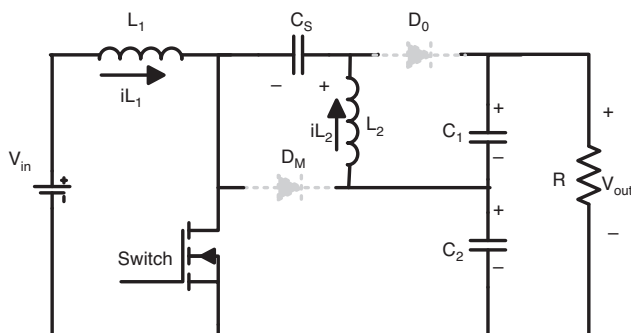


Fig. 5. Proposed converter switched ON condition circuit.

C_2 and inductor L_2 discharges the energy through diode D_0 . The switch voltage is almost equal to capacitor voltage C_2 . The main theoretical waveforms of the proposed converter are presented in Fig. 7.

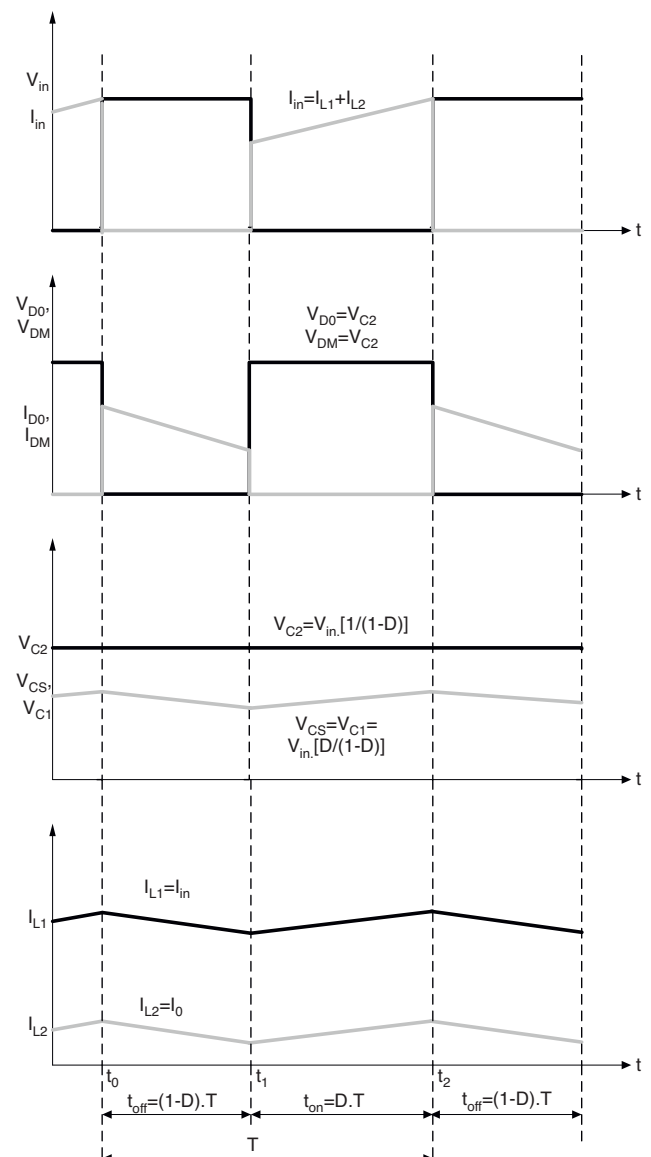


Fig. 7. Main theoretical waveforms.

Table 1
Converters formulas.

Parameters	Boost converter (Hart, 2011)	SEPIC (Hart, 2011)	Modified SEPIC (Melo et al., 2010; Gules et al., 2014)	Proposed converter
Switch Duty Cycle	$D = 1 - \frac{V_{in}}{V_{out}}$	$D = \frac{V_{out}}{V_{out} + V_{in}}$	$D = \frac{V_{out} - V_{in}}{V_{out} + V_{in}}$	$D = \frac{V_{out} - V_{in}}{V_{out} + V_{in}}$
Inductance	$L_1 = \frac{V_{out} D}{\Delta i_L f}$	$L_1 = \frac{\Delta i_{L1} f}{V_{out} D}$ $L_2 = \frac{\Delta i_{L2} f}{V_{out} D}$	$L_1 = L_2 = \frac{V_{out} D}{\Delta i_L f}$	$L_1 = L_2 = \frac{V_{out} D}{\Delta i_L f}$
Capacitors	$C_0 = \frac{D}{R(\Delta V_{out}/V_{out})f}$	$C_1 = \frac{D}{R(\Delta V_{C1}/V_{out})f}$ $C_0 = \frac{D}{R(\Delta V_{out}/V_{out})f}$	$C_S = C_M = \frac{I_{out}}{\Delta V_C f}$ $C_0 = \frac{D}{R(\Delta V_{out}/V_{out})f}$ $\Delta V_C = \left(\frac{V_{in}}{1-D}\right) \cdot 0.1^a$	$C_S = \frac{I_{out}}{\Delta V_C f}$ $C_1 = C_2 = \frac{1}{2} \left(\frac{D}{R(\Delta V_{out}/V_{out})f}\right)$ $\Delta V_C = \left(\frac{V_{in}}{1-D}\right) \cdot 0.1^a$

^a Nominal capacitor voltage ripple

Table 2
Converters parameters.

Parameters/Components	Boost converter	SEPIC	Modified SEPIC	Proposed converter
Input voltage (V_{in})	15 V	15 V	15 V	15 V
Switching frequency (f)	24 kHz	24 kHz	24 kHz	24 kHz
Duty cycle (D)	0.9	0.91	0.82	0.82
L_1	112.5 μ H	113.75 μ H	102 μ H	102 μ H
L_2	–	113.75 μ H	102 μ H	102 μ H
C_1	–	1.518 μ F	–	50 μ F
C_2	–	–	–	50 μ F
C_0	100 μ F	100 μ F	100 μ F	–
C_S	–	–	3.37 μ F	3.37 μ F
C_M	–	–	3.37 μ F	–
R	224.88 Ω	224.88 Ω	224.88 Ω	224.88 Ω

The voltage across the switch and all diodes are equal to the capacitor C_2 voltage. The output voltage is equal to the sum of the capacitor voltage C_1 and C_2 . The performances of the conventional boost, SEPIC and modified SEPIC were presented in this paper as the proposed converter is obtained from the design modification of these converters. The equation was derived for the proposed converter to calculate the inductance and capacitance using the conventional design.

The static gain of the proposed converter depends on the average inductance voltage with zero steady state. The duty cycle relation is presented in (1) considering continuous conduction mode operation. Duty cycle relation of the proposed converter is a combination of both boost and SEPIC converters. The output voltage of the converter is greater than that of the conventional boost and SEPIC converter.

$$D = \frac{(V_{out} - V_{in})}{(V_{out} + V_{in})} \quad (1)$$

The capacitor C_2 voltage V_{C2} is calculated by (2) and is equal to the output voltage of the conventional boost converter. The switching voltage of the proposed converter was the same as the C_2 capacitor's voltage. During the off condition of the switch the diodes D_0 and D_M were in conduction mode and the relation was obtained as (3),

$$\frac{V_{C2}}{V_{in}} = \frac{1}{1 - D} \quad (2)$$

$$V_{out} = V_{C1} + V_{C2} \quad (3)$$

The voltage across the series capacitor, V_{CS} and C_1 capacitor voltage, V_{C1} was calculated by (4),

$$V_{CS} = V_{C1} = V_{in} \left(\frac{D}{1 - D} \right) \quad (4)$$

The design considerations for the proposed converter, and for other ones, were obtained by assuming the following ratings (Gules et al., 2014):

Input voltage = 15 V,
Output voltage = 150 V,
Output power = 100 W,
Switching frequency = 24 kHz.

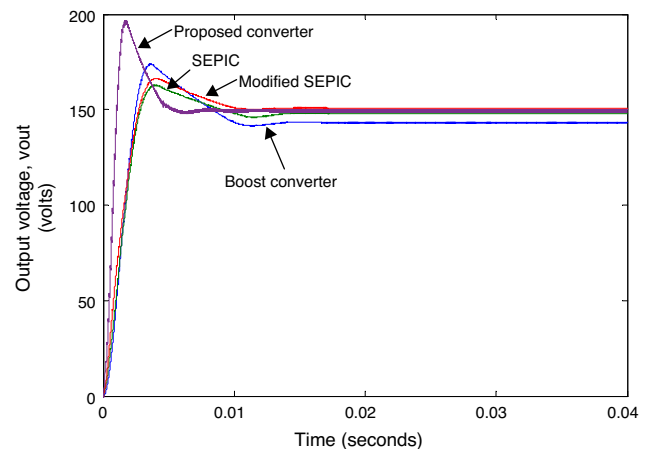


Fig. 8. Output voltage of converters.

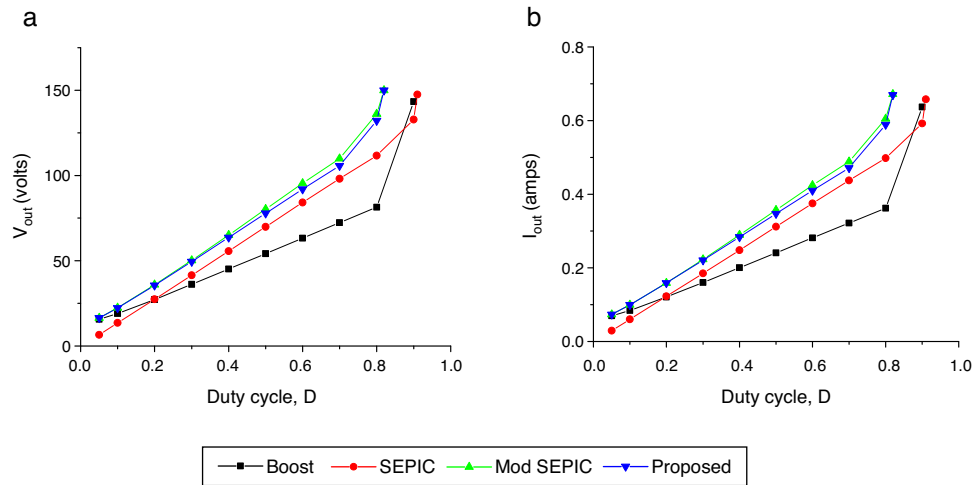


Fig. 9. (a) Output voltage of DC-DC converters, (b) output current of DC-DC converters.

The inductances L_1 and L_2 were designed using the stated expression in Table I by assuming the current ripple (Δi_L) as 5A. The average current rate in inductor L_1 was equal to the input current and the average current rate in inductor L_2 is equal to the output current of the converter.

For the design of output capacitors C_1 and C_2 , the output voltage ripple (ΔV_{out}) was chosen as 1% of the capacitors' voltage. The series capacitor C_S was calculated using the nominal capacitor voltage ripple (ΔV_C) equal to 10%. A small capacitance value was obtained and a low series equivalent resistance was used for the capacitors (Kim & Moon, 2015).

The selection of the semiconductor switch rating was done based on the sum of the current flowing rate in L_1 and L_2 . Fig. 7 shows that the switching current starts flowing through the switch during the turn-on period. The rating of diode in the proposed converter is chosen based on assumption, that the average current of diode is equal to the output current (I_{out}). The total conduction loss of switch and both diodes are equal to the 2 W.

The design expression utilized to design the boost, SEPIC (Hart, 2011), modified SEPIC and proposed converter

parameters as shown in Table 1. The theoretical values estimated and the parameter values of the converter chosen are displayed in Table 2. These parameters were used to obtain the suitable output for the step up conversion in the converters with more reliability.

4. Results and discussion

The proposed converter and other converters shown in Figs. 1–4 have been simulated using MATLAB/Simulink to check the above design parameters as well as to measure their performance and operations. The output voltages of the boost, SEPIC, modified SEPIC and proposed converter are shown in Fig. 8. From Fig. 8, it is observed that the output voltage of the proposed converter (150 V) increases 4.5% in comparison to that of the boost converter (143.3 V). The performances of the converters stability were verified by varying the duty cycle given to the switches and the output voltage of each converter was noted down. Based on that varying condition, the performance of the proposed converter was validated as discussed below.

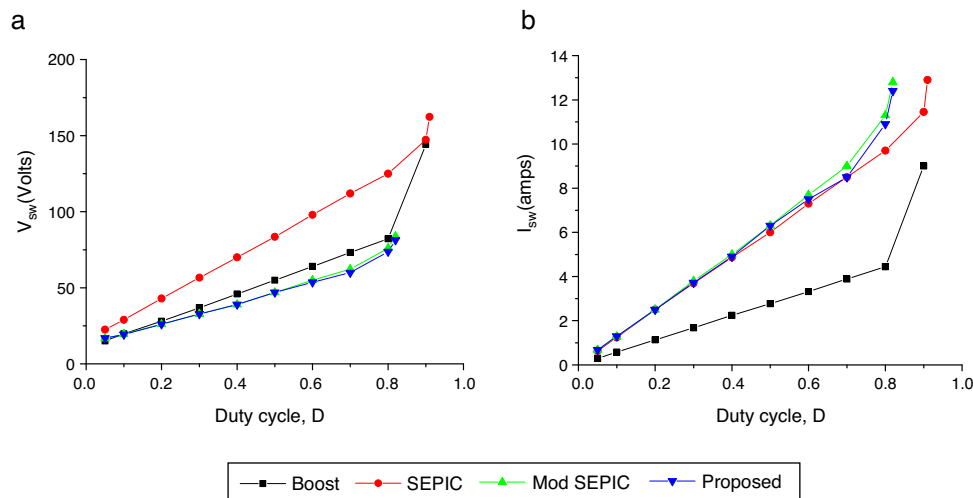


Fig. 10. (a) Switching voltage of DC-DC converters, (b) switching current of DC-DC converters.

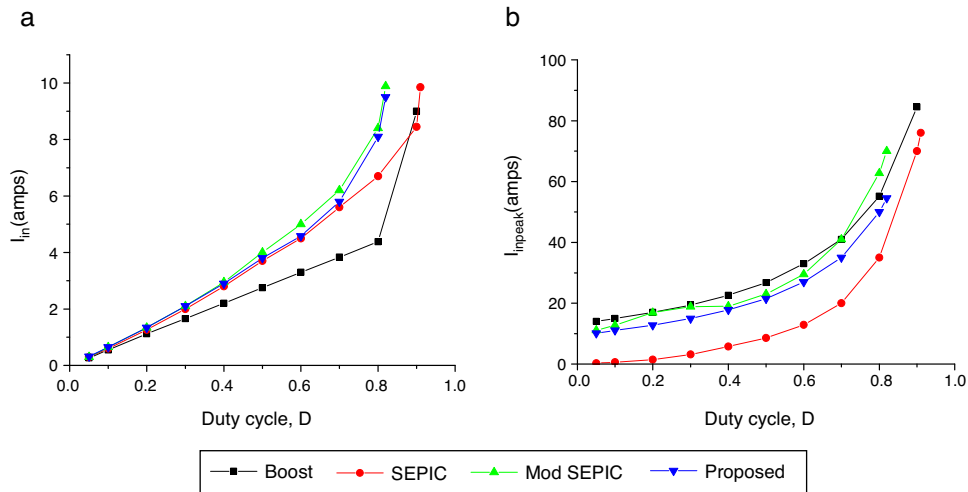


Fig. 11. (a) Input current of DC-DC converters, (b) input peak current of DC-DC converters.

Table 3

Performance measured of proposed and other converters.

Parameter/Components	Boost converter	SEPIC	Modified SEPIC	Proposed converter
Output voltage (V_{out})	143.3 V	147.5 V	150 V	150 V
Switch voltage (V_s)	144.1 V	162.3 V	83.8 V	81.3 V
Inductor starting current (I_{in})	84.5 A	76 A	70 A	54.5 A
Output current (I_{out})	0.6372 A	0.6577 A	0.6715 A	0.6699 A
Output power (P_{out})	91.31 W	97 W	100 W	100 W

The output voltage and output currents of each converter with respect to various duty cycle were plotted in the graph as shown in Fig. 9(a) and (b). From the graph, it is easily observed that the proposed converter and modified SEPIC converter generate the output voltage and current as per the design of converter. But the boost and SEPIC converter gave reduced voltage and current. Also, the duty cycle designed for the boost and SEPIC converters was higher than the proposed converters.

The switching voltage and current of the modeled converters were shown in Fig. 10. The switching voltage of the proposed converter was slightly lower than that of the modified SEPIC

converter whereas the switching voltage was high in the SEPIC and boost converter. Because of this lower switching voltage, the losses also decreased and the converter worked more efficiently in the high step up operation.

The input current and input peak current values are plotted in Fig. 11. When the input current flows through inductor L_1 , the current ripple increases. This reduces the overall efficiency of the converter and also makes the converter to require high rating components. The proposed converter shows low input current ripple compared to the boost, SEPIC and modified SEPIC converters. In addition, the peak current of the proposed converter

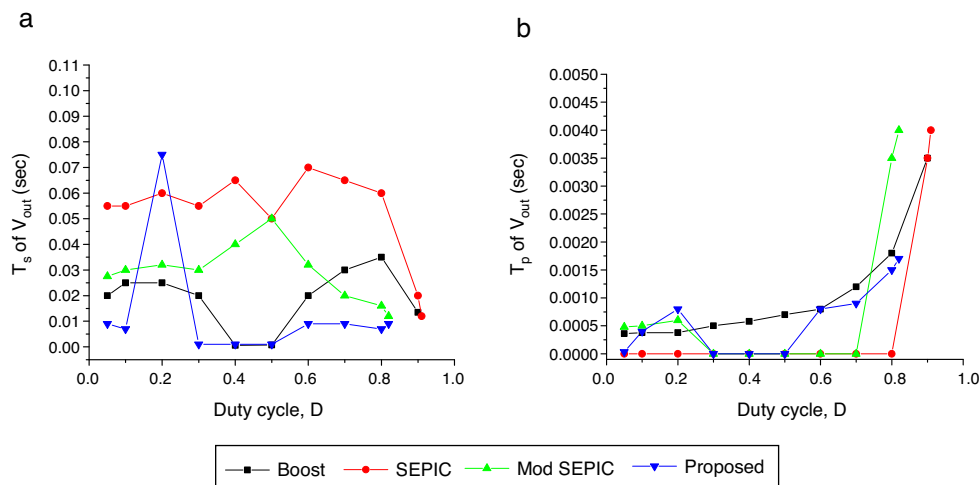


Fig. 12. (a) Settling time of output voltage, (b) peak time of output voltage.

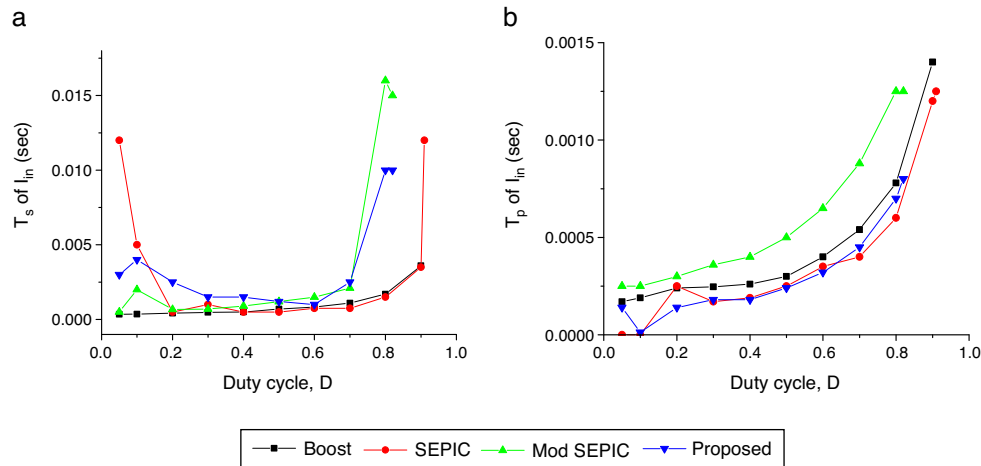


Fig. 13. (a) Settling time of input current, (b) peak time of input current.

is comparatively lower than that of the other converters. The comparative results of the measured parameters of the proposed and compared converters are listed in Table 3.

The time responses of the output voltage for the converters were analyzed and the settling time and peak time of the output voltage are plotted in Fig. 12(a) and (b). From the analysis, it is clear that the proposed converter operates with fast settling and less peak time compared to other converters; because of that, the converter gives a quicker response for the required application.

Similarly, the time response characteristics of the input current were analyzed and are shown in Fig. 13(a) and (b). As the peak time of the proposed converter decreased, the inrush current magnitude also decreased with a quicker response. These analyses show the advantages and the performance improvement of the proposed converter when compared with the other analyzed converter models. Even though the proposed converter has

several advantages compared with other converters, it requires more complex technology.

Fig. 14 shows the obtained efficiency of the various converters along with the proposed one. The graph clearly shows that the proposed converter has more efficiency than the other ones. The proposed converter operates a fast response with low input current for the system. The proposed converter efficiency is equal to 92.5% at full load condition for 100 W whereas for the same condition, the boost, SEPIC and modified SEPIC converters achieve 84.2%, 86.4% and 91.7%, respectively.

5. Conclusion

A high step up non-isolated DC-DC converter is presented in this paper. The proposed converter uses two loading capacitors with equal rating instead of one capacitor in the SEPIC model. These capacitors share the voltage stress and the inrush current. Furthermore, the time response characteristics of the output load voltage improve by reducing the settling and peak times. The performance of the proposed converter model is analyzed under various parameters. The efficiency of the proposed converter is equal to 92.5% with an input voltage of 15 V, an output voltage of 150 V and an output power of 100 W. The proposed converter analysis shows that it has a reduced switching voltage of 81.3 V and reduced starting current of 54.5A. The time response analysis of the proposed converter shows that the output current and voltage characteristics settle to the steady state value quicker in 9 ms. Also, the peak time of the voltage and current of the proposed converter is 1.7 ms.

The validation of the proposed converter concludes that its performance is better than the one of the compared converter models and that it can be a good choice for many of the renewable energy system applications with simple design and high efficiency.

Conflict of interest

The authors have no conflicts of interest to declare.

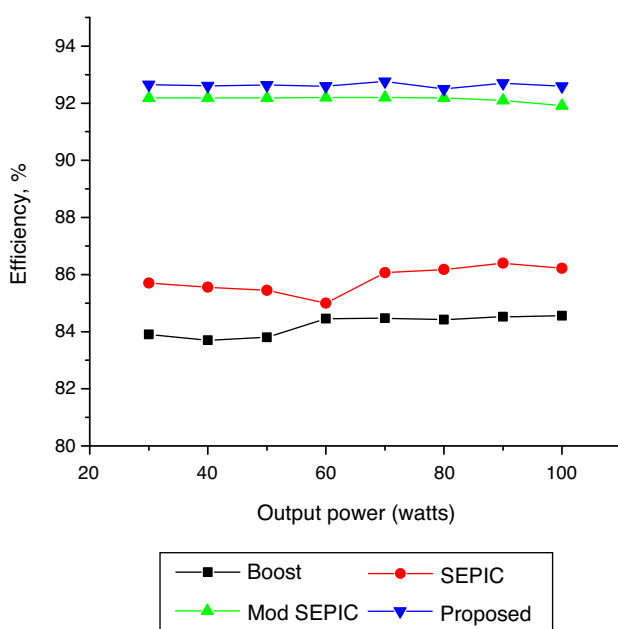


Fig. 14. Measured efficiency of the proposed converter and the other ones.

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