Development of Simulink-Based SiC MOSFET Modeling Platform for Series Connected Devices

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***Abstract*—A new MATLAB/Simulink-based modeling platform has been developed for SiC MOSFET power modules. The modeling platform describes the electrical behavior f a single 1.2 kV/ 350 A SiC MOSFET power module, as well as the series connection of two of them. A fast parameter initialization is followed by an optimization process to facilitate the extraction of the model's parameters in a more automated way relying on a small number of experimental waveforms. Through extensive experimental work, it is shown that the model accurately predicts both static and dynamic performances. The series connection of two SiC power modules has been investigated through the validation of the static and dynamic conditions. Thanks to the developed model, a better understanding of the challenges introduced by uneven voltage balance sharing among series connected devices is possible.**

Keywords—- SiC MOSFETs, Simulink simulation, PSPICE simulation, Device modeling, Parameter extraction, Wide bandgap devices, Series connection

NOMECLATURE

A	Device chip area (cm^2).
A_{gd}	Gate-to-drain area (cm^2).
C_{gd}	Gate-to-drain capacitance (F).
C_{dsj}	Drain-to-source junction capacitance (F).
C_{gs}	Gate-to-source capacitance (F).
C_{oxd}	Oxide's capacitance (F).
ΔV_{tl}	Low current threshold voltage differential (V).
E_{cr}	Critical electric field (MV/cm).
$I_{mos,l}$	Low current region component of the channel current (A).
$I_{mos,h}$	High current region component of the channel current (A).
$I_{d,sat}$	Drain saturation current (A).
I_d	Drain current (A).
K_f	Linear region transconductance factor at 300 K.
K_{f1}	K_f temperature coefficient.
K_{fl}	Low current region transconductance factor.
K_p	Saturation region transconductance at 300 K (A/V^2).
K_{p1}	K_p temperature coefficient.
L_{stray}	Stray inductance of the loop (H).
N_b	Doping density of the base (cm^{-3}).
P_{vf}	Pinch-off voltage factor.
q	Fundamental charge (C).
R_b	Resistance of epitaxial layer (Ω).
R_s	Drain resistance (Ω).
R_{gate}	Gate driver resistance (Ω).
V_{BD}	Device breakdown voltage (V).
V_{ds}	Drain-to-source MOSFET voltage (V).
V_{gs}	Gate-to-source MOSFET voltage (V).
V_t	MOSFET threshold voltage (V).
V_{t1}	V_T temperature coefficient (V/K).
V_{td}	Gate-to-drain depletion threshold voltage (V).
V_{th}	High current channel threshold voltage (V).
V_{tl}	Low current channel threshold voltage (V).
W_b	Width of the drift region (μm).
ε_s	Semiconductor dielectric constant (F/m).
θ	Transverse electric field parameter (V^{-1}).
θ_1	θ temperature coefficient.

I. INTRODUCTION

Because conventional silicon (Si) power devices are approaching their technological limits, the recent advancements in silicon carbide (SiC) technology have brought the beginning of a new era in high power electronics; thanks to superior physical properties of SiC material such as high critical field (i.e., 10× higher than that of Si), high thermal conductivity (i.e., 3× higher than that of Si) and high carrier saturation velocity (2× higher than that of Si). As a result, SiC-based devices are capable of higher operating voltages, lower losses, higher system compactness, harsher working conditions capability (i.e., high temperature, radiation etc.,) and, last but not least, better environmental robustness for a diverse range of high power applications [1].

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Among various kinds of power semiconductor devices, SiC Schottky diodes and SiC MOSFETs are now widely available in the commercial market either as a discrete power switch (e.g., TO220, TO247) or in high power module packages with several dies in parallel [1, 2]. In addition to that, the need for high voltage, high power switches makes the adoption of series connection of SiC MOSFET devices in converter topologies more and more attractive because of the possibility to considerably reduce the number of switches in series. Note that, the series connection could result in higher operating voltage levels, lower switching losses and higher operating frequency [3].

However, this solution is associated with various reliability issues mainly due to the severe voltage unbalances caused by the inevitable variations of the intrinsic device parameters as well as manufacturing differences of the gate drivers causing signal time delays. These issues are further escalated in SiC devices since the technology is rather new and the manufacturing processes are not well-established. Furthermore, due to the considerably higher cost of SiC technology, one of the biggest challenges is the robust circuit design process while avoiding over-sized margins [4].

To address these issues, accurate and reliable device modeling [5-12] is required to reduce the development cost and effort and simultaneously evaluate a realistic converter circuit's functional robustness, before massive production. Regarding SiC power MOSFETs, a comprehensive physics-based model has been presented by McNutt/Hefner in [13], based on the Hefner IGBT model [14].

In this paper, a case study on a 1.2 kV/ 350 A SiC MOSFET power module is presented to evaluate and validate the Simulink-based model. The model's accuracy is initially tested with static and dynamic verification of experimental results. The main purpose of this work is to validate that the present model can be used to facilitate the design process of high power converter systems, based on SiC MOSFETs, so after the initial verification step, the model's precision is evaluated when two devices are connected in series.

This paper is structured as follows. Section II describes the rather new Simulink-based SiC MOSFET modeling platform that is used in this paper in contrast to the usual SPICE-based models that are commonly found in previous research activities [5, 8]. Section III, discusses the parameter identification method based on optimization that is used in order to extract the unknown parameters of the model. Section IV, presents extensive results in static and dynamic conditions for one device and two devices in series, validating the model and discussing its capabilities when it comes to over-voltage and switching loss predictions. Section V, presents the conclusions of the present work.

II. Simulink Implementation

In contrast to the commonly used Spice models, a fundamentally new MATLAB/Simulink model is realized making use of the Simscape language. The platform choice is of major importance for further usage in converter topologies and studies, making the most out of MATLAB's computational power.

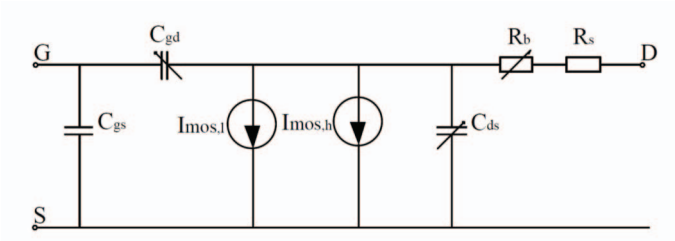

Fig. 1: Simplified SiC MOSFET equivalent circuit implemented in MATLAB/Simulink environment.

Fig. 1 shows the equivalent circuit of a typical MOSFET structure. The layer-structure of the MOSFET along with the governing equations and the conditional statements of the McNutt/Hefner model have been described thoroughly in [13] and therefore are omitted from the presented work.

As it can be seen in Fig. 1, the capacitance C_{gs} is modeled as a fixed capacitance since its value remains approximately constant with the operating bias point. On the other hand, capacitances C_{gd} and C_{ds} are modeled as variable capacitances since their value depend strongly on the operating bias point as indicated in Fig. 6 too. Similarly, resistor R_s represents the resistance of the drain region which due to the fixed doping concentration is constant. The doping concentration in this n^+-region is high, so the value of the aforementioned resistance is usually low. On the other hand, resistor R_b represents the epitaxial drift resistance of the transistor body which is the resistance of the n^--region. The carrier concentration of this region changes as the device switches on or off. As a result, its value is not fixed and it can be represented as a voltage-dependent variable resistor.

One of the most important features of the McNutt/Hefner model is its performance in the sub-threshold region [13]. This feature is incorporated into the model by the use of a variable current source for the low current region ($I_{mos,l}$) in parallel to the one for the high current region ($I_{mos,h}$). The resulting channel current is the sum of those two sources and the final value depend on the V_{ds} as well as on the V_{gs}.

Finally, the user-defined components are programmed based on the model's non-linear equations which can be saved in the Simulink's library. It should be noted that simulation steps are kept within acceptable limits, despite the need to use a fixed time step for the simulation. It should also be highlighted that convergence was easily achieved in most cases, regardless of the parameters used. The optimization tool (Section III) shows excellent compatibility with the model during the parameter extraction procedure, making the platform's choice promising.

III. Parameter Identification Procedure

The model's performance obviously depends strongly on the set of parameters that will be used. The parameter extraction method used is a two-step procedure similar to the

idea initially presented in [15]. At first, a fast initialization procedure sets the starting point of the optimization algorithm. Then, the optimization software simulates the device and changes the parameters comparing the error between the simulated waveforms and the measured ones. The cost function is minimized until the software converges to a solution. The overall idea is shown in Fig. 2.

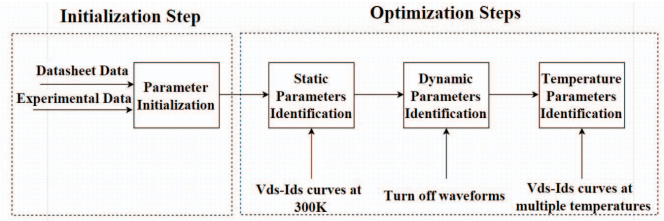

Fig. 2: Two-step parameter extraction procedure for the McNutt/Hefner SiC model.

A. Initialization Step

The initialization of the model's parameters is a crucial aspect of the parameter identification since it facilitates the fast and accurate convergence of the optimization software. Since convexity cannot be easily proven in a complicated system like this, the choice of starting point therefore becomes crucial for the model to converge to a local minimum and not a global one.

The initialization procedure used hereby relies on a small number of experimental measurements along with the information that is commonly found on manufacturer's datasheets. At first, the saturation region is analyzed and an approximation could be made, as shown in (1):

$$I_{mos,h} = 0.9\, I_{d,sat} \tag{1}$$

where $I_{d,sat}$ is the measured saturation drain current at a given bias.

Based on experimental measurements or data from the datasheet curves in the saturation region, K_{fl}, K_p, θ, V_t and ΔV_{tl} can be initialized, simply by solving equations (1) – (3).

$$I_{mos,l} = K_{fl} K_p \frac{(V_{gs}-V_{tl})^2}{2(1+\theta(V_{gs}-V_{tl}))} \tag{2}$$

$$I_{mos,h} = (1-K_{fl}) K_p \frac{(V_{gs}-V_{th})^2}{2(1+\theta(V_{gs}-V_{th}))} \tag{3}$$

The active region is modeled as follows: the total on-resistance of the device can usually be found on the datasheets and it is comprised by the series combination of R_b and R_s as shown in Fig. 1. As explained before, the epitaxial resistance is dominant in devices of this rating so an assumption can be taken as in (4), in order to decompose the total on-resistance and initialize the value of R_s:

$$R_b = 10\, R_s \tag{4}$$

Moreover, the width of the base region can be found based on the breakdown voltage of the device and the critical electric field value which is assumed to be *2 MV/cm* for SiC devices:

$$W_b = \frac{2\, V_{BD}}{E_{cr}} \tag{5}$$

The doping of the base region can be found based on (6):

$$N_b = \frac{\varepsilon_s\, E_{cr}^2}{q V_{BD}} \tag{6}$$

Finally, assuming an empirical pinch-off factor $P_{vf} = 0.9$ and taking one measured point for the linear region, K_f can be found based on current's equation of the McNutt/Hefner model, for the linear region. It should also be noted that the device chip area A can be approximated based on the manufacturer datasheet [13].

Additionally, the parameters defining the dynamic performance of the model should be initialized. Firstly, the input capacitance C_{gs} is approximately constant and is usually given in the datasheets. The oxide capacitance C_{oxd} requires extensive measurements in order to be determined but for simplicity its value can be initialized in the region of C_{gs}. Furthermore, the gate to drain area A_{gd} can be empirically assumed to be one tenth of the total device chip area A [5].

Finally, the temperature-dependent parameters are difficult to estimate and thus they have been set initially to 1.

B. Optimization Steps

The previous approach relies on a small number of experimental measurements, datasheets points, empirical assumptions and physics-based equations. In order to minimize the error introduced in the parameter initialization step, an optimization tool developed at Aalborg University has been used [16].

The optimization tool was described thoroughly in [16]. The idea behind it is similar to the one described in [15]. The model is simulated and the resulting static and dynamic waveforms are compared with the experimental ones, generating an error. Optimization methods are then used in order to change the parameters based on the information of the error gradient. After a number of iterations, the algorithms converge to a solution and return the optimized parameters.

Due to the large number of parameters related to the McNutt/Hefner model, an intelligent optimization procedure is followed in this paper, as shown in Fig. 2. The optimization procedure is broken into three steps in order to help the software to converge to a minimum in a fast and reliable way:

i) At first, the I_d-V_{ds} characteristics of the device are loaded and an optimization of the parameters closely related to the static performance of the device is taking place, at the reference temperature of *300 K*. It should be noted that for the reliable extraction of the parameters, various gate biases should be used. Typically the software converges to a solution after approximately 300 iterations.

ii) In the second step, the optimization of the parameters related to the dynamic performance of the device is conducted. These parameters have been roughly approximated in Section III.A so the expected initial error is significant. The modeling of the body diode of the device has been considered to be outside of the scope of the present study and in order to minimize its effect in the transient response, only the experimentally obtained turn-off waveforms are compared with simulations, since during turn-on the effect of the diode becomes more significant. In the simulations, a rather simple diode model is used [17]. More particularly, the turn-off waveforms of the drain voltage, drain current and gate to source voltage are compared with the respective simulated waveforms and the optimization tool converges to a final solution, typically after 400 iterations.

iii) The I_d-V_{ds} characteristics of the device at different temperatures are compared with the simulated ones and the temperature related parameters are extracted.

C. Final set of Parameters

Table I shows the resulting accuracy of the model for the three optimization steps, namely, static characteristics at room temperature, turn-off characteristics at room temperature and static characteristics at different temperatures. It can be noted that the initial error in the static and dynamic waveforms at the reference temperature is relatively low due to the initialization. However, the optimization method reduces the error significantly. In the case of the static performance for different temperatures, the initialization method used was insufficient so the initial error is large. Despite this, the optimization routine managed to converge to an acceptable solution. It should be noted that the error is calculated as the mean relative error of all the waveforms in each case.

TABLE I. MODEL'S ACCURACY

	Initial Error	*Final Error*
Static (T=300 K)	16 %	4.5 %
Dynamic (T=300 K)	15.5 %	7 %
Static (Various T)	61 %	5 %

Table II summarizes the initial set of parameters as identified according to III.A as well as the final set of parameters as found by the optimization tool. It is worth noting that the extracted parameters after the optimization, are in agreement with the physics behind the device's behavior and their value is close to the expected one.

IV. MODEL VERIFICATION

In this section, experimental waveforms are compared with the simulated ones based on the final set of the extracted parameters. These waveforms verify the model's static and dynamic performances. The model is validated for two cases: (a) single device, and (b) series connection of two devices.

TABLE II. SET OF PARAMETERS FOR THE 1.2 KV/ 350 A SIC MOSFET MODULE.

Parameter	*Initial Value*	*Final Value*	*Identification Step*
K_{fl}	0.1	0.07	Static
ΔV_{tl} (V)	0	0	Static
V_t (V)	4.1	5.3	Static
θ (V^{-1})	0.014	0.035	Static
K_p (A/V^2)	27	30.7	Static
R_s (Ω)	0.72	1.7	Static
W_b (μm)	12	14	Static
P_{vf}	0.9	0.43	Static
K_f	1.07	5.8	Static
N_b (cm^{-3})	$1.78 \cdot 10^{16}$	$1.8 \cdot 10^{16}$	Static/Dynamic
A (cm^2)	0.78	0.8	Static/Dynamic
C_{gs} (F)	14.5	15.7	Dynamic
C_{oxd} (F)	10	10.2	Dynamic
V_{td} (V)	0	0	Dynamic
A_{gd} (cm^2)	0.078	0.089	Dynamic
V_{t1}	-0.01	-0.018	Temperature
K_{f1}	1	2.65	Temperature
K_{p1}	1	1.55	Temperature
θ_1	1	2.5	Temperature

A. Single Device Verification

In this section, experimental results verify the accuracy of the developed model for a 1.2 kV/ 350 A SiC MOSFET from Microsemi [18]. At first, Fig. 3 illustrates the I_d-V_{ds} characteristics of the device for different gate biases at the reference room temperature of 300 K. It can be depicted that the model performs with high accuracy regardless of the gate bias and manages to simulate the behavior of the device in an accurate way both in the linear as well as in the saturation region. As noted in Table II, the mean error of these waveforms is approximately 4.5 %.

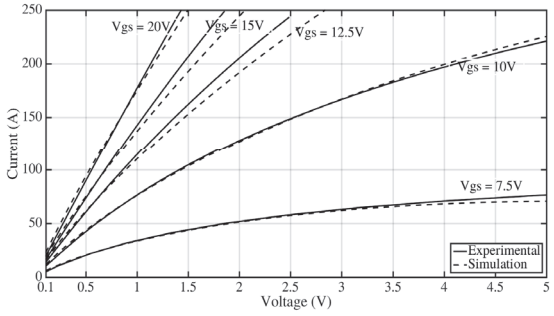

Fig. 3: I_d-V_{ds} characteristics at 300 K for various gate biases.

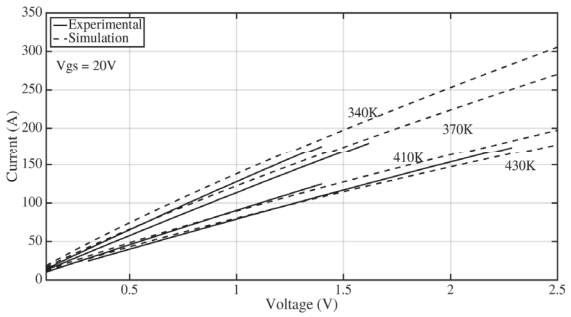

Fig. 4: I_d-V_{ds} characteristics at 20 V gate bias for various temperatures.

Similarly, the temperature coefficients extracted in the third step of the optimization procedure are used in order to simulate the device's performance at various temperatures. Fig. 4 illustrates the resulting waveforms when 20 V gate bias is applied in different temperatures.

Fig. 5 shows the equivalent schematic of the experimental setup that is used for double-pulsed dynamic measurements. The same circuit is simulated taking into consideration an estimated 150 nH total loop stray inductance.

Before the dynamic verification of the model, the three resulting capacitances used in the model are evaluated based on the information that is found on the manufacturer's datasheet. The capacitances are playing a dominant role in the dynamic response of the device and their proper modeling is considered one of the greatest challenges. Fig. 6 shows a comparison between the capacitances of the model (C_{dsj}, C_{gs}, C_{gd}) and the ones found in the datasheet, as a function of the drain-to-source voltage.

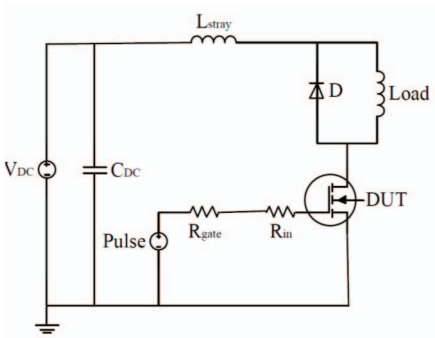

Fig. 5: Schematic of the experimental setup for double-pulsed dynamic measurements.

Fig. 7 depicts the turn-off drain voltage and drain current waveforms of the studied power module while Fig. 8 depicts the gate-to-source turn-off voltage waveform. The gate resistance in this case is chosen to be 15 Ω in order to keep the device in its safe operating area despite the high inductance. The bus voltage is set to 800 V and the current at turn-off is approximately 300 A.

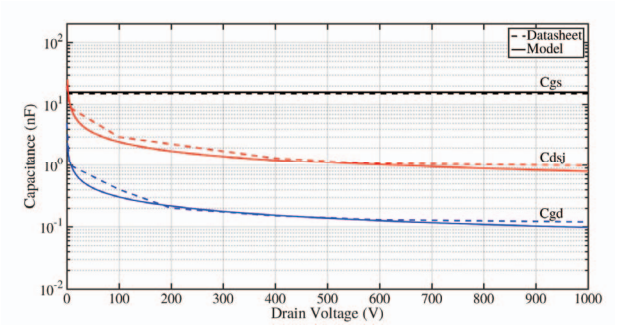

Fig. 6: Comparison of the MOSFET internal capacitance value between datasheet and model as a function of the drain-to-source voltage.

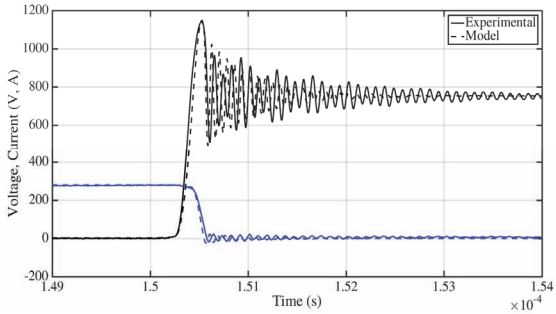

Fig. 7: Turn-off waveforms of the 1.2 kV/ 350 A SiC MOSFET power module at V_{DS}=800 V, I_D = 300 A and T =25 ˚C.

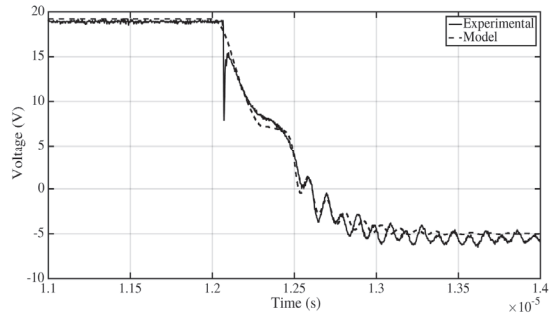

Fig. 8: Gate-to-source turn-off waveform of the 1.2 kV/ 350 A SiC MOSFET power module at V_{DS}=800 V, I_D = 300 A and T =25 ˚C.

Similarly, Fig. 9 and 10 show the respective turn-on waveforms. The current after turn-on in this case is approximately 220 A.

The figures below verify that the model performs with high accuracy as it manages to predict the experimentally acquired waveforms. Additionally, the single device model has been also evaluated by comparing the turn-off overvoltage values as well as its switching losses together with the experimental measurements.

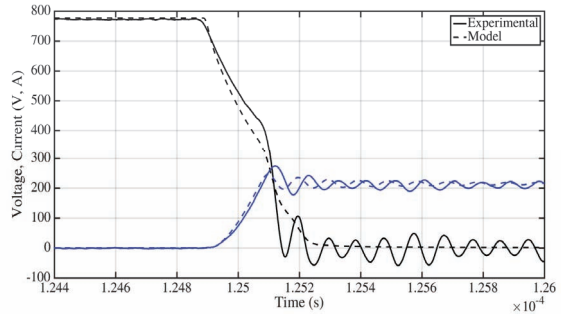

Fig. 9: Turn-on waveforms of the 1.2 kV/ 350 A SiC MOSFET power module at V_{DS}=800 V, I_D = 300 A and T =25 ˚C.

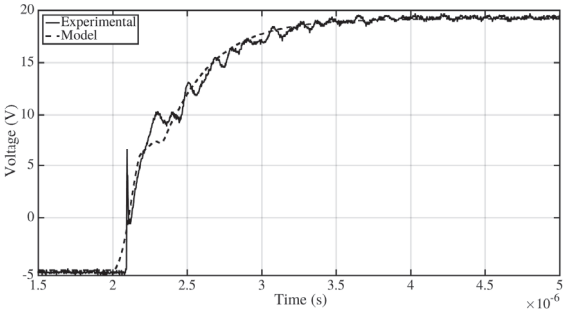

Fig. 10: Gate-to-source turn-on waveform of the 1.2 kV/ 350 A SiC MOSFET power module at V_{DS}=800 V, I_D = 300 A and T =25 ˚C.

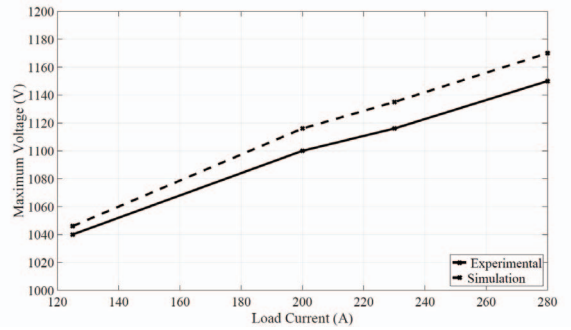

Fig. 11: Turn-off overvoltage prediction as a function of the load current for a constant applied voltage (V_{DS} = 800 V, T = 300 ˚K).

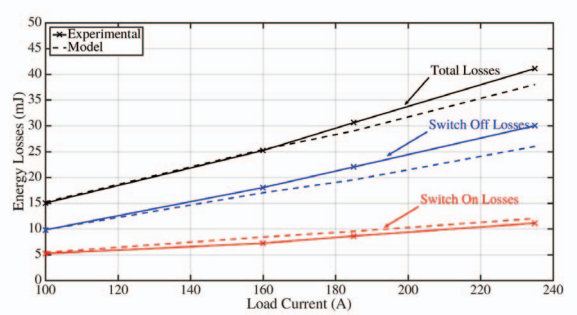

Fig. 12: Energy loss prediction as a function of the load current for a constant applied voltage (V_{DS} = 800 V, T = 300 ˚K).

Fig. 11 and 12 illustrate the maximum over-voltage variation and the extracted energy losses as a function of the load current at 300 K. Both figures show that the model is capable of predicting both the over-voltage as well as the switching losses with relatively high precision. It can be noticed, that during switch-off the model results in smaller losses despite the fact that it exhibits higher over-voltage. This characteristic is attributed to a slightly shorter total transient time, which come errors introduced by the modeling of the gate driver circuit. In contrast, the turn-on losses seem to be very well predicted and the small difference could be attributed to the effect of the relatively simple diode model that was used.

Overall, SiC MOSFET model and experimental switching data evidences a fair qualitative agreement and hence verifying the applicability of the developed model for future converter simulation.

B. Series Connection Verification

The series operation of power semiconductor devices is arguably an attractive solution [19, 20]. The challenge of achieving equal voltage sharing has been investigated in the literature for different topologies based on conventional Si devices [21, 22]. In order to facilitate the design process, a model should be able to predict the dynamic and static voltage sharing under all conditions. Due to the non-linearity of the model's equations, the verification of the single device does not suffice and further investigation on the performance of the model when two devices are connected in series is necessary. In this section, the previously developed SiC power MOSFET module will be verified for the series of two devices.

Fig. 13 reveals the turn-off waveforms of two SiC MOSFETs connected in series, with the bus voltage set to 1.6 kV and the current during turn-off at 350 A. The devices are driven by separate drivers with equal gate resistances (R_g= 20 Ω. The driver's signals were measured and a *4 ns* delay was found in the driver of the lower device, resulting in a small difference in the voltage sharing, as shown in Fig. 14.

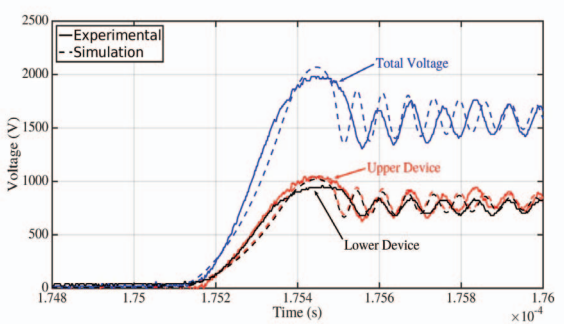

Fig. 13: Turn-off waveforms of two 1.2 kV/ 350 A SiC MOSFETs connected in series at V_{DS}=1600 V, I_D = 350 A, R_{g1} = R_{g2} =20 Ω and T =25 ˚C.

As can be noticed in Fig. 13, the large gate resistance slows down the transient of both series connected devices. Consequently, the gate resistance dominates the transient behavior, and as a result the delay of the gate driver signals and the possible spread of the intrinsic parameters of the modules are not affecting the voltage sharing balance. Nevertheless, the model manages to predict with accuracy the transient behavior of each device along with their final voltage sharing.

In order to investigate the impact of R_g variations, the gate resistances are intentionally modified and the effect of this modification is investigated. The gate resistance of the lower device is set to 8.2 Ω while the one of the upper device is set to 9.0 Ω.

The gate voltage waveforms (without a load) are shown in Fig. 14. It can be depicted that the upper device receives the signal faster due to the delay in the lower device driver, but the difference in the gate resistance value makes the rise of its gate voltage slightly slower.

Despite the small difference in the two signals, severe unbalance is observed as depicted in Fig. 15. The total bus voltage is set to 1.2 kV and the load current equals to 350 A during the turn-off transient. The lower device in this case is blocking approximately 800 V while the upper device only 400 V. The model follows with reasonable accuracy the dynamic as well as the static voltage sharing of the series connected devices. It can also be said that the difference in the gate resistances dominates all other differences that may exist between the intrinsic parameters of the devices, which is something that is beneficiary for the model's verification in the series connection.

Finally, an extreme unbalance is introduced in the dynamic simulation setup. The gate resistance of the lower device is set at 4.0 Ω while the upper devices gate resistance is set at 5.8 Ω. A snubber capacitance of *10 nF* is connected in parallel to the output of the devices under test to provide the needed damping of the oscillations. As a result of the above, a severe unbalance is observed, as reported in Fig. 16, and the voltage level is set to *200 V*. The lower device in this case blocks *178 V* while the upper one only *22 V*.

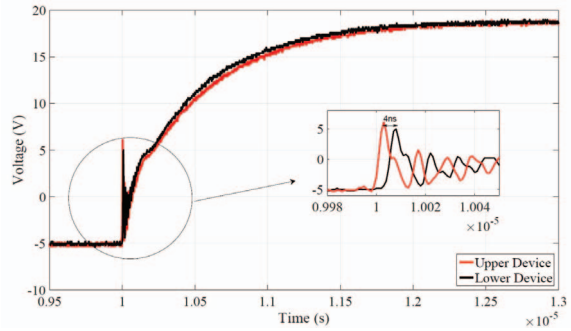

Fig. 14: Gate-to-source turn-on waveform of two 1.2 kV/ 350 A SiC MOSFETs connected in series, with intentionally mismatched gate resistances R_{g1} = 8.2 Ω and R_{g2} = 9.0 Ω.

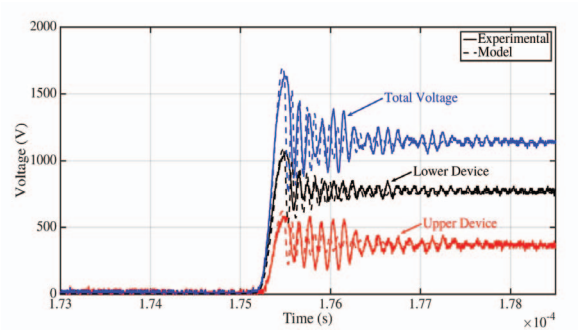

Fig. 15: Turn-off waveforms of two 1.2 kV/ 350 A SiC MOSFETs connected in series at V_{DS}=1200 V, I_D = 350 A, R_{g1} = 8.2 Ω, R_{g2} =9 Ω and T =25 ˚C.

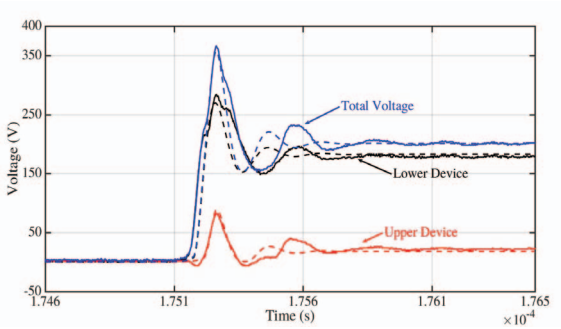

Fig. 16: Turn-off waveforms of two 1.2 kV/ 350 A SiC MOSFETs connected in series at V_{DS}=200 V, I_D = 50 A, R_{g1} = 4.0 Ω, R_{g2} =5.8 Ω and T =25 ˚C.

The model once again predicts with relatively accuracy once again the dynamic and static voltage sharing between the two devices, verifying that it can be used to facilitate the design procedure of a converter system with at least two SiC MOSFET power modules connected in series.

V. Conclusions

The analysis in this paper has focused on an original McNutt/Hefner model which has been implemented in MATLAB/Simulink environment making use of the Simscape language. The model has been validated by predicting the static and dynamic performances of a commercial 1.2 kV/ 350 A SiC MOSFET power module. The parameter extraction procedure is broken into two parts. A first identification procedure gives the initial list of extracted parameters which is then further optimized thanks to an automated optimization tool.

This study contributes to the prediction of a SiC MOSFET power module behavior as well as its connection in a series configuration. The presented results verify that the model could facilitate and help with the design of SiC MOSFETs for high voltage converters with multiple devices connected in series.

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