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Robust Output Voltage Control of Multi-Mode Non-Inverting DC-DC Converter

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ABSTRACT

Linear robust controller design based on Uncertainty and Disturbance Estimator theory for nonlinear uncertain single input single output systems with external disturbances is discussed in the paper with application to the output voltage control of a unidirectional universal multimode buck/boost/buck-boost converter. The converter is characterized by different nonlinear static and dynamic behavior in each of the operating modes. The proposed controller forces the system to maintain nearly nominal performance through the whole range of operation space by appropriately estimating and canceling the terms including nonlinearities, parametric uncertainties and external disturbances. In addition, measurement noise is included in the analysis to demonstrate the trade-offs of the proposed method. Despite the non-triviality and relative complexity of the method, the resulting controller structure is simple, allowing low cost low part count analog implementation. Extended simulation results are presented to demonstrate the effectiveness of the proposed control approach.

Keywords: Uncertainty and disturbance estimator, multimode dc-dc converter, robust control.

I. INTRODUCTION

Battery powered systems have grown tremendously in recent decade (Aharon, & Kuperman, 2011; Aharon, & Kuperman, 2011). To prolong the service time of such devices, efficient power management is required to extend the battery life. As an example, consider a system with a 3.3 V power supply fed by a Li-Ion battery cell. During the discharge process, battery terminal voltage may drop from 4.2 to 2.5 V, i.e. the source voltage may be above, equal to or below the target load voltage. Consequently, in order to efficiently utilize the battery capacity, interfacing dc-dc converter should possess buck-boost characteristics. A non-inverting unidirectional converter, capable of operating in buck, boost and buck-boost modes (Aharon, Kuperman, & Shmilovitz, 2015) has demonstrated remarkable performance, operating with battery-powered systems (Sahu & Rincon-Mora, 2004; Lee, Huang, Wang, Wu, Hung, Ho, Lai, & Chen, 2012; Lee, Khaligh, & Emadi, 2009; Restrepo, Calvente, Cid-Pastor, Aroudi, & Giral, 2011;. Wei, Chen, Wu & Ko, 2012; Kuperman, Aharon, Malki & Kara, 2013). Despite impressive performance, such converter is not straightforward to modulate and control (Lee, Khaligh & Emadi, 2009; Lee, Khaligh, Chakraborty & Emadi, 2009). Moreover, since such a converter is capable of supporting all the three mentioned modes, three different transfer functions need to be appropriately stabilized by the controller (Wei, Chen, Wu & Ko, 2012; Restrepo, Calvente, Romero, Vidal-Idiarte & Giral, 2009). In addition, since the converter possesses nonlinear behavior in each of the three modes, the coefficients of transfer functions obtained by linearization are operating point dependent, burdening the control task.

In order to decrease the complexity of control design, cascaded control structure is usually employed in such applications. Typical cascaded control structure of a power converter is shown in Fig. 1 (Chen, 2012; Erickson & Maksimovic, 2001) The controller consists of two

loops, usually decoupled in frequency domain, i.e. their respective bandwidth are at least 5-8 times apart. The outer (slow) loop performs output voltage regulation by comparing the sensed output voltage v_O to a reference value v_O^{REF}, processing the difference to obtain a reference current i_L^{REF} for the inner (fast) inductor current loop. The latter creates a duty cycle signal d (acting as the control input to the power converter) by processing the difference between the reference current and sensed inductor current i_L, The converter is fed by one controlled (duty cycle d) and two uncontrolled disturbance (input voltage v_{IN} and load current i_O) inputs (Linares-Flores, Barahona-Avalos, Sira-Ramirez & Contreras-Ordaz, 2012). Voltage and current controllers frequency domain decoupling allows each of them to interact with a first order plant and reject only one of the two above mentioned disturbances. Moreover, while shaping one loop, the other one may be assumed "transparent", i.e. when the voltage controller is under consideration, the current loop may be treated as unity gain; when the current loop is concerned, voltage loop signals may be assumed constant.

Current controllers of power supplies are typically implemented by means of analog peak or average mode controllers (Leyva-Ramos, Ortiz-Lopez, Diaz-Saldierna & Morales-Saldana, 2009) possessing extremely high bandwidths while completely rejecting input voltage disturbances (which are typically relatively slow). Moreover, these are relatively easy to design since corresponding current loop plants are usually first order, minimum phase and vary only slightly from one operation mode to another. On the other hand, voltage controllers are more difficult to design since corresponding voltage loop plants are nonlinear (Erickson & Maksimovic, 2001; Olalla, Leyva, El Aroudi, Garces & Queinnec, 2009; Olalla, Leyva, El Aroudi, Garces & Queinnec, 2010), sometimes non-minimum phase and vary significantly from one operation mode to another (Aharon, Kuperman & Shmilovitz, 2015). In addition, load current (disturbance) may vary with relatively high rate. As a result, voltage controller design is typically carried out to achieve specific performance for a worst case plant,

sacrificing the performance in other operating points. In order to eliminate this drawback, some kind of adaptive or robustifying mechanism is necessary at the expense of increased cost, complexity and/or digital implementation (Lopez-Santos, Martinez-Salamero, Garcia, Valderrama-Blavi & Sierra-Polanco, 2015; Linarez-Flores, Hernandez Mendez, Garcia-Rodriguez & Sira-Ramirez, 2014; Maccari, Montagner, Pinheiro & Oliveira, 2012). In this paper, robust Uncertainty and Disturbance Estimator (UDE) based controller design is proposed allowing both analog implementation and maintaining nearly nominal performance through the whole operating region of the power converter.

The UDE-based strategy introduced in (Zhong & Rees, 2004) and further elaborated in (Stobart, Kuperman & Zhong, 2011; Kuperman & Zhong, 2011; Stobart, Kuperman & Zhong, 2011; Zhong, Kuperman & Stobart, 2011; Chandar & Talole, 2014; Kuperman, 2015) is able to quickly estimate uncertainties and disturbances and thus provides excellent robust performance. It is based on the assumption that a continuous signal can be approximated as it is appropriately filtered. The controller consists of two main loops operating as follows: inner (fast) loop estimates lumped uncertainty and disturbance, causing the system to deviate from nominal plant and cancels it, while outer (slow) loop forces the closed loop system to follow desired dynamics. The approach was recently successfully applied to a variety of control problems (Talole & Phadke, 2008; Talole & Phadke, 2009; Talole, Chandar, & Kolhe. 2011; Kolhe, Shaheed, Chandar, & Talole, 2013; Su & Lin, 2011; Su & Lin, 2013; Phadke & Talole, 2012; Kuperman & Zhong, 2013; Kuperman & Zhong, 2015). In this paper, the UDE-based control strategy is applied to solving the voltage control problem by stabilization, allowing the utilization of a single robust controller for all three converter modes of operation, achieving similar performance through the whole operating region.

II. MODELING THE MULTIMODE DC-DC POWER CONVERTER

Consider a non-inverting unidirectional multimode DC-DC converter, shown in Fig. 2. The circuit may operate in any of the three modes: buck (T_2 is constantly off, T_1 is switched), boost (T_1 is constantly on, T_2 is switched) and buck-boost (T_1 and T_2 are switched).

PWM modulator utilized by the converter is shown in Fig. 3 (Aharon, Kuperman, & Shmilovitz, 2015). Basic triangular carrier is duplicated using different shift and scale factors to create two carriers as depicted. The control signal $-1 < d < 1$ (cf. Fig. 1) is then compared to both carriers to create each leg driving signals. From Fig. 3, the duty cycles are given by

$$d_1 = \begin{cases} 0, & d \le -1 \\ K_H(1+d), & -1 \le d \le V_H \\ 1, & d \ge V_H \end{cases}$$
$$d_2 = \begin{cases} 0, & d \le V_L \\ K_L(d - V_L), & V_L \le d \le 1 \\ 1, & d \ge 1 \end{cases}, \quad (1)$$

respectively, with $K_H = (1 + V_H)^{-1}$ and $K_L = (1 - V_L)^{-1}$. Converter operating mode is set by control input only as

$$MODE = \begin{cases} buck, & -1 < d < V_L \\ buckboost, & V_L < d < V_H \\ boost, & V_H < d < 1. \end{cases} \quad (2)$$

For more detailed description of modulator operation an interested reader is referred to (Aharon, Kuperman, & Shmilovitz, 2013) and (Aharon, Kuperman, & Shmilovitz, 2015).

An idealized average model of the converter is shown in Fig. 4. In buck mode, T_1 duty cycle is $d_1 = K_H(1+d)$ and T_2 duty cycle is $d_2 = 0$. In boost mode, T_1 duty cycle is $d_1 = 1$ and T_2 duty cycle is $d_2 = K_L(d-V_L)$. In buck-boost mode, T_1 and T_2 duty cycles are $d_1 = K_H(1+d)$ and $d_2 = K_L(d-V_L)$, respectively.

The average model is described by the following sets of equations, depending on the mode of operation:

$$\left.\begin{aligned}\frac{di_L}{dt} &= \frac{1}{L}\left(d_1 v_{IN} - v_O\right)\\ \frac{dv_O}{dt} &= \frac{1}{C}\left(i_L - i_O\right)\end{aligned}\right\} buck, \tag{3}$$

$$\left.\begin{aligned}\frac{di_L}{dt} &= \frac{1}{L}\left(v_{IN} - (1-d_2)v_O\right)\\ \frac{dv_O}{dt} &= \frac{1}{C}\left((1-d_2)i_L - i_O\right)\end{aligned}\right\} boost, \tag{4}$$

$$\left.\begin{aligned}\frac{di_L}{dt} &= \frac{1}{L}\left(d_1 v_{IN} - (1-d_2)v_O\right)\\ \frac{dv_O}{dt} &= \frac{1}{C}\left((1-d_2)i_L - i_O\right)\end{aligned}\right\} buck-boost. \tag{5}$$

If the current loop is properly closed, the inductor current may be assumed to perfectly follow its reference when designing the voltage controller, i.e. $i_L = i_L^{REF}$ cf. Fig. 1 (Aharon, Kuperman, & Shmilovitz, 2015). As a result, the plant to be regulated by the voltage controller is given by

$$\dot{v}_O = C^{-1}\begin{cases} i_L^{REF} - i_O, & buck \\ (v_{IN} - L\dfrac{di_L^{REF}}{dt})v_O^{-1} i_L^{REF} - i_O, & boost \\ (v_{IN} - L\dfrac{di_L^{REF}}{dt})(v_{IN}+v_O)^{-1} i_L^{REF} - i_O, & buck-boost \end{cases} \tag{6}$$

respectively, for each operation mode. In addition, note that un-modeled dynamics is present since passive components possess equivalent series resistances (ESR), conducting MOSFETS are represented by their respective drain-source on-resistances (R_{DSon}) and diodes forward voltages (V_{Don}) are nonzero. Consequently, the three plants are nonlinear in practice (even though the idealized plant is linear in buck mode). Moreover, linearizing output voltage dynamics in boost and buck-boost modes reveals that the resulting voltage-to-inductor current transform functions are non-minimum phase. Nevertheless, once the desired closed loop

bandwidth is set below the worst case unstable zero frequency, this is out of concern. Rearranging (6), the output voltage dynamics may be reformulated as

$$\dot{v}_O = \begin{cases} G_{buck} i_L^{REF} + h_{buck}, & buck \\ G_{boost} i_L^{REF} + h_{boost}, & boost \\ G_{buck\text{-}boost} i_L^{REF} + h_{buck\text{-}boost}, & buck\text{-}boost \end{cases}, \tag{7}$$

where h_{buck}, h_{boost} and $h_{buck\text{-}boost}$ denote the total uncertainty and disturbance (TUD) of each operation mode, respectively, $G_{buck} = C^{-1}$, $G_{boost} = C^{-1} v_{IN} v_O^{-1}$ and $G_{buck\text{-}boost} = C^{-1} v_{IN} (v_{IN} + v_O)^{-1}$. The capacitance as well as input and output voltages do not remain constant during the operation, hence defining

$$G_{buck} = G_n + \left(G_{buck} - G_n\right), \quad G_{boost} = G_n + \left(G_{boost} - G_n\right), \quad G_{buck\text{-}boost} = G_n + \left(G_{buck\text{-}boost} - G_n\right) \tag{8}$$

leads to a general low frequency plant describing (6), given by

$$\dot{v}_O = G_n i_L^{REF} + h, \tag{9}$$

with

$$h = \begin{cases} h_{buck} + \left(G_{buck} - G_n\right) i_L^{REF}, & buck \\ h_{boost} + \left(G_{boost} - G_n\right) i_L^{REF}, & boost \\ h_{buck\text{-}boost} + \left(G_{buck\text{-}boost} - G_n\right) i_L^{REF}, & buck\text{-}boost \end{cases}. \tag{10}$$

III. LINEAR UDE-BASED CONTROL OF THE MULTIMODE DC-DC POWER CONVERTER

A linear time invariant reference model is chosen according to the desired closed-loop converter output voltage behavior as

$$\dot{v}_{Om}(t) = a_m v_{Om}(t) + b_m v_O^{REF}(t), \tag{11}$$

where v_O^{REF} denotes output voltage reference (cf. Fig. 1) and $a_m = -b_m$ are constants. Consequently, the control objective is to force a stable error between the state of the reference model and the state of the system

$$e(t) = v_{Om}(t) - v_O(t) \tag{12}$$

satisfying the following error dynamic equation,

$$\dot{e}(t) = \left(a_m + k\right)e(t), \tag{13}$$

where k is an error feedback gain. If the reference model is chosen to be stable, k may be chosen as zero. If different error dynamics is desired or required to guarantee stability, commonly used control strategies can be used to choose k.

Combining (10) – (13) results in (the arguments of functions in the time-domain are omitted hereafter for brevity)

$$a_m v_O + b_m v_O^{REF} - G_n i_L^{REF} - h = ke. \tag{14}$$

Hence, control signal i_L^* needs to satisfy

$$G_n i_L^{REF} = a_m v_O + b_m v_O^{REF} - h - ke. \tag{15}$$

Nevertheless, (15) cannot be implemented since h is unknown. On the other hand, using (9) there is

$$h = \dot{v}_O - G_n i_L^{REF}. \tag{16}$$

Hence, the unknown/nonlinear dynamics and disturbances can be obtained from the known linear dynamics of the system and the control signal. However, it cannot be directly used to formulate a control law. The UDE-based strategy proposed in (Zhong & Rees; 2004) adopts an estimation of the TUD to construct a control law as follows. Assume that $g_f(t)$ is the impulse response of a linear filter $G_f(s)$, whose pass-band contains as much as possible of frequency content of h. Then TUD can be accurately estimated from the output of the UDE as

$$h_{ude} = h * g_f, \tag{17}$$

where '*' is the convolution operator. Using (17) instead of TUD in (15) re-defines the control signal requirements as

$$G_n i_L^{REF} = a_m v_O + b_m v_O^{REF} - h_{ude} - ke = a_m v_O + b_m v_O^{REF} - \left(\dot{v}_O - G_n i_L^{REF}\right) * g_f - ke. \tag{18}$$

Applying the Laplace transform and rearranging, following desired control law is obtained,

$$I_L^{REF}(s) = \frac{G_n^{-1}}{1 - G_f(s)}\left[\left(a_m - sG_f(s)\right)V_O(s) + b_m V_O^{REF}(s) - kE(s)\right], \quad (19)$$

where $I_L^{REF}(s) = L\{i_L^{REF}(t)\}$, $V_O(s) = L\{v_O(t)\}$, $V_O^{REF}(s) = L\{v_O^{REF}(t)\}$, $E(s) = L\{e(t)\}$ with $L\{\cdot\}$ denoting the Laplace transform operator. Obviously, the control signal is independent of unknown/nonlinear dynamics and disturbances. Note that when $G_f(s)$ is strictly proper, $sG_f(s)$ is implementable and there is no need of measuring or estimating the output voltage derivative. Nevertheless, since measured state fed back to the controller is corrupted by additive noise $n(t)$, substituting $V_O(s)$ with $V_O(s) + N(s)$ in (10) makes the actual control signal to contain noise as well,

$$I_L^{REF}(s) = \frac{G_n^{-1}}{1 - G_f(s)}\left[\left(a_m - sG_f(s)\right)V_O(s) + b_m V_O^{REF}(s) - kE(s) + \left(a_m - sG_f(s) + k\right)N(s)\right] \quad (20)$$

with $N(s) = L\{n(t)\}$.

Substituting (20) into (9) and taking into account the Laplace transform of (2), the closed loop state dynamics is obtained as

$$V_O(s) = Z_m(s)V_O^{REF}(s) + Z_1(s)\left(Z_2(s)H(s) + Z_3(s)N(s)\right), \quad (21)$$

where $H(s) = L\{h(t)\}$, $Z_m(s) = (s - a_m)^{-1}b_m$ is the reference model transfer function, $Z_1(s) = -(s - [a_m+k])^{-1}$, $Z_2(s) = 1 - G_f(s)$ and $Z_3(s) = a_m + k - sG_f(s)$. Note that $Z_m(s)$ is independent on k and G_f, therefore the proposed control law allows decoupling between tracking (determined by $Z_m(s)$) and noise/disturbance rejection (governed by $Z_1(s)$, $Z_2(s)$ and $Z_3(s)$).

The resulting error dynamics is obtained by subtracting (21) from the Laplace transform of (11) as

$$E(s) = Z_1(s)\left(Z_2(s)H(s) + Z_3(s)N(s)\right). \quad (22)$$

According to (13), the TUD is attenuated twice: first by a low-pass filter Z_1(s); second by the filter $Z_2(s)$, possessing high-pass filter properties if $G_f(s)$ is strictly proper. Measurement noise is shaped twice as well, initially by the low-pass filter $Z_1(s)$ and then by a frequency selective

filter $Z_3(s)$. In order to assure that the system output follows the reference model, the right-hand side of (22) must be close to zero in steady state. This is satisfied if $Z_1(s)\cdot Z_2(s)$ and $Z_1(s)\cdot Z_3(s)$ respectively are close to zero at the frequency range where $H(s)$ and $N(s)$ contain significant energy. Note that $Z_1(s)$ independent on G_f, and is decoupled from $Z_2(s)$ and $Z_3(s)$, allowing separate design of the filter $Z_1(s)$ by selecting appropriate k. On the other side, filters $Z_2(s)$ and $Z_3(s)$ are related since both depend on G_f, while a_m is forced by the reference model.

Keeping in mind that the controller should be as simple as possible to allow low part count analog implementation, consider the first order Butterworth filter, given by

$$G_f(s) = \frac{1}{Ts+1}, \tag{23}$$

leading to $Z_2(s) = \frac{Ts}{Ts+1}$ and $Z_3(s) = \left(a_m + K\right)\frac{\left(T\cdot(a_m+K)^{-1}\right)s+1}{Ts+1}$. Obviously, $Z_2(s)$ is a high pass filter and $Z_3(s)$ is a lead-lag filter. Moreover, remarking that stable reference model requires negative a_m with $|a_m| = |b_m|$ and noting that $\frac{1}{1-G_f} = 1+\frac{1}{Ts}$ and $\frac{sG_f}{1-G_f} = \frac{1}{T}$, the control action in (19) reduces to

$$I_L^{REF}(s) = G_n^{-1}\left(\left[1+\frac{1}{Ts}\right]\left[b_m\left(V_O^{REF}(s)-Y(s)\right)-kE(s)\right]-\frac{1}{T}Y(s)\right), \tag{24}$$

where $Y(s) = V_O(s) + N(s)$ and $E(s) = V_O^{REF}(s) - Y(s)$. Block diagram of the corresponding control structure is shown in Fig. 5.

In case the reference signal $v_O^{REF}(t)$ is constant, tracking dynamics has little or no meaning (assuming that during start-up initial transients are governed by a soft-start sequence) and the disturbance rejection is the main issue. In order to robustify the system against TUD, the corner frequency of $Z_1(s)$ should be as low as possible, while the corner frequency of $Z_2(s)$ should be as high as possible. As to measurement noise (which usually resides at the high frequency portion of the spectrum), the requirement regarding the corner frequency of $Z_1(s)$ is

the same. As to $Z_3(s)$, for $|a_m| > 1$ it amplifies the high frequency noise. As a result, if the reference model may be chosen relatively slow, the corner frequency of $Z_1(s)$ will be reduced as well as the high frequency gain of $Z_3(s)$. Moreover, for low enough $|a_m|$ the gain k may be selected as zero, simplifying the controller and reducing the parts count. Obviously, the control design is then reduced to selecting b_m and T only.

When assuming $k = 0$, two remarks should be made. First, the controller reduces to the structure shown in Fig. 6, which was recently shown to be suitable for single operational amplifier analog implementation in (Sitbon, Schacham & Kuperman, 2015)

Second, (24) can be rearranged as

$$\begin{aligned} I_L^{REF}(s) &= G_n^{-1} b_m \left[1 + \frac{1}{Ts}\right] V_O^{REF}(s) - G_n^{-1}\left(T^{-1} + b_m\right)\left(1 + \frac{1}{\left(T + b_m^{-1}\right)s}\right) Y(s) \\ &= H_1(s) V_O^{REF}(s) - H_2(s) Y(s) \end{aligned}, \qquad (25)$$

revealing the two-degrees-of-freedom nature of the controller which consists of two PI actions: prefilter $H_1(s)$ and feedback controller $H_2(s)$. The overall closed loop system is shown in Fig. 7 and will be used for stability and robustness analysis and in the following section.

IV. CONTROLLER DESIGN EXAMPLE

Consider a battery powered system, based on the multi-mode, unidirectional buck-boost DC-DC converter, shown in Fig. 2. The converter is feeding a dynamic load and is supplied by a Li-Ion battery pack of 4 series connected cells. As a result, the input voltage of the converter may vary from 4·4.2 = 16.8 V (full pack) down to 4·2.5 = 10 V (empty pack) while the load voltage is required to be regulated to a constant level of v_O^{REF} = 13 V. The modulator is designed such that the converter operates in buck mode when the input voltage is higher than

14.5 V, in buck-boost mode when the input voltage is between 11.5 V and 14.5 V and in boost mode when the input voltage reduces below 11.5 V. The current loop is assumed to operate properly with 10 kHz (20000π rad/s) bandwidth. The values of converter components along with the values of parasitic elements are given in Table I. Note that neither of the parameters is known to the controller.

The UDE filter time constant is chosen as $T = (2000\pi)^{-1}$[sec/rad] (i.e. equal to 1/10 current loop bandwidth to allow loop decoupling) while the reference model dynamics is selected as $b_m = 20\pi$ rad/s (i.e. "low enough" to improve noise immunity since fast tracking is not required, see the last sentence of Section 2). Nominal capacitance C_n is assumed 500 μF and G_n is set to C_n^{-1}. The consequent Bode diagrams of Z_m and Z_1-Z_3 are shown in Fig. 8, where the frequency characteristics mentioned earlier are evident.

Frequency responses of TUD and noise shaping filters $Z_{12}(s) = Z_1(s)\cdot Z_2(s)$ and $Z_{13}(s) = Z_1(s)\cdot Z_3(s)$ are shown in Figs. 9 and 10, respectively. Obviously, the TUD is processed by a band-pass filter with worst-case attenuation of around -95 dB while the noise is shaped by a low-pass filter with corner frequency of around 9500 kHz (60 krad/s). Hence, the converter switching frequency should be selected above this corner frequency in order to attenuate switching noise and was set to 100 kHz (200π krad/s) in the simulations.

The family of the plant Bode diagrams $P(s) = \frac{V_O(s)}{I_L^{REF}(s)}$ obtained by linearizing (6) around an operating point given by $v_{IN} = V_{IN}$, $v_O = V_O$ and $i_O = I_O$ as (Erickson & Maksimovic, 2001)

$$P(s)=\begin{cases}\dfrac{1}{Cs}, buck\\ \dfrac{V_{IN}}{I_O}\dfrac{1-LI_OV_OV_{IN}^{-2}s}{1+CV_OI_O^{-1}s}, boost\\ \dfrac{V_{IN}}{I_O}\dfrac{1-I_OL\left(V_{IN}+V_O\right)V_{IN}^{-2}s}{1+C\left(V_{IN}+V_O\right)I_O^{-1}s}, buck-boost\end{cases} \quad (26)$$

is shown in Fig. 11 for the input voltages of $10 < v_{IN} < 16.8$ V and output currents of $1 \text{ A} < i_O < 5$ A. It may be concluded that the plant undergoes significant variation upon both mode and operation point changes, acting as an integrator in buck mode and lag-lead in boost and buck-boost modes. Moreover, while the plant is represented by a single transfer function in the buck mode, multiple transfer functions characterize the plant in other two modes due to nonlinearity.

Corresponding family of loop gains $P(s)H_2(s)$ (cf. Fig. 7) is shown in Fig. 12. As expected, the bandwidth of the loop gain is circa T^{-1} for all operation points and mode. Moreover, the loop is stable with the worst case phase margin of 45°. This demonstrate the robustness of the controller, allowing to achieve nearly constant bandwidth and phase margin despite plant nonlinearities (leading to multiple transfer function representation shown in Fig. 11).

The family of tracking transfer functions $\frac{V_O(s)}{V_O^{REF}(s)} = H_1(s)\frac{P(s)}{1+P(s)H_2(s)}$ is shown in Fig. 13. Note that following (11), the tracking transfer functions should follow the reference model $Z_m(s)$, defined by a first-order low-pass filted with the cutoff frequency of $b_m = 20\pi$ rad/s. According to Fig. 13, all the tracking transfer functions closely follow the reference model whithin the bandwidth of interest, again validating the controller robustness. It should be noted that the tracking transfer function do diverge beyond the bandwidth of interest, which is of course irrelevant for closed loop performance.

V. TIME-DOMAIN SIMULATION RESULTS

A. Performance verification

The system under investigation was simulated using PSIM software. Simulation circuit is shown in Fig. 14. The battery pack is modeled using a variable voltage source while the load consists of passive and active components. A 13 Ω resistor represents constant resistive load component while pulsed current load of 1A average, 2 A peak-to-peak plays the role of the dynamic component. Voltage controller is implemented according to (24), driving the average current controller and modulator, designed folowing the guidelines given in (Aharon, Kuperman, & Shmilovitz, 2015).

Two simulations were carried out. In the first, output voltage reference was held at 13 V while input voltage was reduced ramp-like from 16.8 V (full battery) down to 10 V (depleted battery). The results are shown in Fig. 15. The converter passes through three operating modes with the reduction of battery voltage, yet dynamic response to load changes and zero steady state error remain nearly unaltered despite mode transitions. The control signal (inductor current reference i_L^{REF}) is shown as well along with actual inductor current i_L to validate correct operation of the current controller.

In the second simulation, tracking capabilities of the controller were examined by altering the output voltage reference from 10 V to 18 V and back while reducing input voltage ramp-like from 16.8 V (full battery) down to 10 V (depleted battery) and keeping the constant load current of 3 A . The result is shown in Fig. 16. It may be concluded that the system follows the reference model precisely.

B. Comparison to PI control

The purpose of the comparison below is demonstrating that the two-degrees-of-freedom controller is capable of decoupling tracking and disturbance rejection performance while the classical PI controller is not. Following (9), a PI controller is designed as

$$C_{PI}(s) = G_n^{-1}\left(2\omega_d + \frac{(\omega_d)^2}{s}\right), \tag{27}$$

where ω_d rad/s is the desired nominal bandwidth. It is well-known that in case a PI controller is utilized, tracking and disturbance rejection are coupled (Zhang, Xi, Yang & Xu, 2002). Consequently, in case the controller is designed to match the tracking bandwidth of the UDE-controlled system (i.e. $\omega_d = 20\pi$ rad/s), the disturbance rejection is expected to be sacrificed. Simulation result, comparing tracking voltage error $v_O^{REF} - v_O$ of UDE and PI based controllers under the conditions of the first simulation above is shown in Fig. 17. As expected, the PI controller fails to assure decent tracking performance since the resulting disturbance rejection capabilities are insufficient.

VI. CONCLUSIONS

A method of designing a linear robust controller for nonlinear uncertain single input single output systems with external disturbances, based on Uncertainty and Disturbance Estimator theory was proposed in the paper. The approach was successfully applied to control the output voltage of a unidirectional multi-mode buck-boost converter. By quickly estimating and canceling the uncertainties and disturbances, the controller forces the system to maintain nearly nominal performance through the whole range of operating points. Despite the relatively non-trivial and complex underlying theory, the resulting controller structure turns out to be relatively simple, allowing low cost analog implementation with low part count. Extended simulation results were presented to demonstrate the feasibility of the proposed method.

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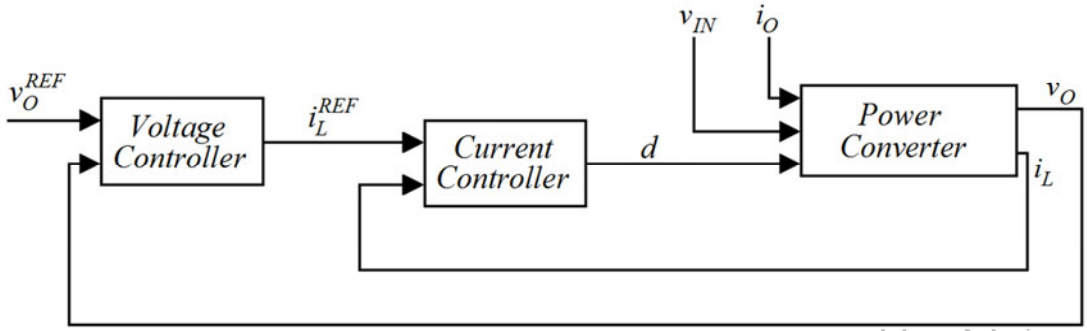

Fig. 1. Typical cascaded control structure of a power converter

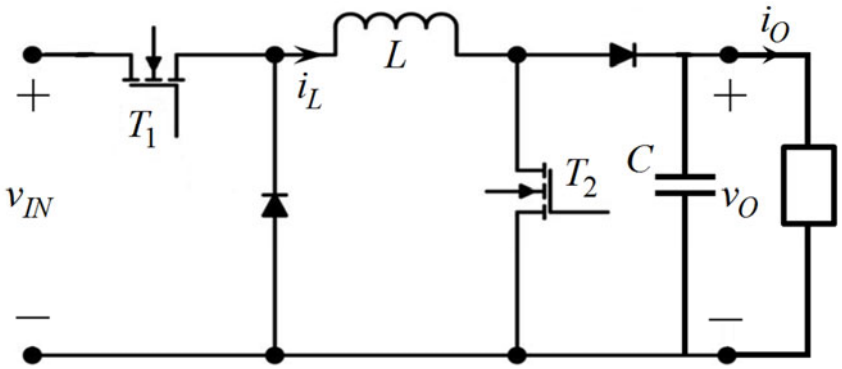

Fig. 2. Multimode noninverting unidirectional DC-DC converter

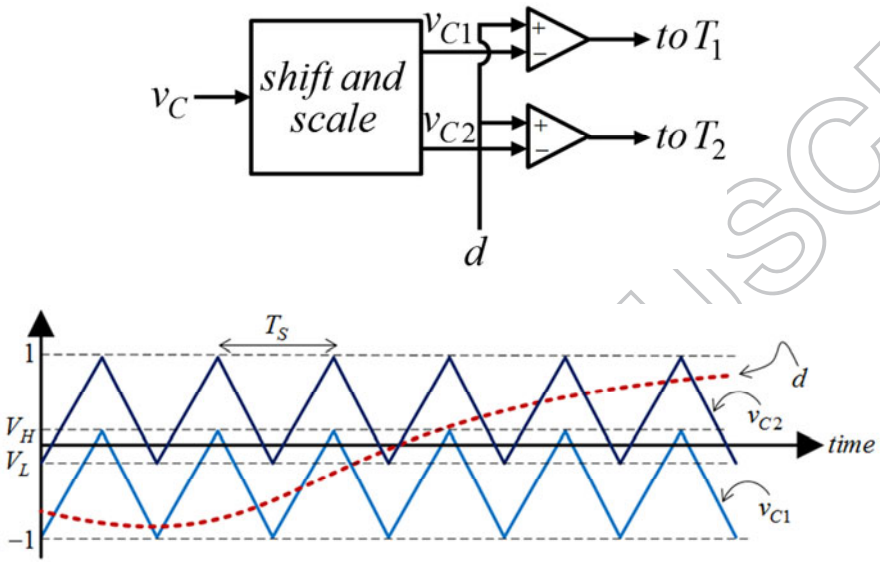

Fig. 3. Modulator structure (top) and corresponding waveforms (bottom).

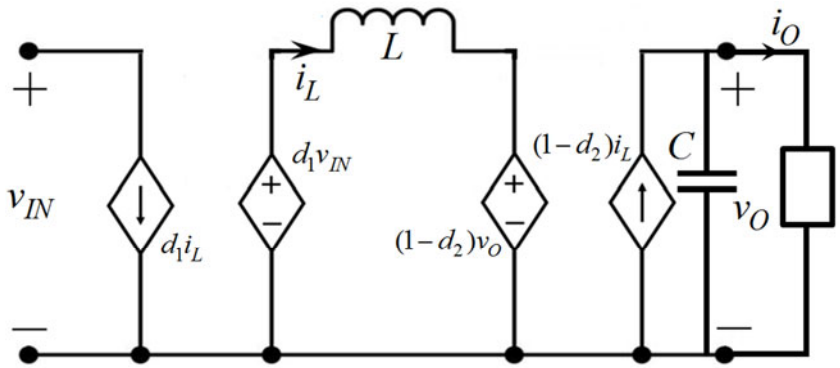

Fig. 4. Average model of the converter

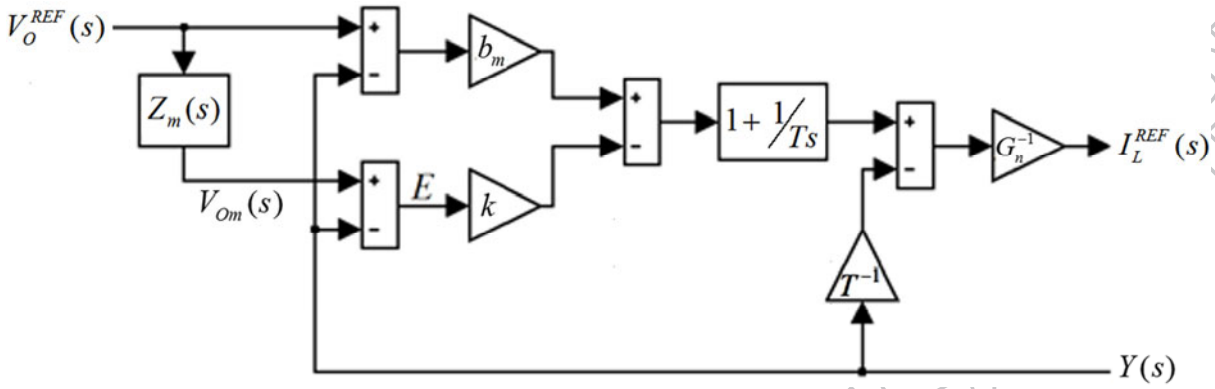

Fig. 5. UDE-based controller block diagram

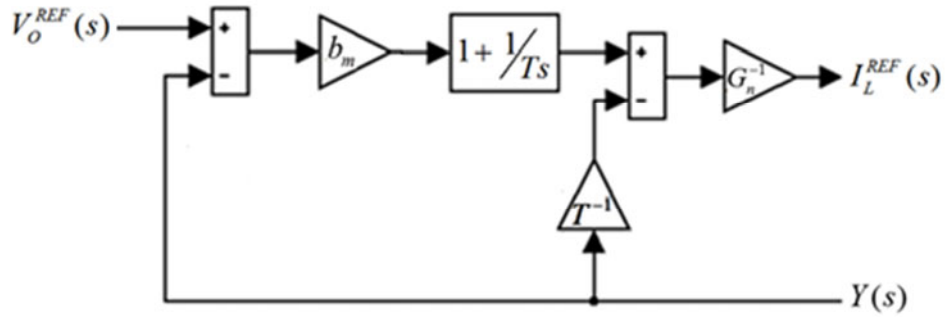

Fig. 6. UDE-based controller block diagram with k = 0, suitable for single operational amplifier analog implementation

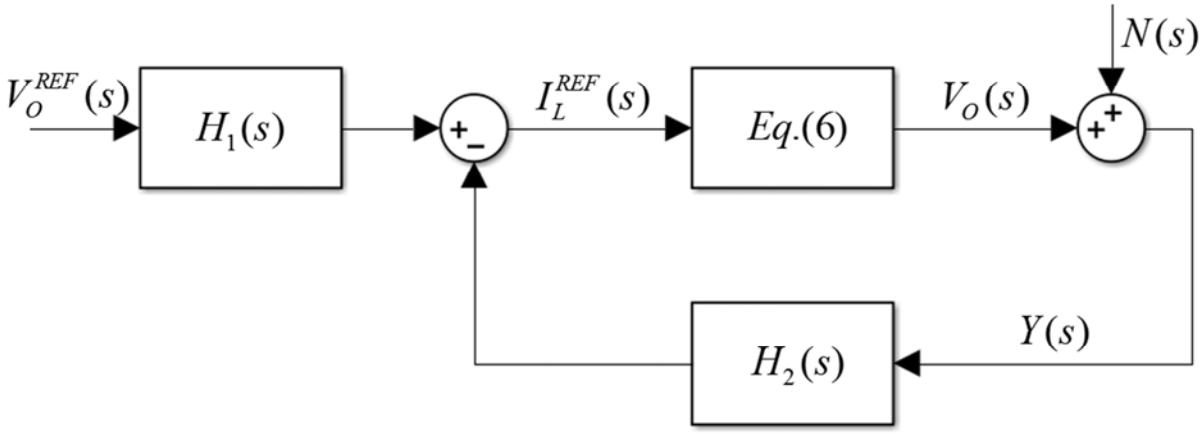

Fig. 7. Overall UDE controller based control-oriented closed loop diagram

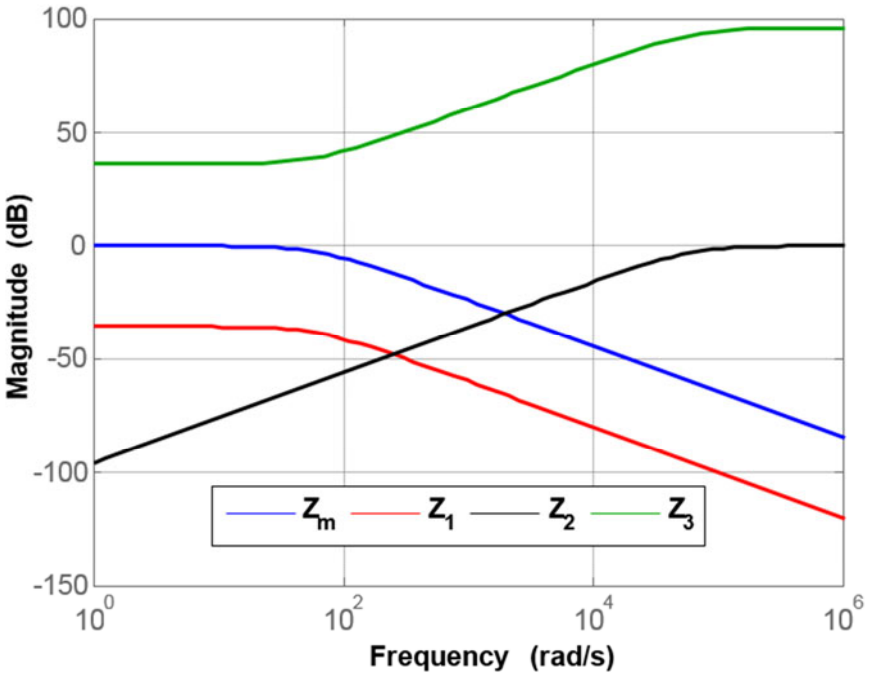

Fig. 8. Frequency responses of filters Z_m and Z_1-Z_3

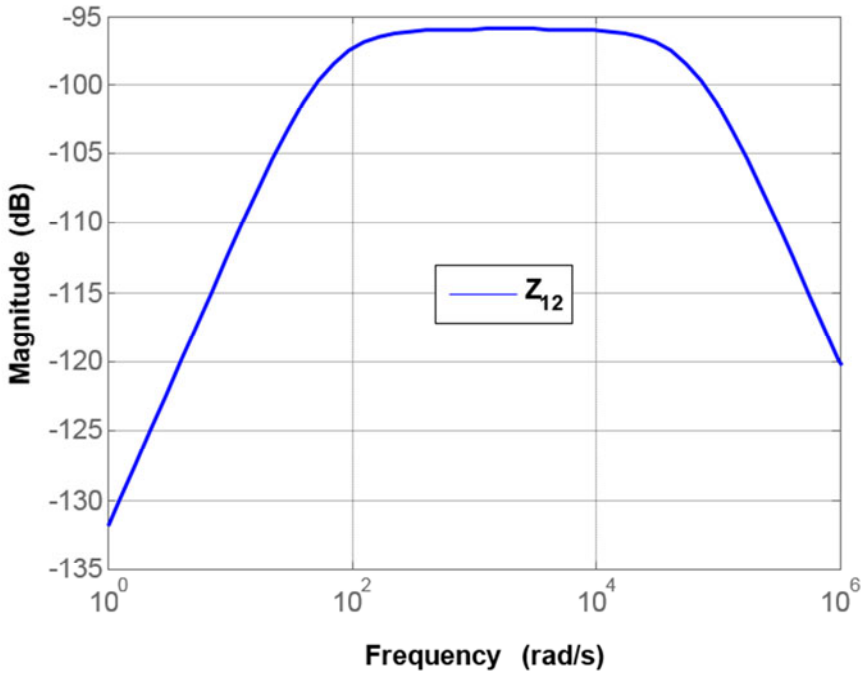

Fig. 9. Frequency response of TUD shaping filter Z_{12}

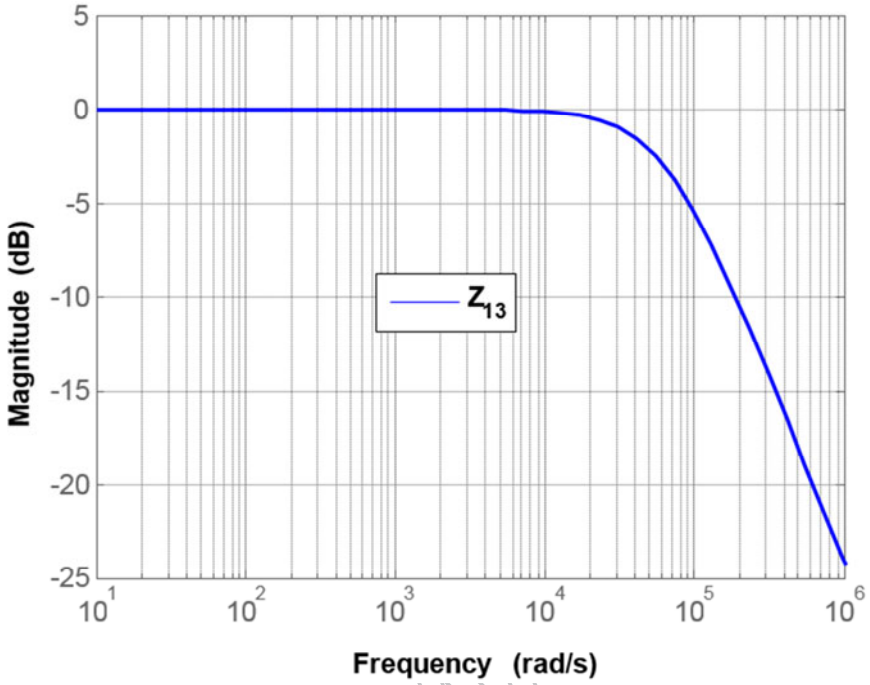

Fig. 10. Frequency response of noise shaping filter Z_{13}

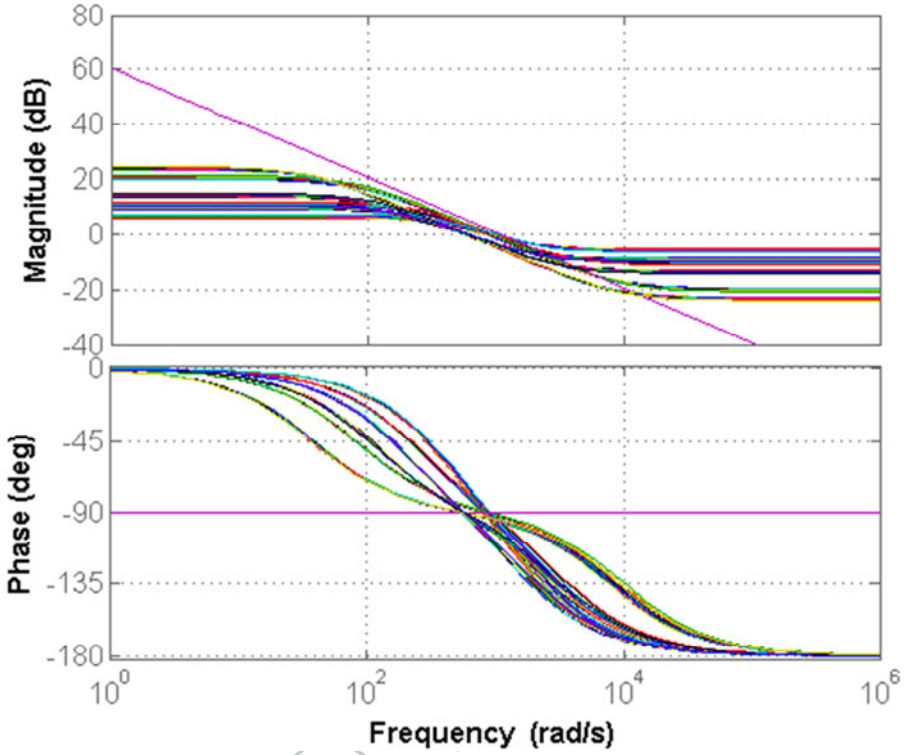

Fig. 11. Family of the plant Bode diagrams

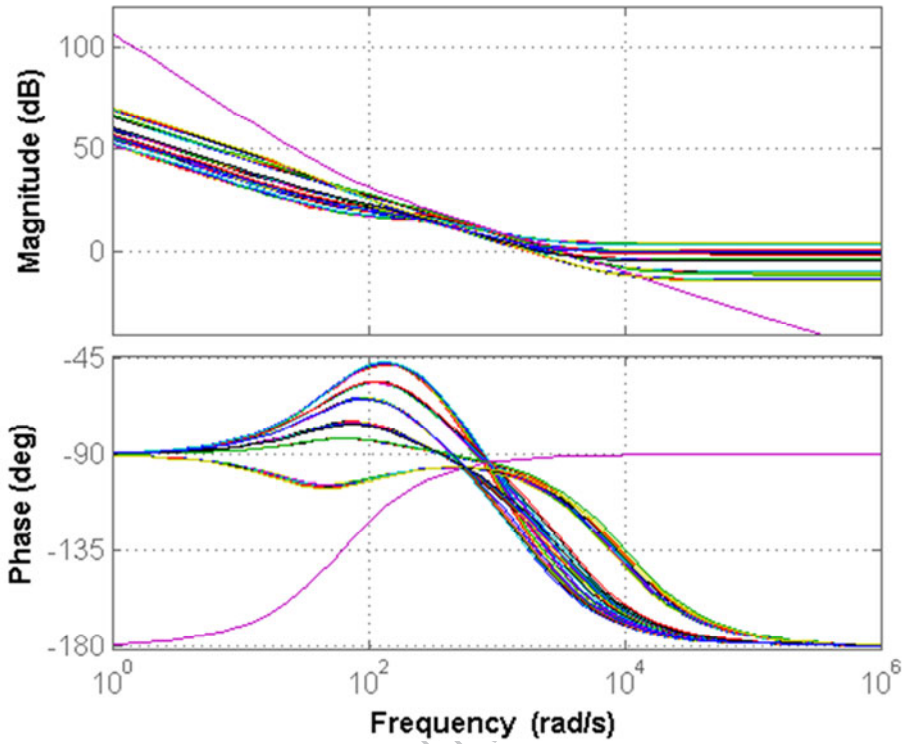

Fig. 12. Family of the loop gain Bode diagrams

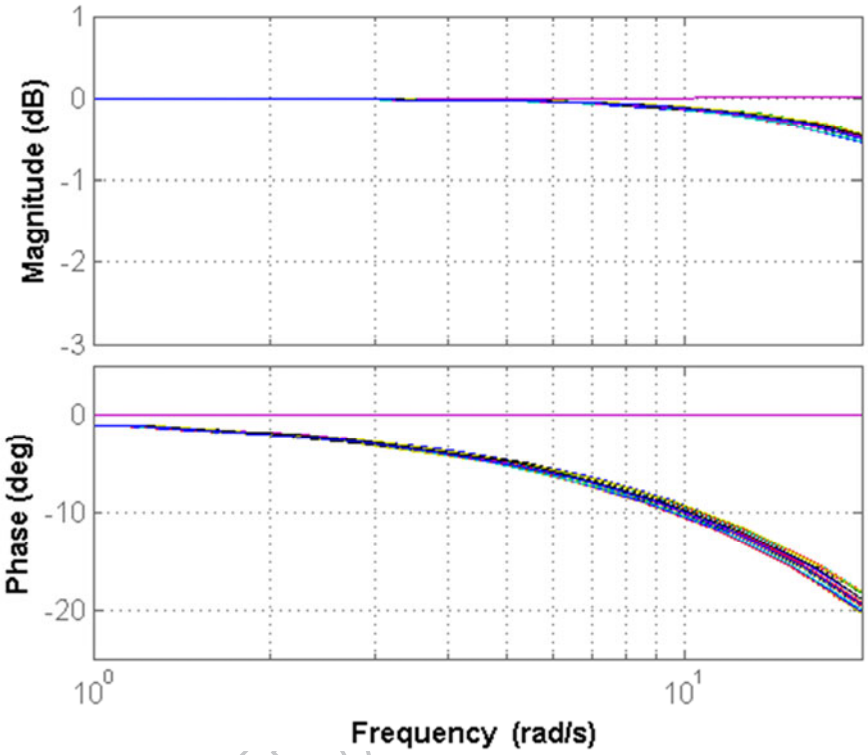

Fig. 13. Family of the tracking transfer function Bode diagrams

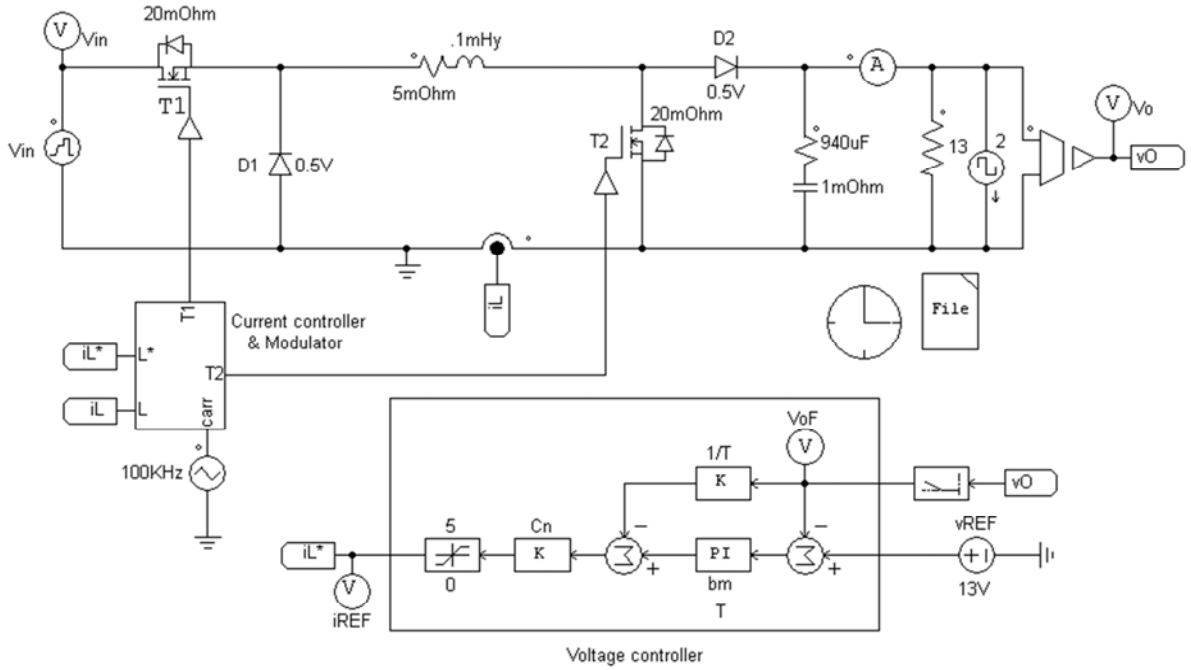

Fig. 14. PSIM simulation setup

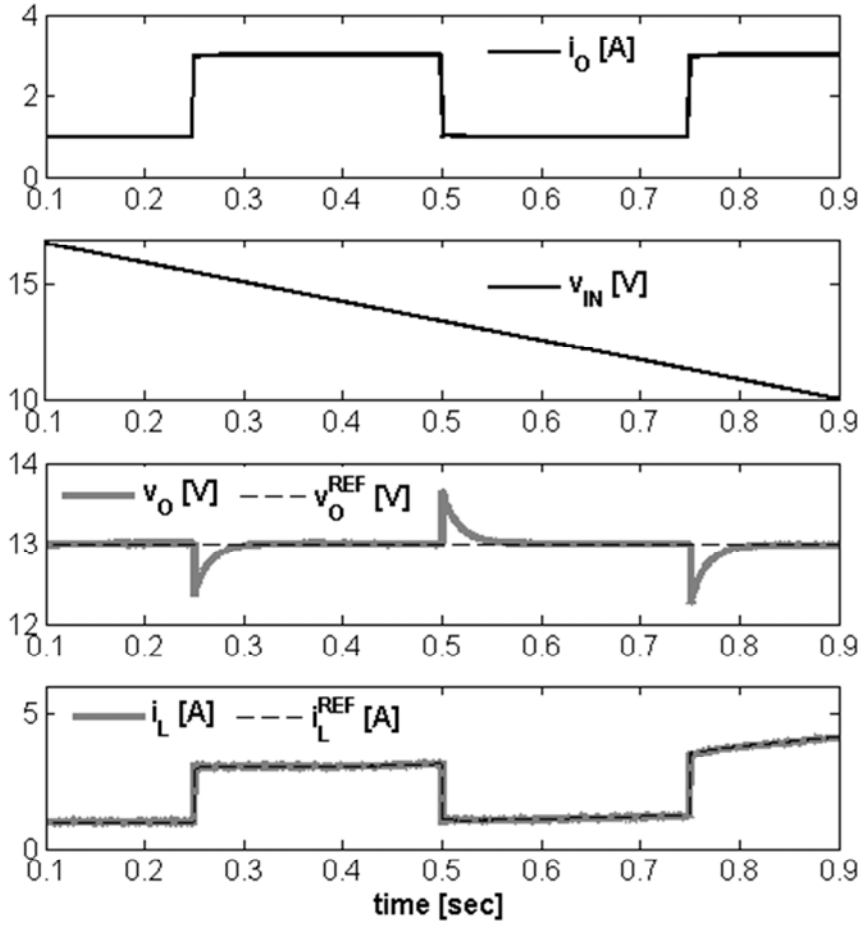

Fig. 15. Disturbance rejection simulation results (from top to bottom): Load current; Input voltage; Reference and output voltages; Reference and inductor currents.

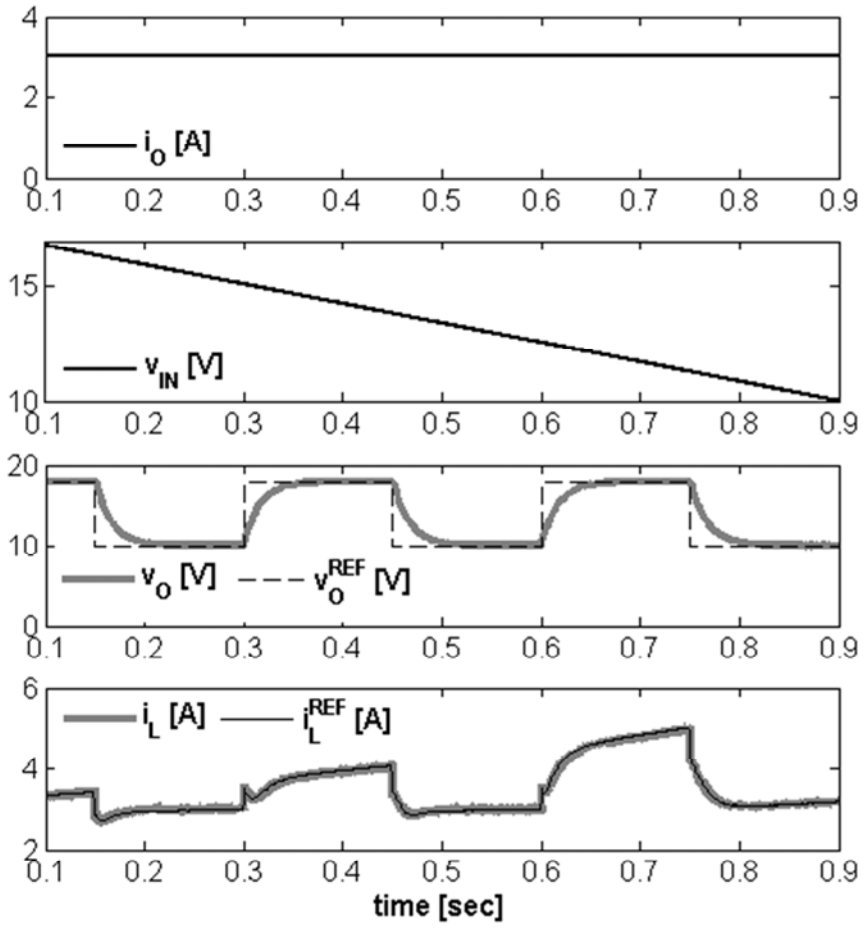

Fig. 16. Tracking simulation results (from top to bottom): Load current; Input voltage; Reference and output voltages; Reference and inductor currents.

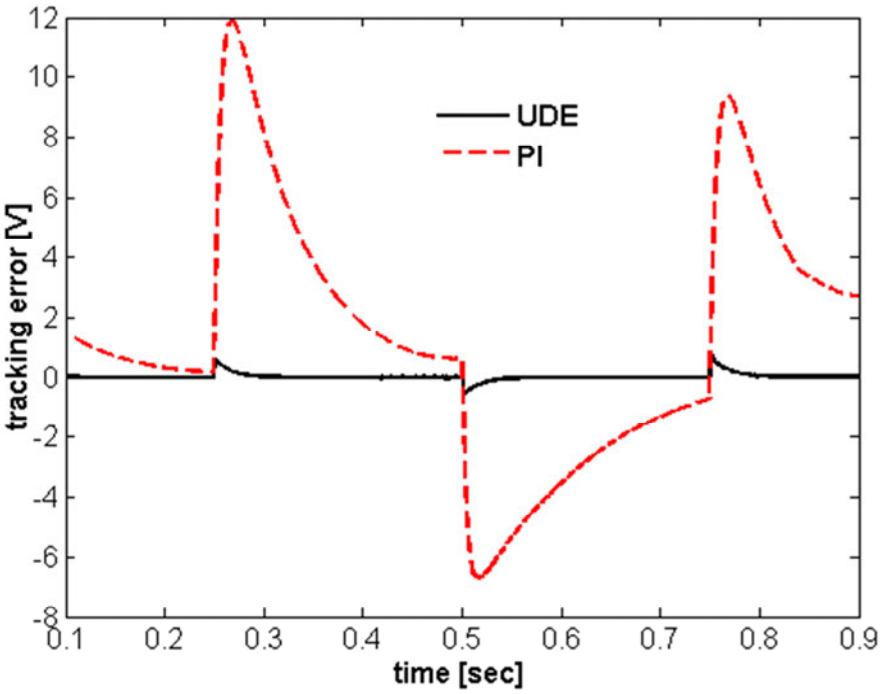

Fig. 17. Output voltage tracking error of 20π rad/s bandwidth UDE and PI controllers

TABLE I CONVERTER COMPONENTS VALUES

Parameter	Value	Units
Inductance L	0.1	mH
ESR(L)	5	mΩ
Capacitance C	940	μF
ESR(C)	1	mΩ
$R_{DSon}(T_1)$	20	mΩ
$R_{DSon}(T_2)$	20	mΩ
$V_{Don}(D_1)$	0.5	V
$V_{Don}(D_2)$	0.5	V
Switching frequency F_s	100	kHz