High Step-Up Converter Based on Charge Pump and Boost Converter

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***Abstract*—In this paper, a novel step-up converter is presented, where the charge pump concept, combined with the traditional boost converter structure, is utilized. Although two inductors are used in such a converter, the difference in value between the two inductors affects the regulation performance of this converter slightly. Furthermore, the behavior of this converter is similar to the traditional boost converter, and hence, the control of this converter can be realized easily. Above all, the energy stored in the two inductors, connected in series with the energy stored in the charge pump capacitor and the input voltage, is released to the load during the demagnetization period. In this paper, the basic operating principles of the proposed converter are presented along with some experimental results to demonstrate the effectiveness of this converter.**

***Index Terms*—Boost converter, charge pump, demagnetization period, high step-up converter.**

I. Introduction

As generally recognized, step-up converters have been widely used in many applications, such as battery-powering device, uninterruptible power supply (UPS), photovoltaic (PV) system, etc., requiring some circuits transferring low voltages to high voltages used as input voltages for dc–ac converters.

Up to now, there have been many researches on how to get circuits with high voltage conversion ratios, based on several converters with output voltages connected in series [1], [2] or the coupling inductor concept [3]–[8] or on the charge pump concept [9]–[18] or even on the last two concepts combined [19]–[24]. The step-up converters mentioned before have some demerits. For example, in [4]–[9], [11], [15]–[17], [20], and [23], there are many complicated circuits presented, where two switches or more and mass passive components cause conversion efficiency to be degraded. Only low-power applications are suitable in [3], [9], [11], [14]–[18], and [24]. Some switches are floating in [4], [9], [10], [13]–[15], and [17], thereby causing additional isolated gate driving circuits to be needed, and hence, making systems complex. The nonlinear relationships between the input and output voltages exist due to high voltage conversion ratios in [3], [4], [11], [16], [17], and [19]–[21], thereby causing the system to be difficult to control.

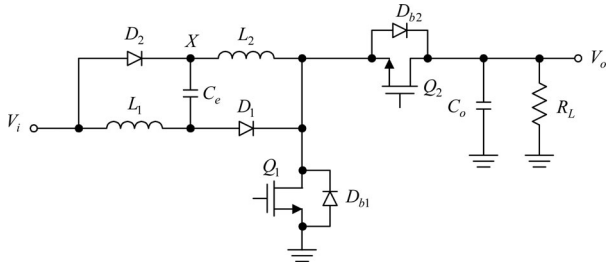

Fig. 1. Proposed step-up converter.

According to the aforementioned, in this paper, a step-up converter with a high voltage conversion ratio is presented, whose two inductors are magnetized simultaneously, and, together with the input voltage and the energy stored in the charge pump capacitor, pump energy into the output. Such a circuit is simple, combining the charge pump concept with the traditional boost converter structure. Although there actually exists the difference in value between the two inductors in this circuit topology, the proposed converter possesses a good and robust performance of regulation, with the behavior similar to that of the traditional boost converter and hence with easy control.

II. Proposed Converter Structure

Fig. 1 shows the proposed step-up converter that contains two inductors L_1 and L_2, two diodes D_1 and D_2, charge pump capacitor C_e, one output capacitor C_o, two MOSFET switches Q_1 and Q_2 with two body diodes D_{b1} and D_{b2} connected in parallel, respectively, and one output resistor R_L. The gate driving signal created from the digital control effort is employed to drive Q_1 that is used as a main switch, and the gate driving signal complementary to that for Q_1 is utilized to drive Q_2 that is used as a synchronous rectifier.

It is noted that the reason why the proposed circuit uses a synchronous rectifier is described next. As generally acknowledged, if the converter operates in discontinuous conduction mode (DCM) with the output voltage regulated using the output diode, the less the load is, the less the duty cycle. Hence, the corresponding control is not so easy because a too small duty cycle is sensitive to the noise. For the convenience of control and analysis, a synchronous rectifier is used herein instead of the output diode, thereby causing that the duty cycle is not changed too much all over the load range. It is noted that the main switch

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and the synchronous rectifier are driven only by one half-bridge gate driver, such as HIP2101, and this is very easy to implement.

Furthermore, one comparison is made between the converter shown in [25, Fig. 9] and the proposed converter. In the circuit shown in [25, Fig. 2], two inductors are magnetized simultaneously, and the input voltage, together with the energy stored in two inductors, passes the energy to the output, whereas in the proposed circuit, two inductors are also magnetized simultaneously, but the input voltage, together with the energy stored in the charge pump capacitor and two inductors, passes the energy to the output. Therefore, the former has a smaller voltage conversion ratio, corresponding to $2D/(1-D)$, than the latter, corresponding to $2/(1-D)$. It is noted that in [25], there is no discussion about what will happen if the value of L_1 is not identical to the value of L_2. If two inductances are different, then in the condition of the same turn-ON time and the same voltage applied, two inductors get magnetized. The moment the switch is turned OFF, the small inductance has a larger current than the big inductance. And hence, at this instant, two inductors connected in series will conflict with the Kirchhoff's current law (KCL).

On the other hand, the other comparison is made between the converter shown in [26, Fig. 2] and the proposed converter. In the circuit shown in [26, Fig. 2], during the turn-ON period, two inductors and one charge pump capacitor are magnetized and charged simultaneously, and the input voltage, together with the energy stored in two capacitors, pumps the energy into the output, whereas during the turn-OFF period, the energy stored in two inductors and one charge pump capacitor connected in series is released to these two capacitors. In the proposed circuit, two inductors are also magnetized simultaneously during the turn-ON period, but the input voltage, together with the energy stored in two inductors and one charge pump capacitor, passes the energy to the output during the turn-OFF period. That is, the voltage boosting in the former is based on the input voltage connected in series with two series capacitors, whereas the voltage boosting in the latter is based on the input voltage connected in series with two series inductors and one charge pump capacitor. Therefore, the former has a voltage conversion ratio of $(3+D)/(1-D)$ that is larger than the voltage conversion ratio of $2/(1-D)$ for the latter. However, the former has more components than the latter, and the difference in number of components between the two is four.

III. Basic Operating Principles

The following description focuses on discussing the basic operating principles of the proposed converter. The values of L_1 and L_2 will affect the operating behavior of this converter remarkably. And hence, there are three cases to be described as follows, with the assumption that the voltages across all the switches and diodes are zero during the turn-ON period, C_e is large enough to keep the voltage across C_e, v_e is constant at the input voltage v_i, and the blanking times between the two switches are zero. It is noted that this converter always operates in the continuous conduction mode (CCM). Hence, the currents flowing through two inductors can be positive or negative, but the corresponding average currents must be zero or positive.

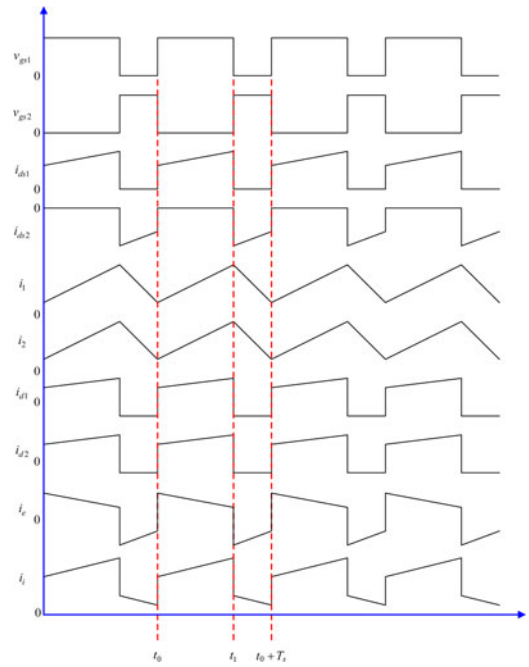

Fig. 2. Key waveforms relevant to case 1.

Moreover, there are some symbols to be given as follows: 1) the input voltage and current are signified by v_i and i_i; 2) the output voltage is expressed by v_o; 3) the voltage and current in C_e are represented by i_e and v_e; 4) the currents flowing through L_1 and L_2 are denoted by i_1 and i_2; 5) the currents in Q_1, Q_2, D_1, and D_2 are indicated by i_{ds1}, i_{ds2}, i_{d1}, and i_{d2}, respectively; and 6) the gate driving signals for Q_1 and Q_2 are signified by v_{gs1} and v_{gs2}, respectively.

A. Case 1

This is an ideal case under the assumption that the value of L_1 is equal to that of L_2. Fig. 2 shows the key waveforms relevant to this case, where T_s is the switching period. For analysis convenience, let

$$L = L_1 + L_2 \tag{1}$$

and

$$i_1 = i_2 = i. \tag{2}$$

1) State 1 ($t_0 \sim t_1$): As shown in Fig. 3, Q_1 is turned ON, Q_2 is turned OFF, and D_1 and D_2 are forward biased. Since the voltage across C_e is equal to v_i, L_1 and L_2 are to be magnetized. During this state, the output energy required is supplied from C_o, and C_e is charged. Therefore, the corresponding differential equations are

$$\begin{cases} L\dfrac{di}{dt} = 2v_i \\ C_o\dfrac{dv_o}{dt} = -\dfrac{v_o}{R_L} \\ i_i = 2i + i_e. \end{cases} \tag{3}$$

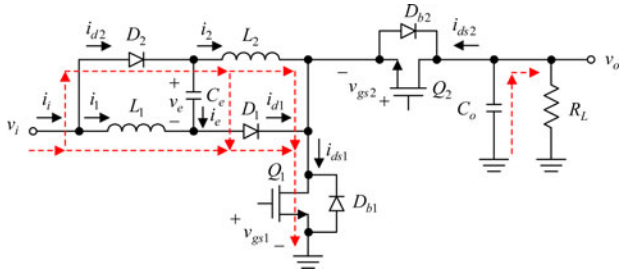

Fig. 3. Current flow in state 1 of case 1.

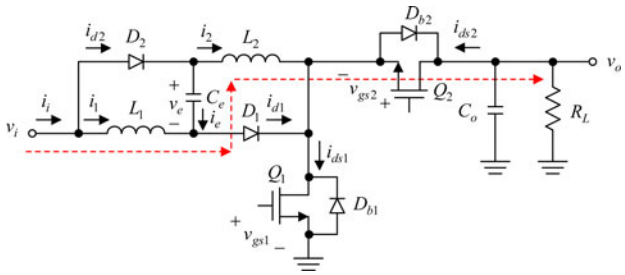

Fig. 4. Current flow in state 2 of case 1.

2) State 2 ($t_1 \sim t_0+T_s$): As depicted in Fig. 4, Q_1 is turned OFF, Q_2 is turned ON, and D_1 and D_2 are reverse biased. At this moment, v_i plus L_1 and L_2 releases energy to the load, thereby causing L_1 and L_2 to be demagnetized. Besides, C_e is discharged. Therefore, the corresponding differential equations are

$$\begin{cases} L\dfrac{d\,i}{dt} = 2v_i - v_o \\ C_o\dfrac{dv_o}{dt} = i - \dfrac{v_o}{R_L} \\ i_i = i. \end{cases} \tag{4}$$

Prior to obtaining the average equations from (3) and (4), there is a symbol $\langle y\rangle$ that is used to represent the average value of a variable y, where y indicates the voltage or current as follows:

$$\langle y\rangle = \frac{1}{T_s}\int_0^{T_s} y\,d\tau. \tag{5}$$

According to (3)–(5), the averaged equations can be obtained to be

$$\begin{cases} L\dfrac{d\langle i\rangle}{dt} = 2\langle v_i\rangle - (1-d)\langle v_o\rangle \\ C_o\dfrac{d\langle v_o\rangle}{dt} = (1-d)\langle i\rangle - \dfrac{\langle v_o\rangle}{R_L} \\ \langle i_i\rangle = (1+d)\langle i\rangle + d\langle i_e\rangle \end{cases} \tag{6}$$

where d is a variable denoting the duty cycle of the pulsewidth modulation (PWM) control signal for Q_1.

Based on the ampere–second balance, $\langle i_e\rangle$ can be expressed as a function of $\langle i\rangle$ to be

$$\langle i_e\rangle = \frac{1-d}{d}\langle i\rangle \tag{7}$$

and hence, by substituting (7) into (6), (6) can be rewritten as

$$\begin{cases} L\dfrac{d\langle i\rangle}{dt} = 2\langle v_i\rangle - (1-d)\langle v_o\rangle \\ C_o\dfrac{d\langle v_o\rangle}{dt} = (1-d)\langle i\rangle - \dfrac{\langle v_o\rangle}{R_L} \\ \langle i_i\rangle = 2\langle i\rangle. \end{cases} \tag{8}$$

Prior to obtaining the small-signal ac model from (8), the perturbation and linearization of (8) are indispensable. First of all, $\langle y\rangle$ is represented by the corresponding dc quiescent value Y plus the superimposed small ac variation $\hat{y}$, along with the assumption that ac variation is small in magnitude compared to the dc quiescent value. Let

$$\begin{cases} \langle v_i\rangle = V_i + \hat{v}_i \\ \langle v_o\rangle = V_o + \hat{v}_o \\ \langle i_i\rangle = I_i + \hat{i}_i \\ \langle i\rangle = I + \hat{i} \\ d = D + \hat{d} \end{cases} \quad \text{with} \quad \begin{cases} |\hat{v}_i| \ll V_i \\ |\hat{v}_o| \ll V_o \\ \left|\hat{i}_i\right| \ll I_i \\ \left|\hat{i}\right| \ll I \\ \left|\hat{d}\right| \ll D. \end{cases} \tag{9}$$

Next, by substituting (9) into (8), the following equations are obtained:

$$\begin{cases} L\dfrac{d(I+\hat{i})}{dt} = 2(V_i+\hat{v}_i) - (1-D+\hat{d})(V_o+\hat{v}_o) \\ C_o\dfrac{d(V_o+\hat{v}_o)}{dt} = (1-D-\hat{d})(I+\hat{i}) - \dfrac{(V_o+\hat{v}_o)}{R_L} \\ I_i + \hat{i}_i = 2(I+\hat{i}). \end{cases} \tag{10}$$

Consequently, the dc quiescent equations from (10) can be obtained to be

$$\begin{cases} 0 = 2V_i - (1-D)V_o \\ 0 = I(1-D) - \dfrac{V_o}{R_L} \\ I_i = 2I \end{cases} \tag{11}$$

and hence, the corresponding voltage conversion ratio of this converter from (11) can be obtained to be

$$\frac{V_o}{V_i} = \frac{2}{1-D}. \tag{12}$$

On the other hand, with the second-order ac terms neglected, the small-signal ac equations can be obtained to be

$$\begin{cases} L\dfrac{d\,\hat{i}}{dt} = (3+D)\hat{v}_i + (V_o+V_i)\hat{d} - (1-D)\hat{v}_o \\ C_o\dfrac{d\,\hat{v}_o}{dt} = (1-D)\hat{i} - \hat{d}I - \dfrac{\hat{v}_o}{R_L} \\ \hat{i}_i = 2\hat{i}. \end{cases} \tag{13}$$

And hence, the resulting small-signal ac model of the proposed high step-up converter with L_1 equal to L_2 is shown in Fig. 5 according to (13), where T_1 and T_2 are the ideal transformers with the turns ratios of 1:2 and $(1-D)$:1, respectively. Hence, by taking the Laplace transform of (13), the relationship

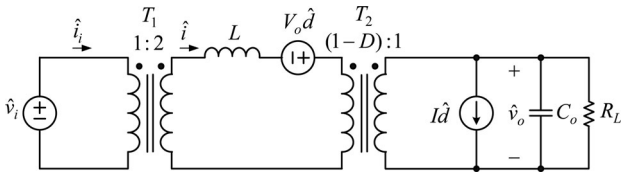

Fig. 5. Small-signal ac model for the proposed high step-up converter with L_1 equal to L_2.

between $\hat{v}_o(s)$, $\hat{v}_i(s)$, and $\hat{d}(s)$ can be expressed to be

$$\hat{v}_o(s) = G_{oi}(s)\hat{v}_i(s) + G_{od}(s)\hat{d}(s) \tag{14}$$

where

$$G_{oi}(s) = \left.\frac{\hat{v}_o(s)}{\hat{v}_i(s)}\right|_{\hat{d}(s)=0} = \frac{2/(1-D)}{1+s(L/R_L(1-D)^2)+s^2(LC_o/(1-D)^2)} \tag{15}$$

$$G_{od}(s) = \left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{v}_i(s)=0} = \frac{(V_o/1-D)\left[1-s(LI/V_o(1-D))\right]}{1+s(L/R_L(1-D)^2)+s^2(LC_o/(1-D)^2)} \tag{16}$$

where $G_{oi}(s)$ is the input-to-output transfer function and $G_{od}(s)$ is the control-to-output transfer function.

B. Case 2

This is an actual condition under the assumption that the value of L_1 is larger than that of L_2 and this converter operates at rated load. Fig. 6 shows the key waveforms pertaining to this case. In this case, as shown in Fig. 7, the duty cycle D multiplied by the switching period T_s is defined as the turn-ON time of the switch Q_1, $t_{\rm ON}$, and T_s minus $t_{\rm ON}$ is defined as the turn-OFF time of the switch Q_1, $t_{\rm OFF}$, corresponding to $(1-D)T_s$. If the value of L_1 is identical to the value of L_2, then i_{L1} is equal to i_{L2} for any time. However, if the value of L_1 is not identical to the value of L_2, say, the value of L_1 is larger than L_2 in this case, then as soon as the switch is turned OFF, i_{L1} is smaller than i_{L2}, and hence, the corresponding time interval AT_s gets started. At this instant, L_2 goes to demagnetization immediately due to the voltage across L_2 being V_i minus V_o. At the same time, the KCL at the point X shown in Fig. 1 must be obeyed, and hence, D_2 is forced to turn ON, thereby causing L_1 to be still magnetized. The moment i_{L1} is equal to i_{L2}, this time interval goes to the end. Hence, there are three operating states in this case, to be discussed as follows.

1) State 1 (t_0~t_1): As shown in Fig. 8, Q_1 is turned ON, Q_2 is turned OFF, and D_1 and D_2 are forward biased. Since the voltage across C_e is equal to v_i, L_1 and L_2 are to be magnetized. During this state, the output energy required is supplied from C_o, and C_e is charged. Besides, i_1 is smaller than i_2 due to L_1

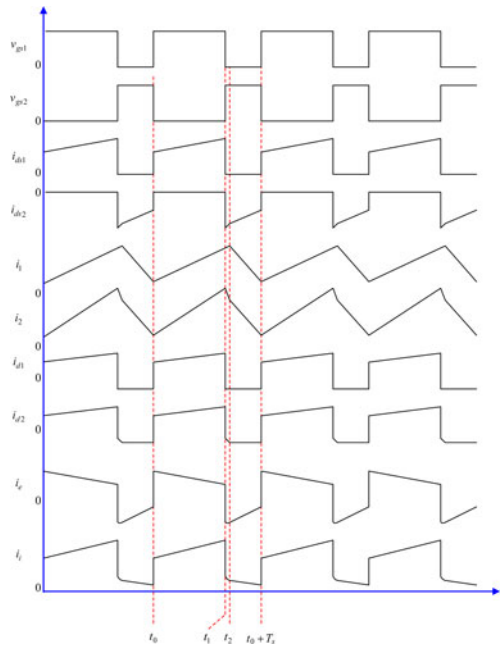

Fig. 6. Key waveforms pertaining to case 2.

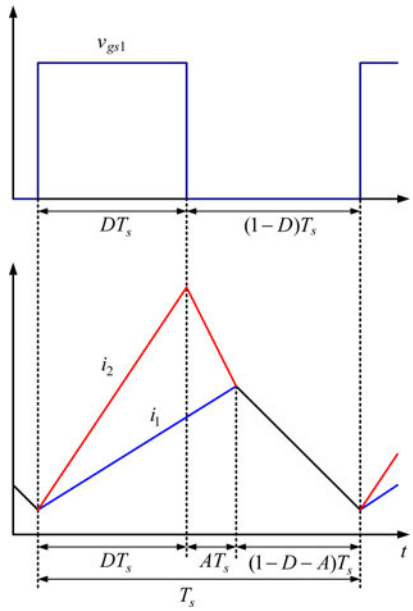

Fig. 7. Classification of operating states for case 2.

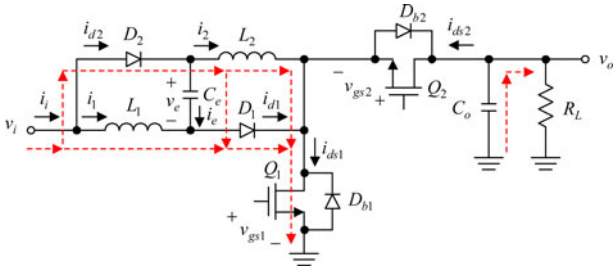

Fig. 8. Current flow in state 1 of case 2.

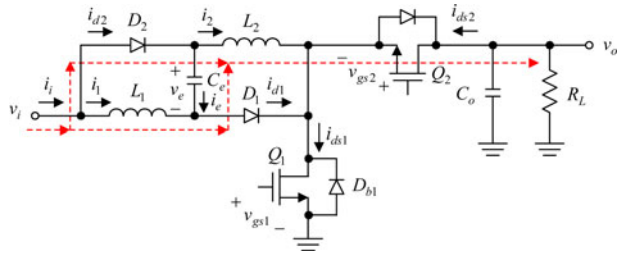

Fig. 9. Current flow in state 2 of case 2.

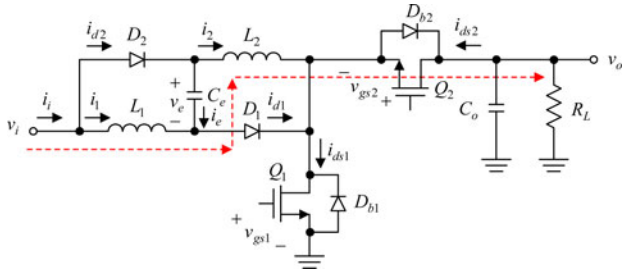

Fig. 10. Current flow in state 3 of case 2.

larger than L_2.

$$\begin{cases} L_1 \dfrac{di_1}{dt} = v_i \\ L_2 \dfrac{di_2}{dt} = v_i \\ C_o \dfrac{dv_o}{dt} = -\dfrac{v_o}{R_L} \\ i_i = i_1 + i_2 + i_e. \end{cases} \tag{17}$$

2) State 2 ($t_1 \sim t_2$): As shown in Fig. 9, Q_1 is turned OFF, Q_2 is turned ON, and D_1 is reverse biased. During this state, i_1 is smaller than i_2, thereby causing D_2 to be forward biased. Hence, L_1 to be still magnetized but L_2 to be demagnetized. Besides, C_e is discharged. As soon as i_1 is equal to i_2, the operation goes to state 3.

$$\begin{cases} L_1 \dfrac{di_1}{dt} = v_i \\ L_2 \dfrac{di_2}{dt} = v_i - v_o \\ C_o \dfrac{dv_o}{dt} = i_2 - \dfrac{v_o}{R_L} \\ i_i = i_2. \end{cases} \tag{18}$$

3) State 3 ($t_2 \sim t_0 + T_s$): As shown in Fig. 10, Q_1 is still turned OFF, Q_2 is still turned ON, D_1 is still reverse biased, and D_2 is reverse biased. At this moment, the input voltage, together with the energy stored in L_1 and L_2, pumps energy into the load, thereby causing L_1 and L_2 to be demagnetized. Besides, C_e is still discharged.

$$\begin{cases} L_1 \dfrac{di_1}{dt} = \dfrac{L_1}{L_1 + L_2}(2v_i - v_o) \\ L_2 \dfrac{di_2}{dt} = \dfrac{L_2}{L_1 + L_2}(2v_i - v_o) \\ C_o \dfrac{dv_o}{dt} = i_1 - \dfrac{v_o}{R_L} \\ i_i = i_1. \end{cases} \tag{19}$$

For analysis convenience, let

$$M_1 = \frac{L_1}{L_1 + L_2} \quad \text{and} \quad M_2 = \frac{L_2}{L_1 + L_2}. \tag{20}$$

Therefore, the equations can be expressed to be

$$\begin{cases} L_1 \dfrac{di_1}{dt} = M_1(2v_i - v_o) \\ L_2 \dfrac{di_2}{dt} = M_2(2v_i - v_o) \\ C_o \dfrac{dv_o}{dt} = i_1 - \dfrac{v_o}{R_L} \\ i_i = i_1. \end{cases} \tag{21}$$

According to (5) and (17)–(21), the averaged equations can be obtained to be

$$\begin{cases} L_1 \dfrac{d\langle i_1 \rangle}{dt} = d\langle v_i \rangle + a\langle v_i \rangle + M_1(1-d-a)(2\langle v_i \rangle - \langle v_o \rangle) \\ L_2 \dfrac{d\langle i_2 \rangle}{dt} = d\langle v_i \rangle + a(\langle v_i \rangle - \langle v_o \rangle) \\ \qquad\qquad + M_2(1-d-a)(2\langle v_i \rangle - \langle v_o \rangle) \\ C_o \dfrac{d\langle v_o \rangle}{dt} = d\left(-\dfrac{\langle v_o \rangle}{R_L}\right) + a\left(\langle i_2 \rangle - \dfrac{\langle v_o \rangle}{R_L}\right) \\ \qquad\qquad + (1-d-a)\left(\langle i_1 \rangle - \dfrac{\langle v_o \rangle}{R_L}\right) \\ \langle i_i \rangle = d(\langle i_1 \rangle + \langle i_2 \rangle + \langle i_e \rangle) + a\langle i_2 \rangle + (1-d-a)\langle i_1 \rangle \end{cases} \tag{22}$$

where a is a variable with the corresponding dc quiescent value of A.

Based on the ampere–second balance, $\langle i_e \rangle$ can be expressed as a function of $\langle i_1 \rangle$ and $\langle i_2 \rangle$ to be

$$\langle i_e \rangle = \frac{a\langle i_1 \rangle + (1-d-a)\langle i_2 \rangle}{d} \tag{23}$$

and hence, by substituting (23) into (22), (22) can be rewritten as

$$\begin{cases} L_1 \dfrac{d\langle i_1 \rangle}{dt} = (d + a + 2M_1 - 2M_1 d - 2M_1 a)\langle v_i \rangle \\ \qquad\qquad + (-M_1 + M_1 d + M_1 a)\langle v_o \rangle \\ L_2 \dfrac{d\langle i_2 \rangle}{dt} = (d + a + 2M_2 - 2M_2 d - 2M_2 a)\langle v_i \rangle \\ \qquad\qquad + (-M_2 + M_2 d + M_2 a - a)\langle v_o \rangle \\ C_o \dfrac{d\langle v_o \rangle}{dt} = -\dfrac{\langle v_o \rangle}{R} + (1-d-a)\langle i_1 \rangle + a\langle i_2 \rangle \\ \langle i_i \rangle = \langle i_1 \rangle + \langle i_2 \rangle. \end{cases} \tag{24}$$

After this, v_i, v_o, i_i, i_1, i_2, d, and a will be represented by the corresponding dc quiescent values plus small ac variations that are much smaller in magnitude than the corresponding dc

quiescent values:

$$\begin{cases} \langle v_i \rangle = V_i + \hat{v}_i \\ \langle v_o \rangle = V_o + \hat{v}_o \\ \langle i_i \rangle = I_i + \hat{i}_i \\ \langle i_1 \rangle = I_1 + \hat{i}_1 \\ \langle i_2 \rangle = I_2 + \hat{i}_2 \\ d = D + \hat{d} \\ a = A + \hat{a} \end{cases} \quad \text{with} \quad \begin{cases} |\hat{v}_i| \ll V_i \\ |\hat{v}_o| \ll V_o \\ \left|\hat{i}_i\right| \ll I_i \\ \left|\hat{i}_1\right| \ll I_1 \\ \left|\hat{i}_2\right| \ll I_2 \\ \left|\hat{d}\right| \ll D \\ |\hat{a}| \ll A. \end{cases} \tag{25}$$

Sequentially, by substituting (25) into (24), (24) can be rewritten to be

$$\begin{cases} L_1 \dfrac{d(I_1 + \hat{i}_1)}{dt} = [(D + \hat{d}) + (A + \hat{a}) + 2M_1 - 2M_1(D + \hat{d}) \\ \qquad -2M_1(A + \hat{a})](V_i + \hat{v}_i) + [-M_1 + M_1 \\ \qquad \times(D + \hat{d}) + M_1(A + \hat{a})](V_o + \hat{v}_o) \\ L_2 \dfrac{d(I_2 + \hat{i}_2)}{dt} = [(D + \hat{d}) + (A + \hat{a}) + 2M_2 - 2M_2(D + \hat{d}) \\ \qquad -2M_2(A + \hat{a})](V_i + \hat{v}_i) + [-M_2 + M_2 \\ \qquad \times(D + \hat{d}) + M_2(A + \hat{a}) - (A + \hat{a})](V_o + \hat{v}_o) \\ C_o \dfrac{d(V_o + \hat{v}_o)}{dt} = -\dfrac{(V_o + \hat{v}_o)}{R_L} + [1 - (D + \hat{d}) - (A + \hat{a})] \\ \qquad \times(I_1 + \hat{i}_1) + (A + \hat{a})(I_2 + \hat{i}_2) \\ (I_i + \hat{i}_i) = (I_1 + \hat{i}_1) + (I_2 + \hat{i}_2). \end{cases} \tag{26}$$

Based on (26), the small-signal ac equation can be obtained to be

$$\begin{cases} L_1 \dfrac{d\hat{i}_1}{dt} = (D + A + 2M_1 - 2M_1 D - 2M_1 A)\hat{v}_i + (-M_1 \\ \qquad + M_1 D + M_1 A)\hat{v}_o + (V_i - 2M_1 V_i + M_1 V_o)\hat{a} \\ \qquad + (V_i - 2M_1 V_i + M_1 V_o)\hat{d} \\ L_2 \dfrac{d\hat{i}_2}{dt} = (D + A + 2M_2 - 2M_2 D - 2M_2 A)\hat{v}_i + (-M_2 \\ \qquad + M_2 D + M_2 A - A)\hat{v}_o + (V_i - 2M_2 V_i + M_2 V_o \\ \qquad - V_o)\hat{a} + (V_i - 3M_2 V_i + M_2 V_o)\hat{d} \\ C_o \dfrac{d\hat{v}_o}{dt} = -\dfrac{\hat{v}_o}{R_L} + (1 - D - A)\hat{i}_1 + A\,\hat{i}_2 + (-I_1 + I_2) \\ \qquad \times\hat{a} - I_1 \hat{d} \\ \hat{i}_i = \hat{i}_1 + \hat{i}_2 \end{cases} \tag{27}$$

and hence, according to (27), the corresponding small-signal ac model can be obtained as in Fig. 11.

If the values of both L_1 and L_2 are identical, Fig. 11 can be retrieved to Fig. 5 under the corresponding condition that $M_1 = M_2 = 0.5$, $L = L_1 + L_2$, $A = \hat{a} = 0$, $I = I_1 = I_2$, and $\hat{i} = \hat{i}_1 = \hat{i}_2$.

C. Case 3

This is an actual condition under the assumption that the value of L_1 is smaller than that of L_2 and this converter operates at

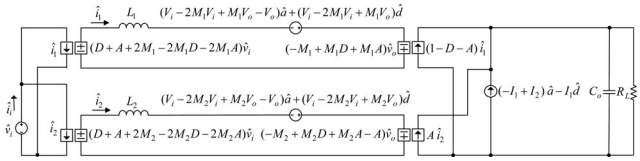

Fig. 11. Small-signal ac model for the proposed high step-up converter with L_1 larger than L_2.

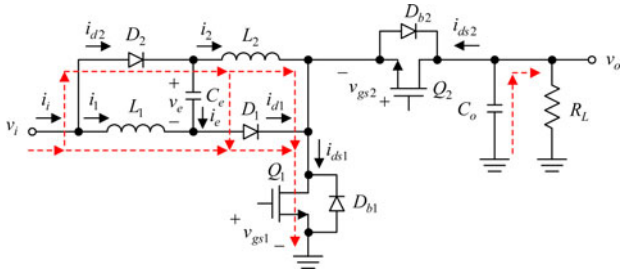

Fig. 12. Current flow in state 1 of case 3.

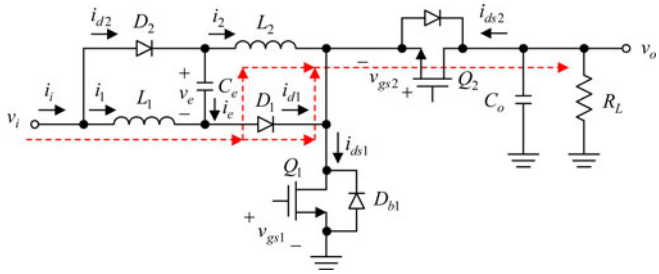

Fig. 13. Current flow in state 2 of case 3.

100% of the rated load. Since the behavior of the converter in this case is similar to that in case 2, only the corresponding basic operating principles are described herein.

1) State 1: As shown in Fig. 12, Q_1 is turned ON, Q_2 is turned OFF, and D_1 and D_2 are forward biased. Since the voltage across C_e is equal to v_i, L_1 and L_2 are to be magnetized. During this state, the output energy required is supplied from C_o and C_e is charged. Besides, i_1 is larger than i_2 due to L_1 smaller than L_2.

2) State 2: As shown in Fig. 13, Q_1 is turned OFF, Q_2 is turned ON, and D_2 is reverse biased. During this state, i_1 is larger than i_2, thereby causing D_1 to be forward biased, and hence, L_2 to be still magnetized but L_1 to be demagnetized. Besides, C_e is discharged. As soon as i_2 is equal to i_1, the operation goes to state 3.

3) State 3: As shown in Fig. 14, Q_1 is still turned OFF, Q_2 is still turned ON, D_2 is still reverse biased, and D_1 is reverse biased. At this moment, the input voltage, together with the energy stored in L_1 and L_2, pumps energy into the load, thus causing L_1 and L_2 to be demagnetized. Aside from this, C_e is still discharged.

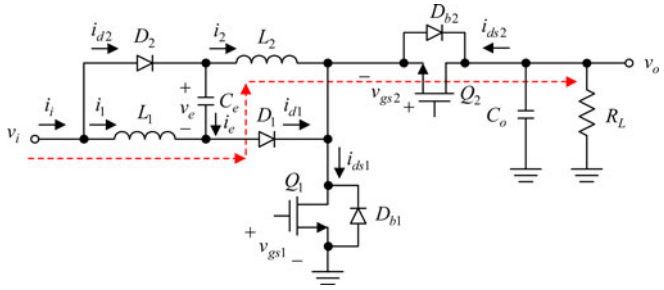

Fig. 14. Current flow in state 3 of case 3.

D. Voltages Conversion Ratios for Three Cases

In the following, the voltage conversion ratio corresponding to each case is obtained based on the voltage–second balance, to be described as follows.

1) Case 1 with $L_1 = L_2$: The voltage conversion ratio in this case can be obtained from the following equation:

$$V_i D + 0.5(2V_i - V_o)(1 - D) = 0, \quad \text{for } L_1 \text{ and } L_2. \tag{28}$$

Hence, the resulting voltage conversion ratio is 2/(1−D) that is identical to (12).

2) Case 2 with $L_1 > L_2$: The voltage conversion ratio in this case can be obtained from the following equations:

$$V_i D + V_i A + \frac{L_1(2V_i - V_o)}{L_1 + L_2}(1 - D - A) = 0, \quad \text{for } L_1 \tag{29}$$

$$V_i D + (V_i - V_o)A + \frac{L_2(2V_i - V_o)}{L_1 + L_2}(1 - D - A) = 0, \quad \text{for } L_2. \tag{30}$$

Hence, by adding (29) and (30) and doing some calculations, the corresponding voltage conversion ratio is 2/(1−D) that is also the same as (12).

3) Case 3 with $L_1 < L_2$: The voltage conversion ratio can be obtained from the following equations:

$$V_i D + (V_i - V_o)A + \frac{L_1(2V_i - V_o)}{L_1 + L_2}(1 - D - A) = 0, \quad \text{for } L_1 \tag{31}$$

$$V_i D + V_i A + \frac{L_2(2V_i - V_o)}{L_1 + L_2}(1 - D - A) = 0, \quad \text{for } L_2. \tag{32}$$

Hence, by adding (31) and (32) and doing some calculation, the accompanying voltage conversion ratio is 2/(1−D) that is still identical to (12).

IV. Control Method Applied

Fig. 15 shows the proposed overall system configuration for the proposed step-up converter. The one-comparator counter-based PWM control strategy without any A/D converter (ADC) based on the field-programmable gate array (FPGA) [27] is utilized, and the parameters of the PI controller are obtained at

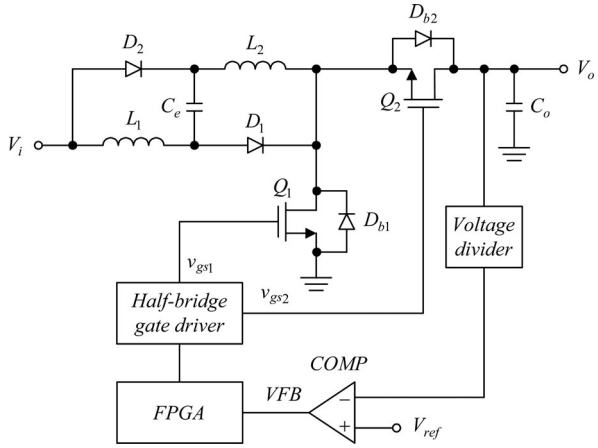

Fig. 15. Overall system configuration.

rated load. The output voltage information after the voltage divider is obtained via the comparator COMP, and then, sent to FPGA having a system clock of 100 MHz, so as to create the desired PWM control signals v_{gs1} and v_{gs2} to drive the MOSFET switches Q_1 and Q_2 after the gate drivers, respectively. Furthermore, one half-bridge gate driver can be used to drive Q_1 and Q_2.

V. Key Parameter Considerations

Before this section is discussed, there are some requirements given as follows: 1) the rated dc input voltage is from 10 to 16 V with 12 V rated; 2) the dc output voltage is 60 V; 3) the rated dc output current $I_{o\text{-rated}}$ is 1 A; 4) the switching frequency f_s is 195 kHz, i.e., the switching period T_s is 5.1 μs; 5) one 330 μF Rubycon capacitor is selected for C_o; 6) the product name of Q_1 and Q_2 is IRF3710ZS; 7) the product name of the half-bridge gate driver is HIP2101; 8) the product name of D_1 and D_2 is STPS15H100CB; and 9) the product name of FPGA is EP1C3T100.

The key parameter design contains design of two inductors L_1 and L_2 and one charge pump capacitor C_e, to be described as follows. Before this topic is discussed, there are some assumptions to be given: 1) the values of L_1 and L_2 are identical and are set to L with the current slew rate *di/dt* being 0.6 A/μs during the magnetization period; and 2) the converter operates in the rated condition with the voltage sag ΔV on C_e being 0.15% of the voltage across itself during the discharge period. Aside from this, the component stresses are also included herein.

A. Design of Two Inductors

The values of two inductors can be figured out according to the following equation:

$$L = \frac{V_i}{(di/dt)}. \tag{33}$$

Therefore, the value of L can be calculated to be 24 μH under the rated input voltage. As generally recognized, in practice, an inductor, made of the ferrite core with air gap, has a tolerance of about 20%, that is, if this inductor is made

TABLE I
COMPONENT STRESSES

	Q_1	Q_2	D_1	D_2	L_1	L_2	C_o	C_e
Voltage Stress (V)	a	a	b	b	c	c	a	d
Current Stress (A)	e	f	f	f	f	f	g	f

TABLE II
COMPONENT STRESS VALUES

	Q_1	Q_2	D_1	D_2	L_1	L_2	C_o	C_e
Voltage Stress (V)	60	60	30	30	18	18	60	12
Current Stress (A)	6.5	3.25	3.25	3.25	3.25	3.25	2.25	3.25

of the ferrite core with air gap, the corresponding inductance will be increased or reduced by a factor of about 20%. Hence, for observation convenience, the values of two inductors with 20% tolerance of the calculated value are set to 19.2 or 28.8 μH. Finally, four T106-18 toroidal cores, made by micrometals along with twisted copper conductor of $\phi 0.1 \times 140$, are used to obtain these four inductances: 20 μH with 17 turns, 20 μH with 17 turns, 24.1 μH with 19 turns, and 29.4 μH with 21 turns.

B. Design of Charge Pump Capacitor

The value of the charge pump capacitor can be worked out based on the following equation:

$$C_e = \frac{\Delta V}{\int_0^{(1-D)T_s} i_e \, dt}. \tag{34}$$

Therefore, the value of C_e can be calculated to be 270.3 μF. Finally, one 270 μF OSCON capacitor is chosen for C_e.

C. Component Stresses

In this section, the steady-state stresses on the components of the proposed converter except the body diodes of MOSFET switches are tabulated in Table I, on the assumption that the voltage across any MOSFET or diode during the turn-ON period is negligible and the voltage across C_e is V_i. In addition, the following component stresses are obtained under the condition that the value of L_1 is identical to the value of L_2 and the converter operates in the rated condition. Hence, Table II gives the stress value for each component in the proposed circuit.

In Table I, the symbols from 1) to 7) have the following meanings.

1) V_o.
2) $0.5V_o$.
3) $\text{Max}\{V_i, 0.5(V_o - 2V_i)\}$.
4) V_i.
5) $I_{o\text{-rated}} \frac{V_o}{V_i} + DV_i \frac{T_s}{L}$.
6) $0.5I_{o\text{-rated}} \frac{V_o}{V_i} + 0.5DV_i \frac{T_s}{L}$.
7) $0.5I_{o\text{-rated}} \frac{V_o}{V_i} + 0.5DV_i \frac{T_s}{L} - I_{o\text{-rated}}$.

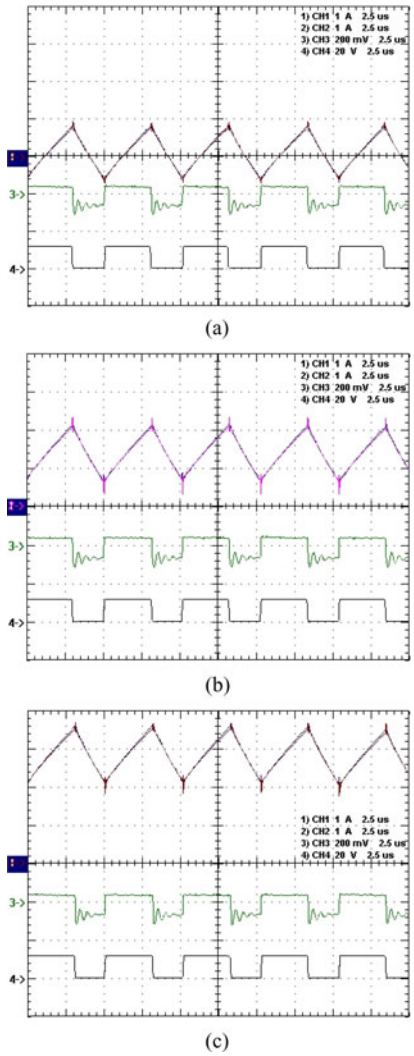

Fig. 16. Measured waveforms from top to bottom i_{L1}, i_{L2}, Δv_e, and v_{gs1} with L_1 equal to L_2 under rated input voltage at (a) no load, (b) half load, and (c) rated load.

VI. EXPERIMENTAL RESULTS

At rated load, Figs. 16–18 show the currents in L_1 and L_2, i_{L1} and i_{L2}, the ac portion of the voltage on C_e, Δv_e, and the gate driving signal of Q_1, v_{gs1}, for L_1 equal to L_2, L_1 smaller than L_2, and L_1 larger than L_2, respectively, with no load, half load, and rated load considered. In Fig. 16, i_{L1} almost overlaps with i_{L2}; in Fig. 17, i_{L1} is larger than i_{L2}; and in Fig. 18, i_{L1} is smaller than i_{L2}. Above all, Figs. 16(a)–18(a) show that this converter still operates in CCM at no load because of positive and negative currents flowing through two inductors, thereby causing the duty cycle to be changed slightly for any load, and hence, this converter to be easy to control. Besides, i_{L1} and i_{L2} are synchronized with each other, and the difference in average value between i_{L1} and i_{L2} is not too much even if the difference in value between L_1 and L_2 is up to 40%, implying that the proposed converter possesses robustness to some extent, that is, this converter has the capability of enduring component tolerance. As for the oscillation on C_e, it occurs due to L_1

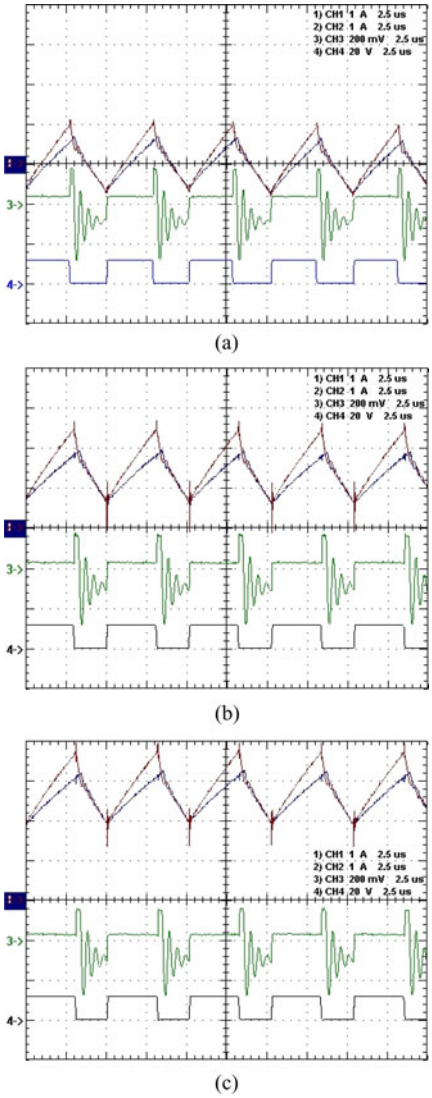

Fig. 17. Measured waveforms from top to bottom i_{L1}, i_{L2}, Δv_e, and v_{gs1} with L_1 smaller than L_2 under rated input voltage at (a) no load, (b) half load, and (c) rated load.

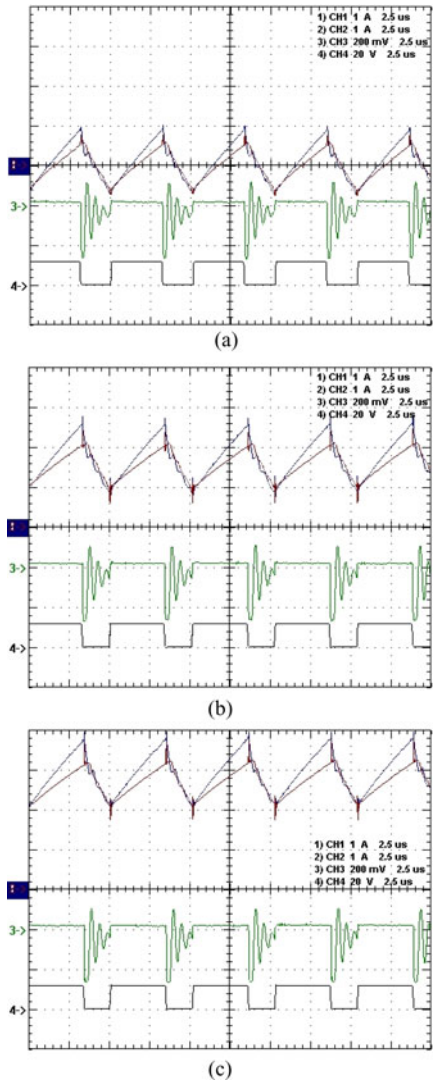

Fig. 18. Measured waveforms from top to bottom i_{L1}, i_{L2}, Δv_e, and v_{gs1} with L_1 larger than L_2 under rated input voltage at (a) no load, (b) half load, and (c) rated load.

and L_2 resonating with the junction capacitances of D_1 and D_2. On the other hand, Figs. 19 and 20 show load regulations under identical and different inductances at three different input voltages, respectively. It can be seen that the percentages of load regulations are all within 3% in Figs. 19 and 20. Aside from this, Figs. 21 and 22 display the curves of efficiency versus load current under identical and different inductances at three different input voltages, respectively. It can also be seen that for these two cases, the values of efficiencies in the rated condition are about 90%.

Figs. 23 and 24 show the load transient responses to further demonstrate the performance of the proposed converter. Since the controller parameter tuning method is widely used in the industry, there are three steps to online tune the parameters of the voltage controller, to be described as following:

1) Step 1: The proportional gain k_p is tuned from zero to the value that makes the output voltage very close to about 80% of the prescribed output voltage. And eventually, k_p is set at 1.0375.
2) Step 2: After this, the integral gain k_i is tuned from zero to the value that makes the output voltage very close to the prescribed output voltage but somewhat oscillate. Then, k_i will be reduced to some value without oscillation. And finally, k_i is chosen as 0.01.
3) Step 3: From this time onward, the differential gain k_d is tuned from zero to the value that accelerates the dynamic response but somewhat oscillate. Then, k_d will be reduced to some value without oscillation. And eventually, k_d is selected to be 2.

Figs. 23 and 24 show the load transient responses due to the load change from 50% to 100% of the rated load and from 100% to 50% of the rated load, respectively. Both the corresponding recovery times are about 10 ms, and both the resulting voltage droops are about 2 V.

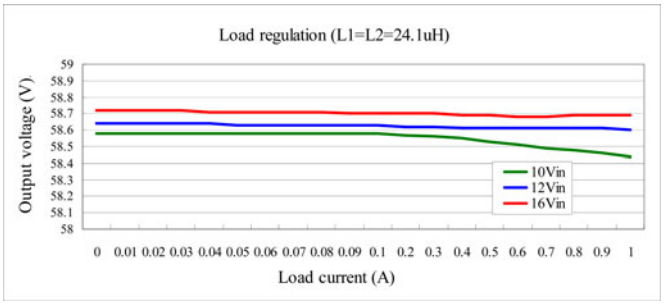

Fig. 19. Curves of load regulation with L_1 equal to L_2 under three different input voltages.

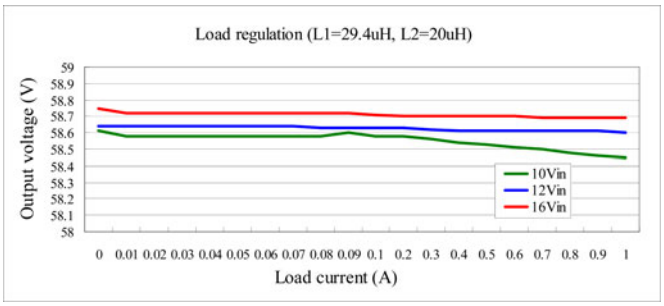

Fig. 20. Curves of load regulation with L_1 larger than L_2 under three different input voltages.

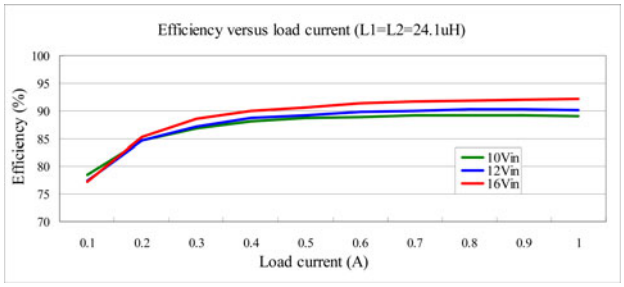

Fig. 21. Curves of efficiency versus load current with L_1 equal to L_2 under three different input voltages.

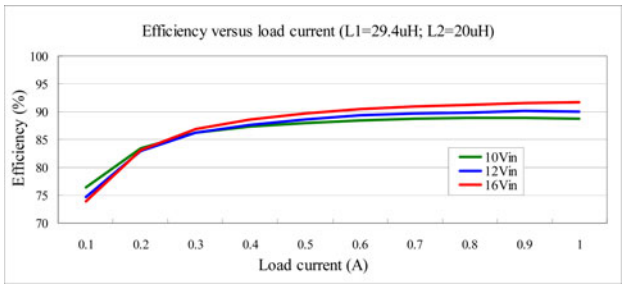

Fig. 22. Curves of efficiency versus load current with L_1 larger than L_2.

From the aforementioned, it can be seen that the proposed topology has good operating performances both in the steady state and in the transient.

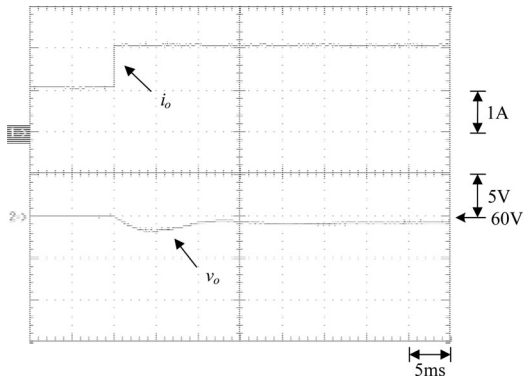

Fig. 23. Load transient response due to load change from 50% to 100% of the rated load.

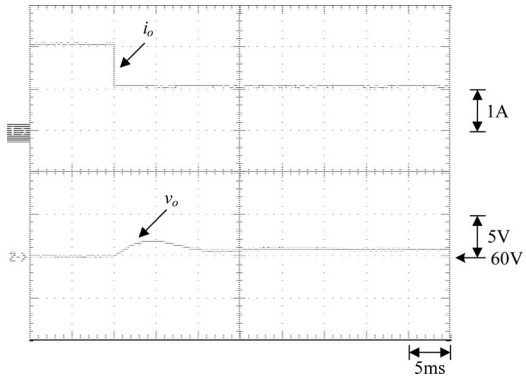

Fig. 24. Load transient response due to load change from 100% to 50% of the rated load.

VII. Conclusion

A novel high step-up converter is presented herein. There are some features in this converter, as summarized as follows:

1) The voltage boosting concept is based on the energy stored in the two inductors, together with the input voltage and the energy stored in the charge pump capacitor, which is released to the load during the demagnetization period.
2) Easy control of this converter can be achieved since this converter is always operated in CCM.
3) A good performance of load regulation can be obtained even though the difference in value between L_1 and L_2 is up to 40%.

However, there are three main drawbacks in the proposed converter, to be described as follows. First of all, at start-up, the surge current will occur. Second, the proposed converter is suitable for the low-current application, but not suitable for the high-current application. This is because a large charging current will flow through the charge pump capacitor in the high-current application, due to the voltage drop across this capacitor being too large. Third, the main switch has to endure the output voltage during the turn-OFF period. These drawbacks will be improved in the future study. Furthermore, the basic operating principles of the proposed converter working without synchronous rectification will also be taken into account in the future.

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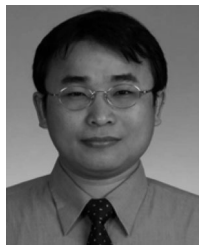

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