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A New Step-Up High Voltage Gain DC-DC Converter

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***Abstract*-A new high voltage gain dc-dc converter is proposed on this work as a viable solution to step-up a low battery voltage into a high voltage dc link. This converter is suitable for non-isolated on-line UPS systems with common neutral connection, that improves bypass circuit installation. Furthermore, smaller size, higher efficiency, and increased reliability are features that spread the transformerless products. The adopted control strategy uses a hybrid control that implements both analog and digital controllers, that implements the average current mode control. It presents characteristic of continuous input current through the batteries that improve its lifetime, the maximum voltage across the controlled switches is equal to one fourth of the total output voltage, and voltage equalization across the dc-link capacitors is intrinsic. In order to verify the feasibility of this topology, principle of operation, theoretical analysis, and experimental waveforms are shown for a 1.55 kW assembled prototype.**

I. INTRODUCTION

Uninterruptable power supply (UPS) systems are employed to supply critical loads with continuous and high quality energy in facilities such as hospitals, data centers, and communication systems etc [1].

Among the different on-line UPS topologies, the transformerless UPS presents higher efficiency due to the absence of the isolation transformer that increases considerably the size/weight of the overall system [2].

The overall advantages of modern transformerless UPS systems over those with isolation transformer (which are now considered obsolete) can be summed up and summarized as input-output power quality enhancement, lower operating and energy cost with high return on investment on the new technology UPS, and significantly enhanced reliability [3].

Accordingly to the output rated voltage of an UPS system, the dc link voltage level must be chosen adequately, in order allow the correct choice of the modulation scheme in the inverter stage, to obtain a sinusoidal output with an acceptable THD content. Thus, the dc-dc converter used in battery bank interface to the dc link must attempt this requirement.

With higher dc bus voltages levels (700Vdc – 800Vdc), commonly required to feed half-bridge voltage source inverters used in UPS systems, the classical boost converter couldn't be used. An alternative might be the utilization of boost converters in cascade, but this solution deals with low efficiency, due to the amount of power processing stages. To overcome this disadvantage some solutions using step-up converters suitable for operating with high voltage gain ratio were proposed in the literature [4-15].

The proposed converter, which is based on the three-state commutation cell [13-15], is shown in Fig. 1. As advantages, it can be emphasized that the input current is non-pulsating with low ripple that increases the lifetime of the battery; the input inductor operates within the double of the switching frequency allowing weight and volume reduction. It can be also observed that the voltage stress across the switches is a fraction of the output voltage and naturally clamped by one

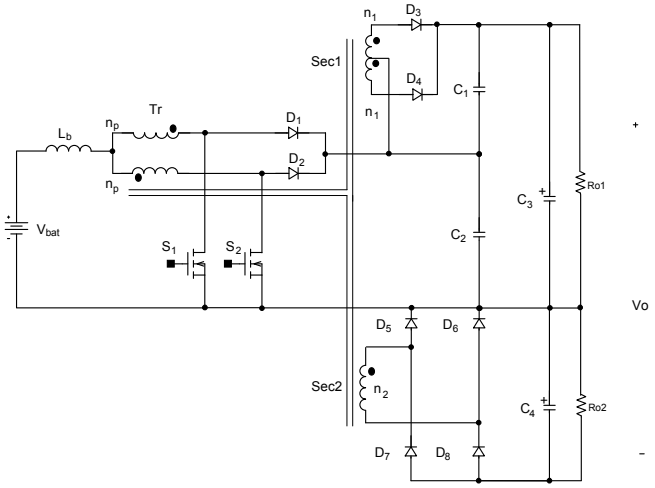


Fig. 1. Proposed topology.

output filter capacitor, so snubbers circuits are not necessary. Another benefit is the naturally voltage equalization in the desired value across the dc link output filter capacitors. As drawback of the converter, is the direct current path between the battery bank and the dc link capacitors, that draws a high inrush current during its connection, and it must be avoided using a NTC thermistor or other limiter.

II. PRINCIPLE OF OPERATION

The converter shown in Fig. 1 is composed by the following devices: voltage source V_{bat}, storage inductor L_b, a transformer T_r, controlled switches S_1 and S_2, rectifier diodes D_1, D_2, D_3, D_4, D_5, D_6, D_7 and D_8, output filter capacitors C_1, C_2, C_3 and C_4, and equivalent load resistors R_{o1}, and R_{o2}.

A. Principle of Operation

In order to explain the principle of operation of this converter, it is analyzed in the continuous conduction mode (CCM) operation, with a duty cycle value of the switches higher than 0.5. For this purpose, the semiconductors and magnetic elements are considered ideals.

During one commutation period of the converter operation, it presents four operating intervals that are described as follows, and its main theoretical operation waveforms are shown in Fig. 2.

First Interval (t_0, t_1): The switches S_1 and S_2 are turned on. The energy is stored only in the inductor L_b and is not transferred to the load. All the rectifier diodes are reverse biased in this interval. This interval circuit is represented in Fig. 3.a.

Second Interval (t_1, t_2): In this interval the switch S_2 remains turned on. The voltage across switch S_1 is equal to the voltage across capacitor C_2. The diodes D_1, D_3, D_5 and D_8 are directly biased. The energy stored in the inductor in the first interval, as well as the energy from the voltage source are transferred to the filter capacitors C_1, C_2, C_3, and C_4. The interval circuit is shown in Fig. 3.b.

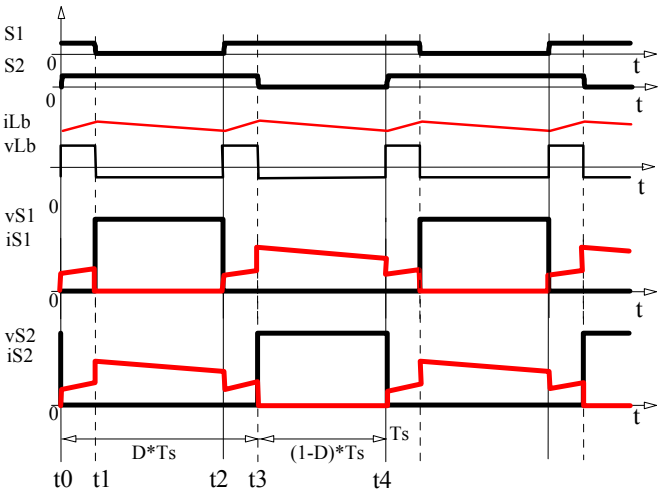
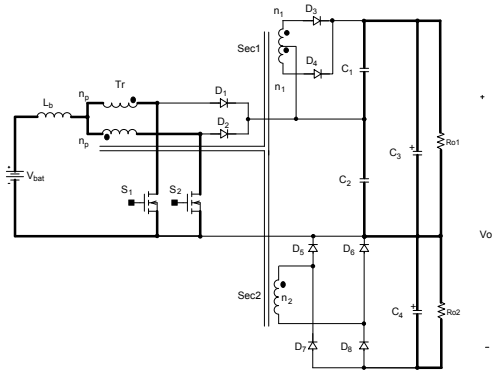


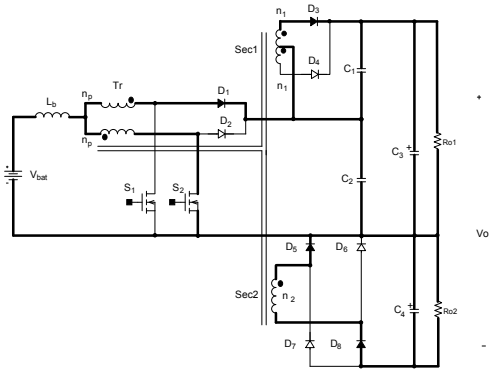
Fig. 2. Theoretical waveforms of the converter.

Third Interval (t_2, t_3): This interval is similar to the first one, where switches S_1 and S_2 are turned on, and the energy is only stored in the inductor L_b. The interval circuit is shown in Fig. 3.c.

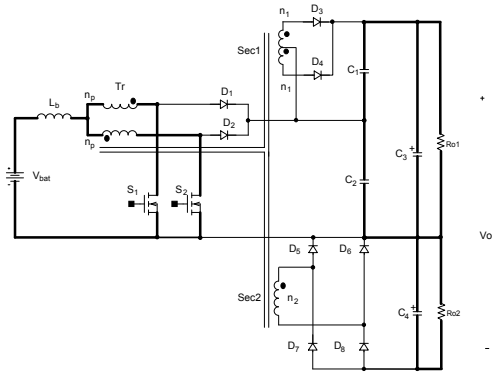
Fourth Interval (t_3, t_4): During this interval, the switch S_1 remains turned on. The voltage across switch S_2 is equal to the voltage across the capacitor C_2. The diodes D_2, D_4, D_6 and D_7 are directly biased. The energy stored in the inductor during the third interval, as well as the energy from the



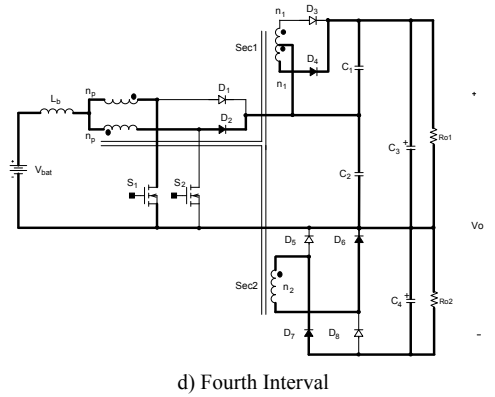
a) First Interval



b) Second Interval



c) Third Interval



d) Fourth Interval

Fig. 3. Theoretical waveforms of the converter.

voltage source are transferred to the filter capacitors C_1, C_2, C_3, and C_4. The interval circuit is shown in Fig. 3.d.

III. THEORETICAL ANALYSIS

A. Static Gain

The output-input voltage ratio, named as static gain of the converter, is given by (1). In order to get the equal voltage values across output capacitors C_3 and C_4, the transformer turns ratio must respect the relation $n_2=n_1+2n_p$.

$$G_V = \frac{V_o}{V_{bat}} = \frac{1}{(1-D)}\left(1+\frac{n_1}{2\cdot n_p}+\frac{n_2}{2\cdot n_p}\right) \quad (1)$$

where V_o is the output voltage, V_{bat} is the battery input voltage, n_p is the primary number of turns, n_1 is the secondary 1 number of turns, n_2 is the secondary 2 number of turns and D is the duty cycle.

B. Inductor Design

The current ripple on the storage inductor can be determined using

$$\Delta I_{Lb} = \frac{(2D-1)(1-D)V_o}{2f_s\left(1+\frac{n_1}{2\cdot n_p}+\frac{n_2}{2\cdot n_p}\right)L_b} \quad (2)$$

In (2), ΔI_{Lb} is the current ripple on the inductor L_b, and f_s is the switching frequency of the converter.

Rearranging the terms in (4), the normalized current ripple on the inductor is given by

$$\overline{\Delta I_{Lb}} = \frac{2\Delta I_{Lb}L_b f_s\left(1+\frac{n_1}{2\cdot n_p}+\frac{n_2}{2\cdot n_p}\right)}{V_o} = (2D-1)(1-D) \quad (3)$$

Fig. 4, which was obtained from (3), shows the normalized current ripple on the inductor as a function of the duty cycle.

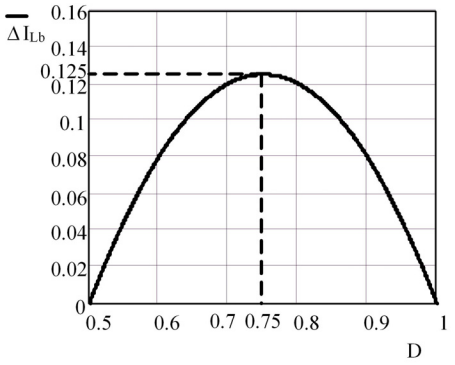


Fig. 4. Normalized ripple current on the inductor L_b.

It is possible to conclude that the maximum current ripple on the inductor occurs when the duty cycle is 0.75 and the normalized current ripple is 0.125. Given a certain value to the current ripple, it is possible to calculate the inductor value using

$$L_b = \frac{V_o}{16 f_s\left(1+\frac{n_1}{2\cdot n_p}+\frac{n_2}{2\cdot n_p}\right)\Delta I_{Lb}} \quad (4)$$

C. Transformer Design

The high frequency transformer must be designed accordingly to the amount of power processed given by

$$P_p = \frac{V_{C1}+0.5\cdot V_{C2}+V_{C4}}{V_{C1}+V_{C2}+V_{C4}}P_o \quad (5)$$

where P_p is the power processed by the transformer, V_{C1}, V_{C2} and V_{C4} are the voltages across the capacitors C_1, C_2 and C_4, respectively, and, P_o is the output power of the converter.

D. Output Capacitors Design

Considering the voltage ripple small, the average voltage across the capacitors C_1, C_2, C_3 and C_4 are described by (6), (7), (8) and (9).

$$V_{C_1} = \frac{V_{bat}}{(1-D)}\cdot\frac{n_1}{2\cdot n_p} \quad (6)$$

$$V_{C_2} = \frac{V_{bat}}{(1-D)} \quad (7)$$

$$V_{C_3} = V_{C_1}+V_{C_2} \quad (8)$$

$$V_{C_4} = \frac{V_{bat}}{(1-D)}\cdot\frac{n_2}{2\cdot n_p} \quad (9)$$

The capacitance of capacitors C_3 and C_4 can be calculated using (10), then

$$C_3 = C_4 \geq \frac{(1-D)P_o}{f_s\Delta V_o V_{bat}\left(1+\frac{n_1}{2\cdot n_p}+\frac{n_2}{2\cdot n_p}\right)} \quad (10)$$

In (10), ΔV_o is the total output voltage ripple. The capacitors C_1 and C_2 are small polypropylene capacitors, used basically to minimize voltage spikes across the switches and diodes.

E. Maximum Voltage across the Switches S_1 and S_2

The maximum voltage across switches S_1 and S_2, without considering the overshoots due to the layout parasitics inductances, is given by

$$V_{S_1} = V_{S_2} = \frac{V_{bat}}{(1-D)} \quad (11)$$

F. Maximum Reverse Voltage across the Diodes

The maximum reverse voltage across the diodes D_1, D_2, D_3, D_4, D_5, D_6, D_7 and D_8 are given by (12), (13) and (14), respectively. Thus,

$$V_{D_1} = V_{D_2} = \frac{V_{bat}}{(1-D)} \tag{12}$$

$$V_{D_3} = V_{D_4} = \frac{V_{bat}}{(1-D)} \cdot \frac{n_1}{n_p} \tag{13}$$

$$V_{D_5} = V_{D_6} = V_{D_7} = V_{D_8} = \frac{V_{bat}}{(1-D)} \cdot \frac{n_2}{2 \cdot n_p}. \tag{14}$$

IV. Experimental Results

A. Specifications

In order to verify the operation and evaluate the performance of the proposed boost converter, a prototype with the specifications shown in Table I was assembled and tested.

TABLE I
Specifications of the Non-Isolated DC-DC Converter using TSSC

Input Voltage Range	V_{bat}	63 - 81 [V_{DC}]
Output Power	P_o	1.55 [kW]
Output Voltage	V_o	710 [V]
Switching Frequency	f_s	40 [kHz]

The assumed parameters are: the maximum boost inductor current ripple $\Delta I_{Lb} = 0.30 I_{bat\max}$, the voltage across capacitor C_2 $V_{C_2} = 200V$, the maximum fixed duty cycle of the switches $D_{max} = 0.689$ for the minimum input voltage, and the output voltage ripple $\Delta Vo=0.02V_o$.

B. Simplified Design Example

The boost inductor is obtained according to (4), substituting values in it is equal to

$$L_b = \frac{700}{16 \cdot 40000 \cdot \left(1 + \frac{18}{2 \cdot 12} + \frac{42}{2 \cdot 12}\right) \cdot 8.46} = 31.2\mu H .$$

The transformer was built using the push-pull DC-DC converter guidelines for the power rating obtained by (5). Thus,

$$P_p = \frac{(152.5 + 0.5 \cdot 202.5 + 355)}{(152.5 + 202.5 + 355)} \cdot 1550 = 1328.9W .$$

The capacitances of the output filter capacitors were calculated using the expression (10). Substituting values,

$$C_2 = C_3 \geq \frac{(1-0.689) \cdot 1550}{40000 \cdot 0.02 \cdot 700 \cdot 63 \cdot \left(1 + \frac{18}{2 \cdot 12} + \frac{42}{2 \cdot 12}\right)} = 3.9\mu F$$

The voltage across such capacitors must be higher than the values calculated using (8) and (9). Thus,

$$V_{C_2} = \frac{63}{(1-0.689)} \cdot \frac{18}{2 \cdot 12} + \frac{63}{(1-0.689)} = 354.5V ,$$

$$V_{C_4} = \frac{63}{(1-0.689)} \cdot \frac{42}{2 \cdot 12} = 354.5V .$$

The breakdown of the controlled switches must be higher than the value obtained using (11). Thus,

$$VS_1 = VS_2 = \frac{63}{(1-0.689)} = 202.5V .$$

The maximum reverse voltage of the rectifier diodes must be higher than the values calculated from (12), (13) and (14). Thus,

$$V_{D_1} = V_{D_2} = \frac{63}{(1-0.689)} = 202.5V ,$$

$$V_{D_3} = V_{D_4} = \frac{63}{(1-0.689)} \cdot \frac{18}{12} = 303.8V ,$$

$$V_{D_5} = V_{D_6} = V_{D_7} = V_{D_8} = \frac{63}{(1-0.689)} \cdot \frac{42}{2 \cdot 12} = 354.5V .$$

The main components used to assemble the experimental prototype are listed in Table II.

TABLE II
Prototype Main Components

Diodes D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8	30ETH06 (IRF)
Inductor L_b	L_b =36 μH
Output Filter Capacitors C_3, C_4	470 μF / 450 V (EPCOS), (Electrolytic Snap-In)
Capacitor C_1	1.8 μF / 630 V (EPCOS), (Polypropylene Film)
Capacitor C_2	470 nF / 630 V (EPCOS), (Polypropylene Film)
Switches S_1, S_2	FQA38N30 (Fairchild)
High Frequency Transformer	NEE-55/21 (Thornton Ipec) N_p=12 turns (28x26AWG) N_{s1}=18 turns (3x26AWG) N_{s2}=42 turns (3x26AWG)

The implemented capacitance values of the output filter are different from the calculated values, due to non-linear load characteristic used in the inverter stage connected to the dc-bus link.

C. Experimental Waveforms and Curves

Figures 5 and 6 shows the battery bank voltage V_{bat} and current through the boost inductor L_b under nominal load and minimum input voltage conditions.

As can be seen, the current drawn by the proposed converter presents a low current ripple, suitable for battery powered applications.

Figure 7 shows the drain-to-source voltages across the controlled switches S_1 and S_2. As can be seen, it is clamped in almost the output filter capacitor C_2 voltage, as expected in the theoretical analysis.

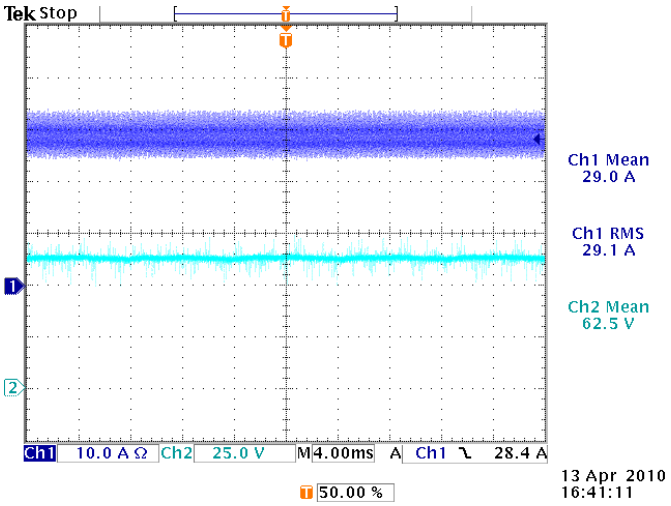


Fig. 5. Battery voltage and current through the inductor L_b. (25V/div.; 10A/div.; 4ms/div.)

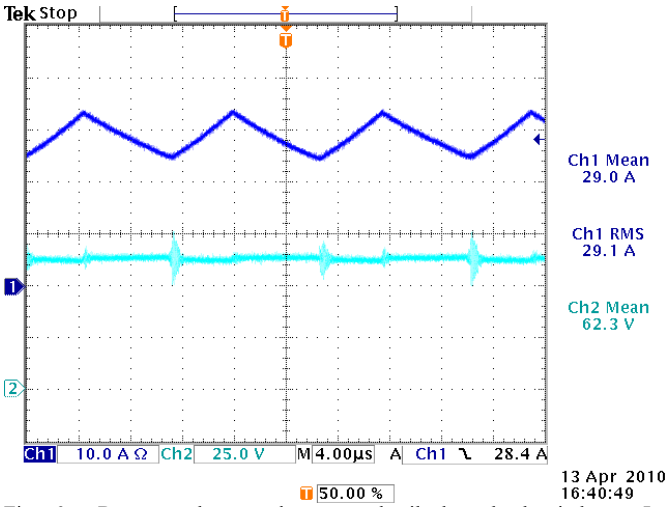


Fig. 6. Battery voltage and current detail through the inductor L_b. (25V/div.; 10A/div.; 4µs/div.)

Figure 8 shows the voltage behavior across the dc-link filter capacitors C_3 and C_4. It can be seen that both voltages are almost balanced and regulated around $355V_{dc}$ even if the load characteristic is unbalanced.

Figure 9 presents the efficiency curve of the converter as a function of the output power.

It can be seen that for this application, the achieved efficiency is high enough. It is important to emphasize that all presented experimental results were made for the lower input voltage level.

Figure 10 shows the picture of the assembled prototype. It can be seen the magnetics components, the controlled switches and the dc-link capacitors. This converter is part of a complete power board of an UPS system with output power of 2kVA and output voltage of 220Vac.

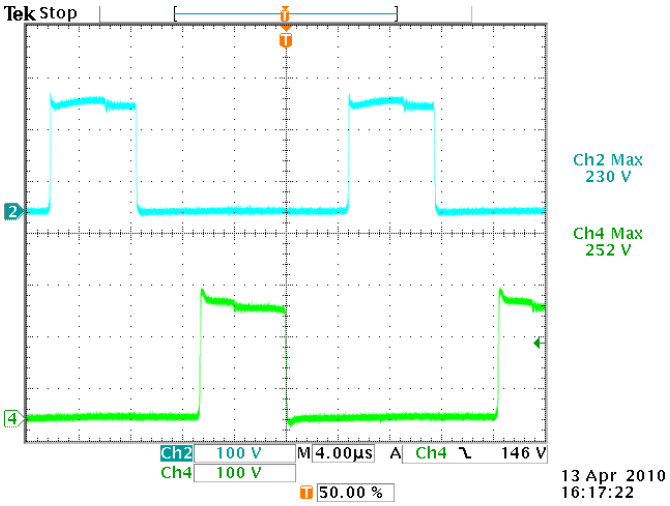


Fig. 7. Measured drain-to-source voltages V_{S1} and V_{S2}. (100V/div.; 100V/div.; 4µs/div.)

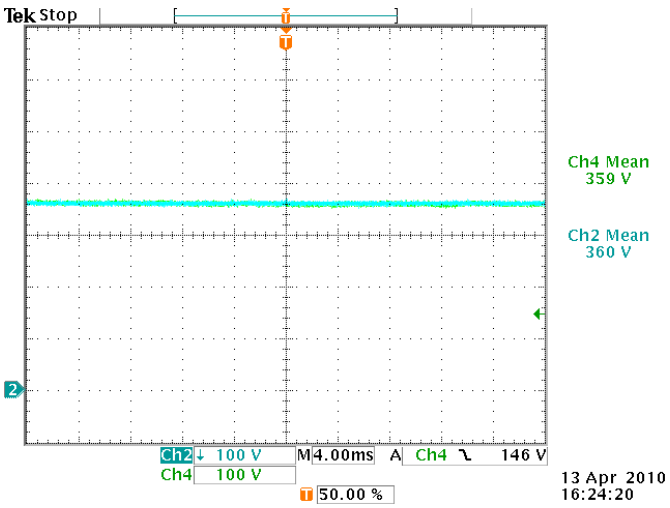


Fig. 8. DC link filter capacitors voltage V_{C1} and V_{C2}. (100V/div.; 100V/div.; 4ms/div.)

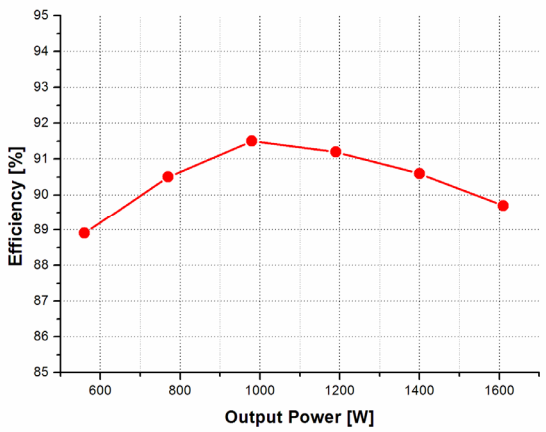


Fig. 9. Measured efficiency of the converter as function of the output power.

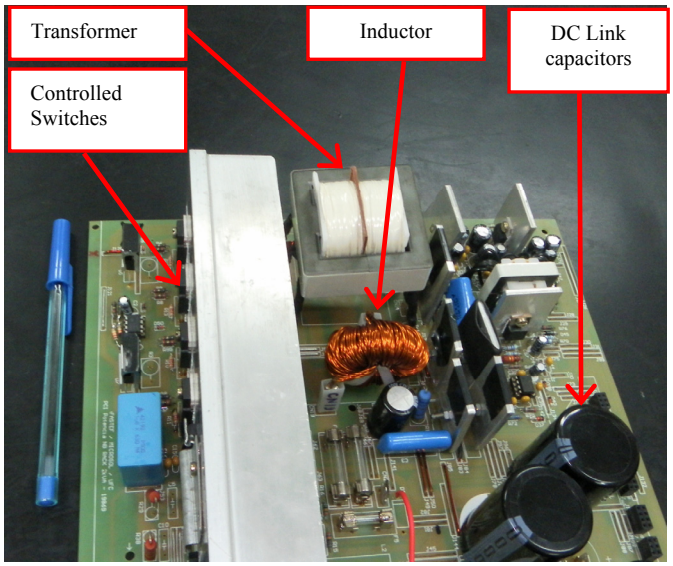


Fig. 10. Picture of the assembled prototype.

V. CONCLUSIONS

This paper proposes a new non-isolated boost converter with a high voltage gain for non-isolated on-line UPS with common neutral point. Also, the proposed converter can be used for the development of stand-alone systems, and grid-connected systems for renewable energies applications.

As shown in the experimental results shown in Figs. 5 to 9, it has the following features: a non-pulsated input current that improves the battery lifetime, the voltage across the controlled switches is one fourth of the total output voltage and the voltage across the dc-link filter capacitors are naturally balanced even if unbalanced loads is connected.

The efficiency curve shown in Fig. 9 confirms such proposal viability for its desired application or others.

ACKNOWLEDGMENT

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