

ESSCIRC ESSDERC 2015

41st European Solid-State Circuits Conference
45th European Solid-State Device Research Conference

WORKSHOP

Advanced DC-DC Converter Techniques

Workshop Chair:
Christoph Sandner
Infineon, Austria

Workshop Venue:
Graz University of Technology
Inffeldgasse 12
September 18, 2015

Conference Organization:
JOANNEUM RESEARCH Forschungsgesellschaft mbH
Graz, Austria

Technical Co-Sponsorship



Advanced DC-DC Converter Techniques

Organizer: Christoph Sandner, Infineon, Austria

This workshop will give insights into different key aspects of DC-DC converter concept and design. The designated speakers are worldwide recognized experts in this field. We target one speech in each of these fields: Inductor based converters, switched capacitor converter concepts and control techniques, buck converter control and stability, and last not least a talk about how to avoid most common mistakes in DC-DC converter circuit design.

Agenda:

08:30	Switched Capacitor DC-DC Converters: Concepts and Control Techniques Hans Meyvaert (KU Leuven, Belgium)	Page 3
09:30	Ripple-Based Control Techniques for Buck Type DC-DC Converter Jesus A. Oliver (UPM Madrid, Spain)	Page 49
10:30	<i>End of Workshop</i>	
11:00	Digital Control for Inductor Based DC-DC Converters Luca Corradini (University of Padova, Italy)	Page 99
12:00	How to avoid most common mistakes in DCDC design: Voltage mode, PWM and fixed frequency Vadim Ivanov (TI, USA)	Page 145

SWITCHED-CAPACITOR DC-DC

Concepts and control techniques

**Hans Meyvaert
Prof. Michiel Steyaert
KU Leuven, Belgium**

Conference Sponsors:



Hans Meyvaert

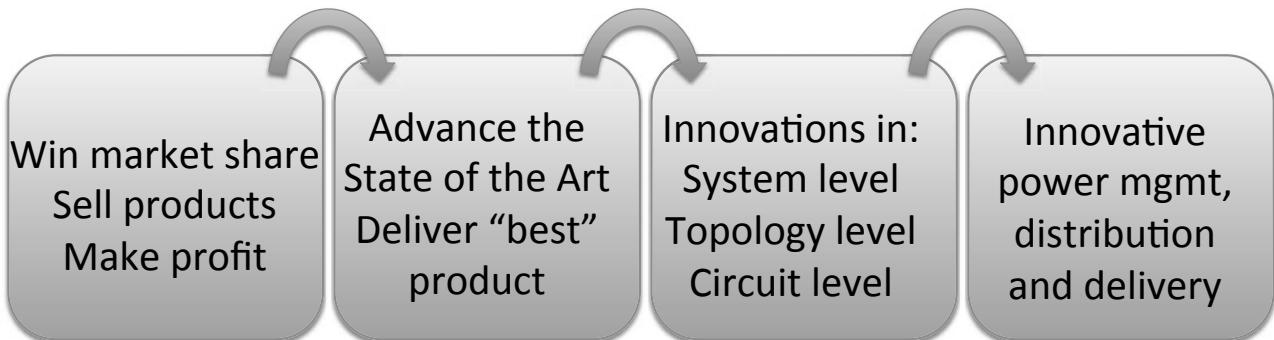
OUTLINE

1. Introduction
2. SC DC-DC: Modeling & Control parameters
3. Control techniques: From theory to practice
4. Comparison of Pro's and Con's of each technique:
For each scenario, a matching control
5. Summary

INTRODUCTION

■ Innovation in power management?

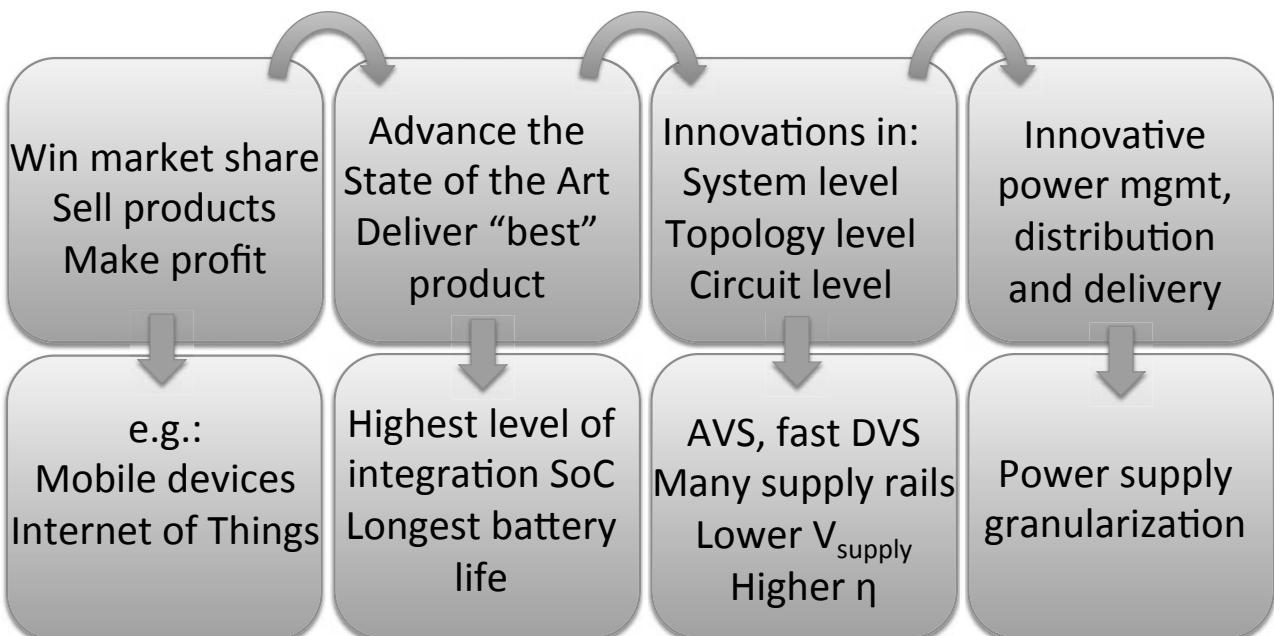
- A business strategy perspective:



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INTRODUCTION



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POWER SUPPLY GRANULARIZATION

■ Enabled by trend: “From discrete towards fully integrated CMOS” [ref. M. Steyaert ESSCIRC’11]

- Once integrated, centralized power mgmt is obsolete

■ Solution to challenges created by SoC approach

- Lower pin count
- Less stringent Power Delivery Network (PDN) requirement
- Possibility to have a multitude of independent V_{supply} rails
- Load optimized power conversion, e.g. POL
- Fast Dynamic Voltage Scaling (DVS) per V_{supply} domain

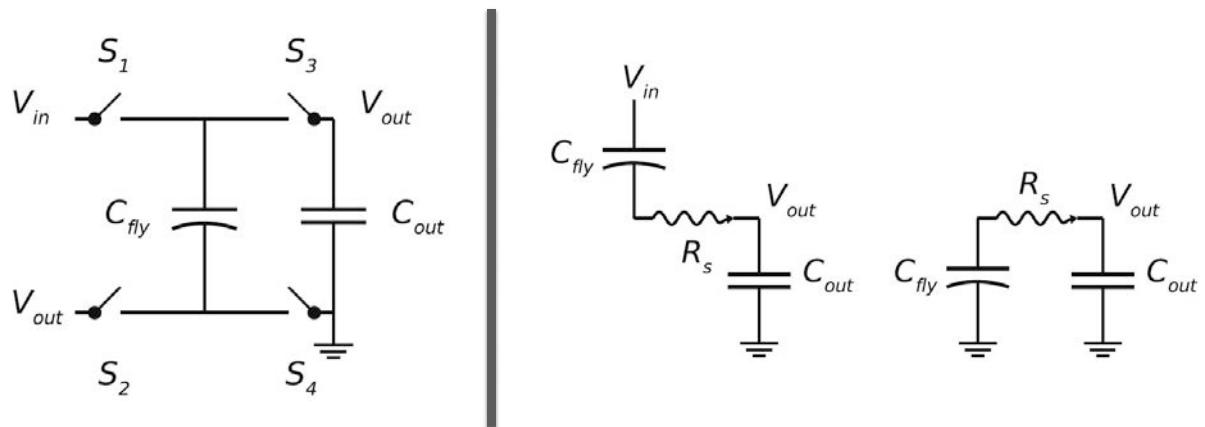
POWER SUPPLY GRANULARIZATION...

■ But... (there is no such thing as a free lunch)

- No longer a large shared C_{decouple} buffer capacitor
 - But **noise** spec in each V_{supply} domain constant, or more strict
- Dynamic Range of the expected load current higher
 - Challenging **transient response** for controller, even though absolute loading current is decreased
- Fast DVS requires equally fast controller
 - **Regulation at high speed**

... REQUIRES CUTTING EDGE CONTROL

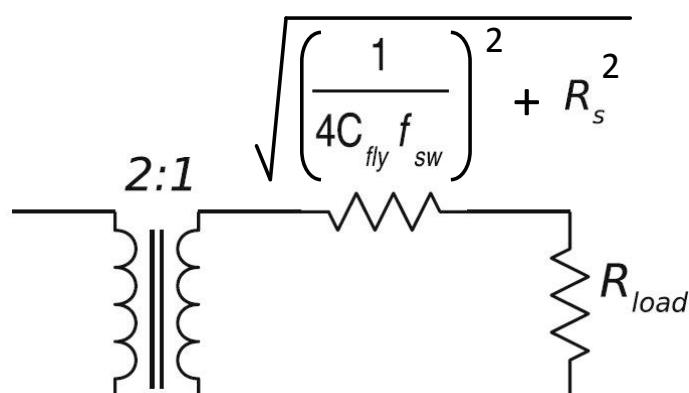
SWITCHED-CAPACITOR DC-DC



VARIABLE STRUCTURE SYSTEM

2 capacitor configurations, activated by non-overlapping CLK

SWITCHED-CAPACITOR DC-DC



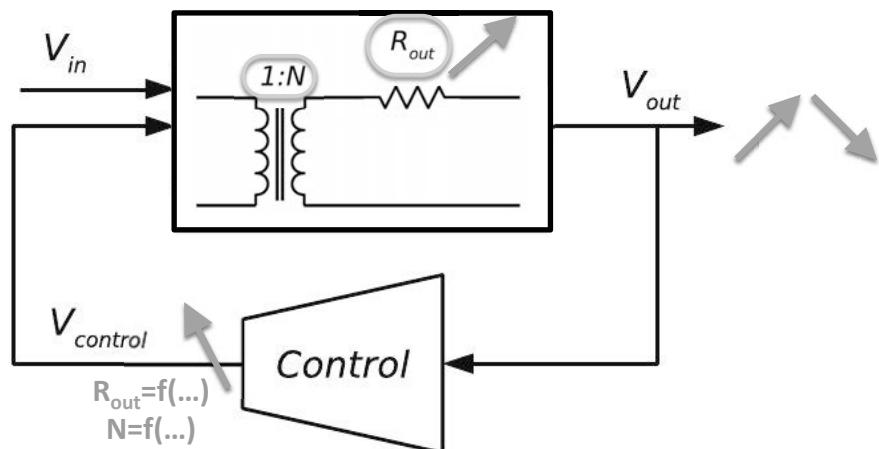
VARIABLE STRUCTURE SYSTEM

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MODELING AND CONTROL PARAMETERS



COARSE SYSTEM PARTITIONING

Conversion and control feedback

MODELING AND CONTROL PARAMETERS

II Charge balance analysis

- Discrete time charge conservation equations
- Transfer function by means of Z-transform
- Exhaustive method for complex topologies

II Averaged State-Space analysis

- State-space equations
- Averaging over the switching period
- Steady-state, small signal modeling

MODELING AND CONTROL PARAMETERS

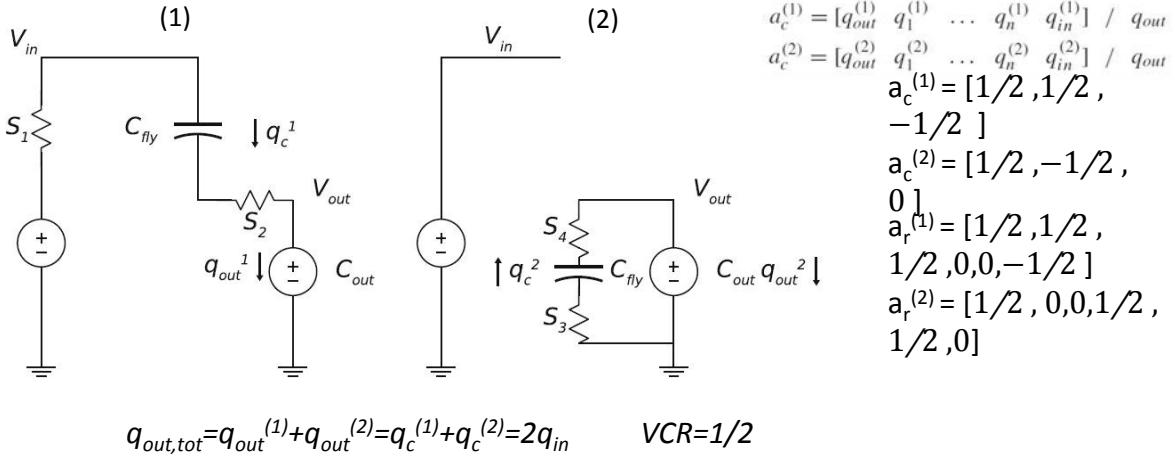
II Charge flow analysis

- Analyze the role of each component
- Extraction of Charge flow vectors \vec{a}_c^i and \vec{a}_r^i [ref. Seeman TPEL'08]

II Branch Analysis

- 2 asymptotic approximations of R_{out} [ref. Seeman TPEL'08]
 - switched-capacitor & resistive

MODELING AND CONTROL PARAMETERS



CHARGE FLOW ANALYSIS

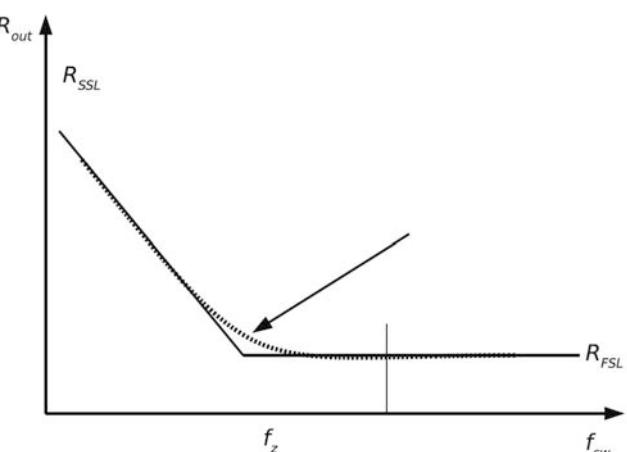
Extraction of the charge flow vectors and voltage conversion ratio (VCR)

MODELING AND CONTROL PARAMETERS

$$R_{SSL} = \sum_{i=1}^n \frac{a_{c,i}^2}{f_{sw} C_i}$$

$$R_{FSL} = 2 \sum_i R_i a_{r,i}^2$$

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2}$$



BRANCH ANALYSIS

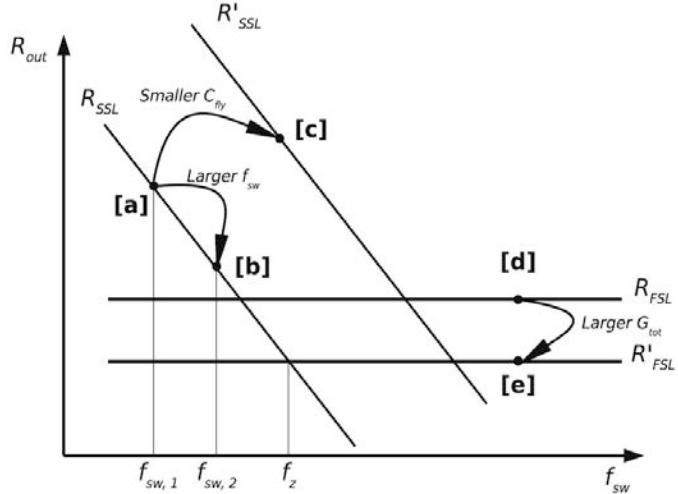
Slow Switching Limit (SSL) and Fast Switching Limit (FSL) approximation
[ref. Seeman TPEL'08]

MODELING AND CONTROL PARAMETERS

$$R_{SSL} = \sum_{i=1}^n \frac{a_{c,i}^2}{f_{sw} C_i}$$

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BRANCH ANALYSIS

Slow Switching Limit (SSL) and Fast Switching Limit (FSL) approximation
[ref. Seeman TPEL'08]

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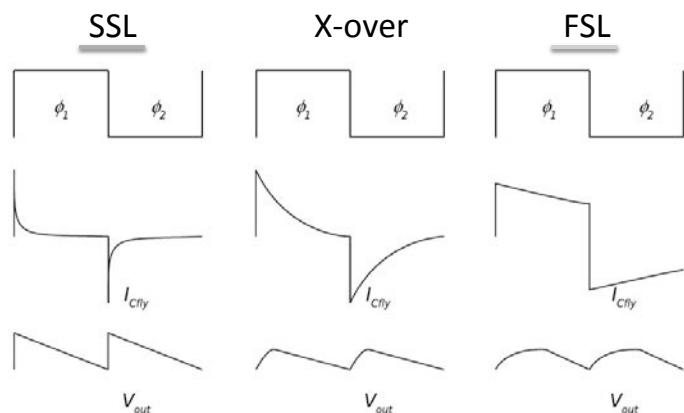
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MODELING AND CONTROL PARAMETERS

$$\underline{R_{SSL}} = \sum_{i=1}^n \frac{a_{c,i}^2}{f_{sw} C_i}$$

$$\underline{R_{FSL}} = 2 \sum_i R_i a_{r,i}^2$$

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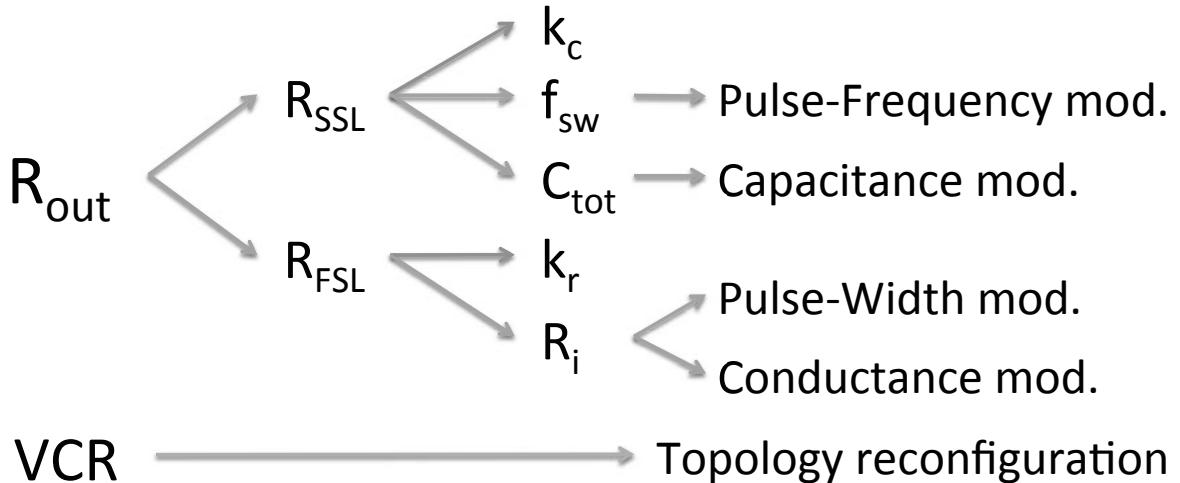
BRANCH ANALYSIS

Slow Switching Limit (SSL) and Fast Switching Limit (FSL) approximation
[ref. Seeman TPEL'08]

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MODELING AND CONTROL PARAMETERS



CONTROL PARAMETER OVERVIEW

$$V_{out} = N V_{in} - I_{load} R_{out}(f_{sw}, C_{tot}, R_i)$$

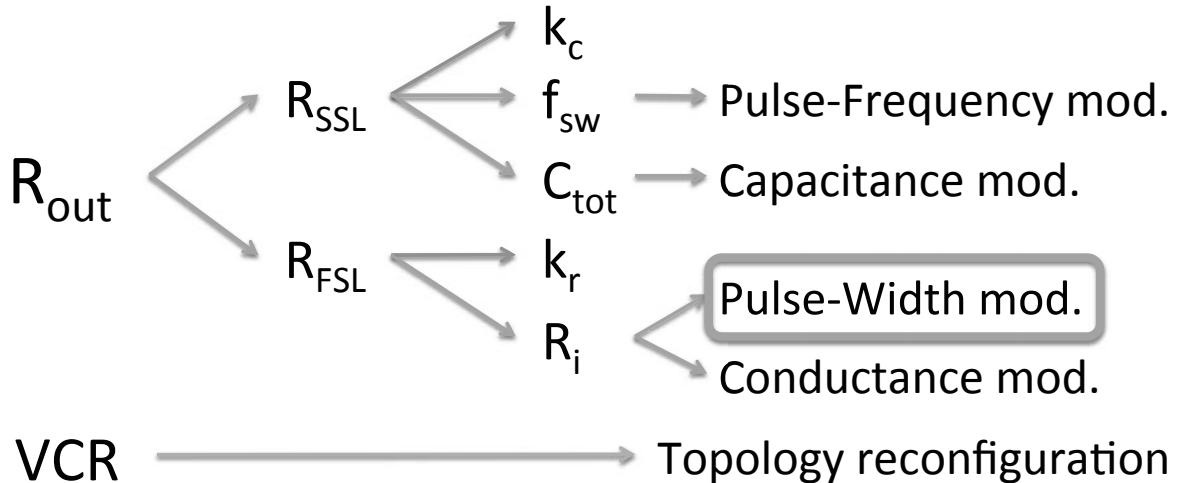
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OUTLINE

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MODELING AND CONTROL PARAMETERS



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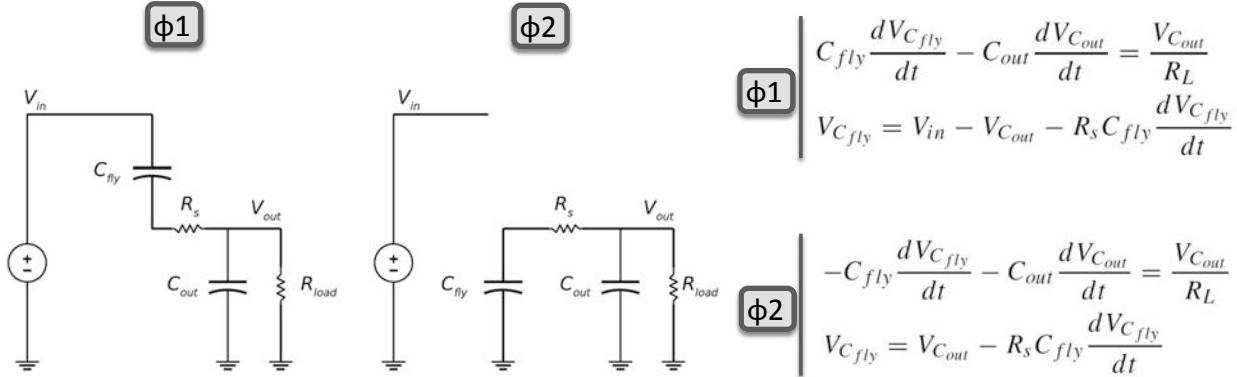
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PULSE-WIDTH MODULATION

- Modify conduction by changing the pulse-width
 - Effect on R_{FSL} and total charge transferred
- Frequency domain analysis in FSL
 - Time-Averaging Approach [Middlebrook & Cuk, PESC'76]
 - Differential equations of each state
 - Averaging the state equations
 - Perturbation, Linearisation

PULSE-WIDTH MODULATION



FREQUENCY DOMAIN ANALYSIS IN FSL

Differential equations describing each phase

PULSE-WIDTH MODULATION

$$\frac{dV_{C_{fly}}}{dt} = \frac{-1}{R_s C_{fly}} V_{C_{fly}} + \frac{1-2D}{R_s C_{fly}} V_{C_{out}} + \frac{D}{R_s C_{fly}} V_{in}$$

$$\frac{dV_{C_{out}}}{dt} = \frac{1-2D}{R_s C_{out}} V_{C_{fly}} - \left(\frac{1}{R_s C_{out}} + \frac{1}{R_L C_{out}} \right) V_{C_{out}} + \frac{D}{R_s C_{out}} V_{in}$$

$$\omega_1 = 1/R_s C_{fly} \quad \omega_2 = 1/R_s C_{out} \quad \omega_3 = 1/R_L C_{out}$$

FREQUENCY DOMAIN ANALYSIS IN FSL

Time averaged combined equations

PULSE-WIDTH MODULATION

$$\frac{dV_{C_{fly}}}{dt} = \omega_1 V_{C_{fly}} + (1 - 2D)\omega_1 V_{C_{out}} + \omega_1 D V_{in}$$

$$\frac{dV_{C_{out}}}{dt} = (1 - 2D)\omega_2 V_{C_{fly}} - (\omega_2 + \omega_3) V_{C_{out}} + D\omega_2 V_{in}$$

$$V_{C_{fly}} = \overline{V_{C_{fly}}} + \tilde{v}_{C_{fly}}$$

$$V_{C_{out}} = \overline{V_{C_{out}}} + \tilde{v}_{C_{out}}$$

$$D = D + d$$

FREQUENCY DOMAIN ANALYSIS IN FSL

Perturbation and linearization around the operation point

PULSE-WIDTH MODULATION

$$\frac{\tilde{v}_{C_{out}}}{\tilde{d}} = \frac{-2\omega_2 \overline{V_{C_{fly}}} + (1 - 2\bar{D})\omega_2 \frac{-2\omega_1 \overline{V_{C_{out}}} + \omega_1 \overline{V_{in}}}{s - \omega_1} + \omega_2 \overline{V_{in}}}{s + (\omega_2 + \omega_3) - \frac{(1 - 2\bar{D})\omega_2}{s - \omega_1}}$$

- 2 poles, 1 zero
- Operation point and load-condition dependency
- Fixed Switching frequency

FREQUENCY DOMAIN ANALYSIS IN FSL

Frequency-domain transfer-function

PULSE-WIDTH MODULATION

D=0.5

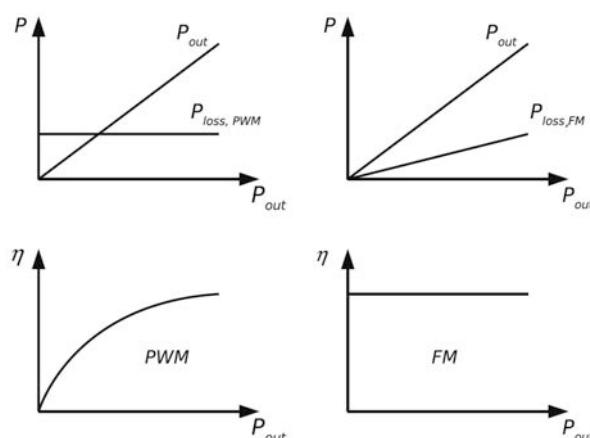
$$\frac{\tilde{v}_{C_{out}}}{\tilde{d}} = \frac{\omega_2 \overline{V_{in}} - 2 \omega_2 \overline{V_{C_{fly}}}}{s + \omega_2 + \omega_3}$$

- Only one pole remaining

FREQUENCY DOMAIN ANALYSIS IN FSL

Frequency-domain transfer-function: 50% duty cycle simplification

PULSE-WIDTH MODULATION



POWER LOSS: PWM VS PFM

Disadvantage of PWM at light loading

PULSE-WIDTH MODULATION ...

II Converter dynamics

- 2 poles, 1 zero
- Load dependent

II Switching dynamics

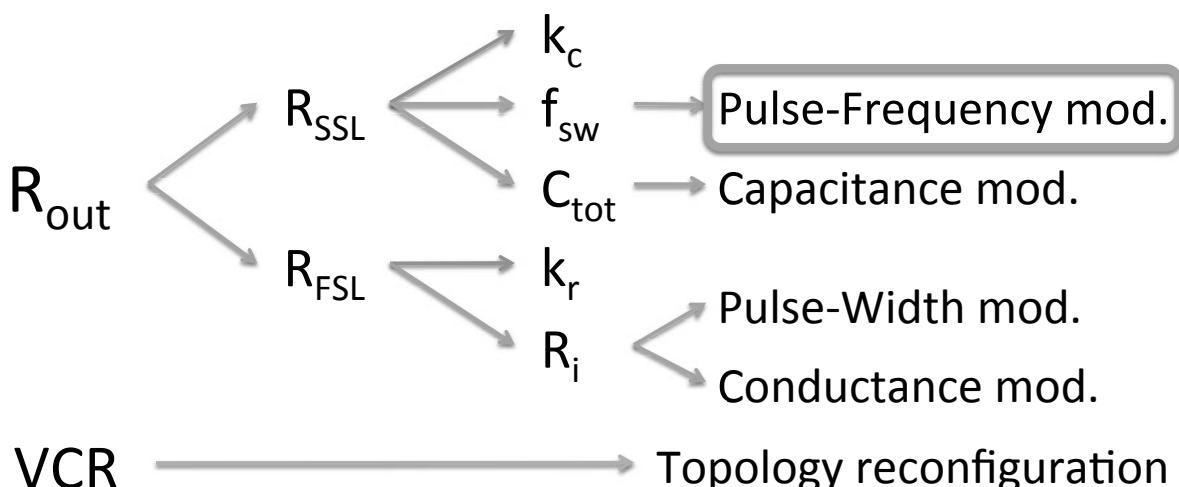
- Fixed and relatively “high” to eliminate R_{SSL} dependency R_{OUT}
- Disadvantage towards low loading

II Charge dynamics

- Constant current → best for low ripple on output voltage

... NOT THE #1 CHOICE

MODELING AND CONTROL PARAMETERS



CONTROL PARAMETER OVERVIEW

$$V_{out} = N V_{in} - I_{load} R_{out}(f_{sw}, C_{tot}, R_i)$$

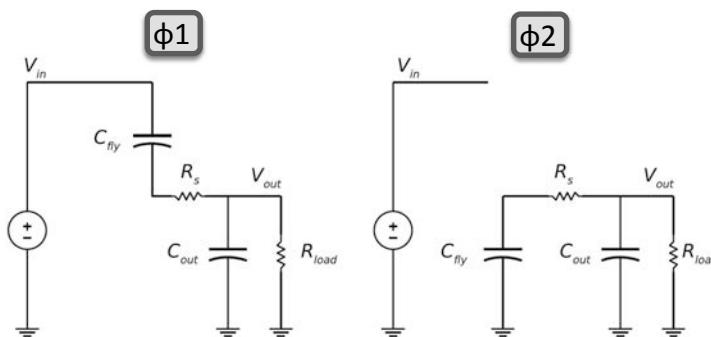
PULSE-FREQUENCY MODULATION

- Modify charge transfer by changing the frequency
 - Effect on R_{SSL} and total charge transferred

■ Frequency domain analysis in SSL

- Charge balance analysis
 - Time-Averaging Approach not valid
- Difference equation of charge conservation
 - Z-transform

PULSE-FREQUENCY MODULATION



$$C_{fly}(V_{in} - V_{out}(n-1)) + C_{out}V_{out}(n-1) = (C_{fly} + C_{out})V_{out}(n) + \frac{I_{load}T(n)}{2}$$

FREQUENCY DOMAIN ANALYSIS IN SSL

Difference equation of charge conservation

PULSE-FREQUENCY MODULATION

$$C_{fly}(V_{in} - V_{out}(n-1)) + C_{out}V_{out}(n-1) = (C_{fly} + C_{out})V_{out}(n) + \frac{I_{load}T(n)}{2}$$



Z-transform

$$\frac{V_{out}}{T} = \frac{-I_{load}}{2} \frac{z}{z(C_{fly} + C_{out}) - (C_{out} - C_{fly})}$$

|| 1 pole, 1 zero

- Stable

FREQUENCY DOMAIN ANALYSIS IN SSL

System transfer function

PULSE-FREQUENCY MODULATION...

|| Converter dynamics

- Just 1 pole
- load dependent

|| Switching dynamics

- Scales with output power
- Switch losses also scale with output power

|| Charge dynamics

- Impulsive charge transfer → frequency dependent ripple, max at low load

...INTERESTING !!

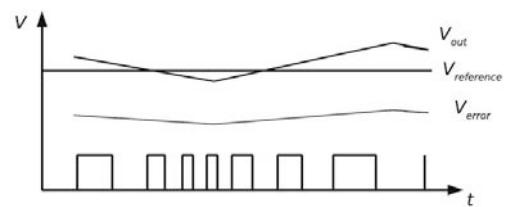
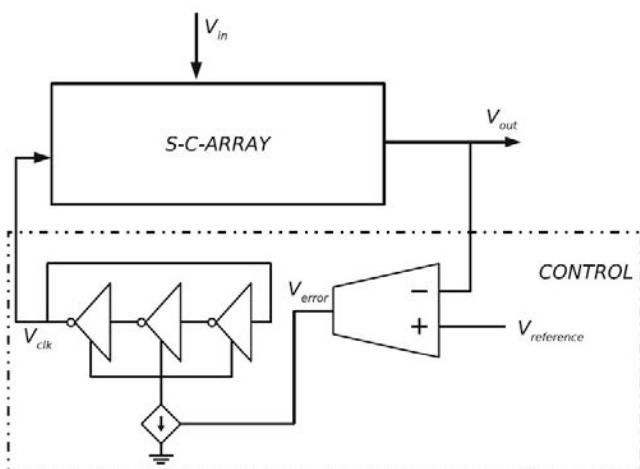
PULSE-FREQUENCY MODULATION

II Implementing PFM

Continuous-time control
 [ref. T. Van Breussegem Springer'13]

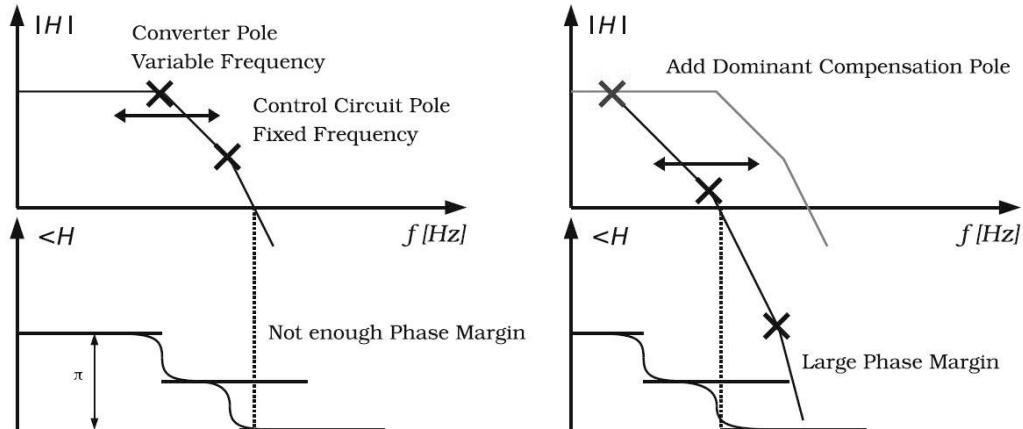
Discrete-time control
 [ref. T. Van Breussegem Springer'13]

CONTINUOUS-TIME PFM



CONTINUOUS-TIME CONTROL ARCHITECTURE

CONTINUOUS-TIME PFM



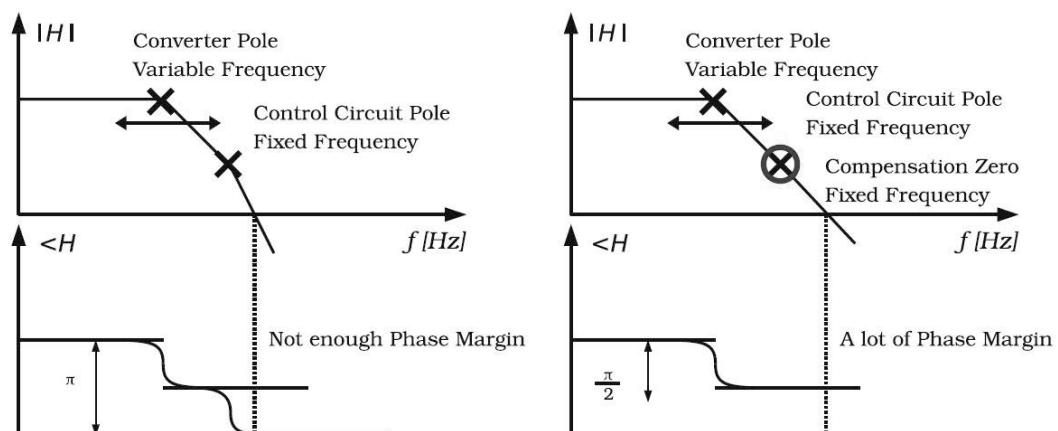
CONTINUOUS-TIME CONTROL ARCHITECTURE

Stability considerations

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CONTINUOUS-TIME PFM

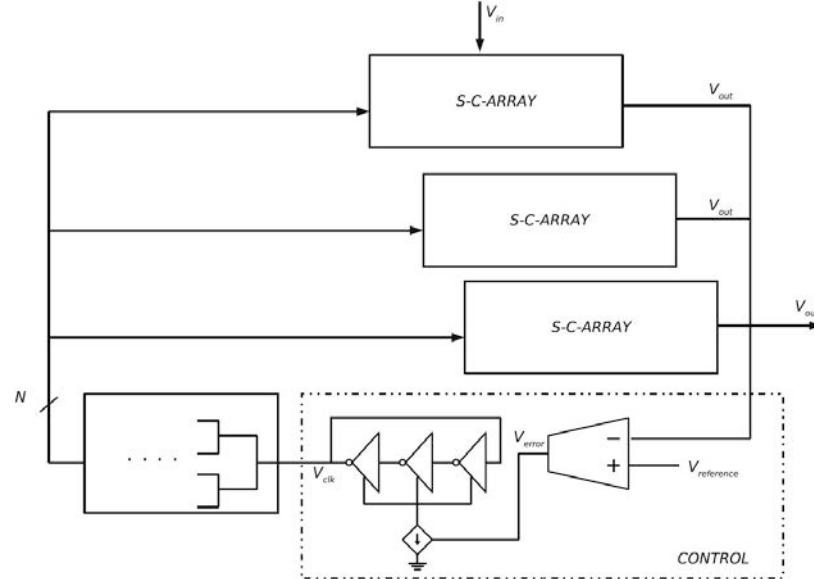


CONTINUOUS-TIME CONTROL ARCHITECTURE

Stability considerations

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CONTINUOUS-TIME CONTROL ARCHITECTURE

Implementation for time-interleaved converter

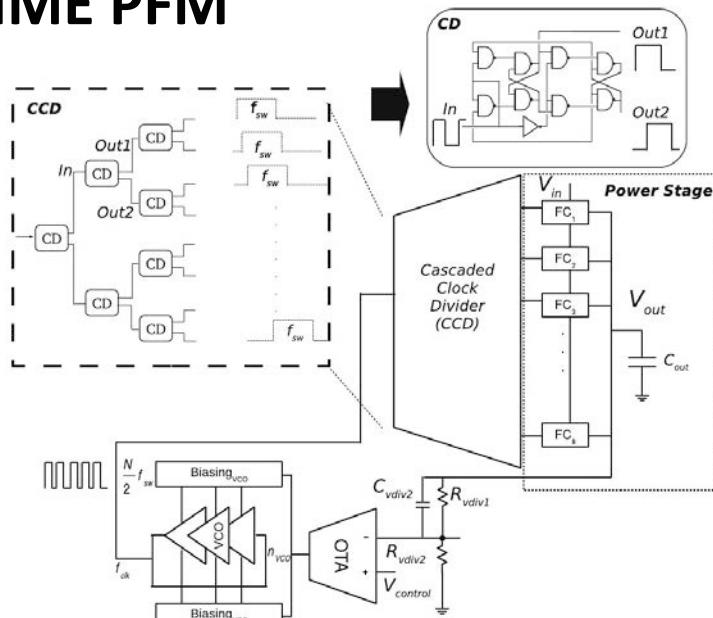
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CONTINUOUS-TIME PFM

$$V_{\text{ripple}} = 0.5\% V_{\text{out}}$$

$$V_{\text{out}} = 2V$$



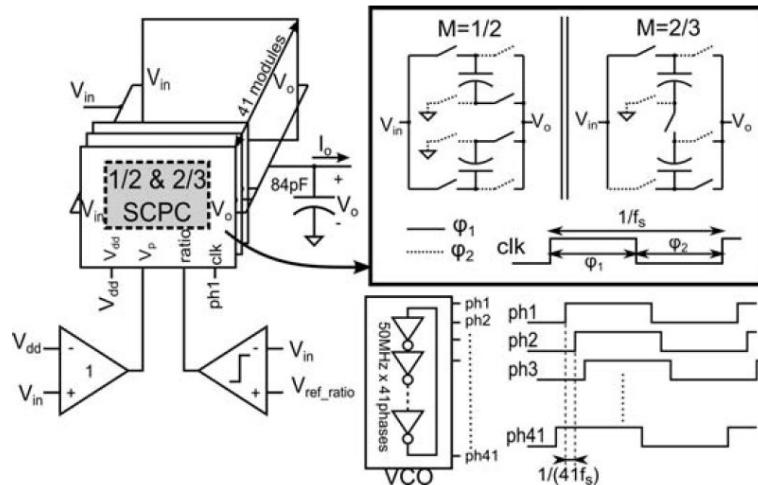
IMPLEMENTATIONS

T. Van Breussegem VLSI'09

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CONTINUOUS-TIME PFM



IMPLEMENTATIONS

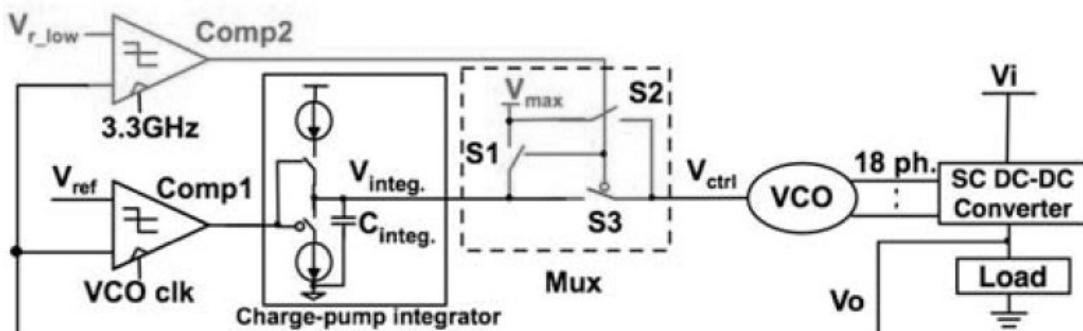
G. Villar Piqué ISSCC'12

3.8mV ripple at $V_{out} = 0.7V$

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CONTINUOUS-TIME PFM



IMPLEMENTATIONS

H.-P. Le ISSCC'13

sub-ns transient response with hysteretic bypass

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PULSE-FREQUENCY MODULATION

II Implementing PFM

Continuous-time control

[ref. T. Van Breussegem
Springer'13]

Discrete-time control

[ref. T. Van Breussegem
Springer'13]

DISCRETE-TIME CONTROL

II Boundary detection .. Reaction

- What boundary
- How many boundaries

... Closer look at this boundary

DISCRETE-TIME PFM

$$\boxed{\phi 1} \quad \left| \begin{array}{l} C_{fly} \frac{dV_{C_{fly}}}{dt} - C_{out} \frac{dV_{C_{out}}}{dt} = \frac{V_{C_{out}}}{R_L} \\ V_{C_{fly}} = V_{in} - V_{C_{out}} - R_s C_{fly} \frac{dV_{C_{fly}}}{dt} \end{array} \right. \rightarrow$$

$$\begin{aligned} 0 &= \frac{V_{in} - V_{C_{out}} - V_{C_{fly}}}{R_s C_{fly}} \\ 0 &= -\frac{V_{C_{fly}}}{R_s C_{out}} - \left(\frac{1}{R_s C_{out}} + \frac{1}{R_L C_{out}} \right) V_{C_{out}} + \frac{V_{in}}{R_s C_{out}} \end{aligned}$$

$$\boxed{\phi 2} \quad \left| \begin{array}{l} -C_{fly} \frac{dV_{C_{fly}}}{dt} - C_{out} \frac{dV_{C_{out}}}{dt} = \frac{V_{C_{out}}}{R_L} \\ V_{C_{fly}} = V_{C_{out}} - R_s C_{fly} \frac{dV_{C_{fly}}}{dt} \end{array} \right. \rightarrow$$

$$\begin{aligned} 0 &= \frac{V_{C_{out}} - V_{C_{fly}}}{R_s C_{fly}} \\ 0 &= \frac{V_{C_{fly}}}{R_s C_{out}} - \left(\frac{1}{R_s C_{out}} + \frac{1}{R_L C_{out}} \right) V_{C_{out}} \end{aligned}$$

CLOSER LOOK AT HYSTERETIC BOUNDARY

Equilibrium point of each phase

DISCRETE-TIME PFM

$$\boxed{\phi 1} \quad \left| \begin{array}{l} 0 = \frac{V_{in} - V_{C_{out}} - V_{C_{fly}}}{R_s C_{fly}} \\ 0 = -\frac{V_{C_{fly}}}{R_s C_{out}} - \left(\frac{1}{R_s C_{out}} + \frac{1}{R_L C_{out}} \right) V_{C_{out}} + \frac{V_{in}}{R_s C_{out}} \end{array} \right. \rightarrow$$

$$\begin{aligned} V_{C_{out}} &= V_{in} - V_{C_{fly}} \\ V_{C_{out}} &= 0 \end{aligned} \quad (\text{ } V_{in}, \text{ } 0)$$

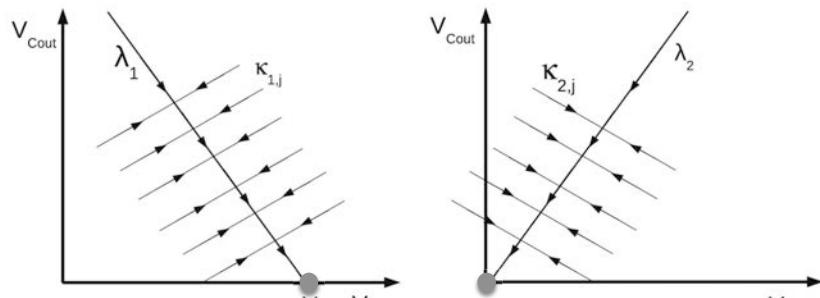
$$\boxed{\phi 2} \quad \left| \begin{array}{l} 0 = \frac{V_{C_{out}} - V_{C_{fly}}}{R_s C_{fly}} \\ 0 = \frac{V_{C_{fly}}}{R_s C_{out}} - \left(\frac{1}{R_s C_{out}} + \frac{1}{R_L C_{out}} \right) V_{C_{out}} \end{array} \right. \rightarrow$$

$$\begin{aligned} V_{C_{out}} &= V_{C_{fly}} \\ V_{C_{out}} &= 0 \end{aligned} \quad (0, 0)$$

CLOSER LOOK AT HYSTERETIC BOUNDARY

Equilibrium point of each phase

DISCRETE-TIME PFM



$$V_{Cout} = V_{in} - V_{Cfly}$$

$$V_{Cout} = V_{Cfly}$$

DISCRETE-TIME PFM

Equilibrium vector field of each phase

DISCRETE-TIME PFM

$$\boxed{\phi 1} \quad \frac{dV_{C_{out},1}}{dV_{C_{fly},1}} = K_C \left(1 - \frac{K_R V_{C_{out}}}{V_{in} - V_{C_{out}} - V_{C_{fly}}} \right)$$

$$K_C = \frac{C_{fly}}{C_{out}}$$

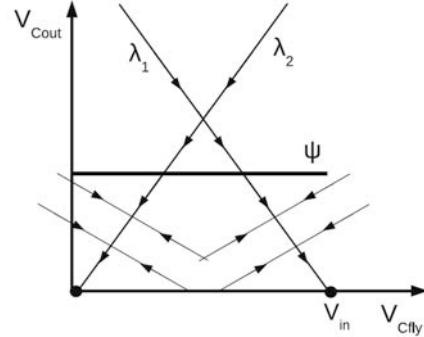
$$K_R = \frac{R_s}{R_L}$$

$$\boxed{\phi 2} \quad \frac{dV_{C_{out},2}}{dV_{C_{fly},2}} = -K_C \left(1 - \frac{K_R V_{C_{out}}}{V_{C_{out}} - V_{C_{fly}}} \right)$$

CLOSER LOOK AT HYSTERETIC BOUNDARY

Trajectories of each phase in the $V_{Cout} - V_{Cfly}$ space

DISCRETE-TIME PFM



$$\psi : V_{Control} - V_{Cout} = 0$$

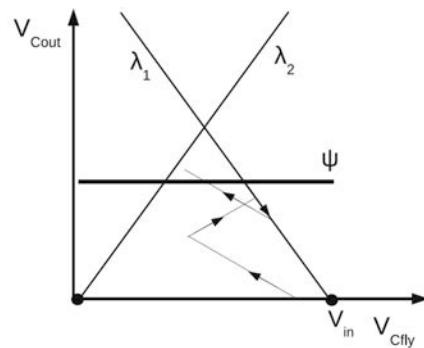
DISCRETE-TIME PFM

Introduction of one control boundary

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DISCRETE-TIME PFM



$$V_{Control} - V_{Cout} > 0$$

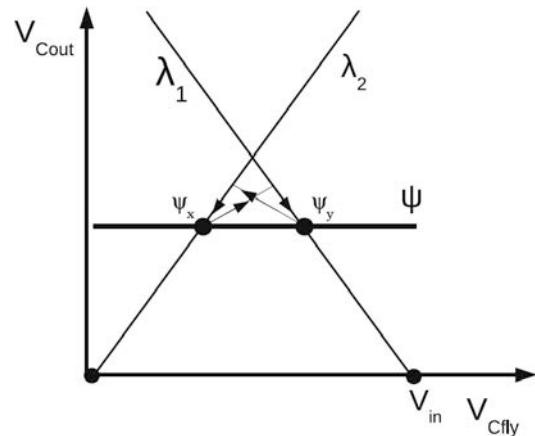
DISCRETE-TIME PFM

Start-up switching

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DISCRETE-TIME PFM



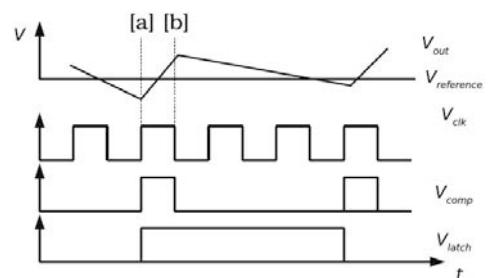
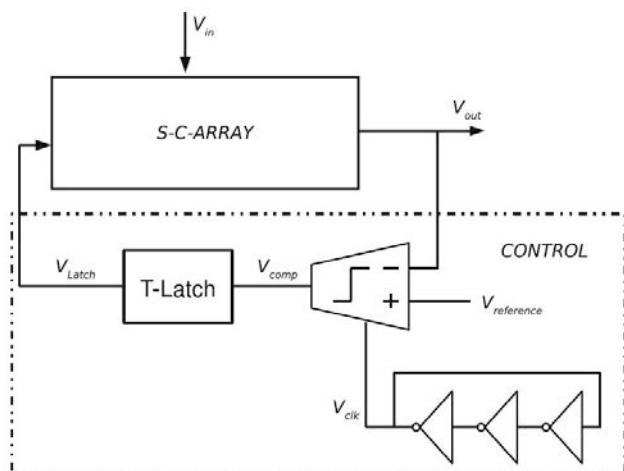
DISCRETE-TIME PFM

Steady-state operation

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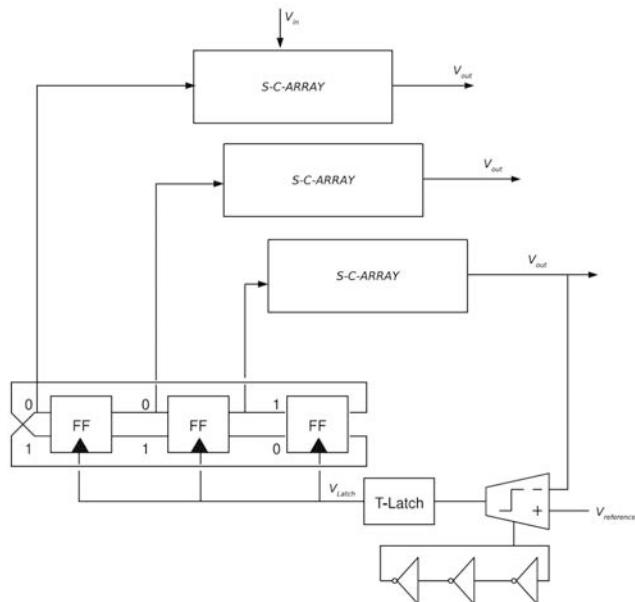
DISCRETE-TIME PFM



DISCRETE-TIME CONTROL ARCHITECTURE

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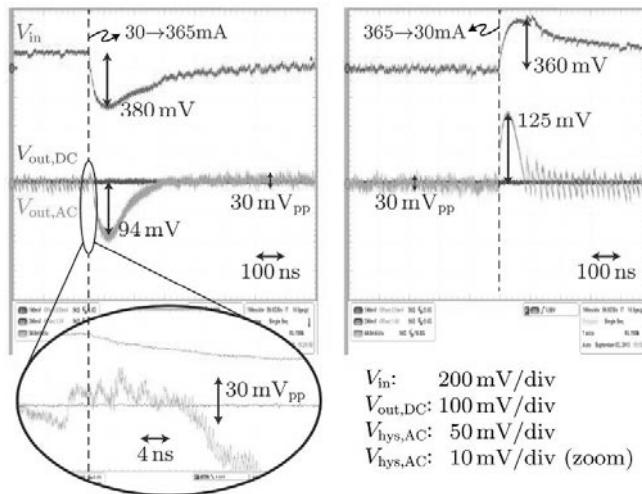
DISCRETE-TIME CONTROL ARCHITECTURE

Implementation for time-interleaved converter

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DISCRETE-TIME PFM



IMPLEMENTATIONS

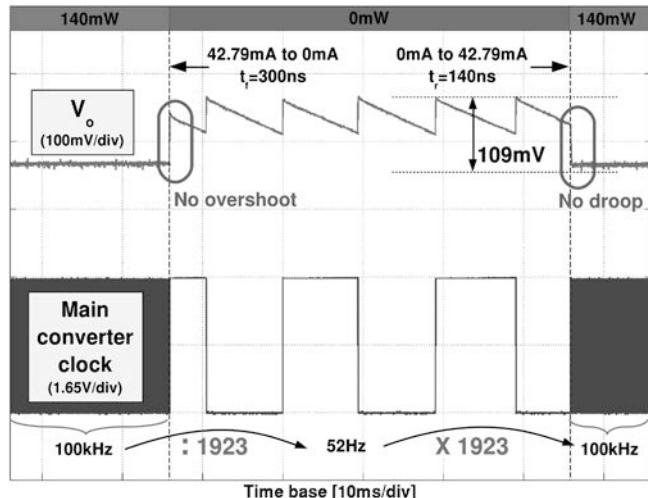
T. Andersen ISSCC'14

sub-ns response with 4GHz comparator

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DISCRETE-TIME PFM



IMPLEMENTATIONS

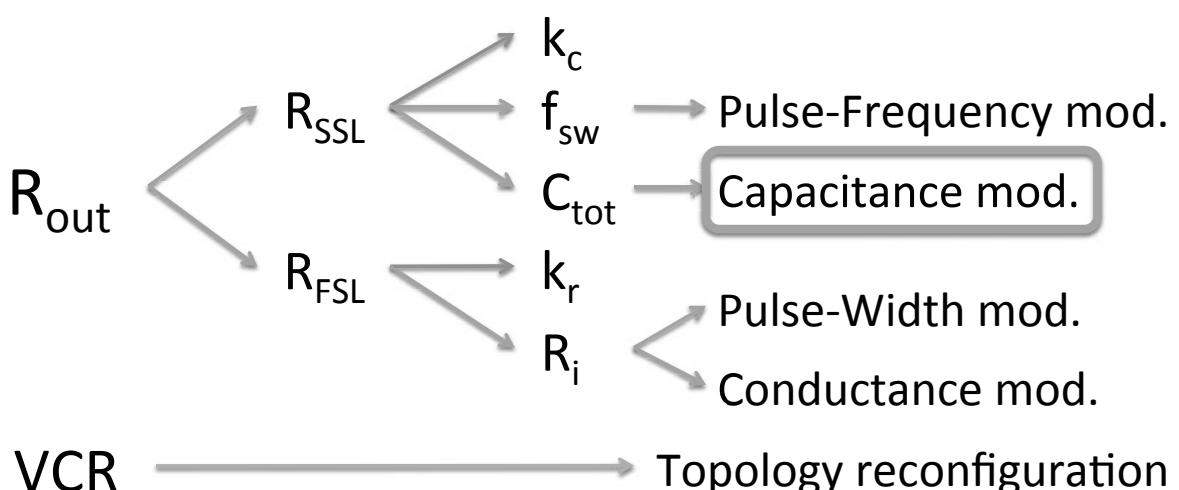
H. Meyvaert ISSCC'15

Full load-step at 3.3V_{out}

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MODELING AND CONTROL PARAMETERS



CONTROL PARAMETER OVERVIEW

$$V_{out} = N V_{in} - I_{load} R_{out}(f_{sw}, C_{tot}, R_i)$$

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CAPACITANCE MODULATION

II Modify charge transfer by changing the transfer medium

- Effect on R_{SSL} and total charge transferred

II Fixed Frequency

- Predictable noise spectrum

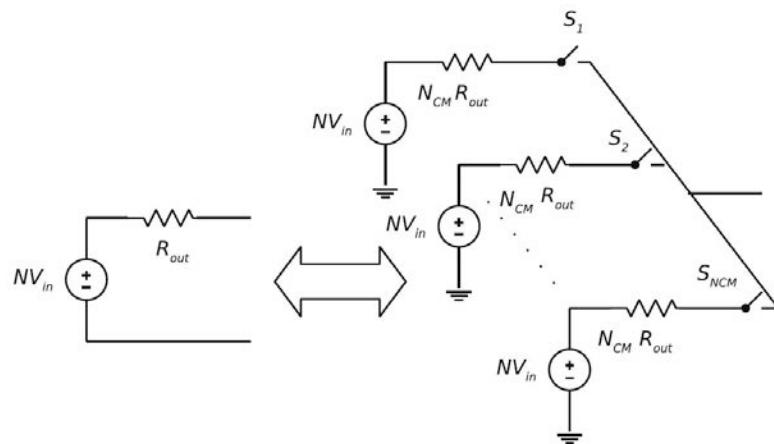
II Double boundary

- Limited regulation accuracy

II Relative changes

- Impact on transient response

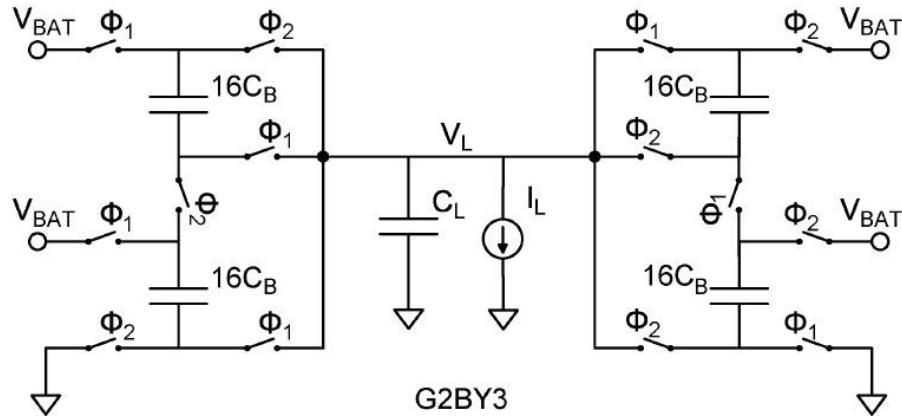
CAPACITANCE MODULATION



BY MEANS OF FRAGMENTATION

$G_{out,max}$ and anything below in discrete steps

CAPACITANCE MODULATION



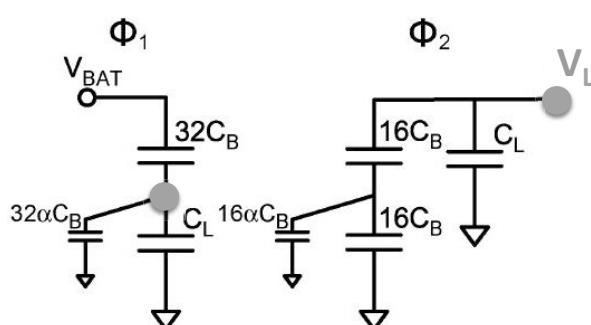
CHARGE TRANSFER PER CYCLE

In a 2/3 converter
 [ref. Y.K. Ramadass JSSC'10]

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CAPACITANCE MODULATION



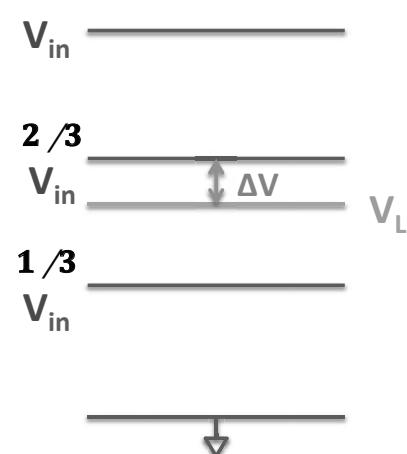
$$Q_{\phi 1} = 32C_B \Delta V_{\phi 1}$$

$$Q_{\phi 2} = 16C_B \Delta V_{\phi 2} || 16C_B \Delta V_{\phi 2}$$

$$Q_{\phi 1} = 32C_B V_{C1} - V_{C2} = 48C_B \Delta V$$

$$Q_{\phi 2} = 8C_B 2(V_{C2} - V_{C1}) = 24C_B \Delta V$$

$$Q_{tot} = 72C_B \Delta V$$



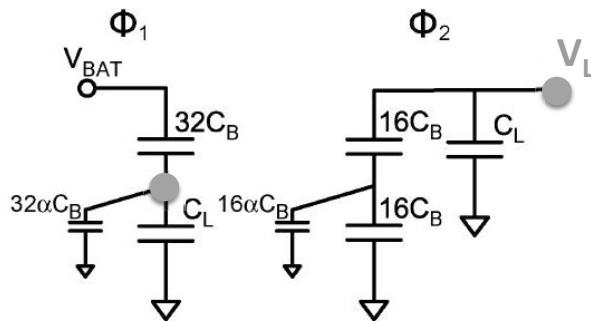
$$V_{C1} @ C_{B,\phi 1, end} = 1/3 V_{in} + \Delta V$$

$$V_{C2} @ C_{B,\phi 2, end} = 1/3 V_{in} - \Delta V/2$$

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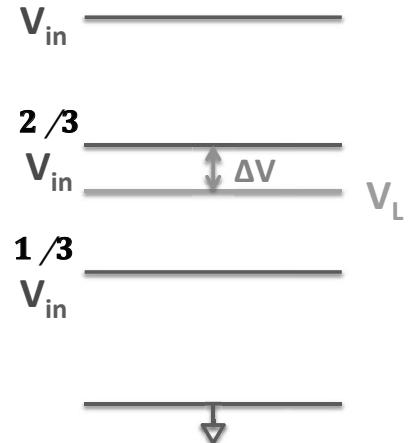
CAPACITANCE MODULATION



$$Q_{\text{tot}} = 72C_B \Delta V$$

$$I_{\text{tot}} = f_{\text{sw}} 72C_B \Delta V$$

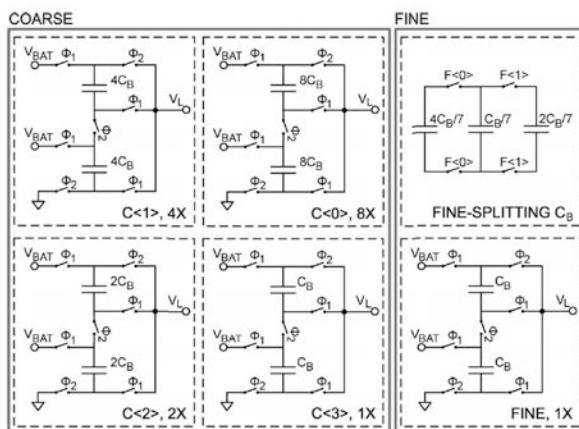
$$R_{\text{out}} = \Delta V / I_{\text{tot}} = 1/f_{\text{sw}} 72CB$$



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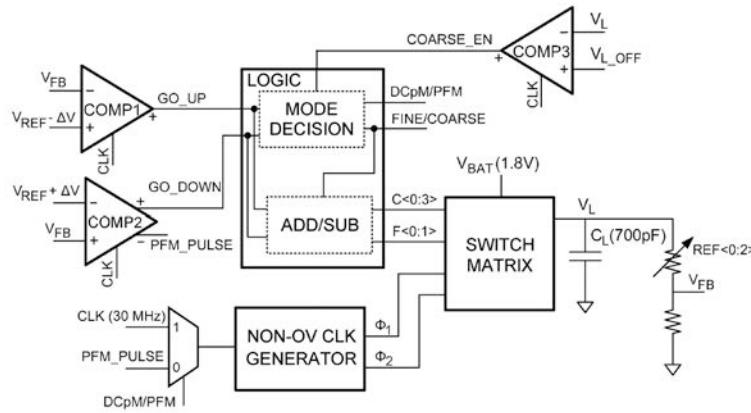
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CAPACITANCE MODULATION



BINARY FRAGMENTATION OF TOTAL CAPACITANCE

CAPACITANCE MODULATION



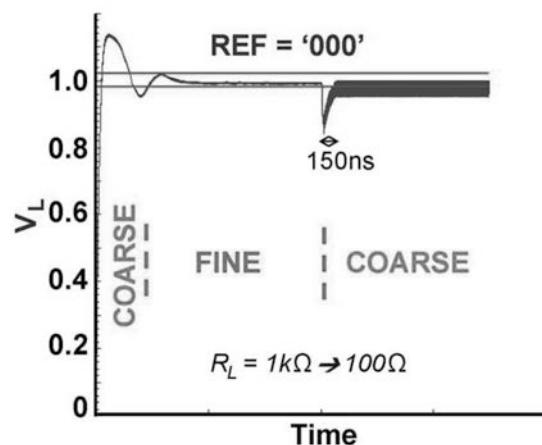
VOLTAGE MODE CONTROL

Dual boundary + additional boundary to improve transient control

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CAPACITANCE MODULATION

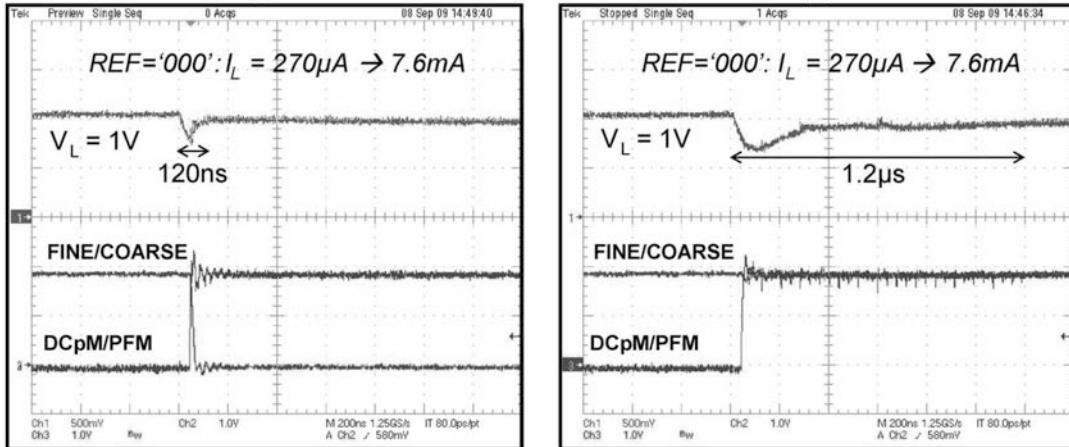


OPERATION AND TRANSIENT RESPONSE

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CAPACITANCE MODULATION



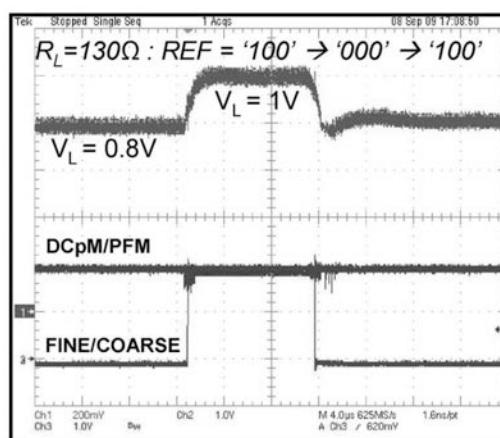
OPERATION AND TRANSIENT RESPONSE

With and without 3rd "COURSE" boundary

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CAPACITANCE MODULATION



OPERATION AND TRANSIENT RESPONSE

Load-voltage step

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CAPACITANCE MODULATION SUMMARY

II Converter dynamics

- Dual boundary

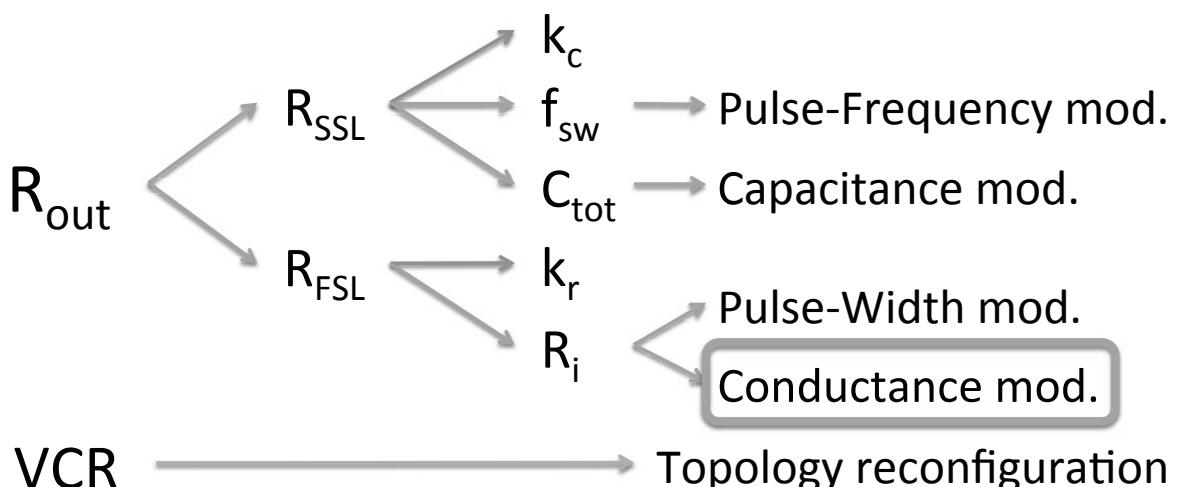
II Switching dynamics

- Fixed frequency, but loss scaling
- Advantage towards low loading

II Charge dynamics

- Impulsive charge transfer → frequency dependent ripple , lower ripple at higher f_{sw}

MODELING AND CONTROL PARAMETERS



CONTROL PARAMETER OVERVIEW

$$V_{out} = N V_{in} - I_{load} R_{out}(f_{sw}, C_{tot}, R_i)$$

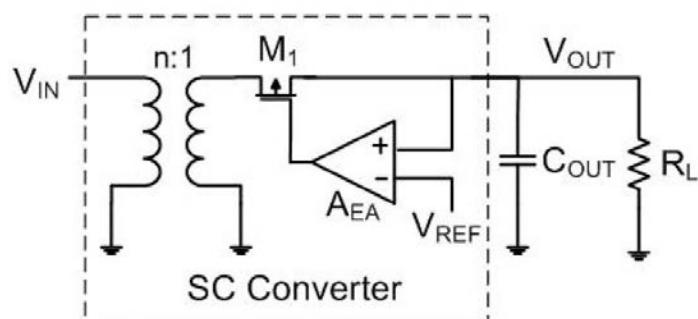
CONDUCTANCE MODULATION

III Pulse-Width Modulation

III Linear regulation

- Discrete
 - R_{FSL} equivalent of capacitance modulation in R_{SSL}
 - Finite step-size = finite resolution
 - Dual boundary voltage control can reduce transient response
 - Not discussed further but recent research available: R. Jain JSSC'15
- Continuous
 - Continuous-time amplifier, continuous R_{FSL}
 - Switch conductance non-linear with drive

CONDUCTANCE MODULATION

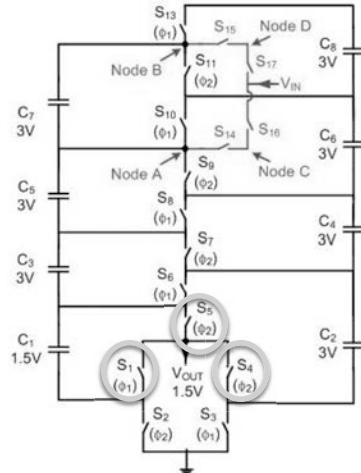


$$GBW = A_{EA} gmtot / COUT$$

CONTROL ARCHITECTURE

Linear regulation, **within** the switched-capacitor converter
 [ref. V. Ng PhD Berkeley '11 / V. Ng TPEL'13]

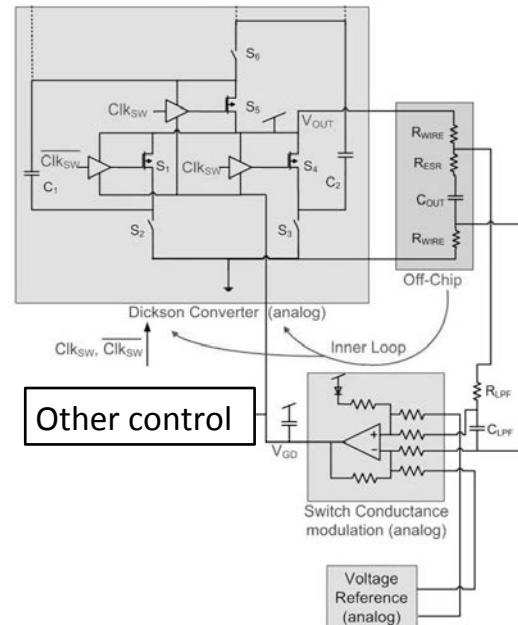
CONDUCTANCE MODULATION



APPLICATION OF CONDUCTANCE MODULATION

Where to insert conductance modulation?

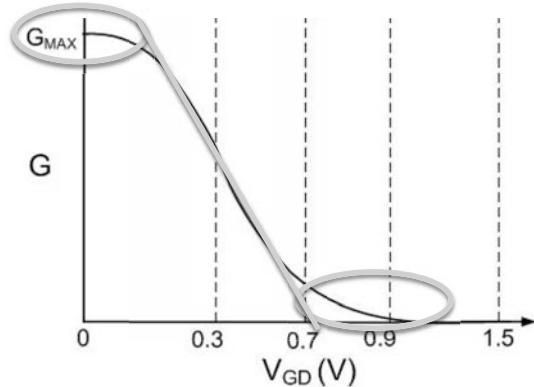
CONDUCTANCE MODULATION



CONTROL ARCHITECTURE

Continuous-time amplifier feedback

CONDUCTANCE MODULATION



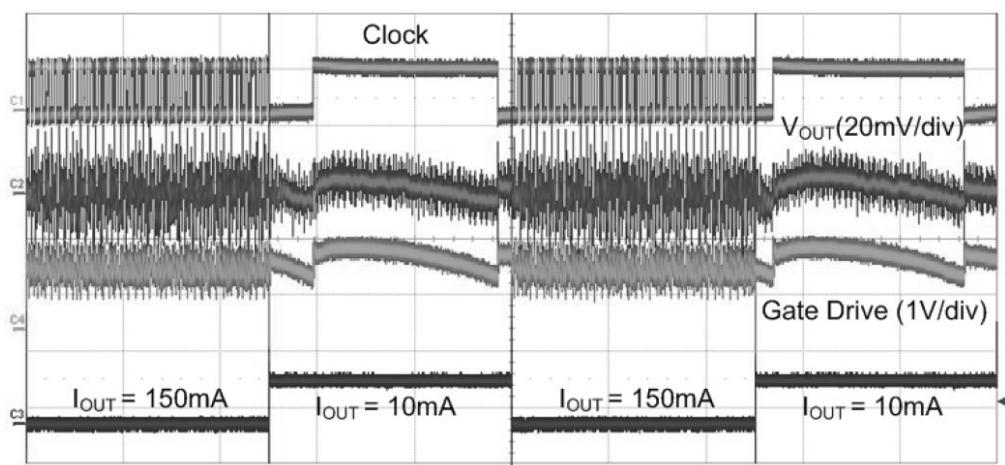
MOSFET CONDUCTANCE CHARACTERISTIC

G as function of gate-drive voltage

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CONDUCTANCE MODULATION



MEASUREMENT RESULT

Gate drive evolution over clock period

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CONDUCTANCE MODULATION SUMMARY

II Converter dynamics

- 1 converter pole ($D=0.5$)

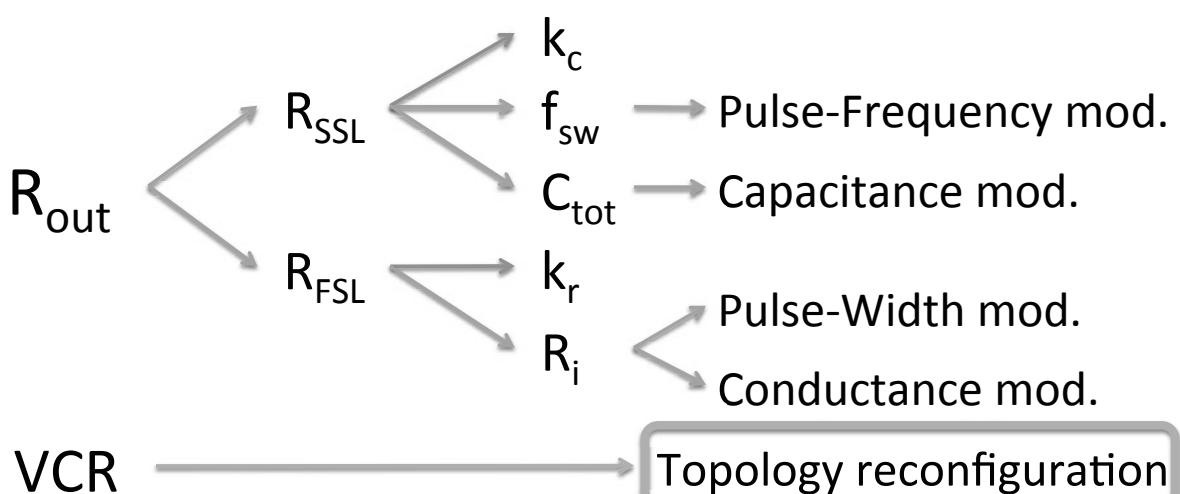
II Switching dynamics

- Fixed frequency
- Disadvantage towards low loading, f_{sw} can 'track' to G_{FSL}

II Charge dynamics

- Active regulation of charge transfer → best for low ripple on output voltage

MODELING AND CONTROL PARAMETERS



CONTROL PARAMETER OVERVIEW

$$V_{out} = N V_{in} - I_{load} R_{out}(f_{sw}, C_{tot}, R_i)$$

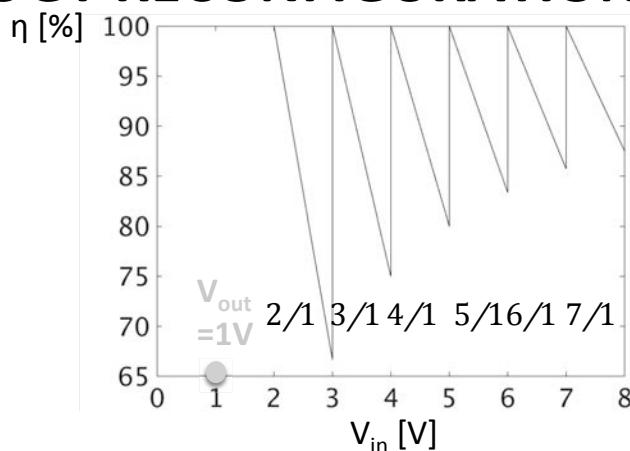
TOPOLOGY RECONFIGURATION

- Supplemental control approach
 - “Outer loop” to improve performance

■ 2 Implementation approaches

- Single ***multi-ratio*** converter
 - Only 1 R_{out}
 - low impact on current density and efficiency
- Multi ***single-ratio*** converters in series
 - High # Ratios, cascade of R_{out} of each converter
 - higher impact on current density and efficiency

TOPOLOGY RECONFIGURATION



MULTI-RATIO CONVERSION

Higher efficiency in a broader range

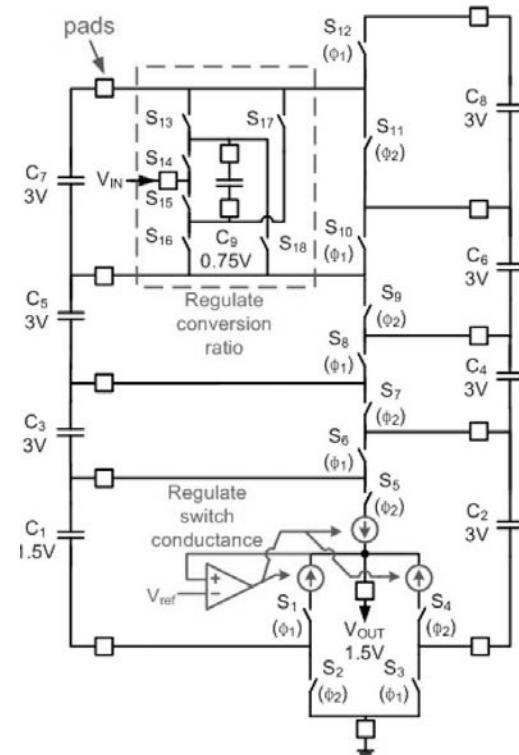
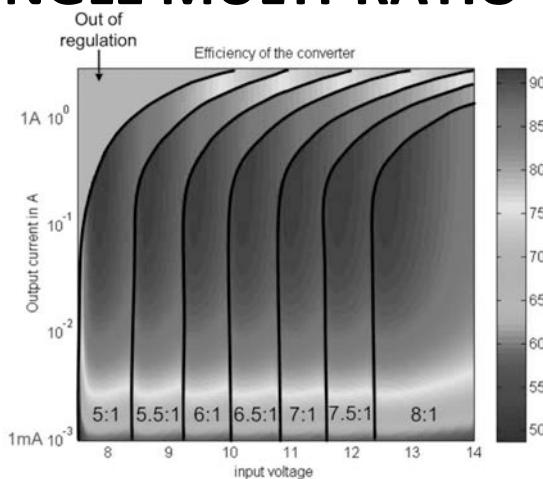
TOPOLOGY RECONFIGURATION

VCR, $V_{in} = 1V$	V_{out} [V]	n_{MAX} @ X-over
1/1	1	80%
4/5	0.8	93.8%
3/4	0.75	88%
2/3	0.66	91%
3/5	0.6	83.3%
1/2	0.5	

HIGH EFFICIENCY VOLTAGE SETTINGS

Trade-offs: # Ratios (complexity, robustness) versus granularity (performance)

SINGLE MULTI-RATIO TR

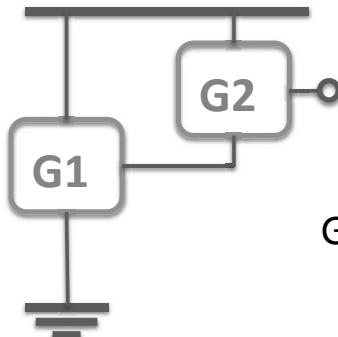


7-RATIO CONVERTER

Half-integer-ratio steps

[ref. V. Ng PhD Berkeley '11 / V. Ng TPEL'13]

MULTI SINGLE-RATIO TR

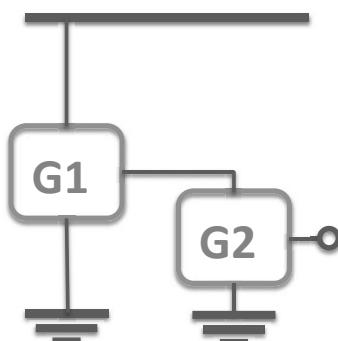


$$G_{\text{tot}} = G_1 + (1 - G_1)G_2$$

MULTIPLICATION OF CASCADED RATIO'S

[ref. L.G. Salem CICC'14]

MULTI SINGLE-RATIO TR

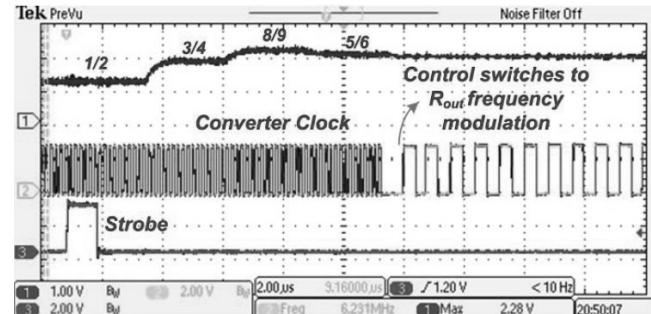
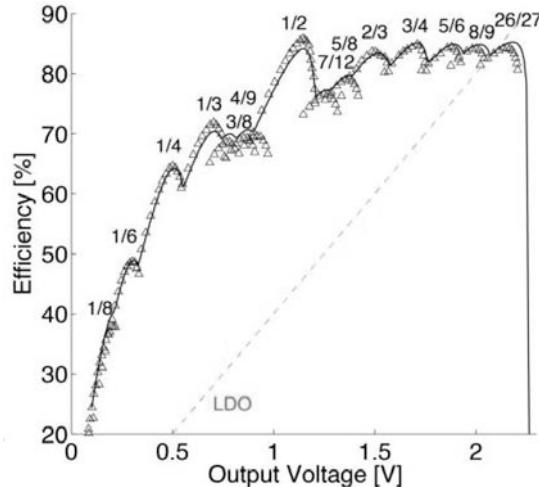


$$G_{\text{tot}} = G_1 G_2$$

MULTIPLICATION OF CASCADED RATIO'S

[ref. L.G. Salem CICC'14]

MULTI SINGLE-RATIO TR



45-RATIO

3 stage recursive: 3 cascaded converters

Ternary cells: individual cells are **single multi-ratio** (1/3, 1/2, 2/3)

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Hans Meyvaert

TOPOLOGY RECONFIGURATION

SUMMARY

Extending high efficiency regime of SC converters

- Closer match between **steady-state** $VCR_{topology}$ and VCR_{actual}
- Not suited for load regulation
- Secondary loop as performance enhancement

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OUTLINE

1. Introduction
2. SC DC-DC: Modeling & Control parameters
3. Control techniques: From theory to practice
4. Comparison of Pro's and Con's of each technique:
For each scenario, a matching control
5. Summary

COMPARISON OF DISCUSSED CONTROL

- As applications differ, so do their requirements
 - Select most suitable control
 - Combine control techniques into hybrid solutions
- Main characteristics
 - Output voltage ripple amplitude and spectrum
 - Transient response
 - Efficiency
 - Steady-state
 - Load current variation
 - Input/output voltage variation

COMPARISON OF DISCUSSED CONTROL

Technique		η - Load	Noise	Transient Response	Regulation range
PFM CT	$R_{SSL} - f_{sw}$	++	-	+	+
PFM DT	$R_{SSL} - f_{sw}$	++	--	++	++
CAP MOD	$R_{SSL} - C_{fly}$	++	+/-	+	+
PWM	$R_{FSL} - R_{on}$	--	++	+	-
V_{GS}	$R_{FSL} - R_{on}$	--	++	+	-

II η over load variation

- PFM: Linear scaling, DT slightly better than CT
- Cap modulation: Linear scaling
- PWM / Conductance modulation: penalty at light load

COMPARISON OF DISCUSSED CONTROL

Technique		η - Load	Noise	Transient Response	Regulation range
PFM CT	$R_{SSL} - f_{sw}$	++	-	+	+
PFM DT	$R_{SSL} - f_{sw}$	++	--	++	++
CAP MOD	$R_{SSL} - C_{fly}$	++	+/-	+	+
PWM	$R_{FSL} - R_{on}$	--	++	+	-
V_{GS}	$R_{FSL} - R_{on}$	--	++	+	-

II Noise

- Conductance modulation: linear regulation and predictable spectrum
- Cap modulation: dual boundary, but predictable spectrum
- PFM CT: noise symmetrically around average V_{out} , unpredictable spectrum
- PFM DT: lower bound referenced ripple, unpredictable spectrum

COMPARISON OF DISCUSSED CONTROL

Technique		η - Load	Noise	Transient Response	Regulation range
PFM CT	$R_{SSL} - f_{sw}$	++	-	+	+
PFM DT	$R_{SSL} - f_{sw}$	++	--	++	++
CAP MOD	$R_{SSL} - C_{fly}$	++	+/-	+	+
PWM	$R_{FSL} - R_{on}$	--	++	+	-
V_{GS}	$R_{FSL} - R_{on}$	--	++	+	-

II Transient response

- PFM DT: single-step response, down to ns range
- PFM CT / Conductance modulation : response related to CT amplifier power
- Cap modulation: multiple-step response

COMPARISON OF DISCUSSED CONTROL

Technique		η - Load	Noise	Transient Response	Regulation range
PFM CT	$R_{SSL} - f_{sw}$	++	-	+	+
PFM DT	$R_{SSL} - f_{sw}$	++	--	++	++
CAP MOD	$R_{SSL} - C_{fly}$	++	+/-	+	+
PWM	$R_{FSL} - R_{on}$	--	++	+	-
V_{GS}	$R_{FSL} - R_{on}$	--	++	+	-

II Regulation range

- PFM DT: full frequency range
- PFM CT: frequency range limited by VCO
- PWM: duty cycle limited
- Cap modulation: Converter granularization limited

OUTLINE

1. Introduction
2. SC DC-DC: Modeling & Control parameters
3. Control techniques: From theory to practice
4. Comparison of Pro's and Con's of each technique:
For each scenario, a matching control
5. Summary

SUMMARY

- Discussed Switched-Capacitor DC-DC operation
 - Identified parameters suitable for control
- Discussed regulation techniques that have been used in recent state of the art
 - Background
 - Implementations
- Compared the strengths and weaknesses
 - Over key controller requirements

Thank you for your attention



RIPPLE-BASED CONTROL TECHNIQUES FOR BUCK TYPE DC- DC CONVERTER

Jesús A. Oliver

Universidad Politécnica de Madrid

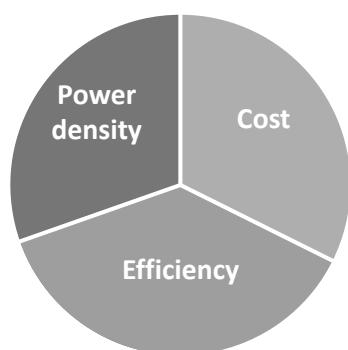


Conference Sponsors:



WHY VERY FAST CONTROLS?

Figures of merit of
power converter

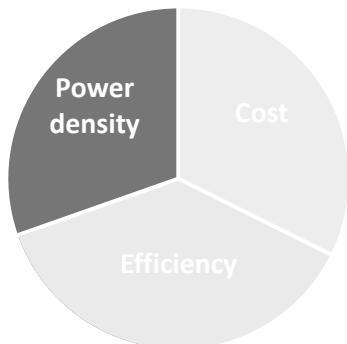


Can a very fast control improve
the figures of merit of a power
converter?

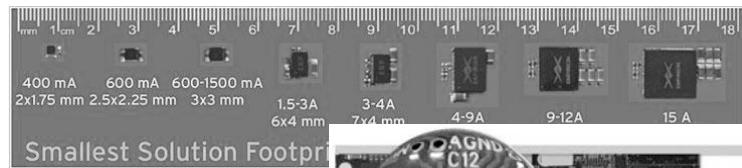
WHY VERY FAST CONTROLS?

**ESSCIRC
ESSDERC
2015**

Figures of merit of power converter



A very fast control can reduce the size of the converter in point-of-load converters by reducing the required output capacitance!



Enpirion-Altera integrated converters still has output capacitor outside



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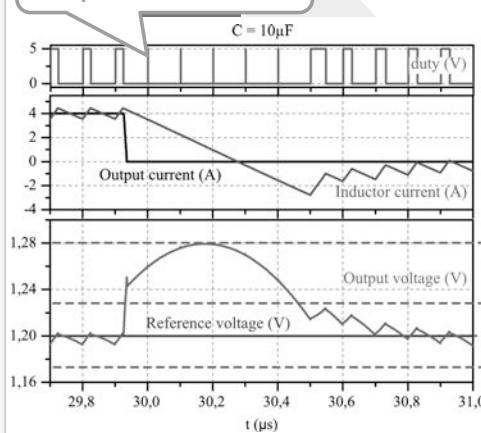
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WHY VERY FAST CONTROLS?

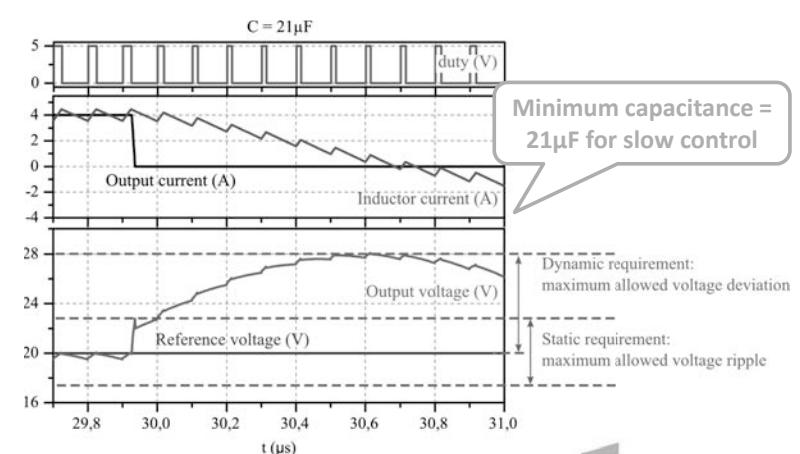
**ESSCIRC
ESSDERC
2015**

Figures of merit of power converter

Minimum capacitance = 10 μ F for fast control



A very fast control can reduce the size of the converter in point-of-load converters by reducing the required output capacitance!

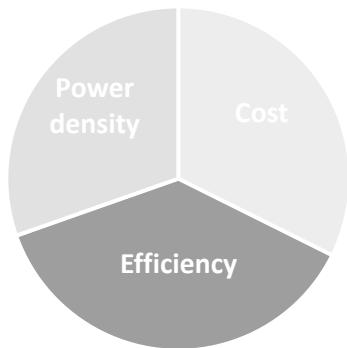


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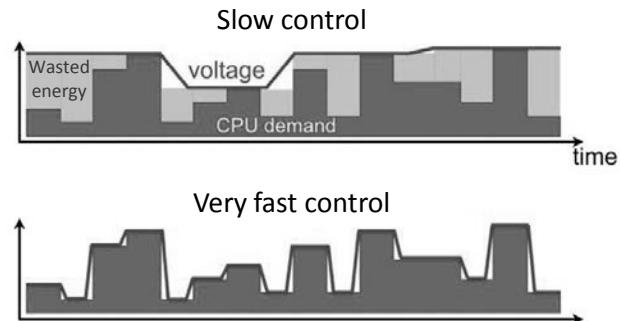
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WHY VERY FAST CONTROLS?

Figures of merit of power converter



A very fast control can improve the efficiency and reduce the stress of the system in applications with Dynamic Voltage Scaling!

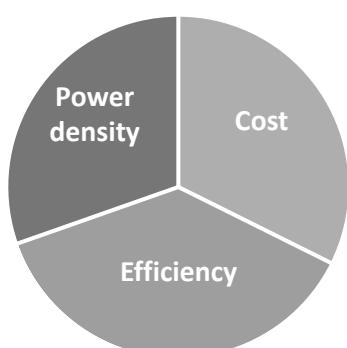


<http://www.eecs.harvard.edu/~wonyoung/research.html>

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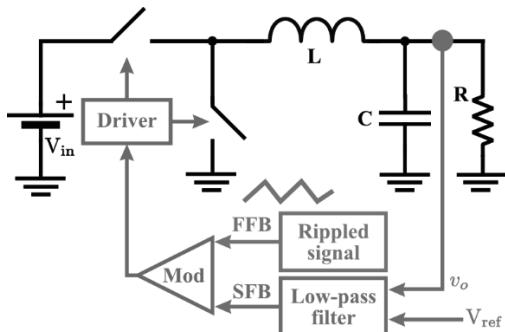
WHY VERY FAST CONTROLS?

Figures of merit of power converter



- The control is not only something to brag about, but it can have tangible effects on the figures of merits of the power supply
- The control just needs to be fast enough to minimize the voltage deviation
- Low-cost, integrable, fast controls are needed to be able to improve the figures of merit.
- Little point in creating a very fast control at the expense of increasing the size or cost of the converter

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- These controls use a rippled signal from the power stage to modulate the control such as in current mode control
- The fast dynamic response is given through the fast feedback path (FFB) and the zero steady-state error is given by the slow feedback path (SFB)
- Simple implementation but often dependency on parasitic elements



TEXAS
INSTRUMENTS D-CAP series

ON Semiconductor®



V² control

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OUTLINE

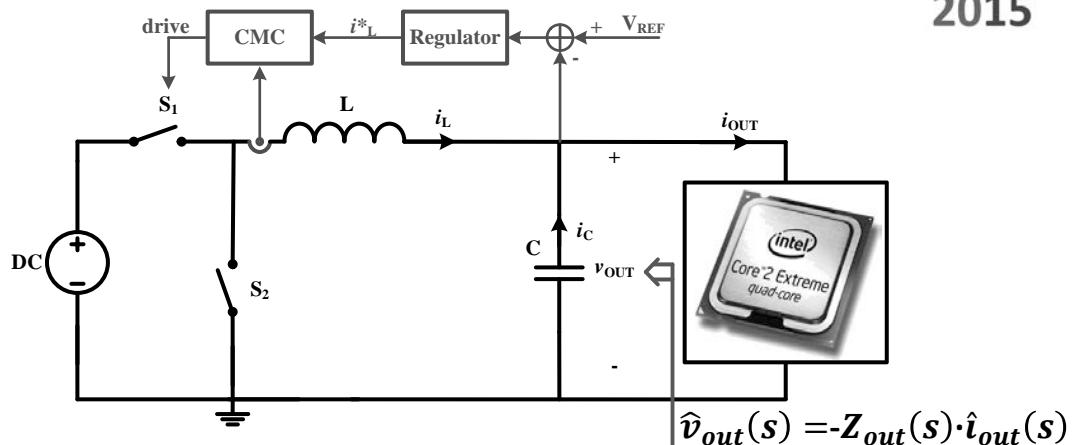
60'

- Review of basic concepts
 - Current Mode Control
 - Voltage Mode Control
 - Robustness to C_{out} variation
- Ripple based controls
- V^1 Concept
- Modeling techniques
- Conclusions

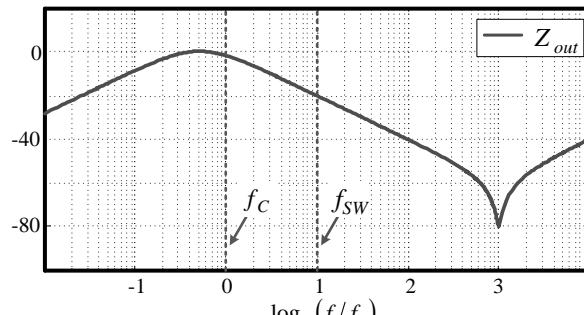
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- Review of basic concepts
 - Current Mode Control
 - Voltage Mode Control
 - Robustness to C_{out} variation
- Ripple based controls
- V^1 Concept
- Modeling techniques
- Conclusions

INTRODUCTION



$$\hat{v}_{out}(s) = -Z_{out}(s) \cdot \hat{i}_{out}(s)$$



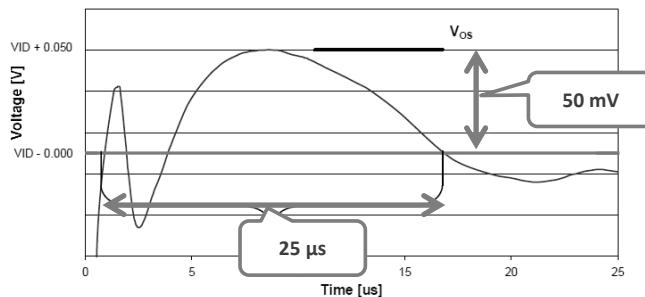
INTRODUCTION



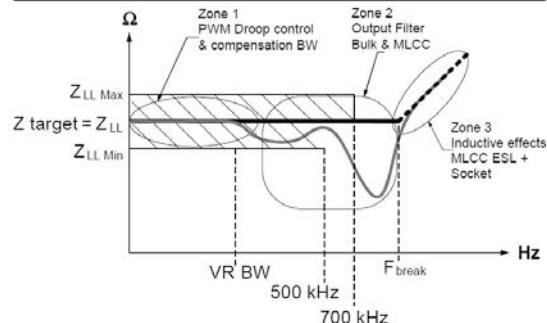
Intel application notes - **Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1**, Design Guidelines, September 2009



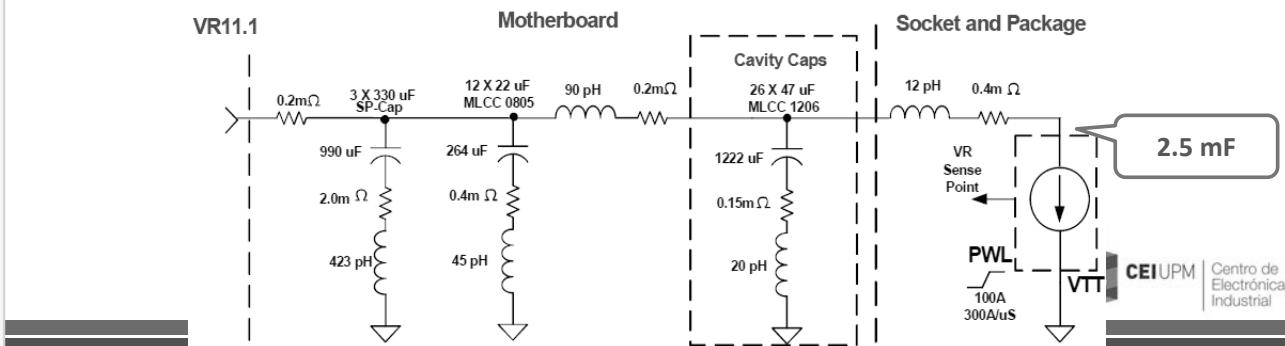
Output voltage deviation



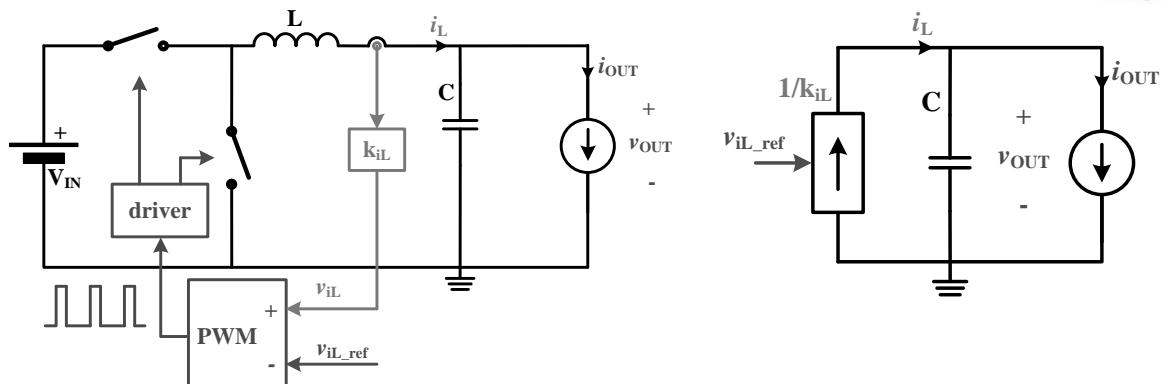
Output Impedance specification



Recommended Output Capacitor



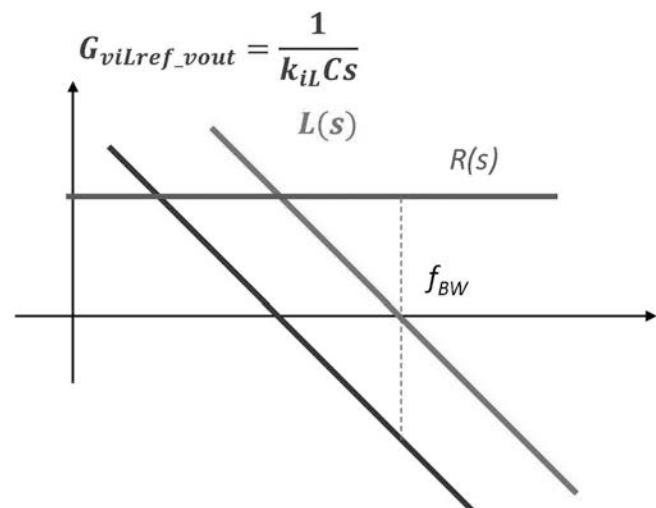
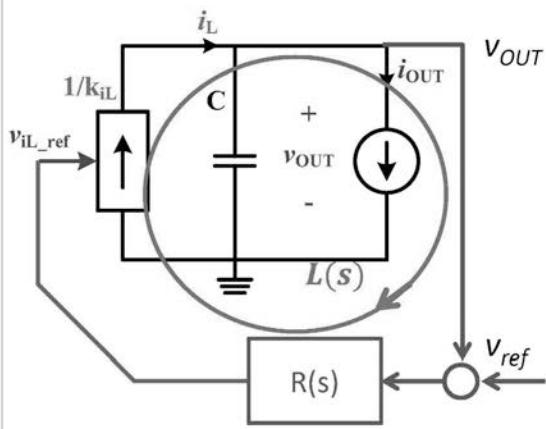
1ST ORDER APPROXIMATION OF CURRENT MODE CONTROL



- Simple approximation for current mode control
- Simple interpretation
- Good physical insight
- Does not predict sub-harmonic oscillations
- Does not consider audio-susceptibility

VOLTAGE CONTROLLER DESIGN

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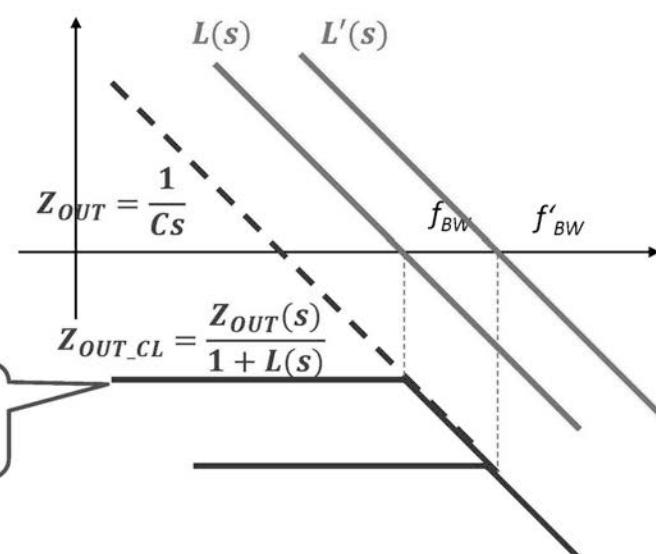
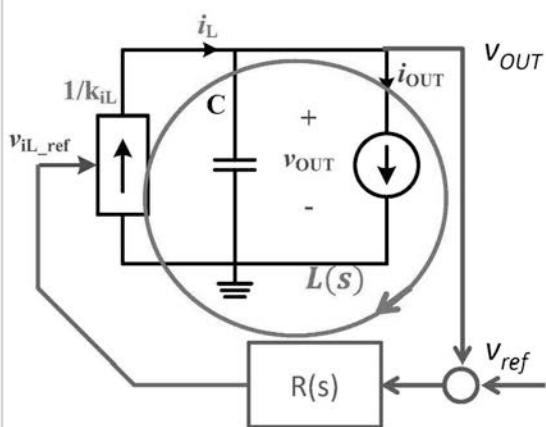


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VOLTAGE CONTROLLER DESIGN: INFLUENCE ON OUTPUT IMPEDANCE

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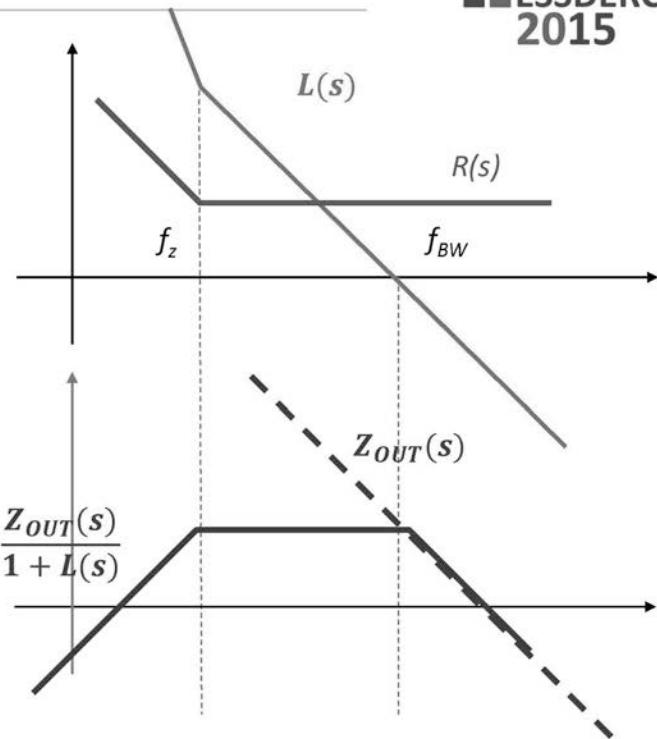
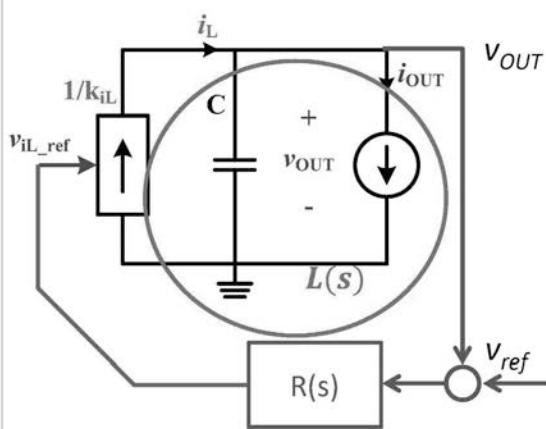


Easy to shape the closed loop output impedance

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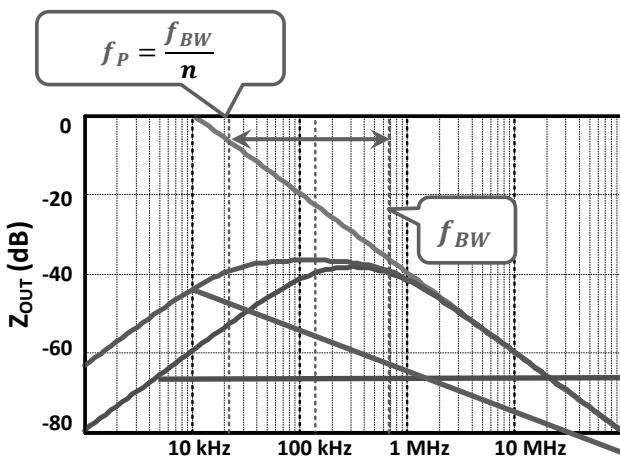
ZERO ERROR IN STEADY STATE



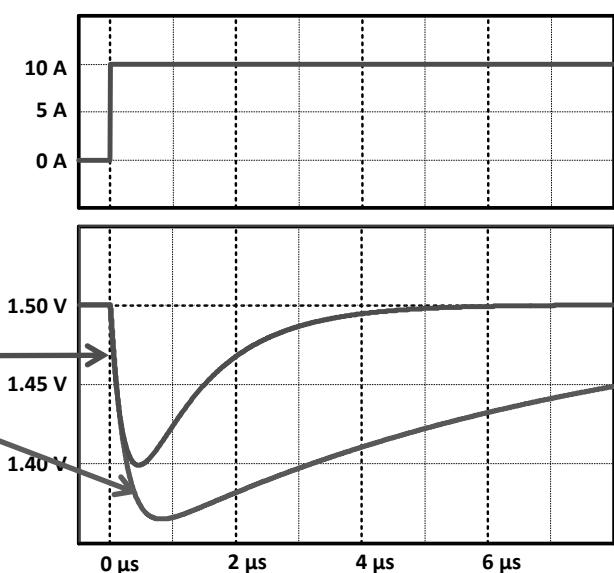
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TRANSIENT RESPONSE

$$Z_{OUT}(s) = \frac{s}{C \left(s + \frac{2\pi f_{BW}}{N} \right) (s + 2\pi f_{BW})} \quad \Delta v_{OUT}(t) = -\Delta I \frac{N}{(N-1)C2\pi f_{BW}} (e^{-\frac{2\pi f_{BW} t}{N}} - e^{-2\pi f_{BW} t}) h(t)$$



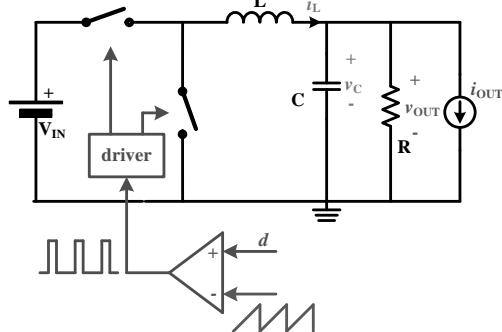
The bigger the robustness the slower the response



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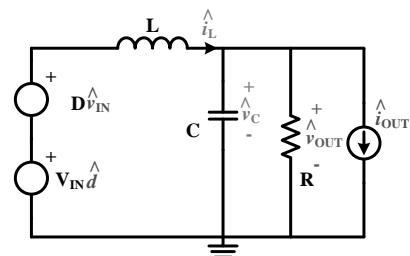
- Review of basic concepts
 - Current Mode Control
 - Voltage Mode Control
 - Robustness to C_{out} variation
 - Ripple based controls
 - V^1 Concept
 - Modeling techniques
 - Conclusions

VOLTAGE MODE CONTROL



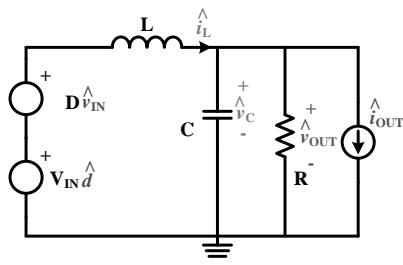
Converter example

V_{IN}	5 V
V_{OUT}	1.5 V
L	100 nH
C	15 μ F
f_{sw}	5 MHz
R	0.1 Ω

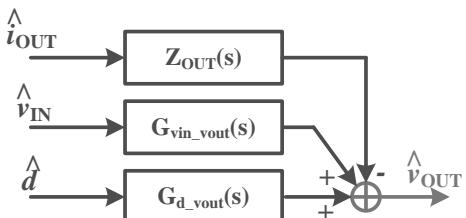


R. W. Ericson and D. Maksimović, "Fundamentals of Power Electronic", second edition, University of Colorado, Boulder, Colorado

VMC MODEL: OPEN-LOOP TRANSFER FUNCTIONS



Transfer Functions



State-space equations

$$\frac{d}{dt} \hat{i}_L = \frac{D}{L} \hat{v}_{in} + \frac{V_{IN}}{L} \hat{d} - \hat{v}_c$$

$$\frac{d}{dt} \hat{v}_c = \frac{R}{1+sC} \hat{i}_L - \frac{R}{1+sC} \hat{i}_{OUT}$$

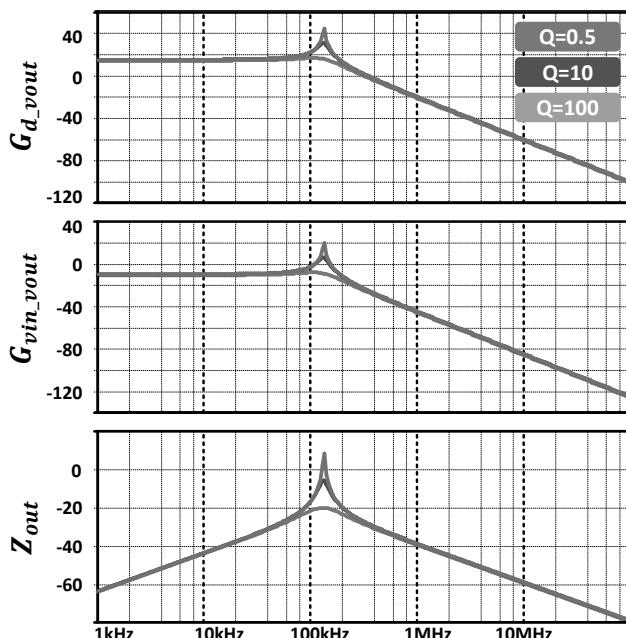
$$G_{d_vout} = \frac{\hat{v}_{out}}{\hat{d}} = \frac{V_{IN}}{1 + s \frac{L}{R} + s^2 LC}$$

$$G_{vin_vout} = \frac{\hat{v}_{out}}{\hat{v}_{in}} = \frac{D}{1 + s \frac{L}{R} + s^2 LC}$$

$$Z_{out} = -\frac{\hat{v}_{out}}{\hat{i}_{out}} = \frac{sL}{1 + s \frac{L}{R} + s^2 LC}$$

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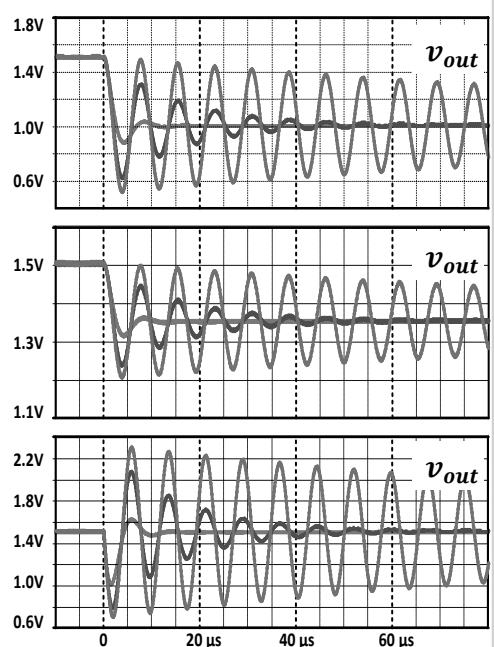
VMC MODEL: OPEN-LOOP TRANSFER FUNCTIONS



$\Delta d = -0.1$

$\Delta v_{IN} = -0.5V$

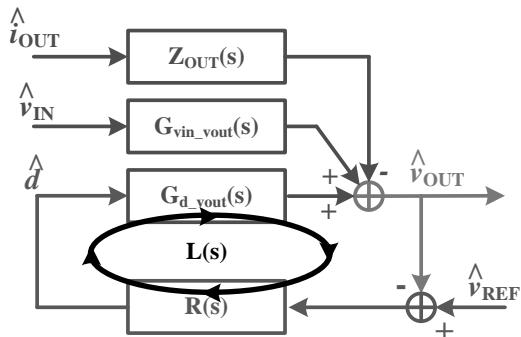
$\Delta i_{OUT} = 10A$



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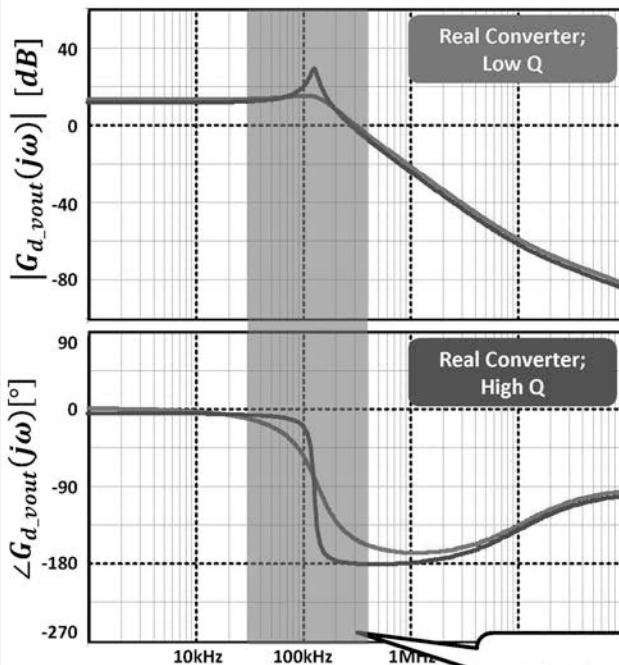
CLOSING THE CONTROL LOOP

Transfer Functions

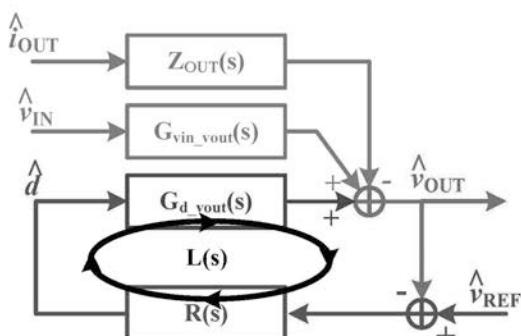


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CLOSING THE CONTROL LOOP



Transfer Functions

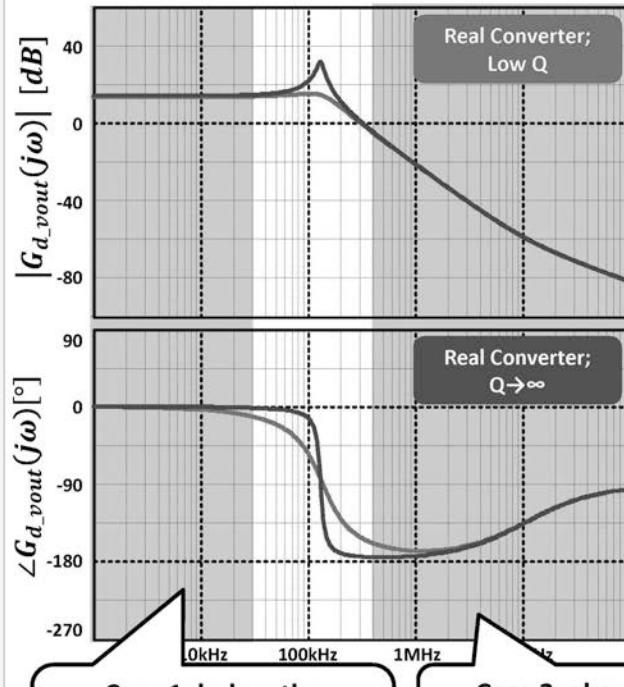


Where to close the Loop?

Big Phase Variation

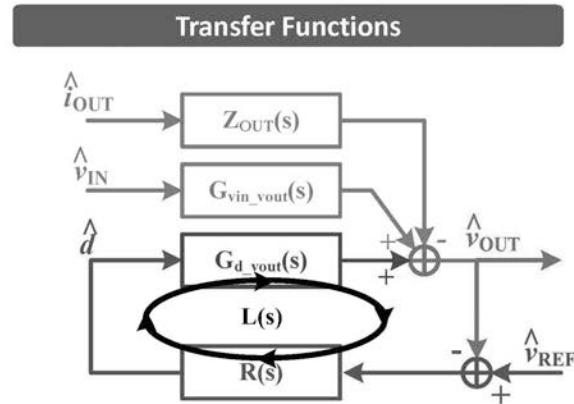
CLOSING THE CONTROL LOOP

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ESSDERC
2015



Case 1: below the resonance – $BW < f_{RES}/(Q \cdot GM)$

Case 2: above the resonance – $BW > 4f_{RES}$

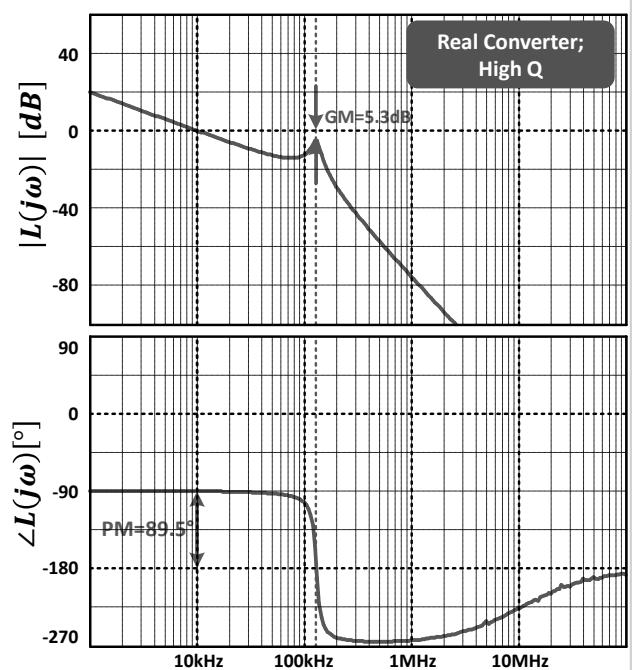
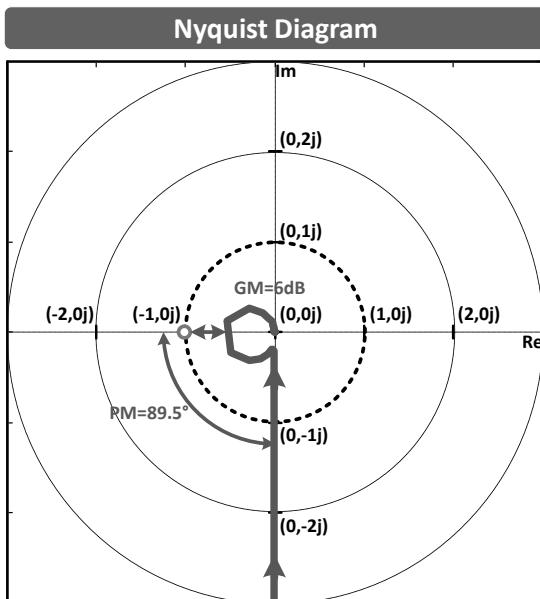


BUT: $BW < f_{SW}/5$

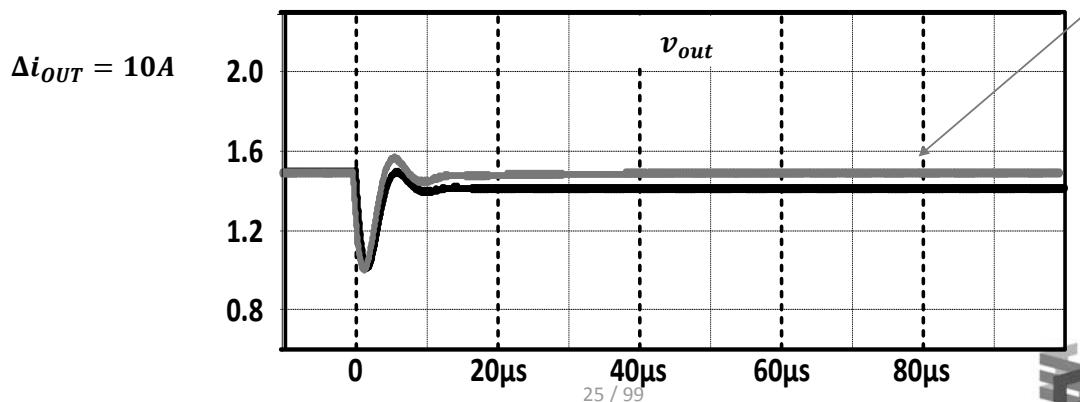
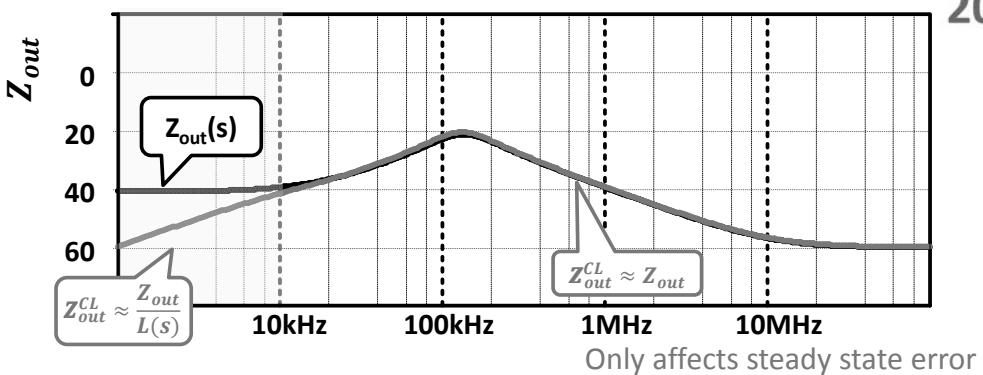
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CASE 1: CLOSING THE LOOP BELOW THE RESONANCE

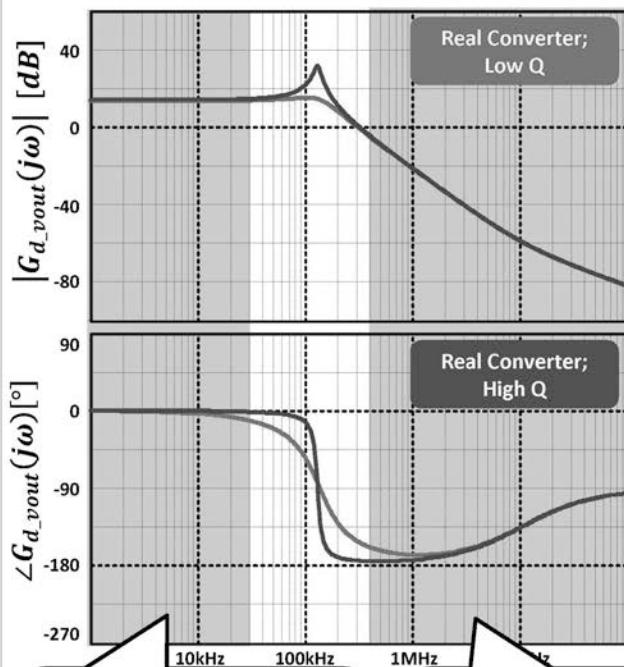
ESSCIRC
ESSDERC
2015



CASE 1: CLOSED LOOP TRANSFER FUNCTIONS: LOW Q

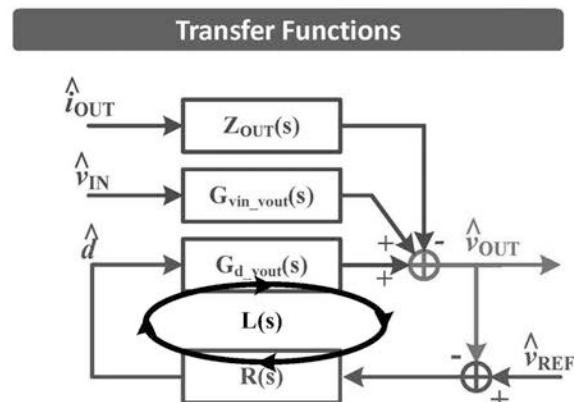


CLOSING THE CONTROL LOOP



Case 1: below the resonance – $BW < f_{RES}/4$

Case 2: above the resonance – $BW > 4f_{RES}$



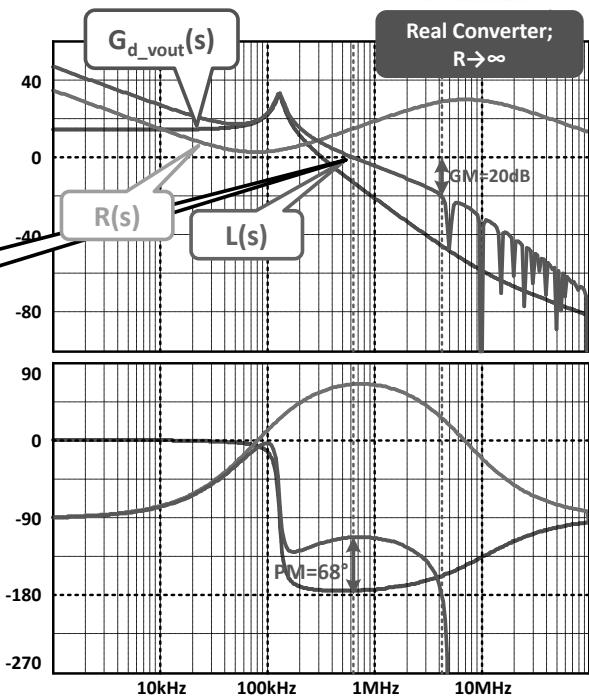
BUT: $BW < f_{SW}/5$

CASE 2: CLOSING THE LOOP ABOVE THE RESONANCE

Example BW = 700 kHz
 $f_{RES} = 130$ kHz , $f_{SW} = 5$ MHz

$$R(s) = \frac{A_0 \left(1 + \frac{s}{z}\right)^2}{s \left(1 + \frac{s}{p}\right)^2}$$

Type III Regulator



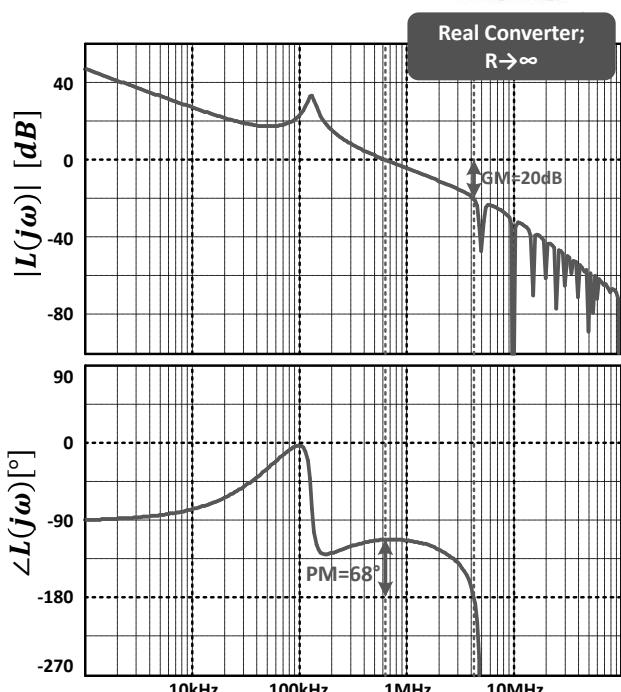
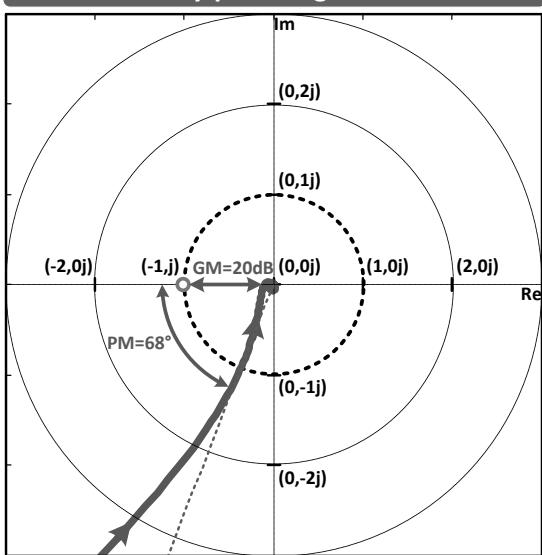
Venable, H. Dean. "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis." Proc. Powercon 10. 1983. San Diego, CA, pp. H1-1 to H1-12.



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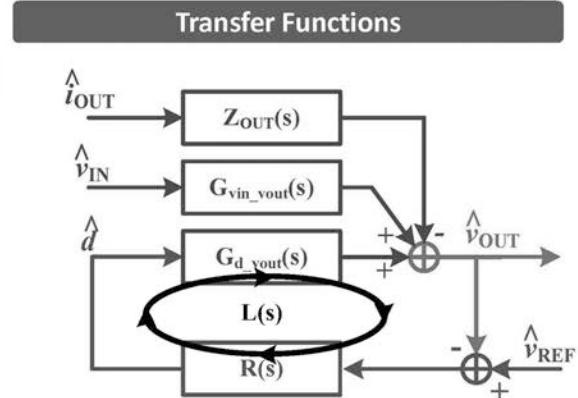
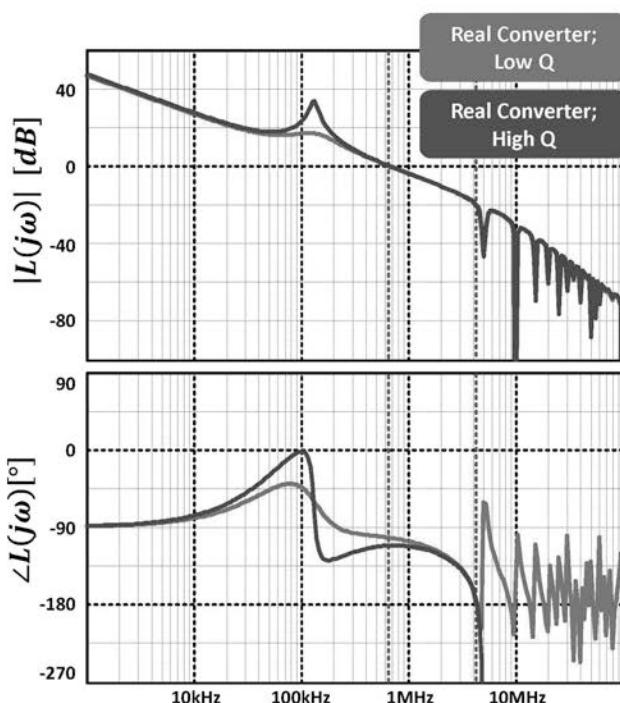
CASE 2: CLOSING THE LOOP ABOVE THE RESONANCE

Nyquist Diagram



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CASE 2: CLOSING THE LOOP ABOVE THE RESONANCE



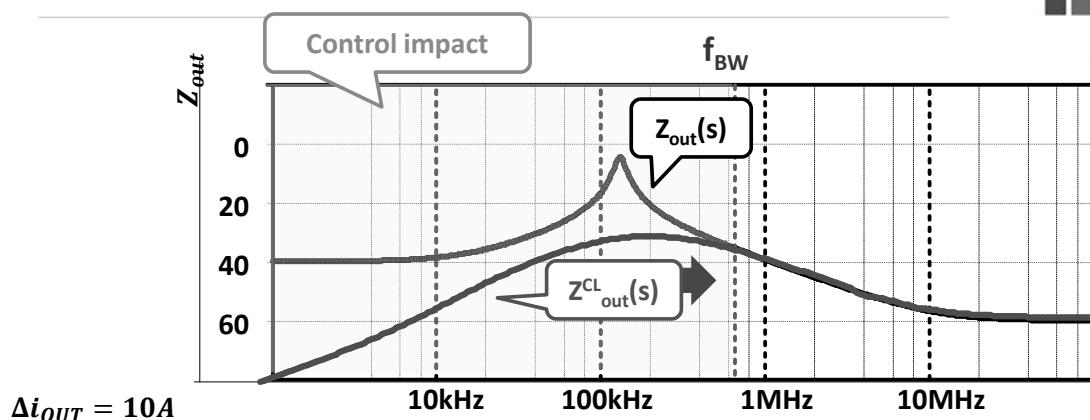
$$G_{vref_vout} = \frac{\hat{v}_{out}}{\hat{v}_{ref}} = \frac{L(s)}{1 + L(s)}$$

$$G_{vin_vout}^{CL} = \frac{\hat{v}_{out}}{\hat{v}_{in}} = \frac{G_{vin_vout}}{1 + L(s)}$$

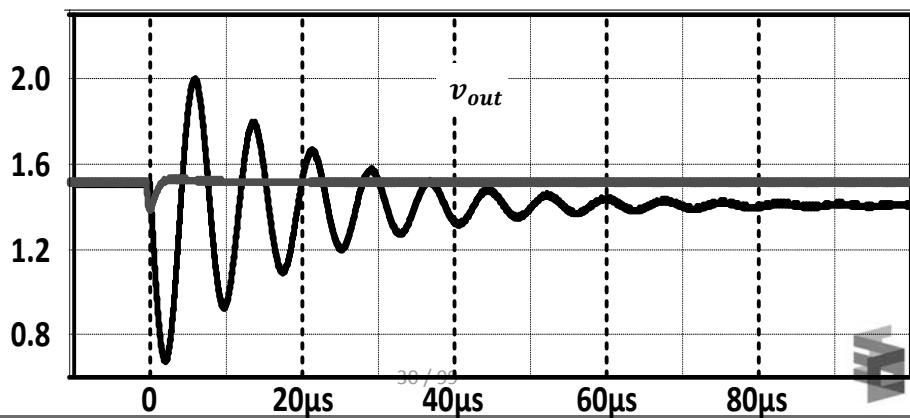
$$Z_{out}^{CL} = -\frac{\hat{v}_{out}}{\hat{i}_{out}} = \frac{Z_{out}}{1 + L(s)}$$

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CASE 2: CLOSED LOOP TRANSFER FUNCTIONS: $R \rightarrow \infty$



$$\Delta i_{OUT} = 10A$$

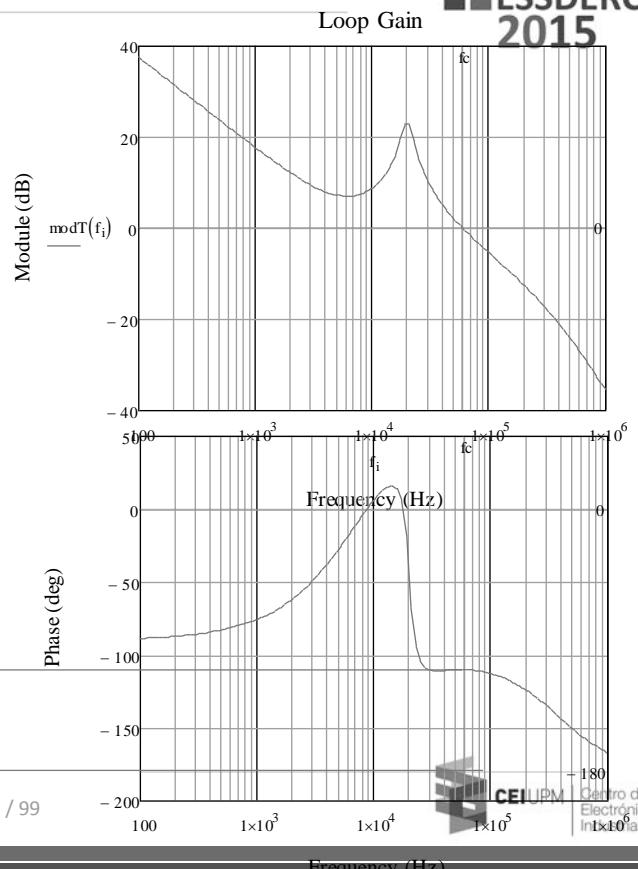
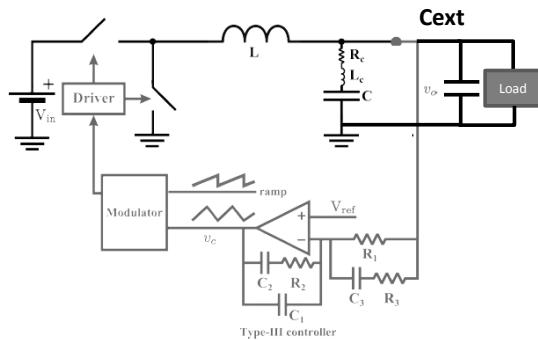


60'

- Review of basic concepts
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 - Conclusions

SENSITIVITY TO C_{out} VARIATION

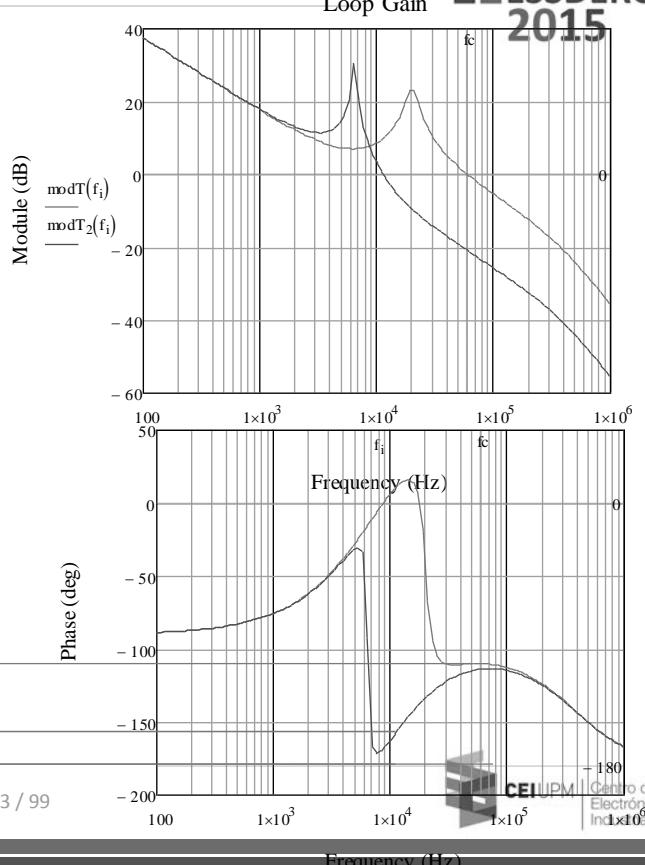
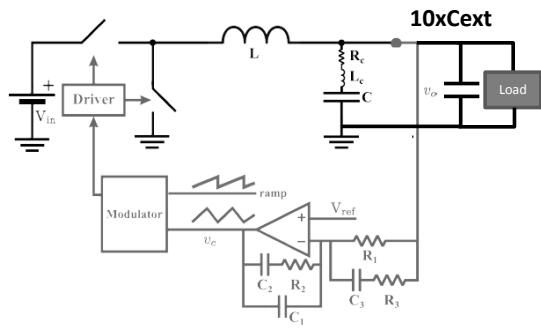
■ Voltage mode control



SENSITIVITY TO C_{OUT} VARIATION

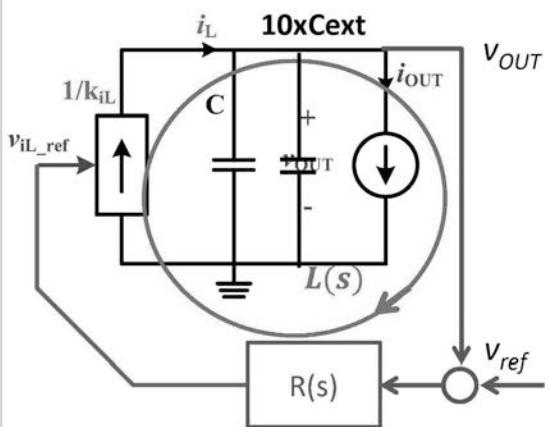
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ESSDERC
2015

- Voltage mode control

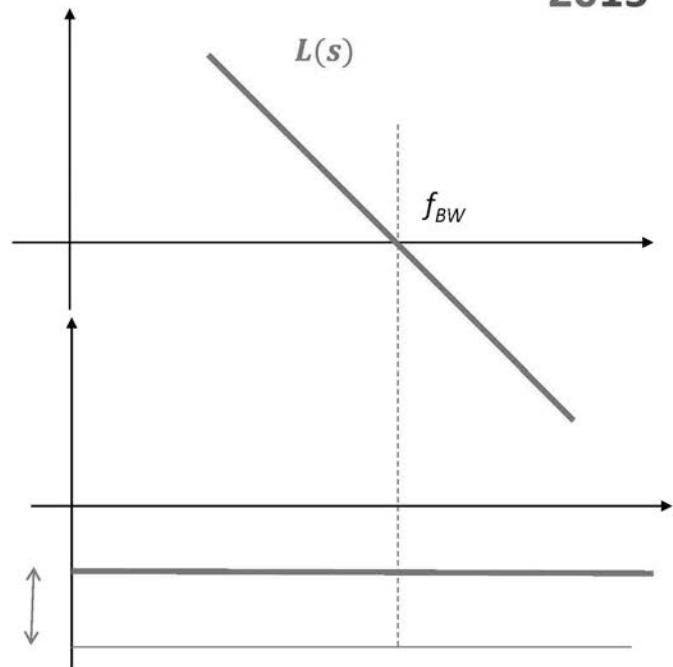


SENSITIVITY FOR CURRENT MODE CONTROL

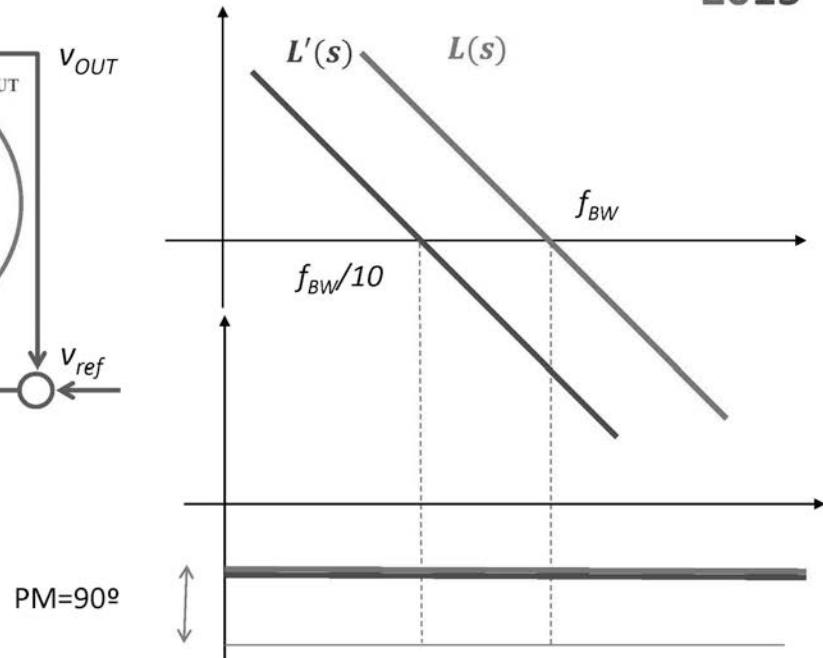
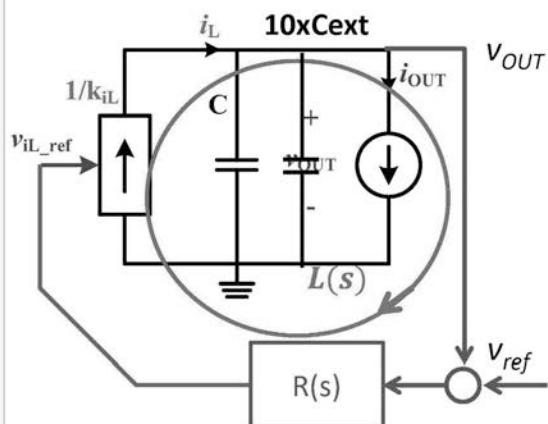
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ESSDERC
2015



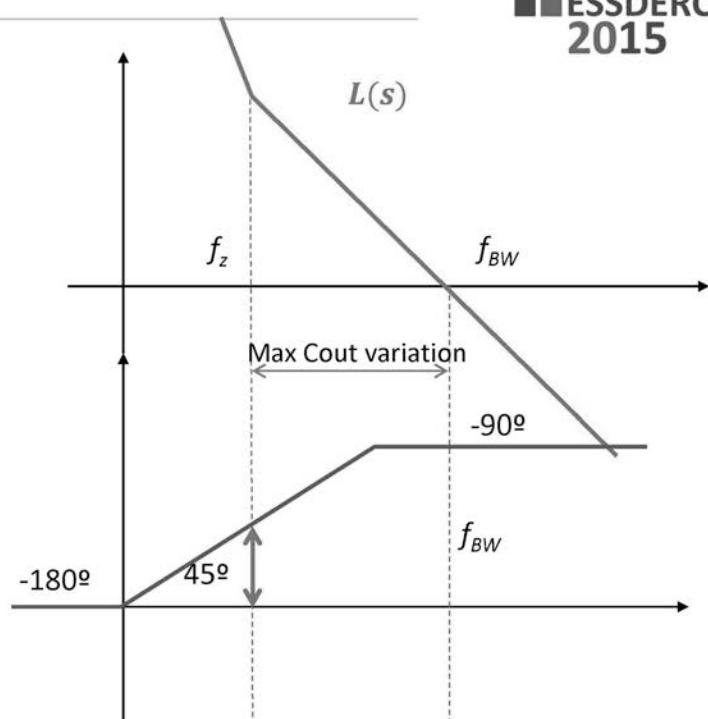
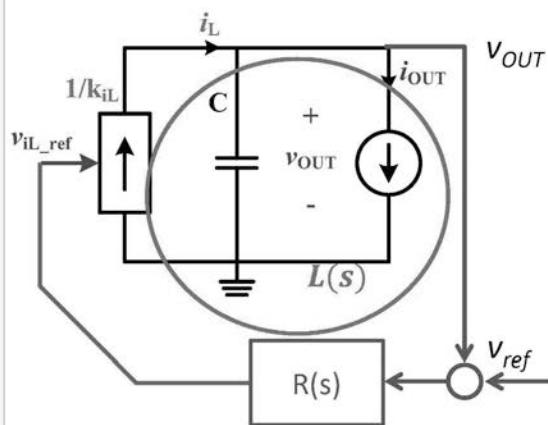
PM = 90°



SENSITIVITY FOR CURRENT MODE CONTROL



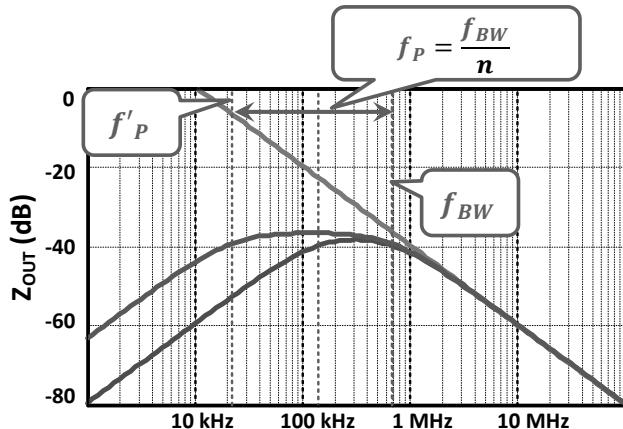
SENSITIVITY TO C_{OUT} VARIATION



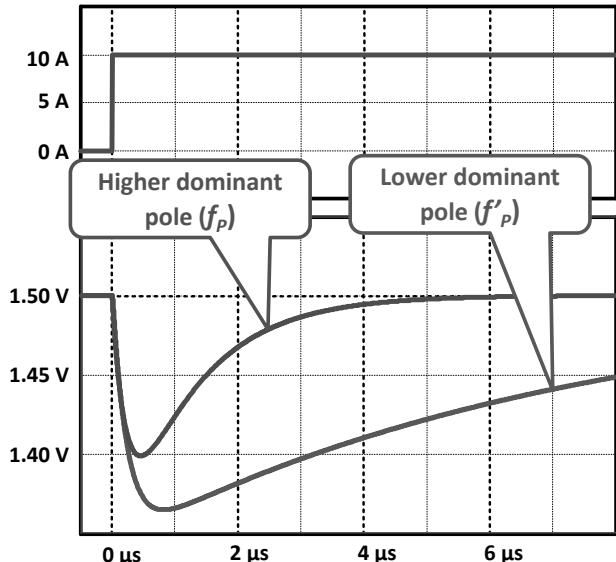
TRADE-OFF SENSITIVITY/TRANSIENT RESPONSE

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$$Z_{OUT}(s) = \frac{s}{C \left(s + \frac{2\pi f_{BW}}{N} \right) (s + 2\pi f_{BW})} \quad v_{OUT}(t) = V_{REF} - \frac{N \Delta I}{(N-1)C 2\pi f_{BW}} (e^{-\frac{2\pi f_{BW} t}{N}} - e^{-2\pi f_{BW} t}) h(t)$$



The bigger the robustness the slower the response



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OUTLINE

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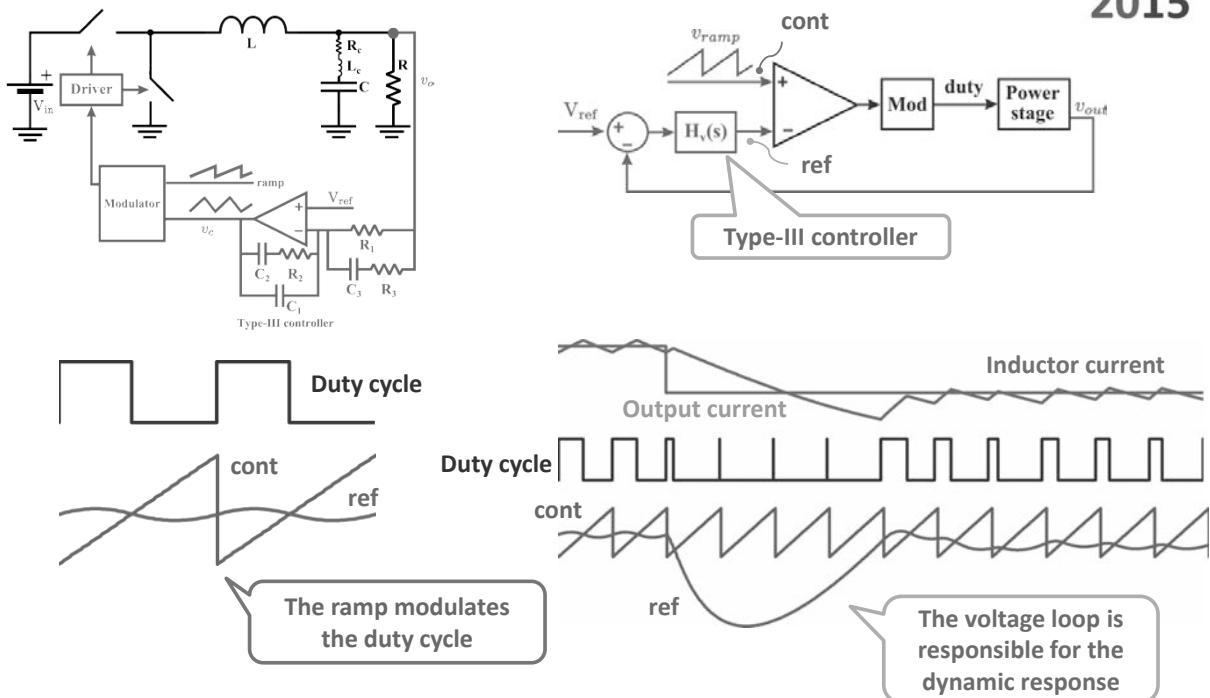
60'

- Review of basic concepts
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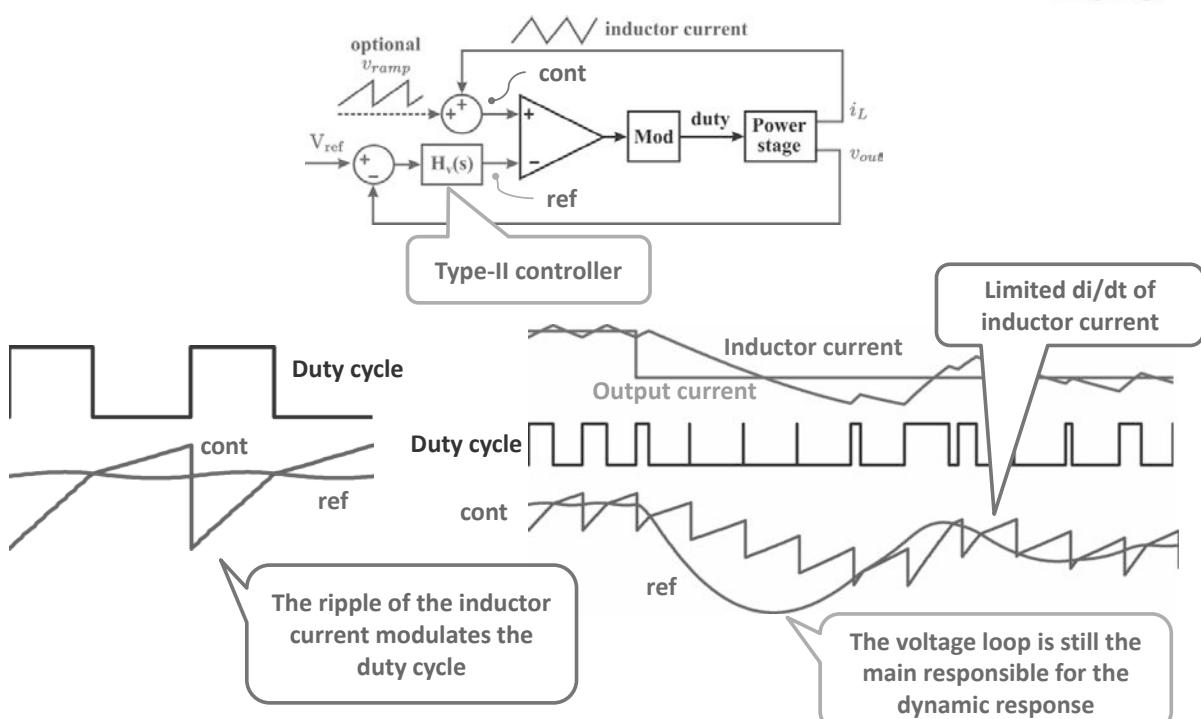
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VOLTAGE MODE CONTROL

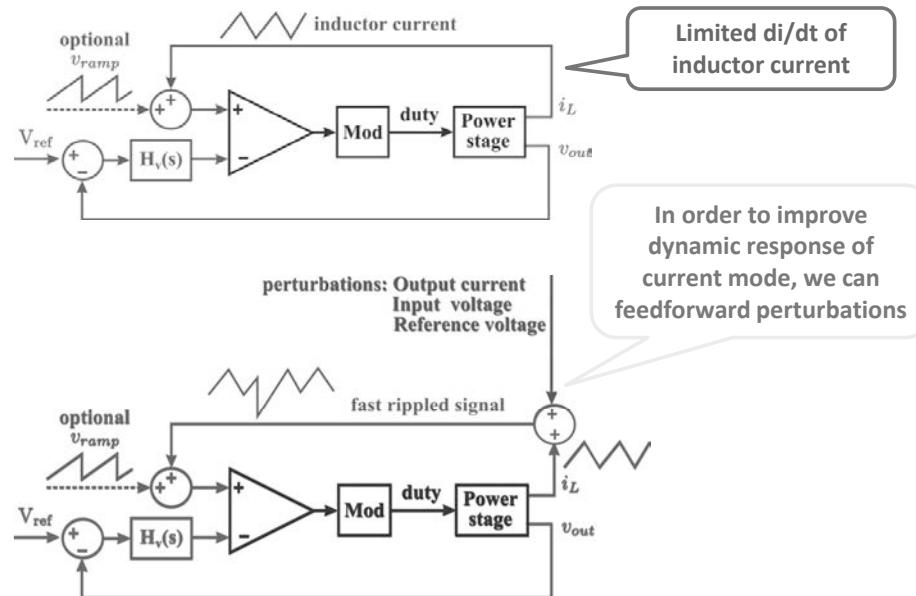


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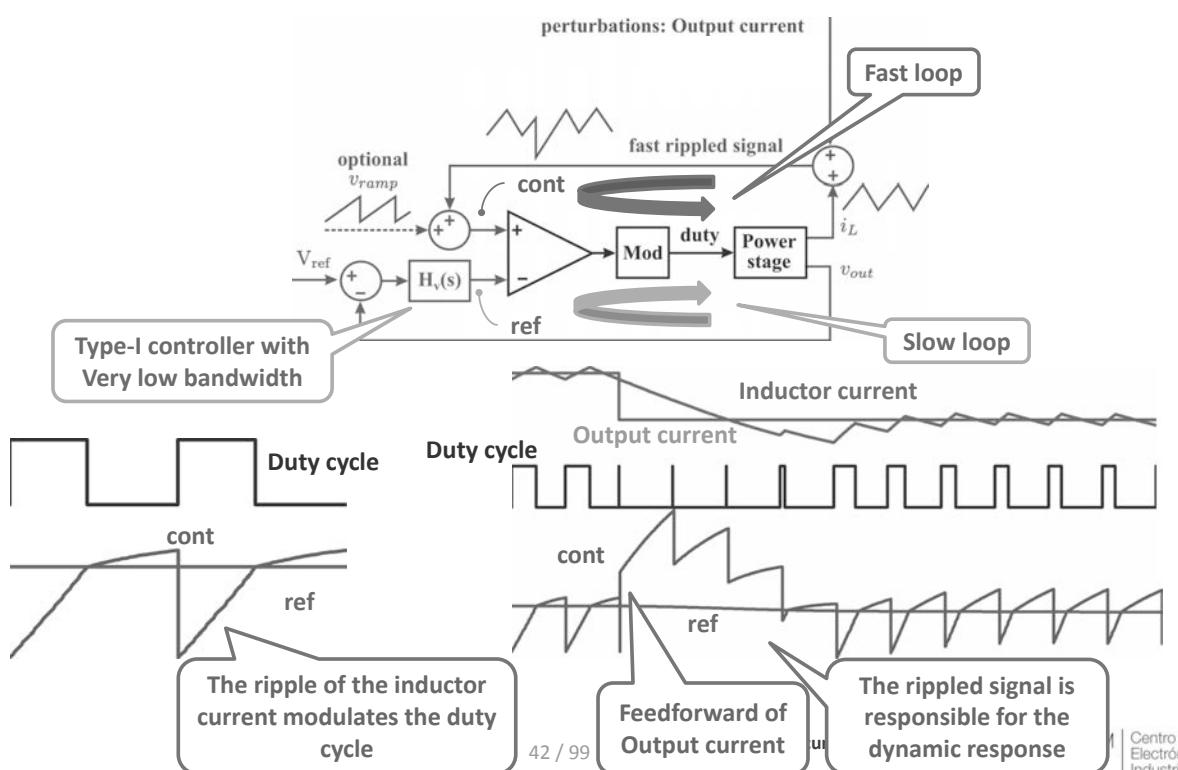
CURRENT MODE CONTROL



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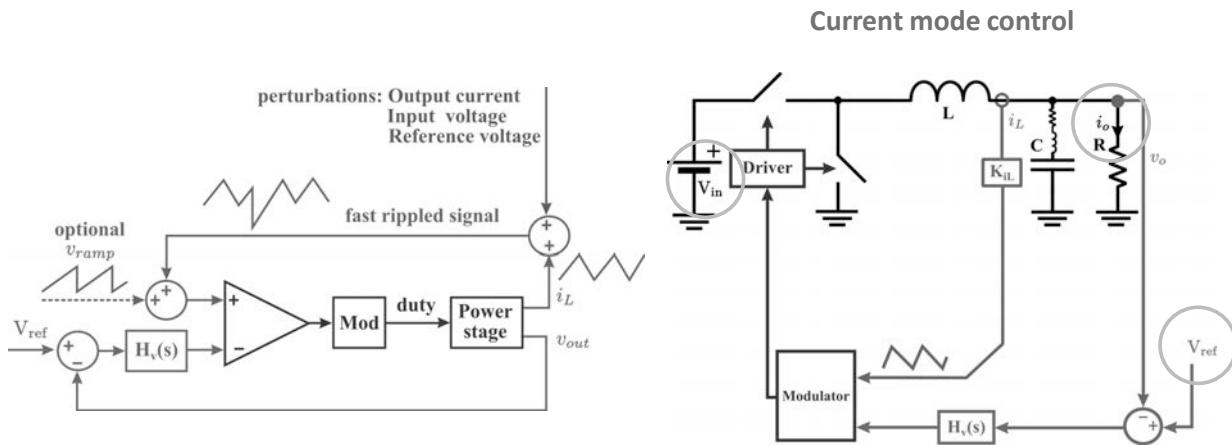


ADVANCED CONTROL TECHNIQUES: FEEDFORWARD OF I_{OUT}



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In current mode control, we have feedback of:

- Output voltage
- Inductor current

The perturbations are:

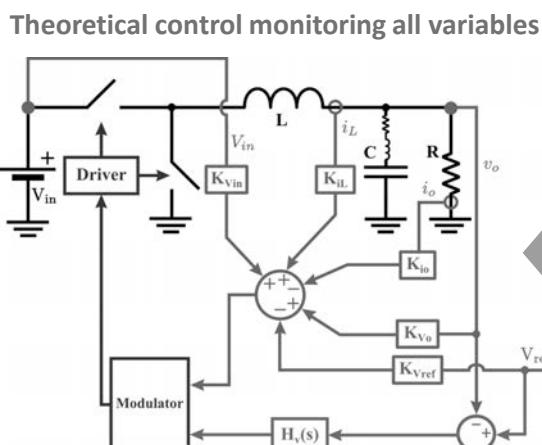
- Input voltage
- Reference voltage
- Output current

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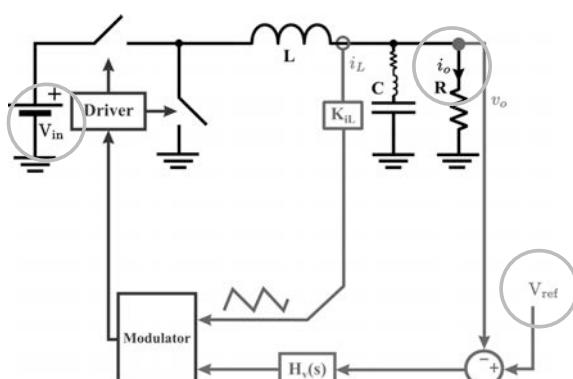
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Current mode control



In current mode control, we have feedback of:

- Output voltage
- Inductor current

The perturbations are:

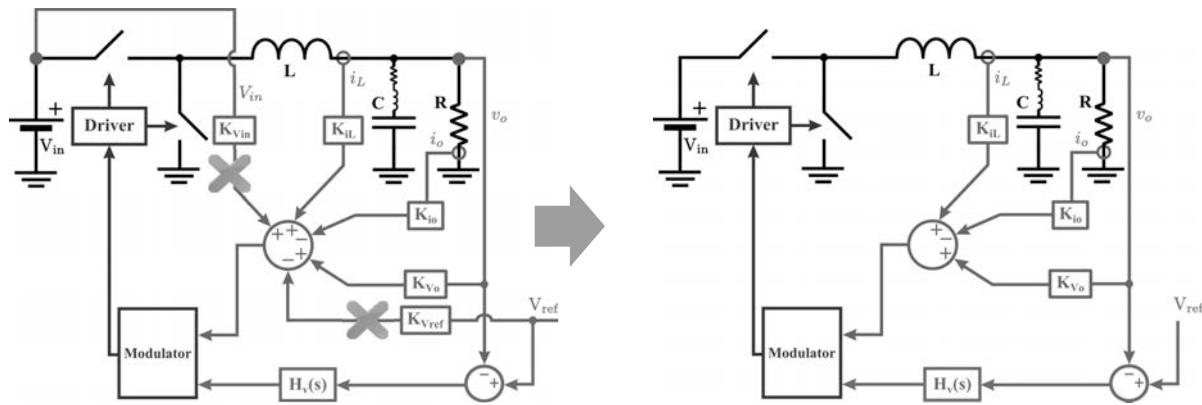
- Input voltage
- Reference voltage
- Output current

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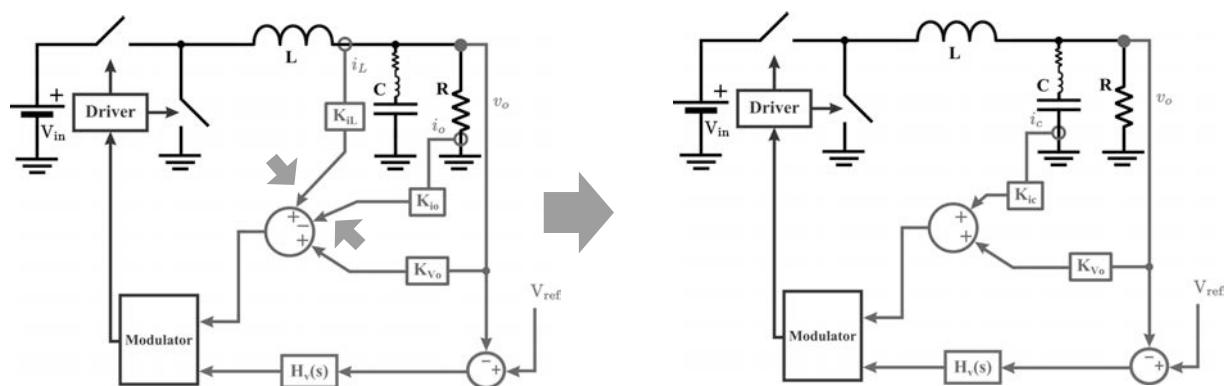
- Feedforward of input voltage normally not needed
- Feedforward of reference voltage only needed for dynamic voltage scaling

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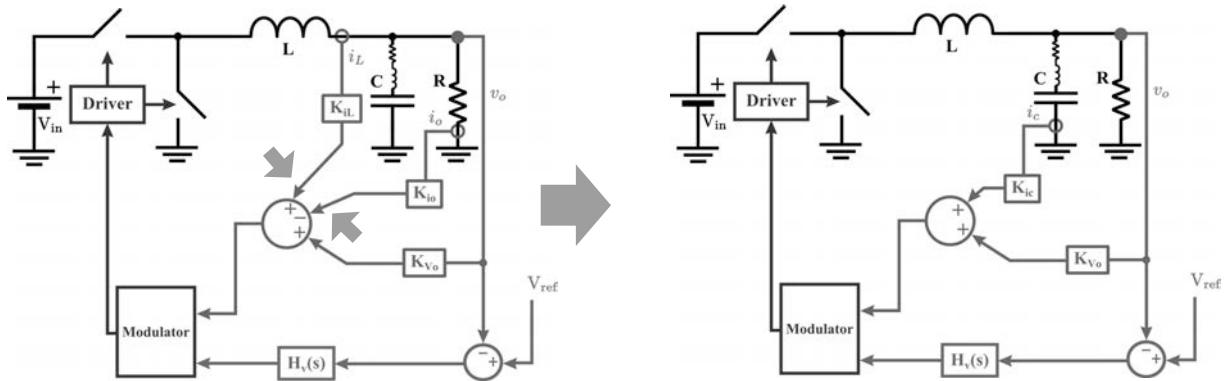
We can group together the inductor current and output current, by using the capacitor current...
...at the expense of one degree of freedom

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HOW TO CREATE RIPPLE-BASED CONTROLS

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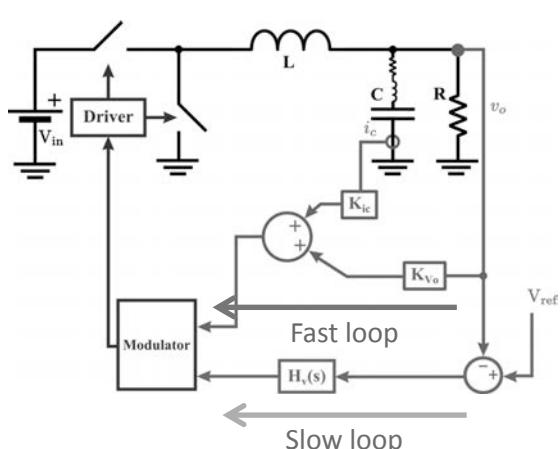
We can group together the inductor current and output current, by using the capacitor current

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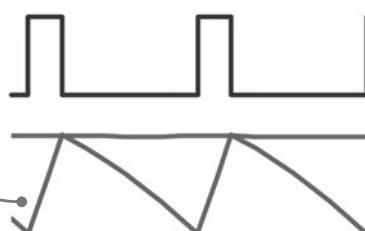


Fast loop:

- Responsible for fast dynamic response

Slow loop:

- Responsible to regulate tightly the output voltage.
- Very low bandwidth



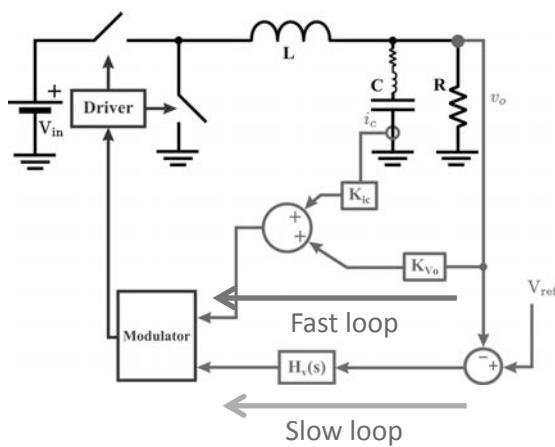
In steady-state, it behaves like a current mode control

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HOW TO CREATE RIPPLE-BASED CONTROLS

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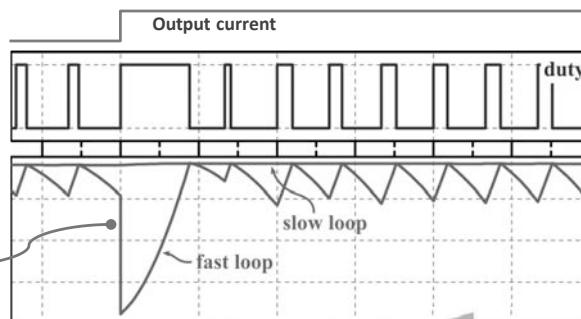
Due to feedforward of output current

Fast loop:

- Responsible for fast dynamic response

Slow loop:

- Responsible to regulate tightly the output voltage.
- Very low bandwidth



In load perturbances, the feedforward of the output current allows for a fast dynamic response

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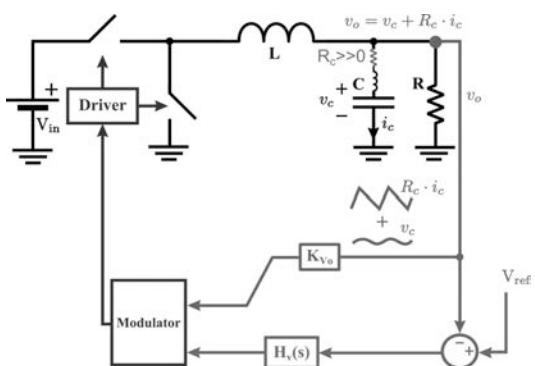
HOW TO CREATE RIPPLE-BASED CONTROLS

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How can we measure the capacitor current?

If the ESR of the output capacitor is high, we don't need to!

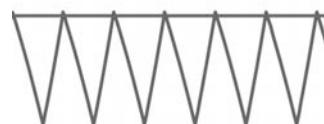
V^2 control



Duty cycle

Inductor current

$$K_{vo} v_o = K_{vo} R_c i_c + K_{vo} v_c$$



For high ESR caps, by only measuring the output voltage, we have feedforward of the output current...
... at the expense of one degree of freedom less



[] D. Goder and W. R. Pelletier, "V2 architecture provides ultra-fast transient response in switch mode power supplies," presented at the Proc. HFPC, 1996, pp. 19–23.



[] ON Semiconductor, "Theory of Operation of V2 Controllers," Application note AND8276

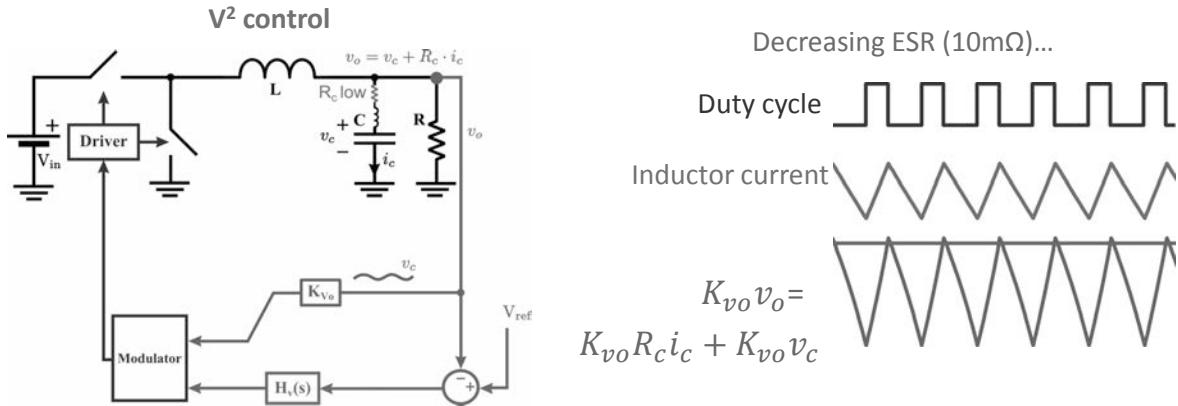
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HOW TO CREATE RIPPLE-BASED CONTROLS

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How can we measure the capacitor current?

But CAREFUL: For lower values of ESR, the feedforward of the output current is limited and sub-harmonic oscillations can appear!!



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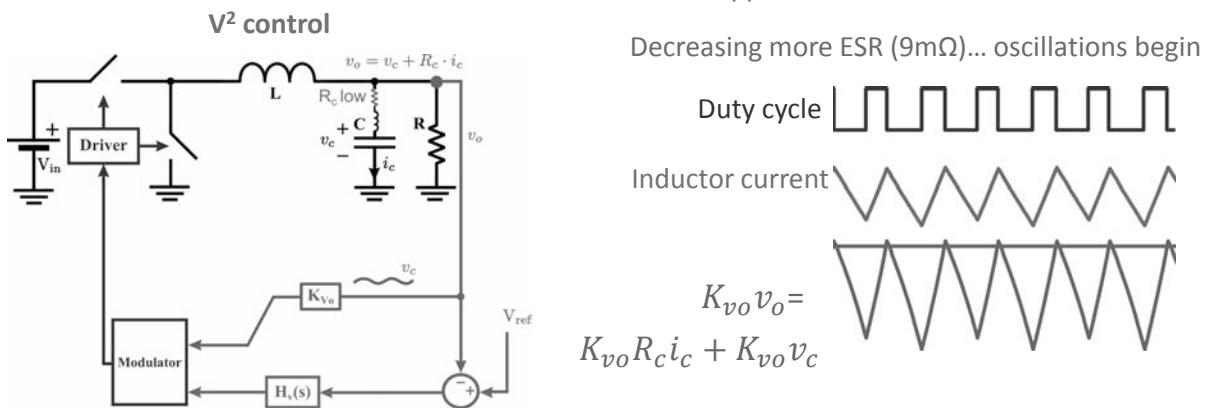
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HOW TO CREATE RIPPLE-BASED CONTROLS

**ESSCIRC
ESSDERC
2015**

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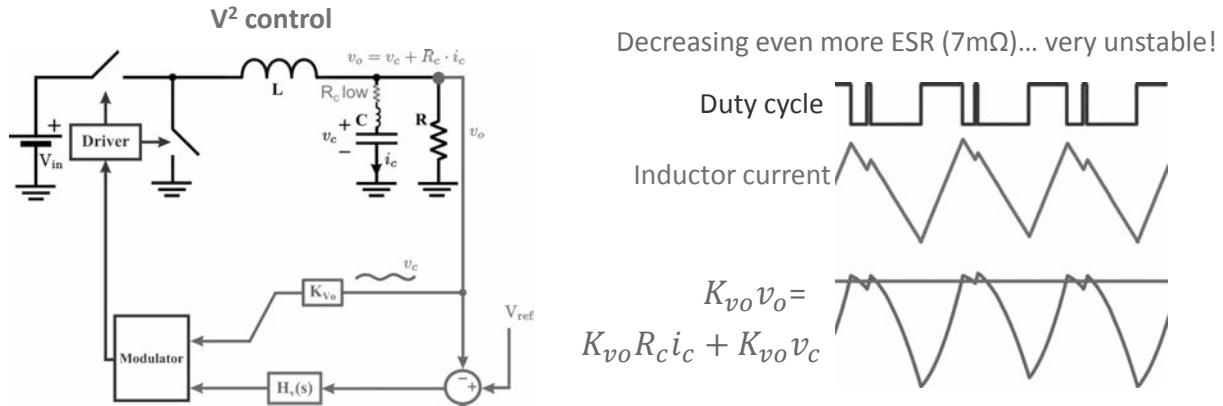
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HOW TO CREATE RIPPLE-BASED CONTROLS

**ESSCIRC
ESSDERC
2015**

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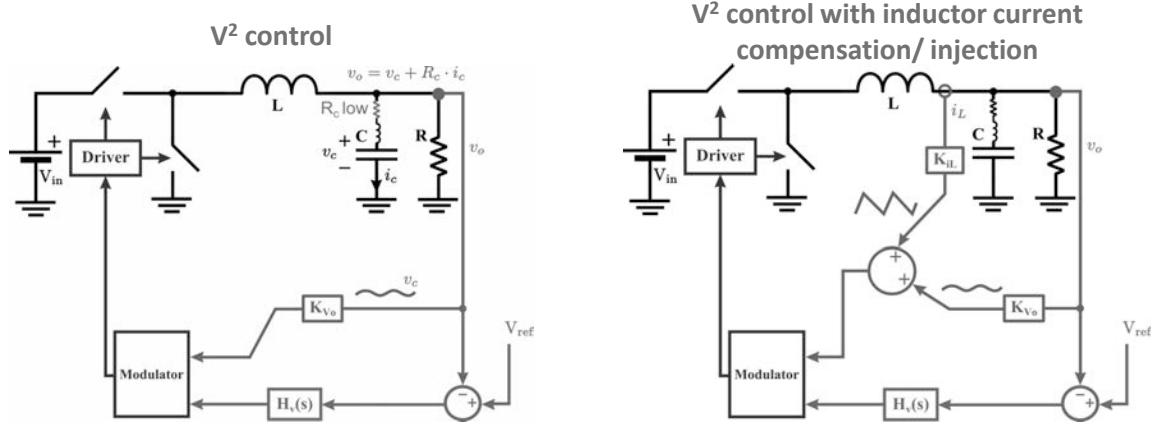
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HOW TO CREATE RIPPLE-BASED CONTROLS

**ESSCIRC
ESSDERC
2015**

How can we measure the capacitor current?

In order to avoid sub-harmonic oscillation for low ESR caps, compensation is needed



Inductor current can be added to
compensate
... but feedforward of output current is
limited



[] W. Huang, "A new control for multi-phase buck converter with fast transient response," in *Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2001. APEC 2001*, 2001, vol. 1, pp. 273–279 vol.1.



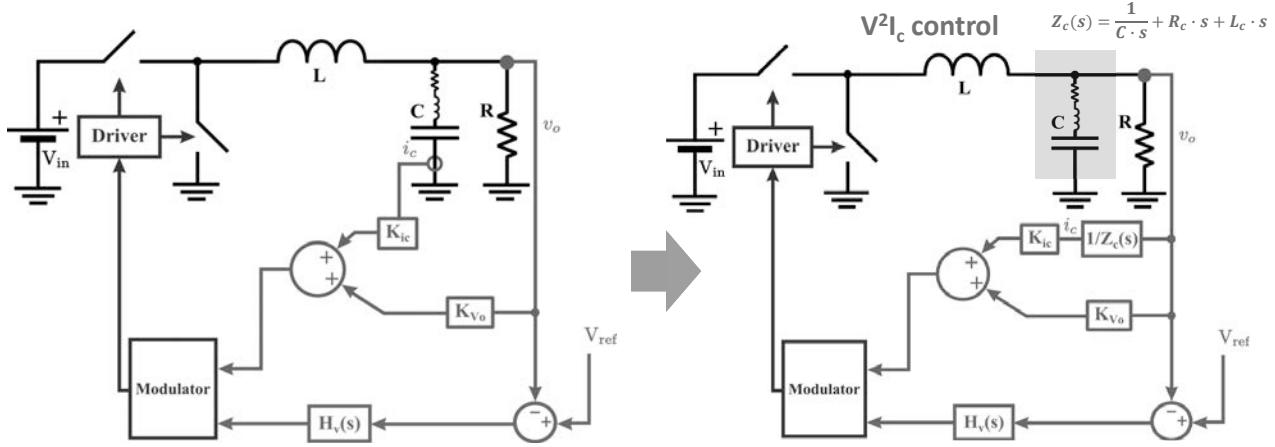
[] "D-CAP™ Mode With All-Ceramic Output Capacitor Application," Application Report SLVA453.

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HOW TO CREATE RIPPLE-BASED CONTROLS

How can we measure the capacitor current?

If the ESR of the cap is not dominant, it is better to remotely sense the capacitor current



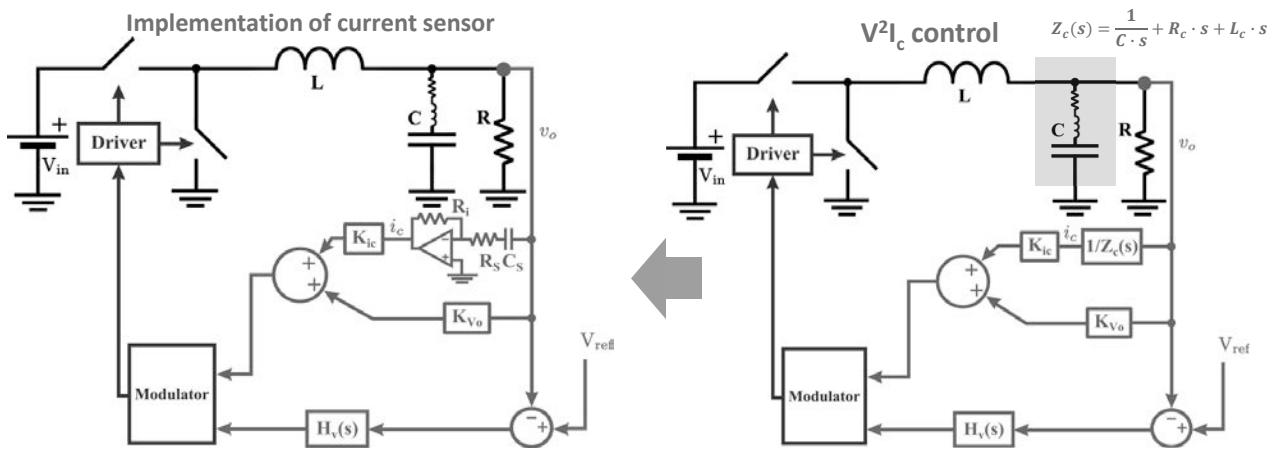
[] M. Del Viejo, P. Alou, J. A. Oliver, O. Garcia, and J. A. Cobos, "V2IC control: A novel control technique with very fast response under load and voltage steps," in 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2011, pp. 231–237.

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HOW TO CREATE RIPPLE-BASED CONTROLS

How can we measure the capacitor current?

If the ESR of the cap is not dominant, it is better to remotely sense the capacitor current

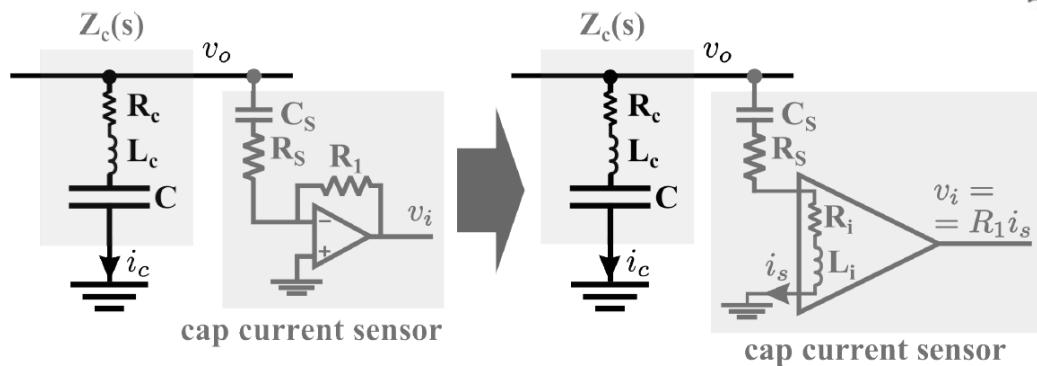


Only the output voltage is sensed

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ESTIMATING THE OUTPUT CAPACITOR CURRENT

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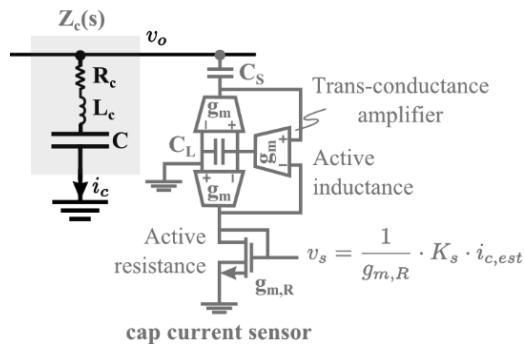
$$v_i = \frac{R_1}{n} i_c$$

$$C_s = C/n, \quad R_s + R_i = R_c \cdot n$$

$$L_i = L_c \cdot n$$

$$L_i = \frac{R_1}{w_B}; \quad R_i = \frac{R_1}{A_{DC}}$$

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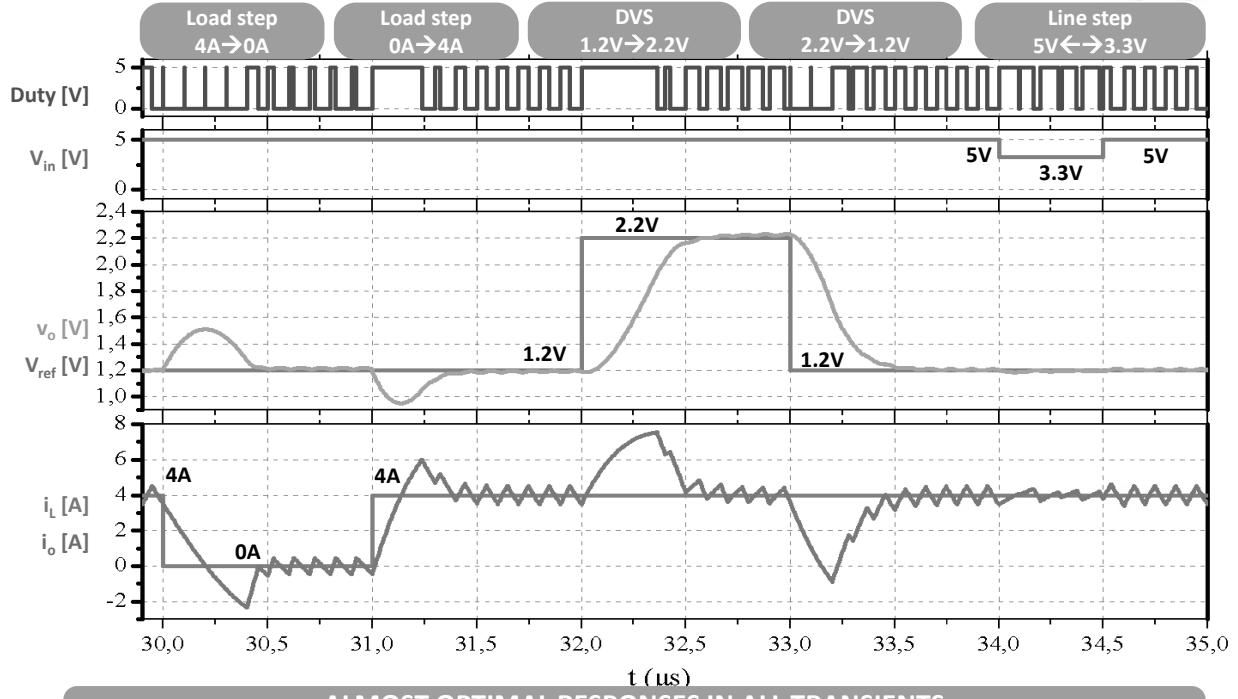
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CONTROL: $V^2 I_C$

$V^2 I_C$ control

Simplis simulation

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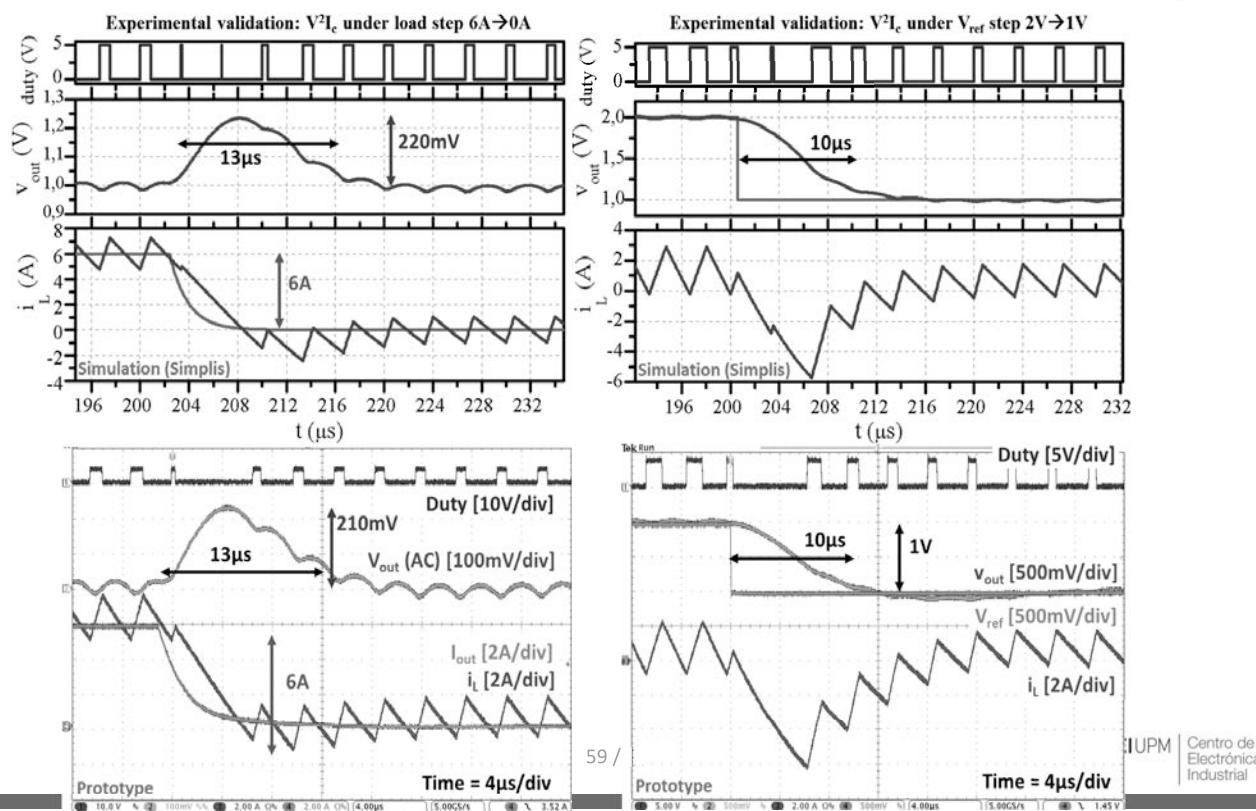


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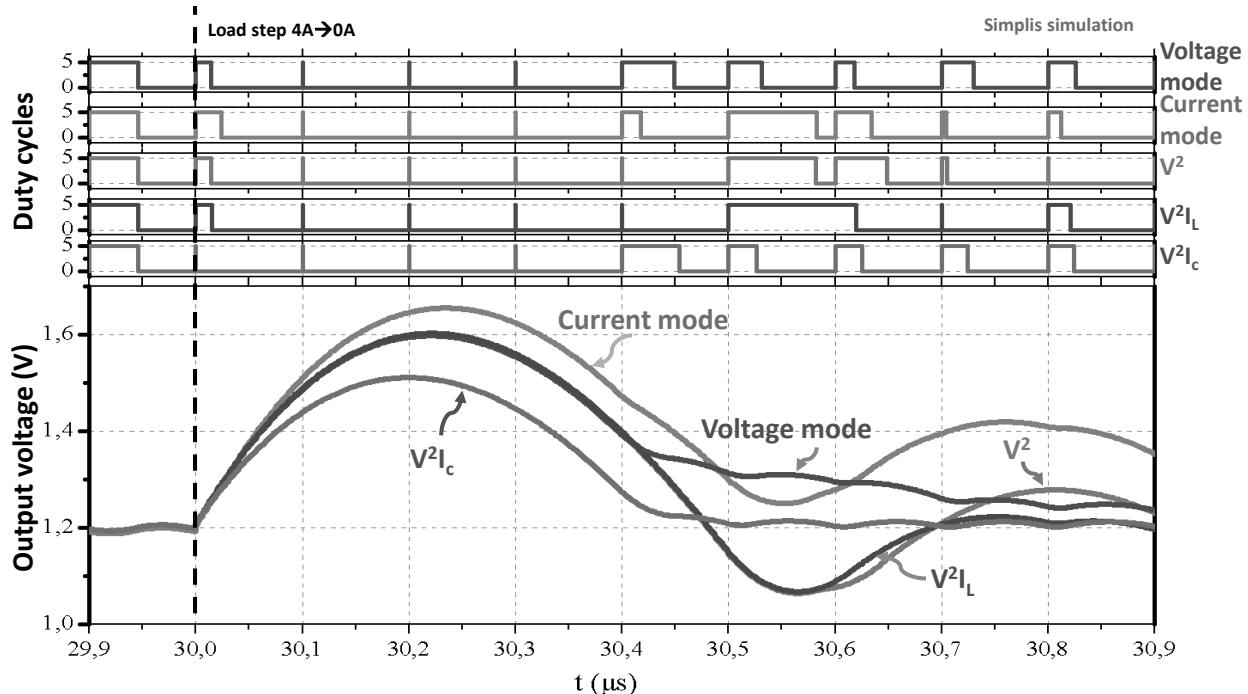
EXPERIMENTAL VALIDATION: V2IC 300KHZ

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2015**



CONTROL: COMPARISON

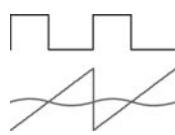
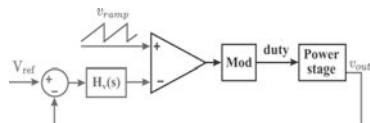
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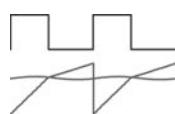
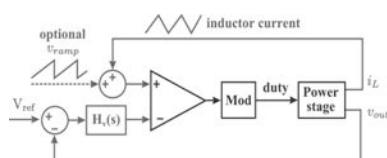
SUMMARY OF COMPARISON OF DIFFERENT CONTROL TECHNIQUES

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2015

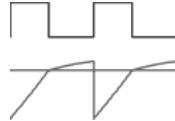
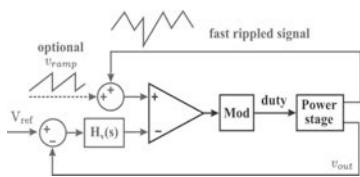
Voltage mode control



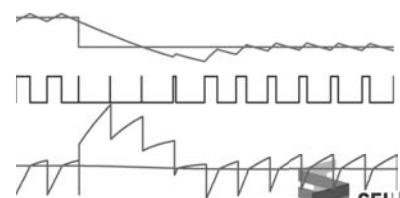
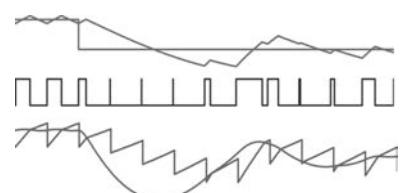
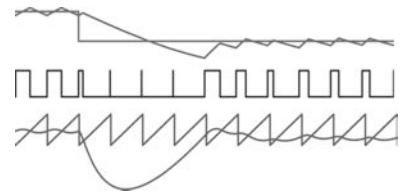
Current mode control



Ripple-based control



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OUTLINE

60'

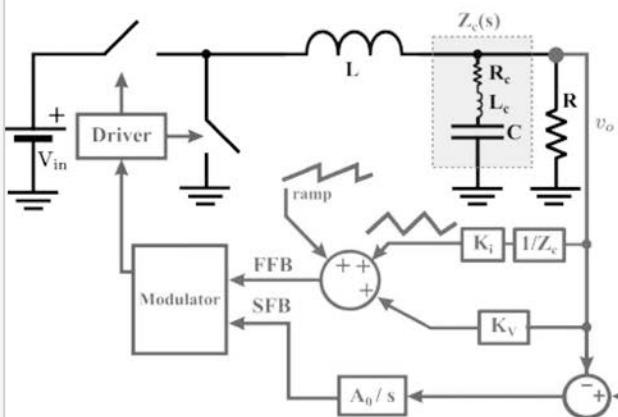
- Review of basic concepts
 - Current Mode Control
 - Voltage Mode Control
 - Robustness to C_{out} variation
- Ripple based controls
- V^1 Concept
- Modeling techniques
- Conclusions

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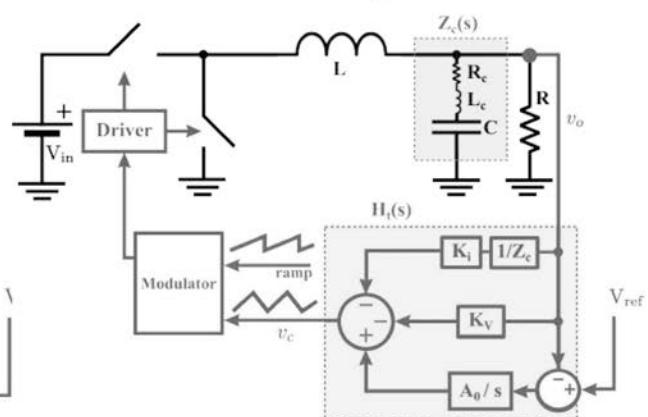
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V1 CONCEPT

V2lc



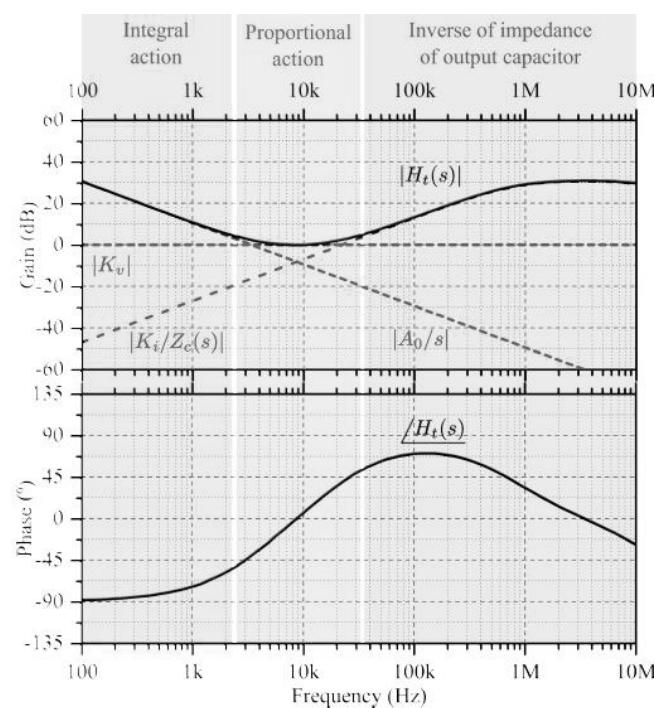
V2lc Alternative Representation



$$H_t(s) = \frac{A_0}{s} + K_v + K_i \cdot \frac{1}{Z_c(s)}$$

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V1 CONCEPT

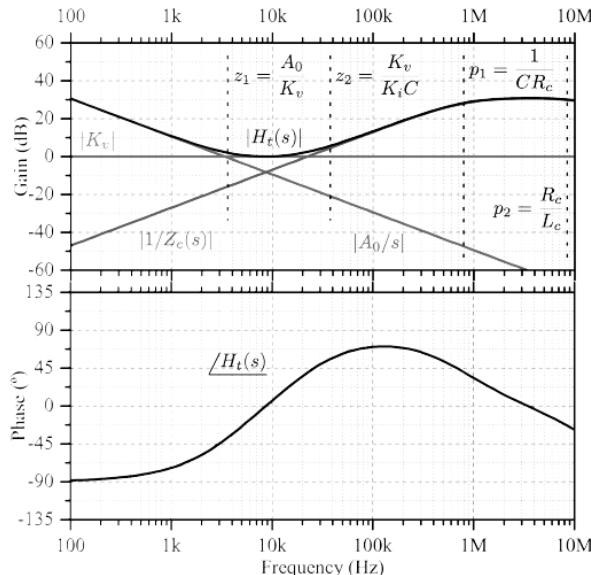


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CONTROLLER DESIGN FOR LOW AND HIGH Q OUPUT CAPACITORS

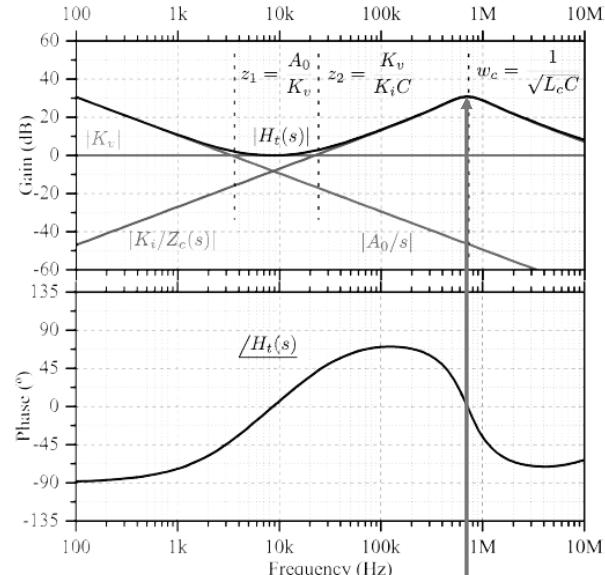
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Low Q capacitors



Can be implemented with type III controller

High Q capacitors



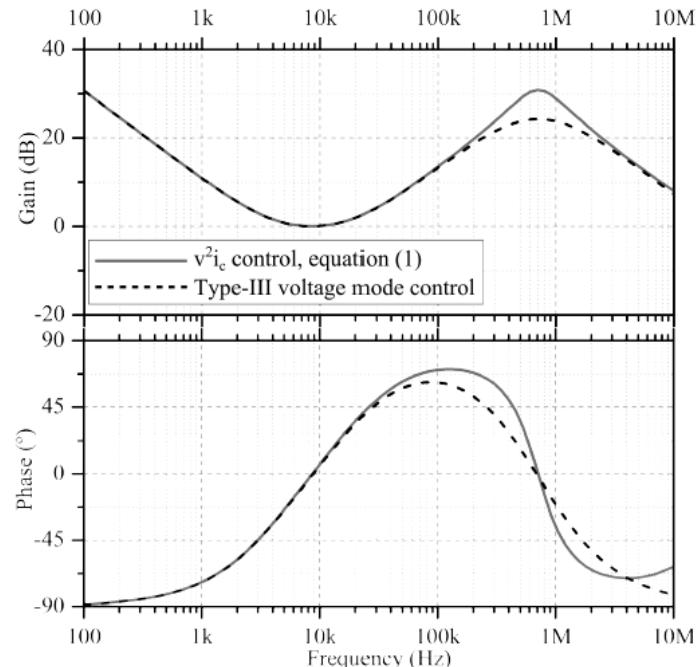
Complex conjugate poles

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COMPARISON OF V2IC VS TYPE III CONTROLLER (HIGH Q OUPUT)

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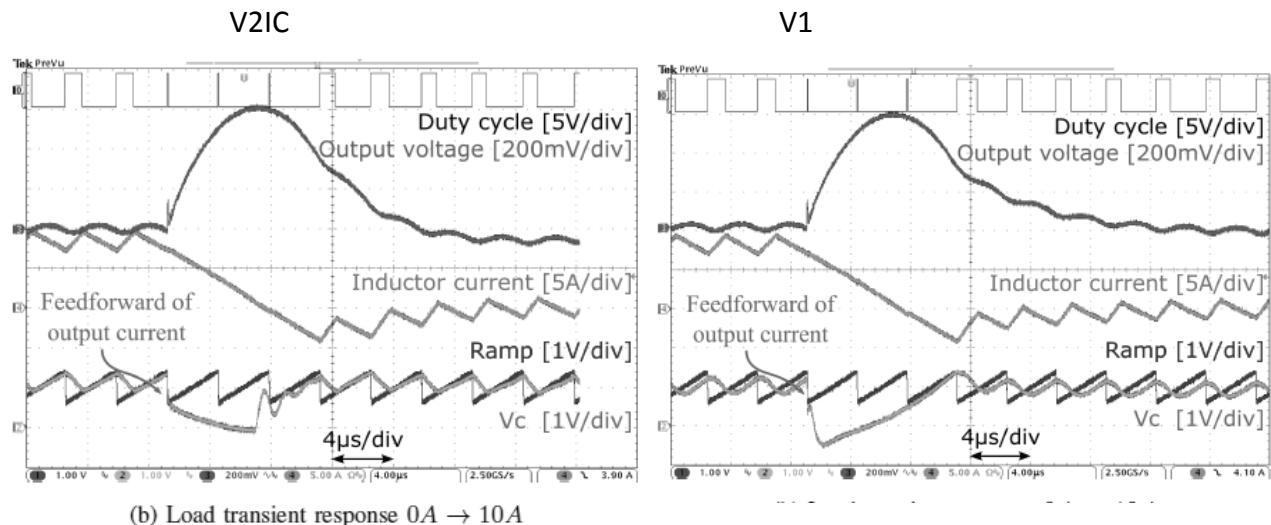


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COMPARISON OF V2IC VS TYPE III CONTROLLER (HIGH Q OUTPUT)

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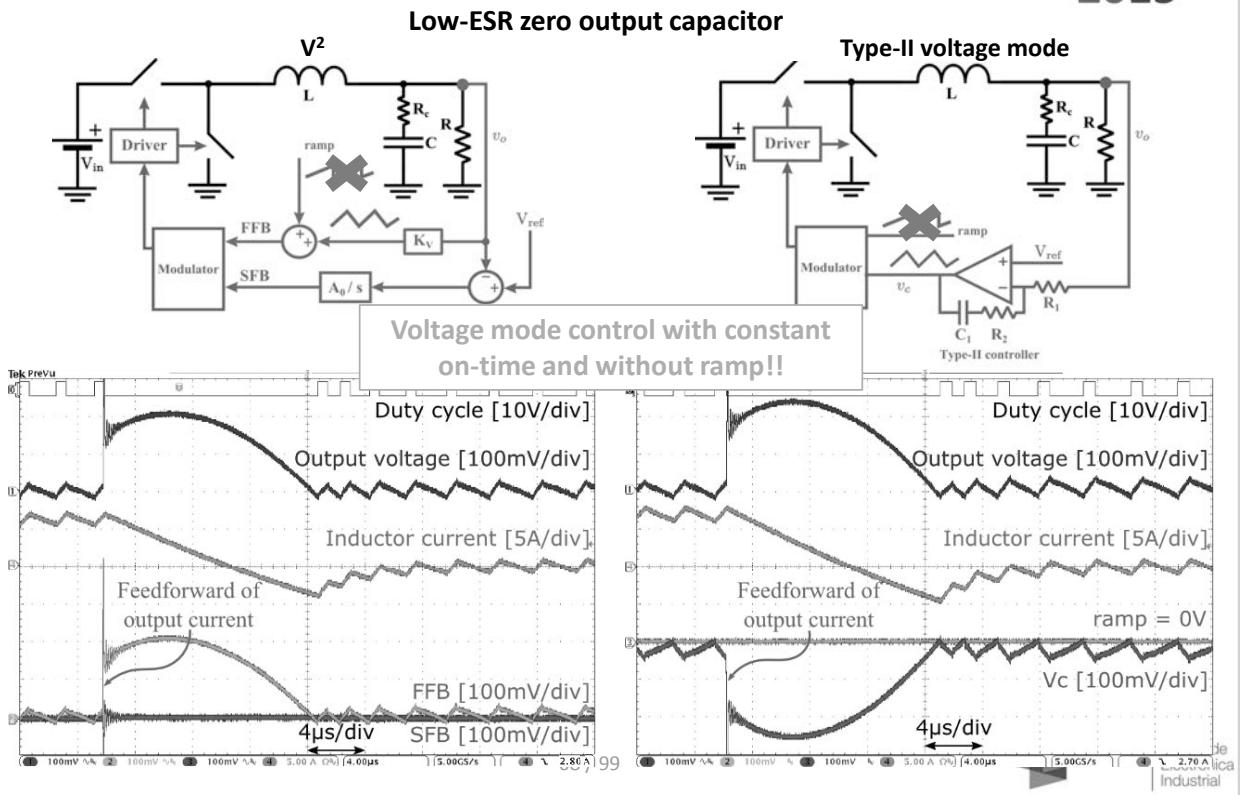


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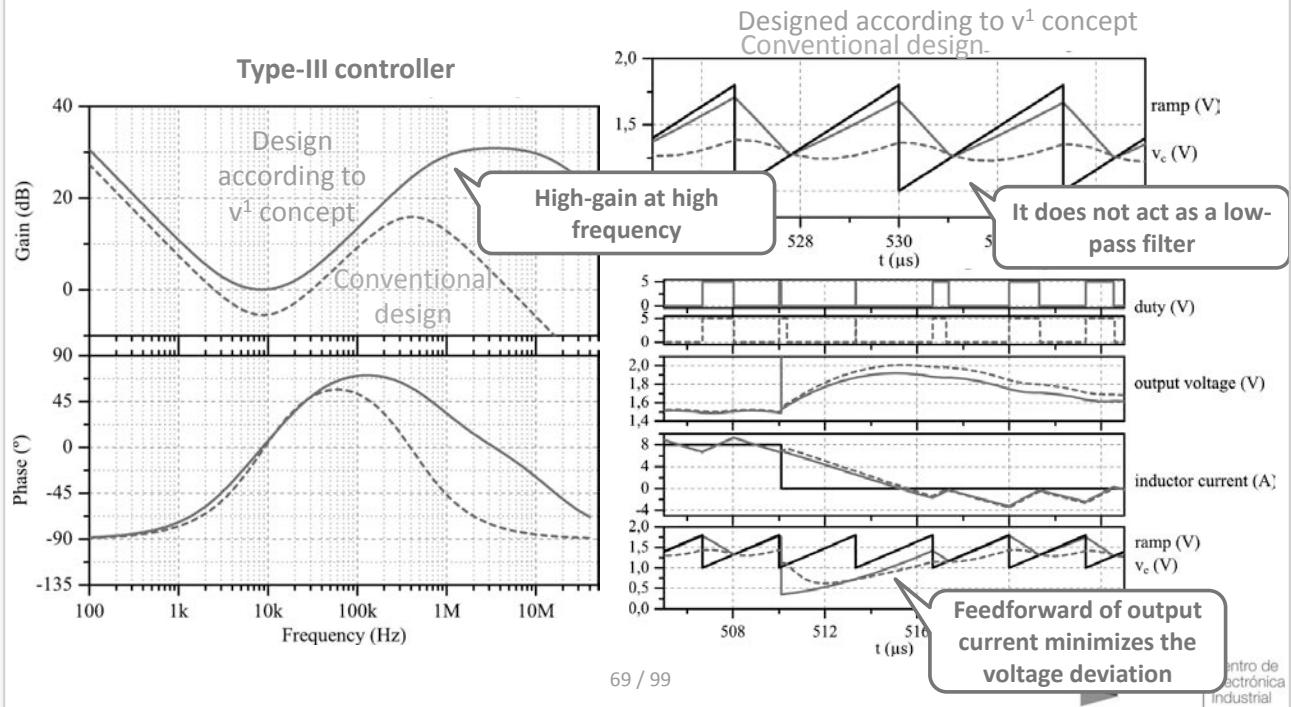
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DESIGN BASED ON V¹ CONCEPT

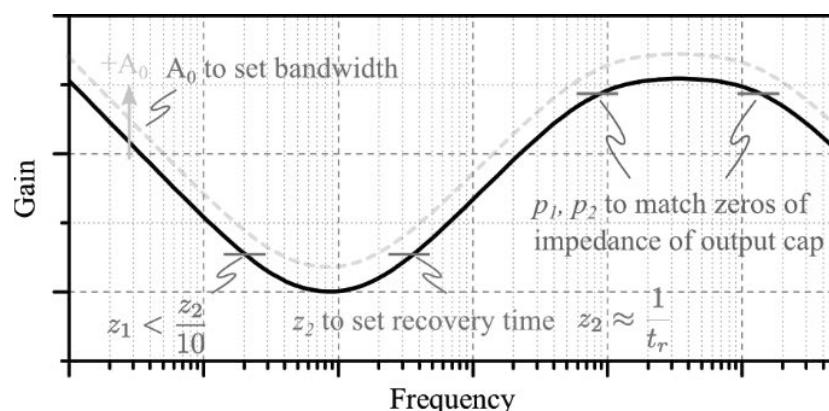
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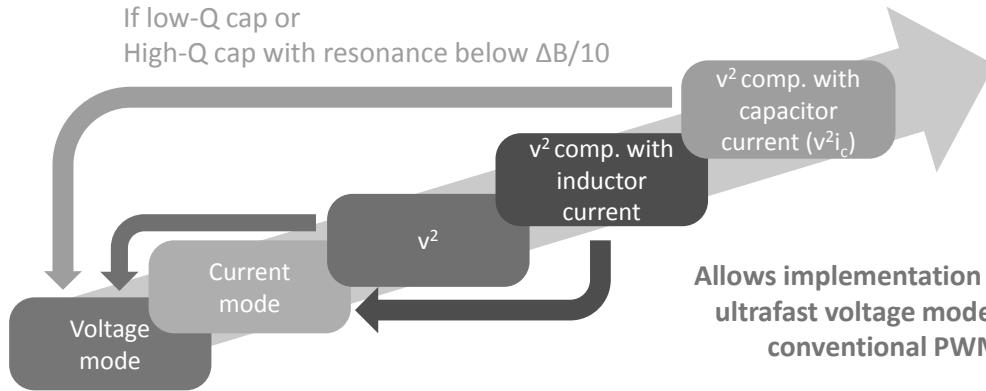
DESIGN BASED ON V¹ CONCEPT



DESIGN BASED ON V¹ CONCEPT



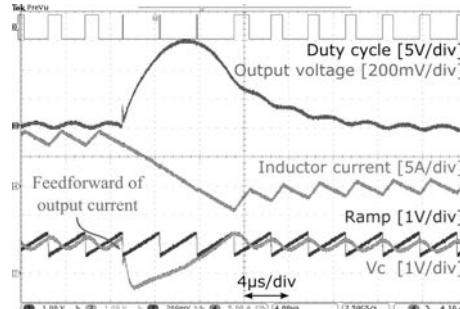
If low-Q cap or
High-Q cap with resonance below $\Delta B/10$



Allows implementation of simple low-cost ultrafast voltage mode controls using a conventional PWM controller!



KNOW-HOW

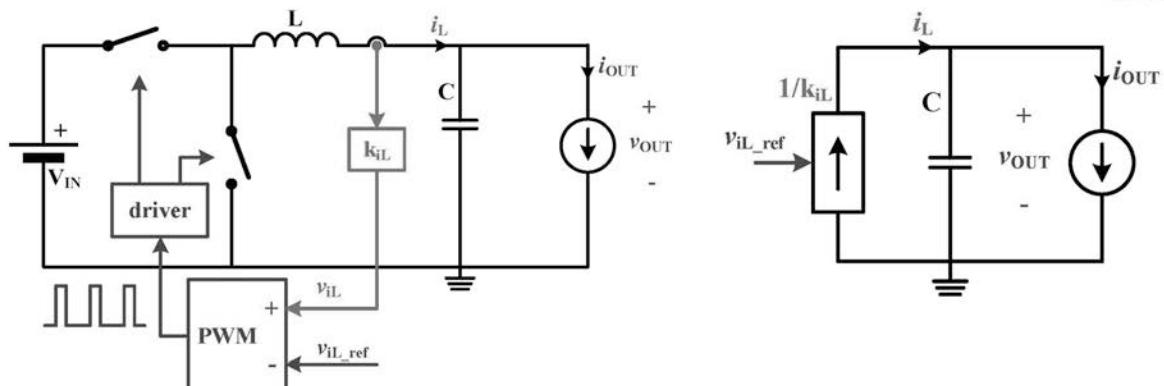


OUTLINE

60'

- Review of basic concepts
 - Current Mode Control
 - Voltage Mode Control
 - Robustness to C_{out} variation
 - Ripple based controls
 - V^1 Concept
- Modeling techniques
- Conclusions

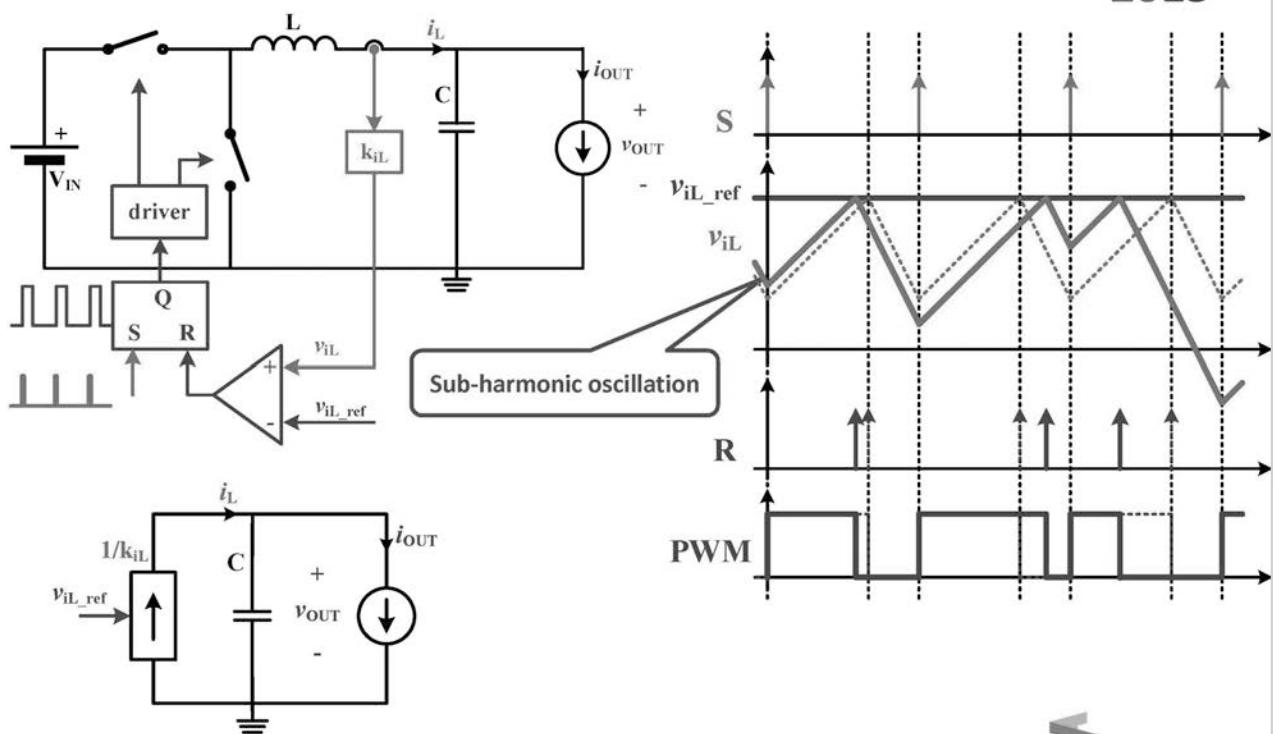
1ST ORDER APPROXIMATION OF CURRENT MODE CONTROL



- Simple approximation for current mode control
- Simple interpretation
- Good physical insight
- Does not predict sub-harmonic oscillations
- Does not consider audio-susceptibility

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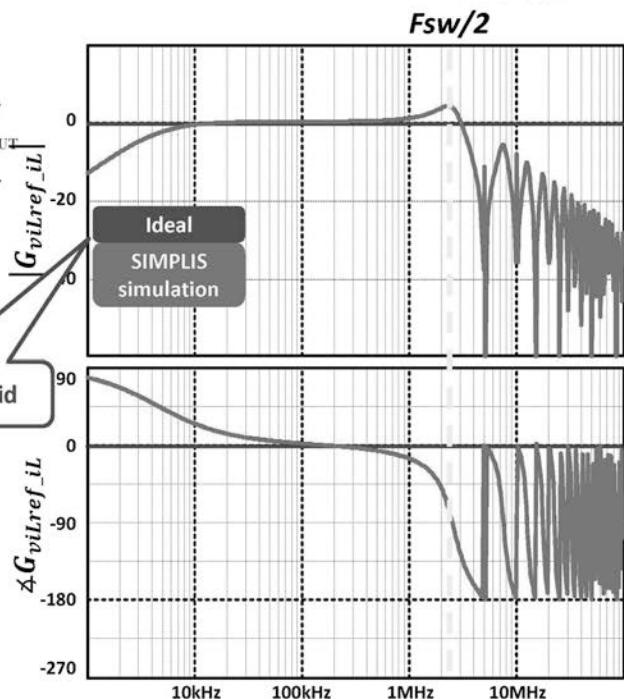
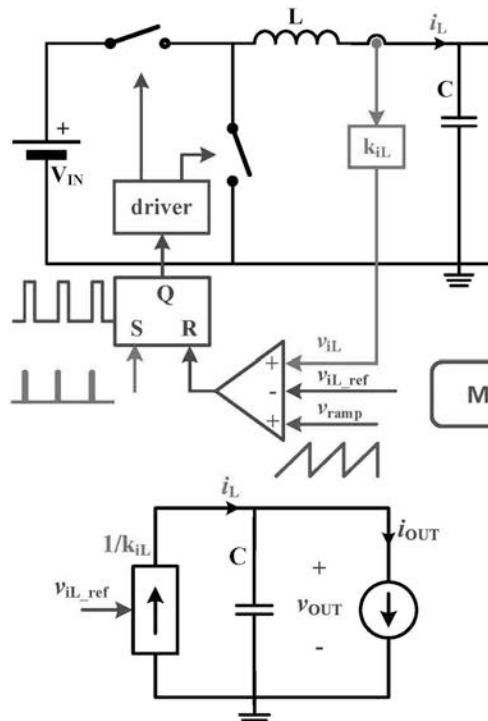
1ST ORDER APPROXIMATION OF CURRENT MODE CONTROL



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1ST ORDER APPROXIMATION OF CURRENT MODE CONTROL

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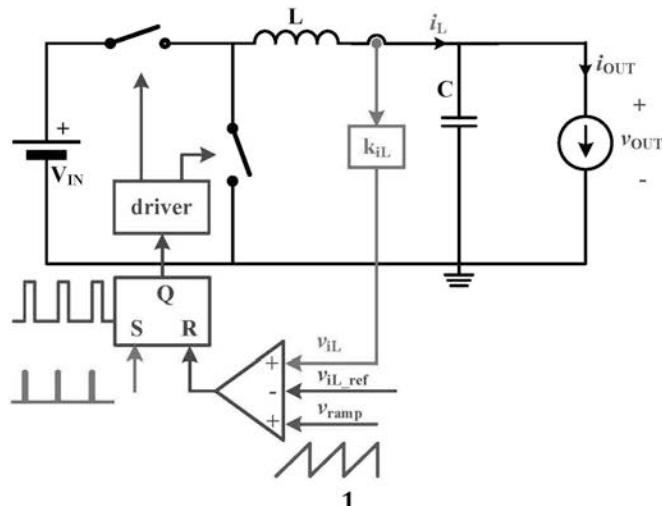


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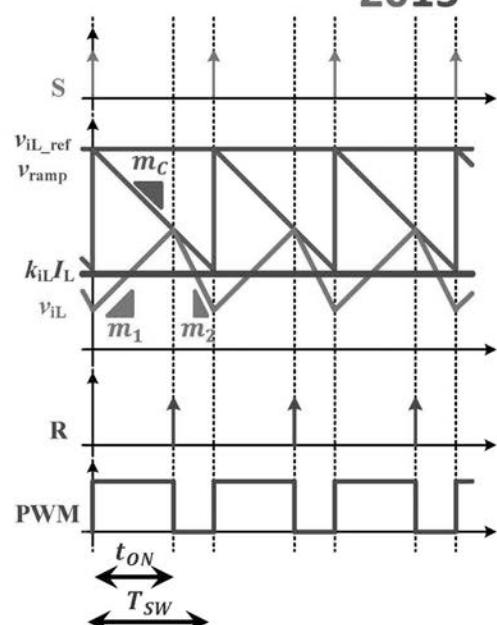
2ND ORDER MODEL FOR PEAK CURRENT MODE CONTROL

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$$v_{iL_ref} - m_C t_{ON} = k_{iL} I_L + \frac{1}{2} m_1 t_{ON}$$

$$d = \frac{(v_{iL_ref} - k_{iL} I_L) f_{SW}}{m_C + \frac{1}{2} m_1}$$

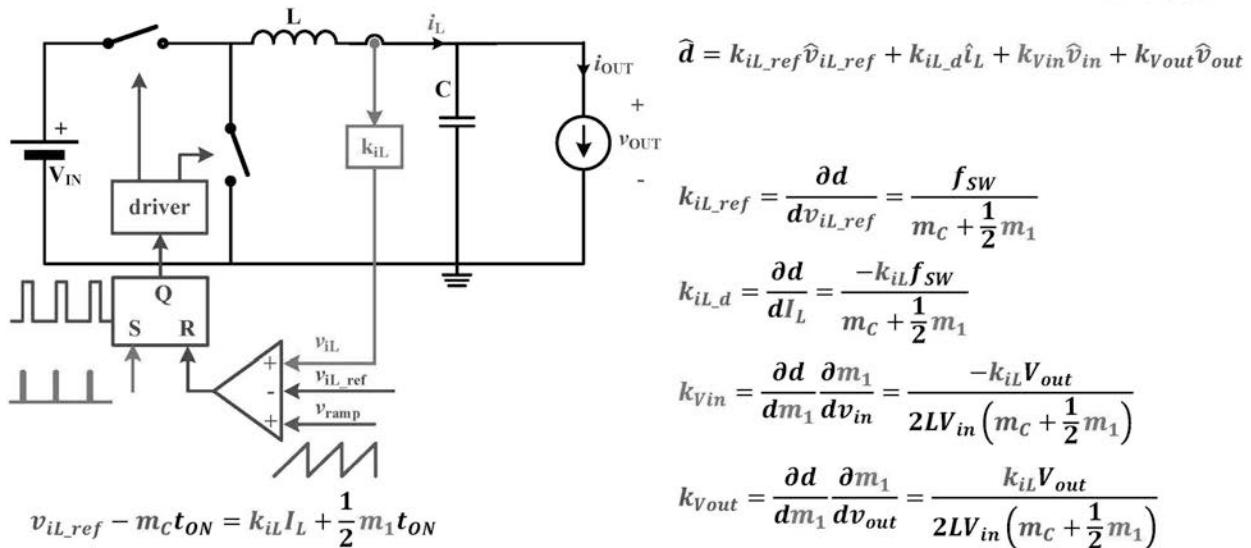


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2ND ORDER MODEL FOR PEAK CURRENT MODE CONTROL

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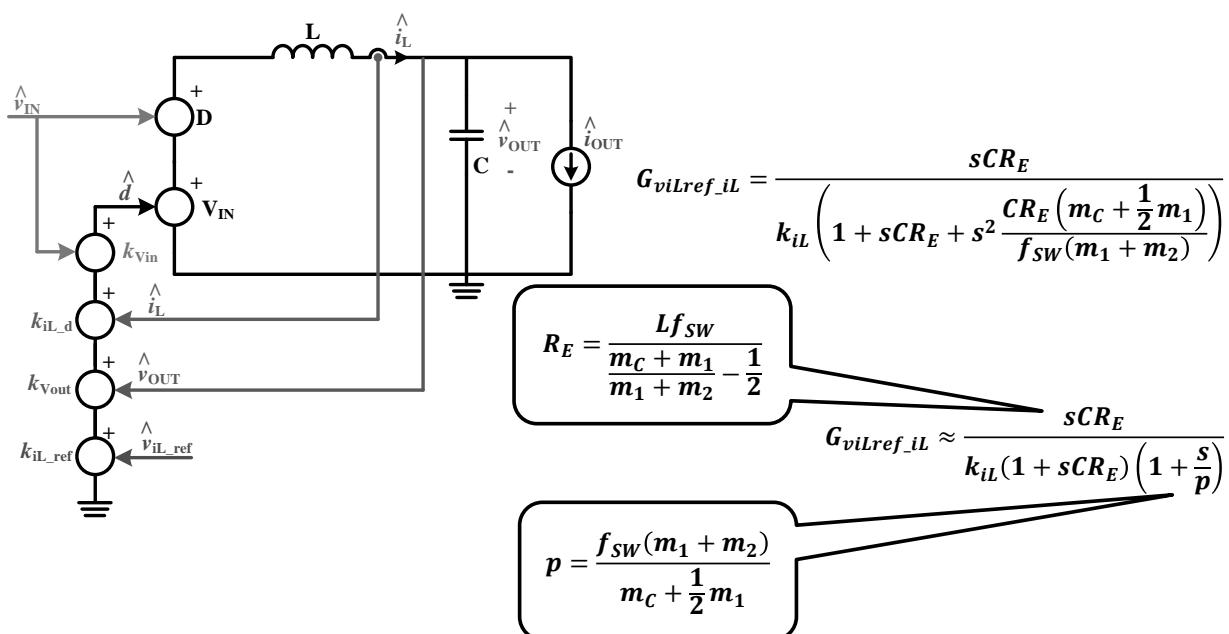
$$d = \frac{(v_{iL_ref} - k_{iL}I_L)f_{SW}}{m_C + \frac{1}{2}m_1}$$

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2ND ORDER MODEL FOR PEAK CURRENT MODE CONTROL

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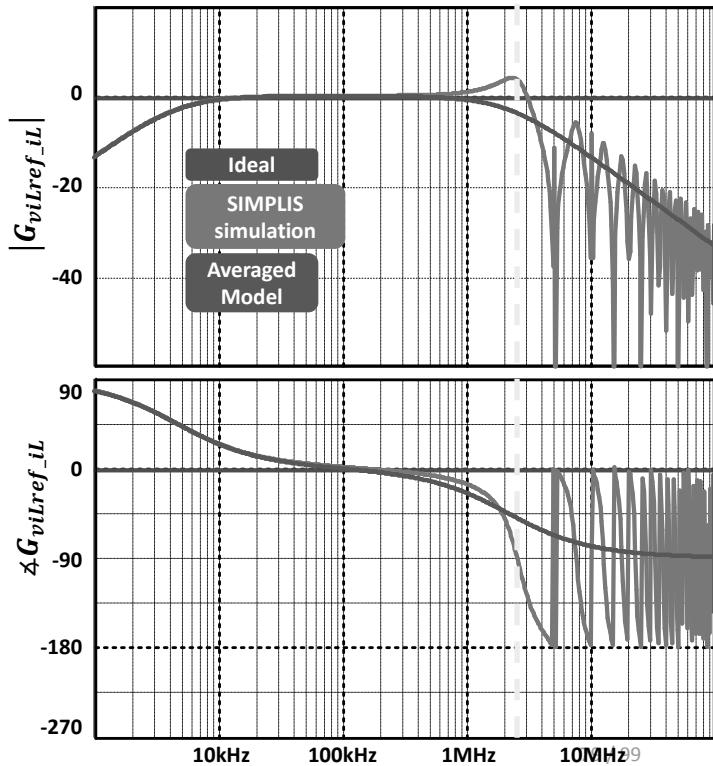
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2ND ORDER MODEL FOR PEAK CURRENT MODE CONTROL

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$f_{sw}/2$



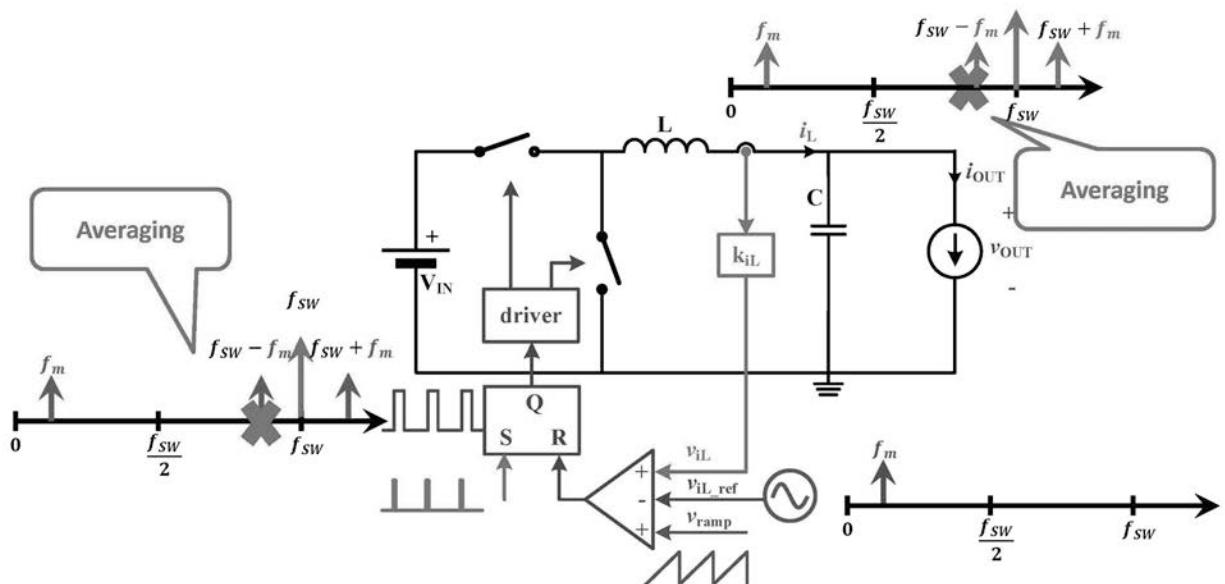
- Accounts for audio-susceptibility
- Accounts for low frequency behavior
- Considers some phase-delay up to 1/5th f_{sw}

- Does not predict sub-harmonic oscillations

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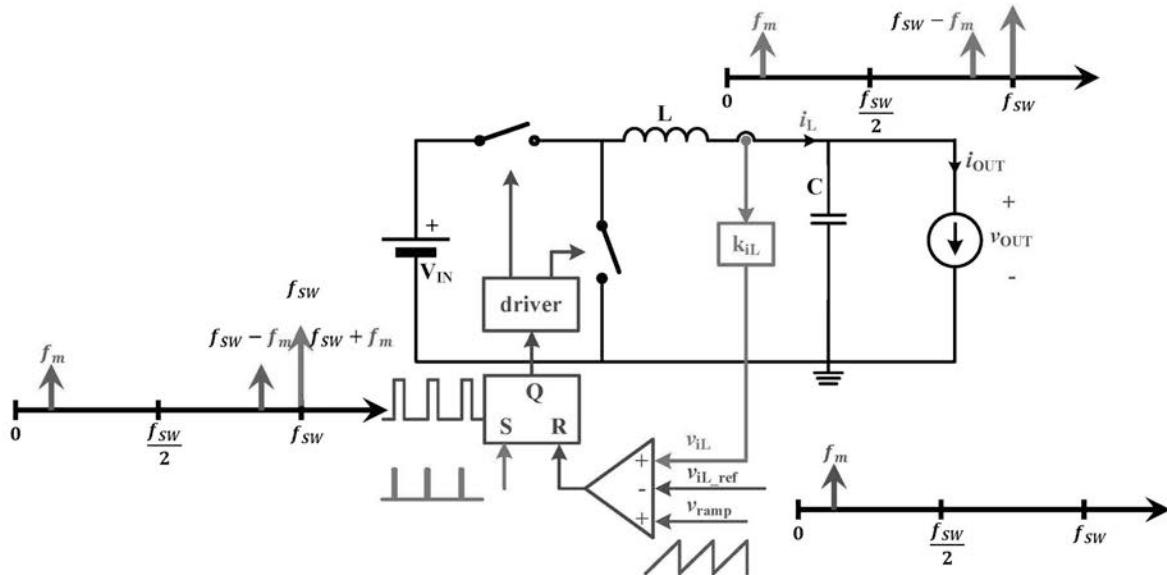
LIMITATIONS OF AVERAGE MODELS FOR PEAK CURRENT MODE CONTROL

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LIMITATIONS OF AVERAGE MODELS FOR PEAK CURRENT MODE CONTROL

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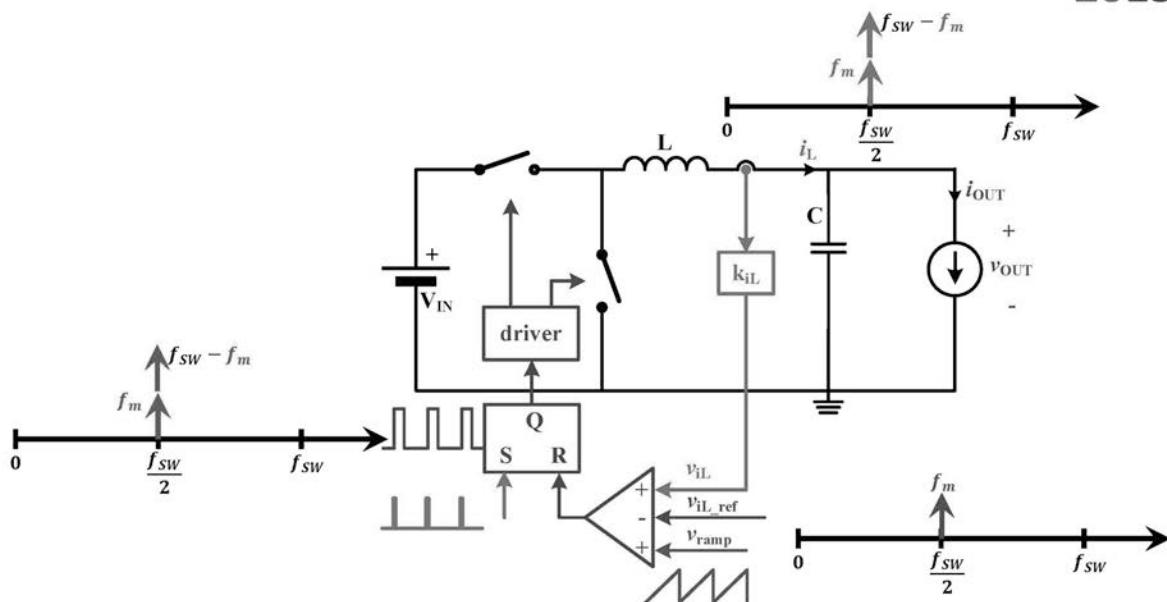


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LIMITATIONS OF AVERAGE MODELS FOR PEAK CURRENT MODE CONTROL

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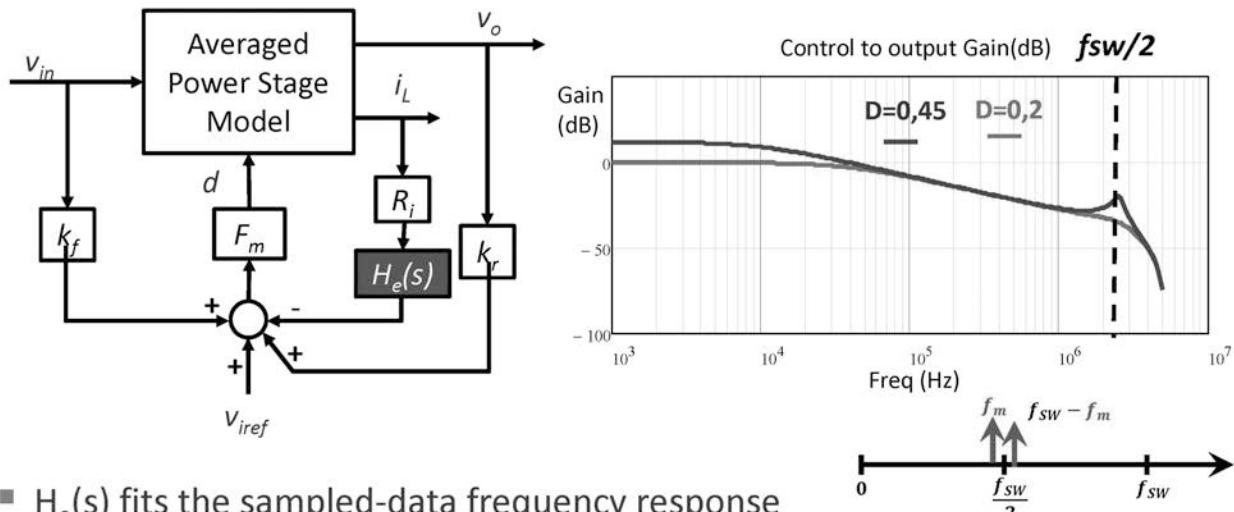
Y. Yan, F. C. Lee and P. Mattavelli, "Unified Three-Terminal Switch Model for Current Mode Controls", IEEE Trans. Power Electron., vol. 27, no. 9, pp. 4060–4070, Sep. 2012

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RIDLEY MODEL FOR PEAK CURRENT MODE CONTROL

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- $H_e(s)$ fits the sampled-data frequency response
- Predicts with high accuracy the sub-harmonic oscillation for constant frequency peak/valley current mode control



Ridley, R.B.; "A new, continuous-time model for current-mode control [power convertors]" Power Electronics, IEEE Transactions on Volume 6, Issue 2, April 1991
Page(s):271 - 280

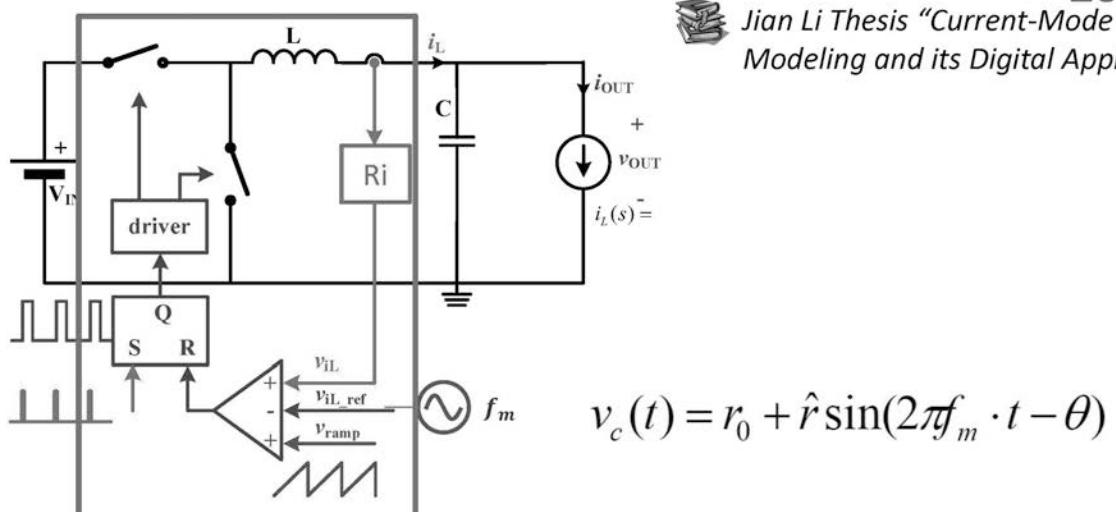
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JIAN LI'S DESCRIBING FUNCTION METHOD FOR PEAK CURRENT MODE CONTROL

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Jian Li Thesis "Current-Mode Control:
Modeling and its Digital Application"

- Derives a continuous time model based on the describing function method

$$i_L(s) = K_{vc}(s) \cdot v_{iL_ref}(s) + K_{vo}(s) \cdot v_o(s) + K_{vi}(s) \cdot v_i(s)$$

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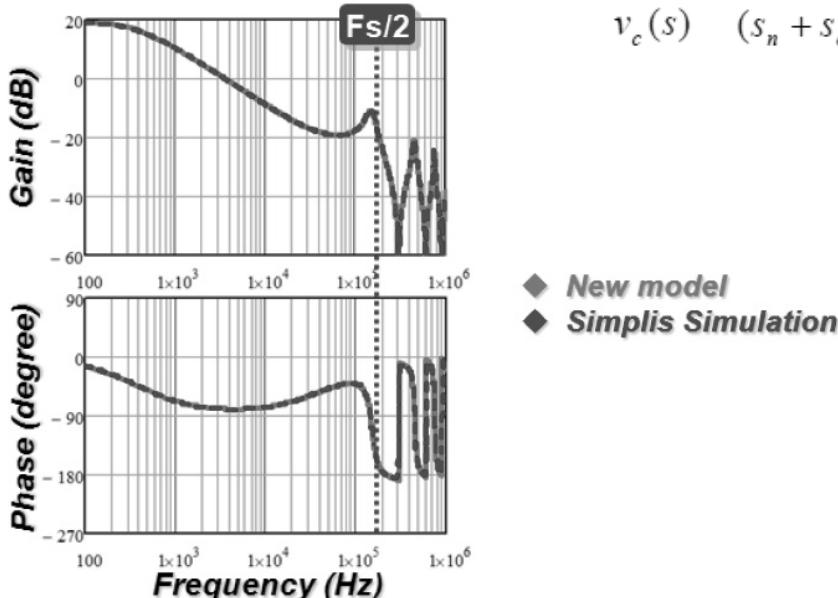
JIAN LI'S CONTINUOUS TIME MODEL FOR PEAK CURRENT MODE CONTROL

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Source: Jian Li Thesis "Current-Mode Control: Modeling and its Digital Application"

Applying the Laplace transform...



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UNIFIED THREE-TERMINAL SWITCH MODEL FOR CURRENT MODE CONTROLS

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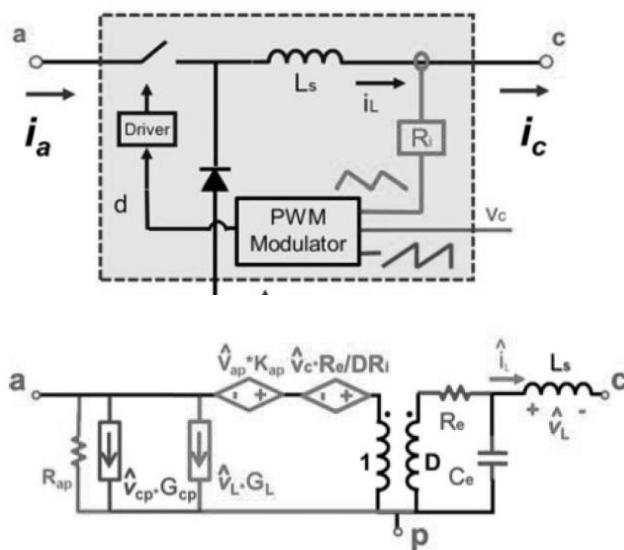


TABLE II.
EQUIVALENT CIRCUIT PARAMETERS

	PEAK CURRENT MODE	CONSTANT ON-TIME
R_e	$R_e = \frac{L_s}{T_{sw}(\frac{s_n + s_e}{s_n + s_f} - \frac{1}{2})}$	$R_e = 2L_s / T_{on}$
C_e	$C_e = T_{sw}^2 / (L_s \pi^2)$	$C_e = T_{on}^2 / (L_s \pi^2)$
K_{ap}	$K_{ap} = -\frac{T_{off}}{2L_s} R_e$	$K_{ap} = D'$
	VALLEY CURRENT MODE	CONSTANT OFF-TIME
R_e	$R_e = \frac{L_s}{T_{sw}(\frac{s_n + s_e}{s_n + s_f} - \frac{1}{2})}$	$R_e = 2L_s / T_{off}$
C_e	$C_e = T_{sw}^2 / (L_s \pi^2)$	$C_e = T_{off}^2 / (L_s \pi^2)$
K_{ap}	$K_{ap} = \frac{T_{off}}{2L_s} R_e$	$K_{ap} \approx -1$

$$G_L = G_{cp} = \frac{I_c}{V_{ap}}, R_{ap} = -\frac{V_{ap}}{DI_c}$$



Y. Yan, F. Lee, and P. Mattavelli, "Unified three-terminal switch model for current mode controls," *IEEE Trans. on Power Electronics* 2012.

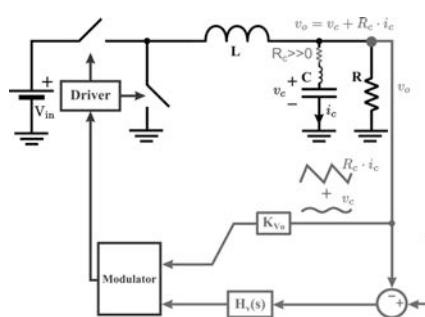
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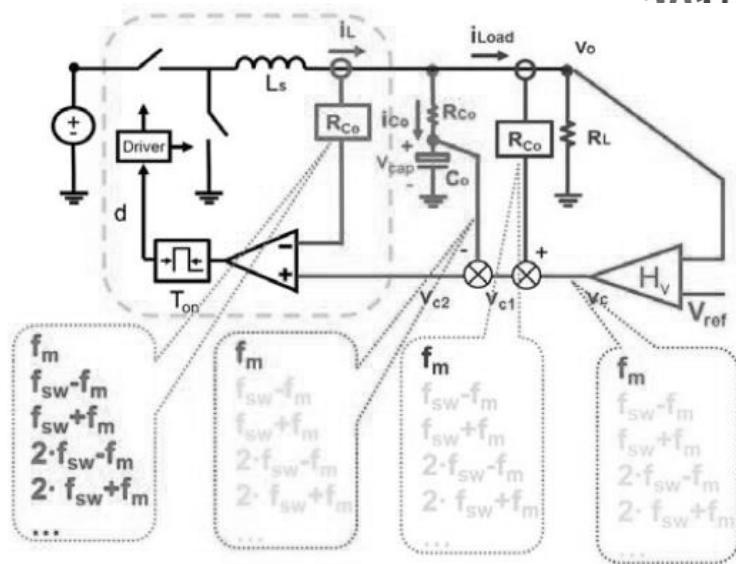
EXTENDING THE DESCRIBING FUNCTION TO V² CONTROL

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V² control



Yan, Yingyi; Lee, Fred C.; Mattavelli, Paolo; Tian, Shuilin, "Small signal analysis of V² control using current mode equivalent circuit model," *Applied Power Electronics Conference and Exposition (APEC)*, 2013



- Assumes that the switching condition is determined by the inductor ripple measured across the output capacitor.
- Neglects the ripple across the capacitor

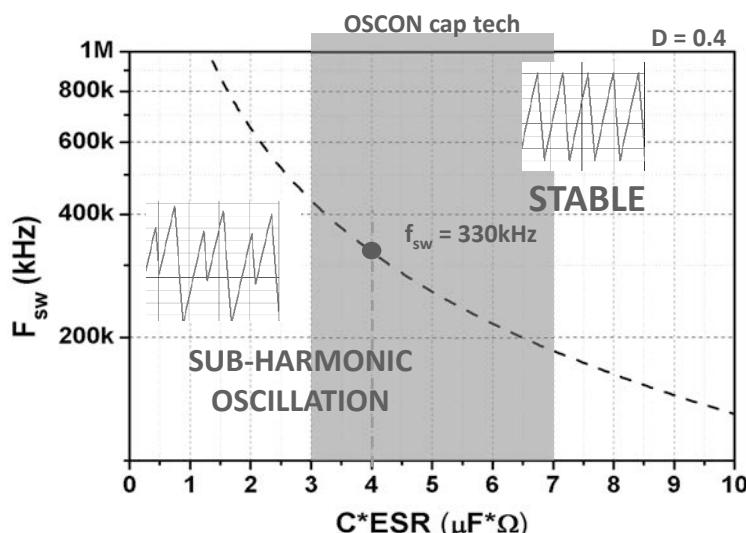
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LIMITATIONS OF THE DESCRIBING FUNCTION

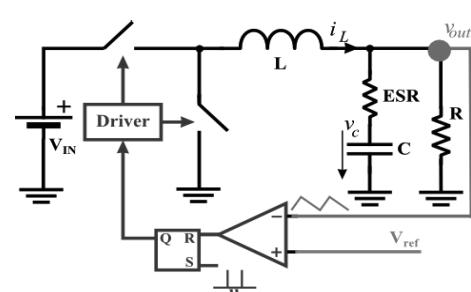
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Describing Function



$$f_{sw} = \frac{1}{C \cdot ESR} \left(\frac{1}{2} + \frac{D^2}{1 - 2D} \right)$$

Stability criterion from DF



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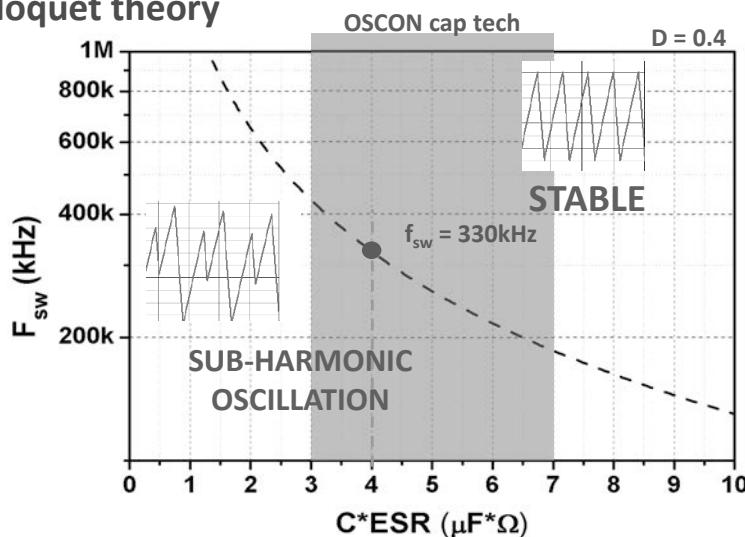
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LIMITATIONS OF THE DESCRIBING FUNCTION

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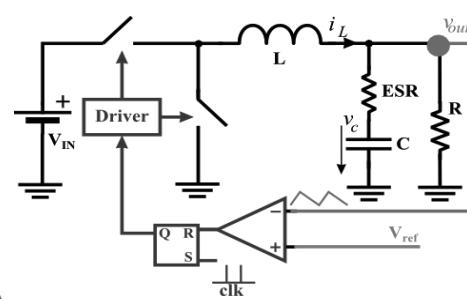
Describing Function

Floquet theory



$$F_{sw} = \frac{1}{C \cdot ESR} \left(\frac{1}{2} + \frac{D^2}{1 - 2D} \right)$$

Stability criterion from DF



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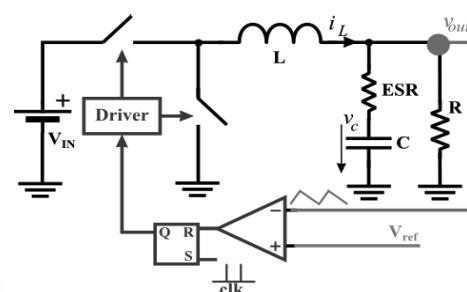
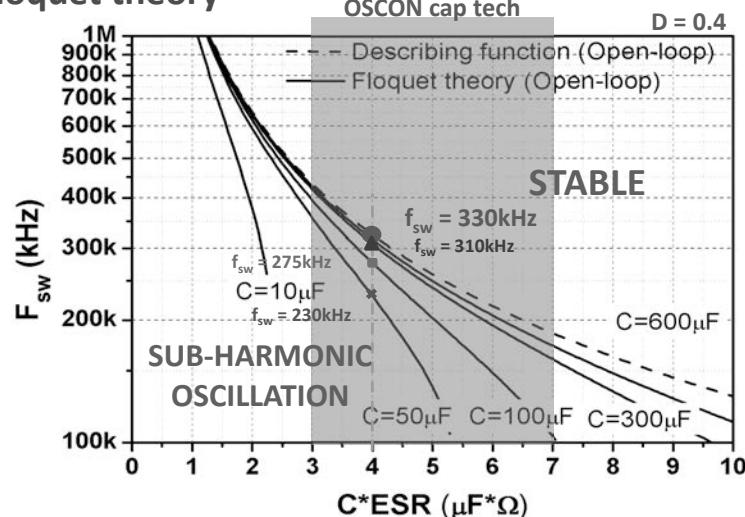
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LIMITATIONS OF THE DESCRIBING FUNCTION

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Describing Function

Floquet theory



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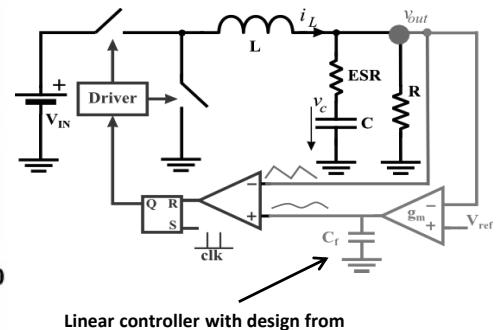
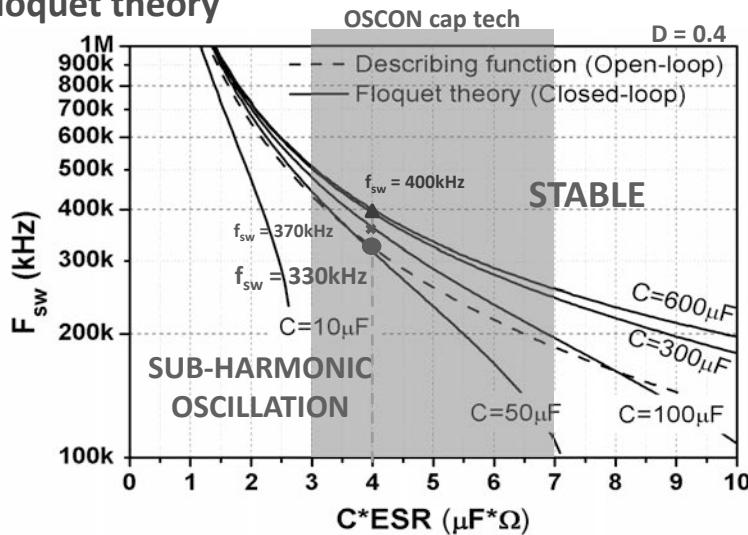
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LIMITATIONS OF THE DESCRIBING FUNCTION

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2015

Describing Function

Floquet theory



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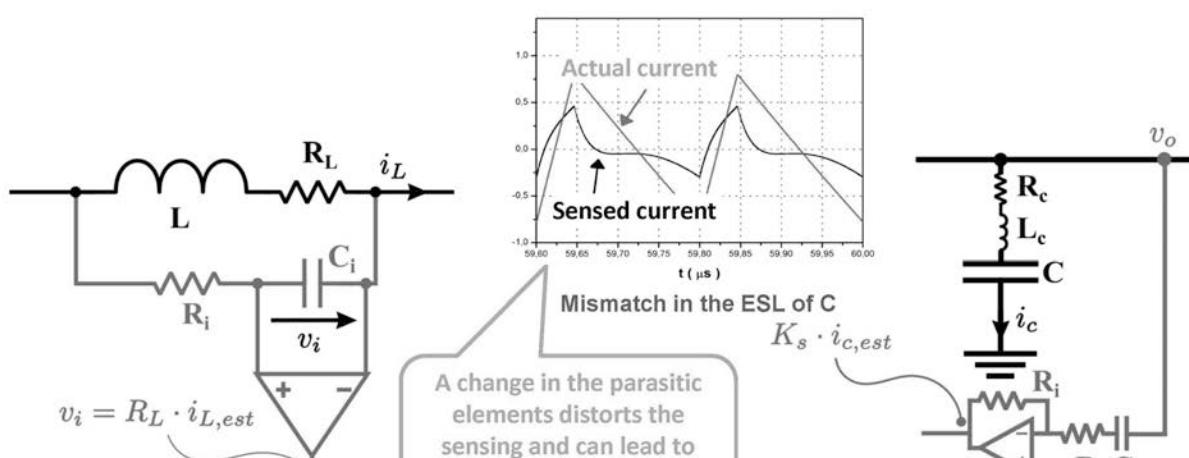
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MODELING CHALLENGES

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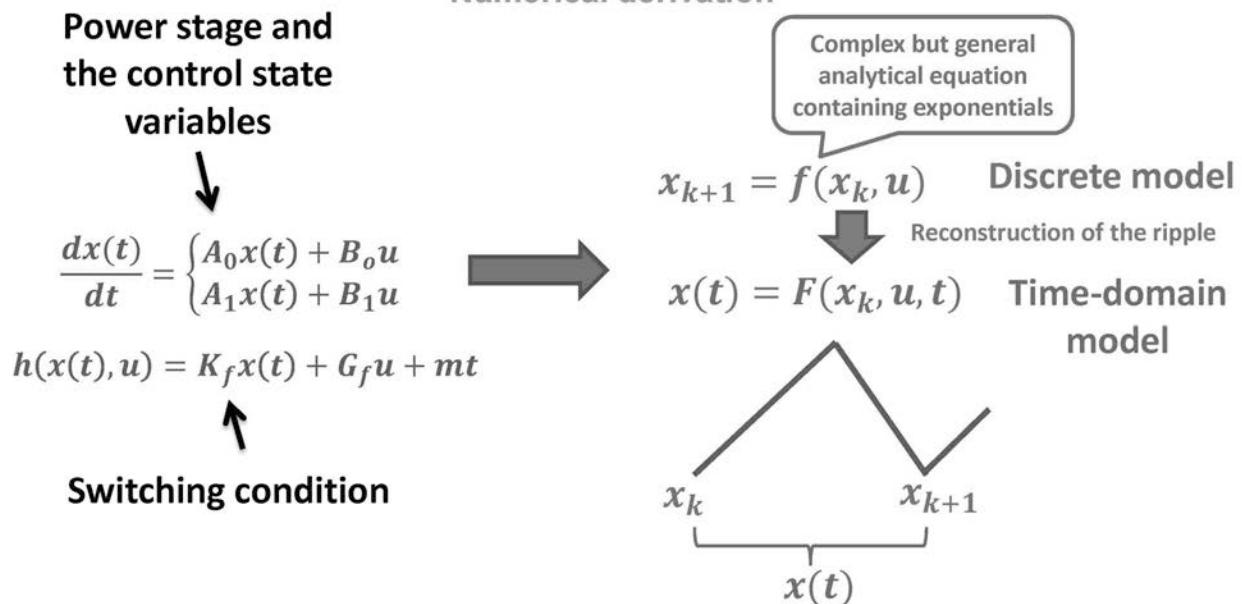
Current estimators

Lossless current sensors based correct matching of parasitic elements!



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[] Cortes, J.; Sivikovic, V.; Alou, P.; Oliver, J.; Cobos, J.; Wisniewski, R., "Accurate analysis of sub-harmonic oscillations of V2 and V2lc controls applied to Buck converter," *Power Electronics, IEEE Transactions on*, early access

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Numerical derivation

State-space model

$$\frac{dx(t)}{dt} = \begin{cases} A_0x(t) + B_0u \\ A_1x(t) + B_1u \end{cases}$$

$$h(x(t), u) = K_f x(t) + G_f u + mt$$

Discrete model

$$x_{k+1} = f(x_k, u)$$

$$x_{k+1} = x_k$$

Periodic operating point

$$x_{k+1} = x_k$$

Two ways of finding the monodromy matrix

Saltation matrix

$$\Phi = S_0(T) \cdot e^{A_0(1-d)T} \cdot S_1(dT) \cdot e^{A_1dT}$$

Jacobian matrix

$$\Phi = \frac{\partial x_{k+1}}{\partial x_k}$$



Cortes, J.; Sivikovic, V.; Alou, P.; Oliver, J.; Cobos, J.; Wisniewski, R., "Accurate analysis of sub-harmonic oscillations of V2 and V2lc controls applied to Buck converter," *Power Electronics, IEEE Transactions on*, early access

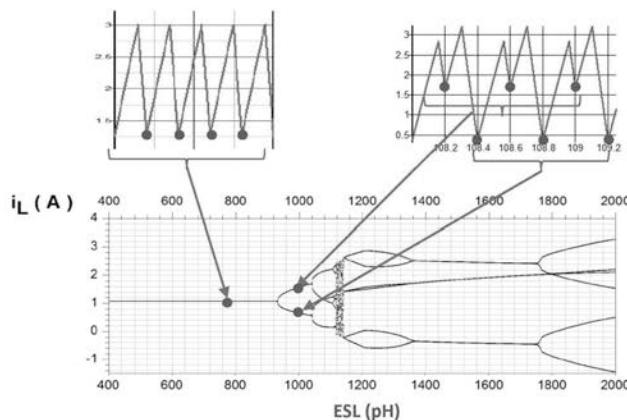
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FLOQUET THEORY

Bifurcation phenomena

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- Sub-harmonic oscillations can be seen as a bifurcation where the system is unable to maintain a T-periodic solution



Bifurcation diagram

Stability is analyzed by Floquet theory.

- If a perturbation grows over a period \rightarrow unstable

$$\Delta x_{k+1} = \Phi_{cycle} \cdot \Delta x_k$$

λ = eigenvalues of Φ_{cycle}

$|\lambda| < 1$, stable

$|\lambda| > 1$, sub-harmonic oscillation

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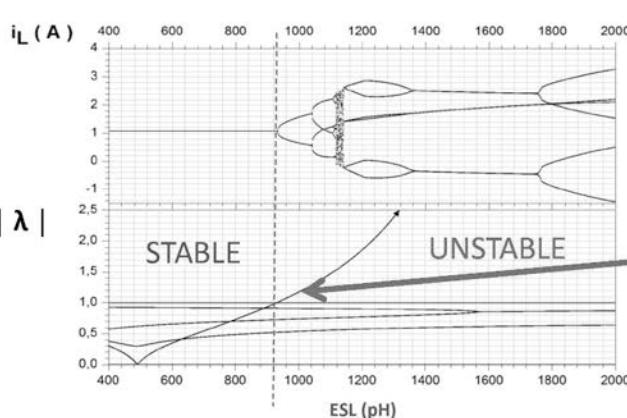
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FLOQUET THEORY

Bifurcation phenomena

**ESSCIRC
ESSDERC
2015**

- Sub-harmonic oscillations can be seen as a bifurcation where the system is unable to maintain a T-periodic solution



Stability is analyzed by Floquet theory.

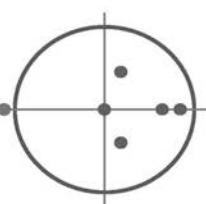
- If a perturbation grows over a period \rightarrow unstable

$$\Delta x_{k+1} = \Phi_{cycle} \cdot \Delta x_k$$

λ = eigenvalues of Φ_{cycle}

$|\lambda| < 1$, stable

$|\lambda| > 1$, sub-harmonic oscillation



Floquet multipliers

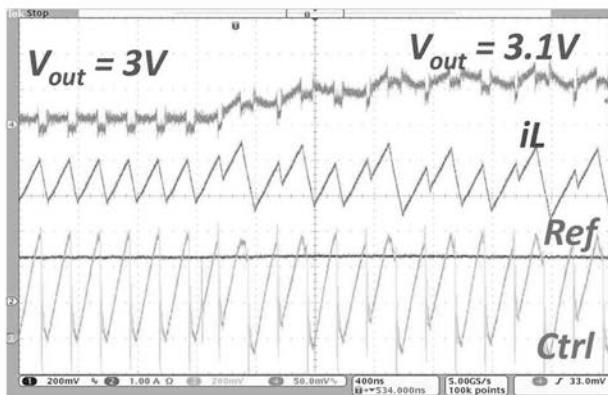
96 / 99

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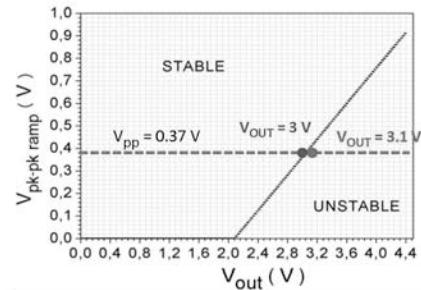
EXPERIMENTAL VALIDATION

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2015

$V^2 I_C$



Experimental sub-harmonic oscillation on $V^2 I_C$ control



Predicted stability behavior

The Floquet theory predicts accurately the oscillation!

$$V_{out} = 3V \rightarrow \lambda = -0.966$$

$$V_{out} = 3.1V \rightarrow \lambda = -1.06$$

Out of unit circle!

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OUTLINE

ESSCIRC
ESSDERC
2015

60'

- Review of basic concepts
 - Current Mode Control
 - Voltage Mode Control
 - Robustness to C_{out} variation
 - Ripple based controls
 - V^1 Concept
 - Modeling techniques
 - Conclusions

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CONTROL LOOP DESIGN PROCEDURE

1

Use accurate models to predict sub-harmonic stability

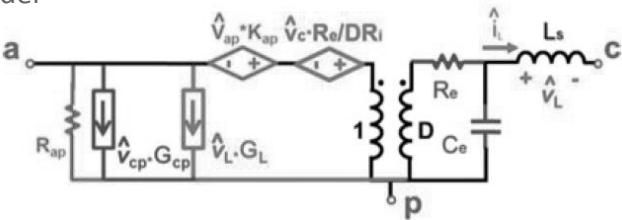
A

Unified three-terminal model

B

Simulation tools:

- SIMPLIS®
- PSIM



2

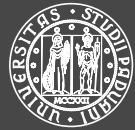
Validate the design by means of:

A

Numerical evaluation of eigenvalues of monodromy matrix Φ

B

Extensive time domain simulation changing parameters



Digital Control of High-Frequency Switched-Mode dc-dc Converters

September 18, 2015

Luca Corradini

Power Electronics Group
<http://pelgroup.dei.unipd.it>

University of Padova
 Department of Information Engineering – DEI

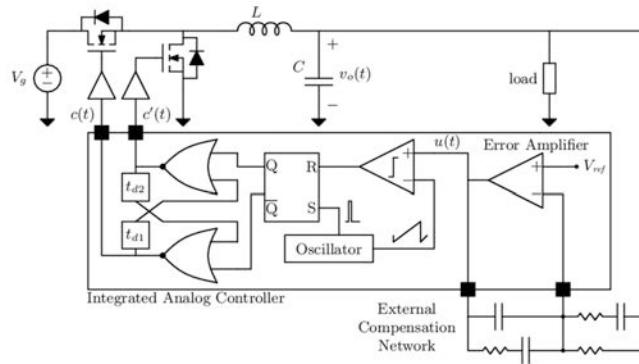


- Digital control *using microcontrollers or DSP chips* has long been used in power electronics at relatively high power levels and at relatively low switching frequencies, as in:
 - Grid-connected three-phase inverters and rectifiers
 - Motor drives
 - Uninterruptible power supplies
- Objectives of this seminar are to outline recent advances in practical digital control for *high-frequency* switched-mode power supplies (SMPS) in application areas such as:
 - Mobile and desktop electronics
 - Server power distribution
 - Telecom/datacom power management
 - Energy-efficient lighting
 - Distributed PV optimizers

$P \lesssim$ several kW
 $f_s \gtrsim$ tens of kHz
 Traditionally
 micro- or DSP-controlled

$P \gtrsim$ hundreds of W
 $f_s \gtrsim$ hundreds of kHz
 Traditionally
 analog-controlled!

Traditional Analog PWM Control: Voltage-Mode Buck Example

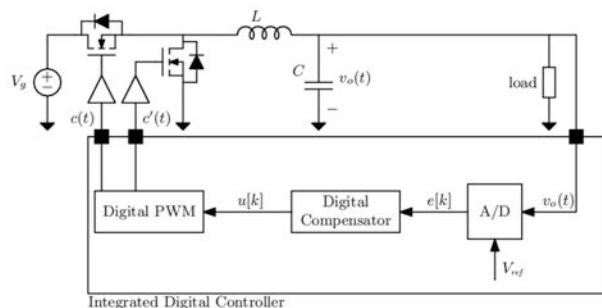


- More than 30 years old technology, widely available
- Simple circuitry, well-known design techniques
- Achievable closed-loop bandwidth $f_c \sim f_s/20 - f_s/5$ depending on the control strategy
- No flexibility, system parameters set through passive components
- Sensitivity to process and temperature variations
- System interface and (digital) power management features possible through added complexity of microcontroller with A/D and D/A hooks

[65] D. Maksimovic and P. Mattavelli, "Digital Control in Power Electronics: A Power Supply Perspective"

3

Why not Digital Control?



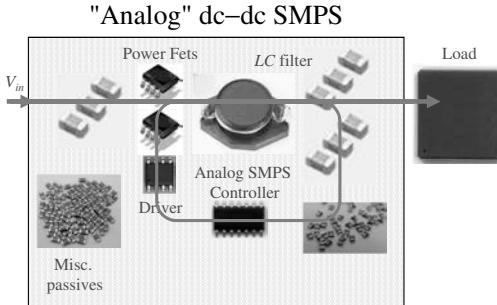
- Scaling, performance and cost advances in digital VLSI are rapid
- External passive components no longer required for loop compensation
- Programmability, flexibility, built-in system interface
- Ability to implement more advanced control techniques
- A/D or DPWM can be more complex and costly than an entire analog PWM controller
- Standard, cost-effective micro-controllers or DSPs are too slow and too complex for majority of mainstream high-frequency SMPS operating in the hundreds of kHz to MHz

[65] D. Maksimovic and P. Mattavelli, "Digital Control in Power Electronics: A Power Supply Perspective"

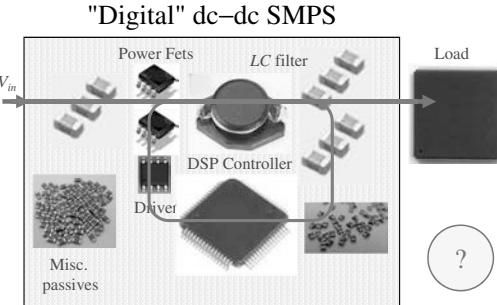
4



Analog vs. "brute force" Digital Loop



- Switching frequency: 1 MHz
- Loop bandwidth: 100 kHz
- Mature, proven technology
- Low cost



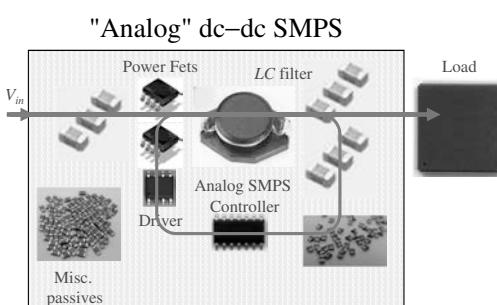
- DSP-based controller:
 - Fast, high-resolution A/D
 - Very high clock-rate DPWM
 - Slow, software-based compensation
 - Poorly flexible architecture
- Switching frequency: 50 kHz
- Loop bandwidth: 3 kHz
- High cost, no obvious benefits

[65] D. Maksimovic and P. Mattavelli, "Digital Control in Power Electronics: A Power Supply Perspective"

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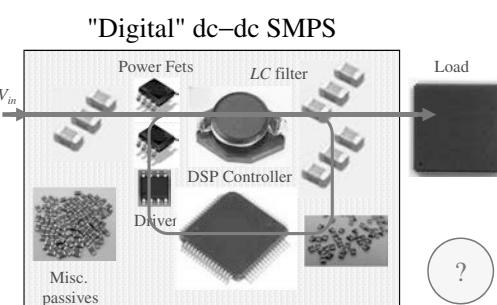


Analog vs. "brute force" Digital Loop



- Switching frequency: 1 MHz
- Loop bandwidth: 100 kHz
- Mature, proven technology

For high-frequency DC-DC applications, new approaches are needed to exploit the advantages of digital VLSI and signal processing technologies

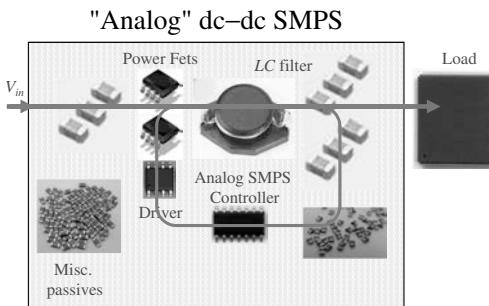


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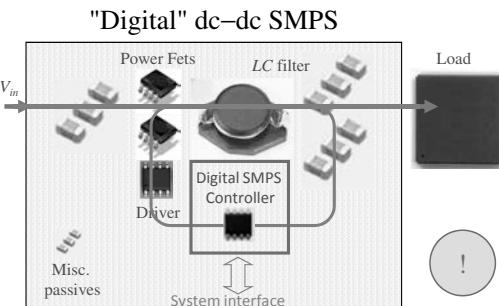
[65] D. Maksimovic and P. Mattavelli, "Digital Control in Power Electronics: A Power Supply Perspective"

6

Analog vs. Hardware-Optimized Digital Loop



- Switching frequency: 1 MHz
- Loop bandwidth: 100 kHz
- Mature, proven technology
- Low cost

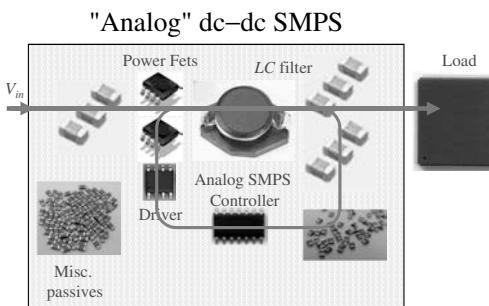


- Custom-designed digital IC:
 - Small-area, low-cost digital CMOS
 - Optimized A/D and DPWM
 - Fast, programmable hardwired compensator
 - Scalable, HDL-based design
 - Fewer discrete components
- Switching frequency: 1 MHz
- Loop bandwidth: 100 kHz
- Lower cost

[65] D. Maksimovic and P. Mattavelli, "Digital Control in Power Electronics: A Power Supply Perspective"

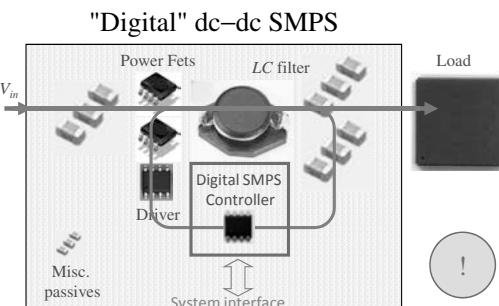
7

Analog vs. Hardware-Optimized Digital Loop



- Switching frequency: 1 MHz
- Loop bandwidth: 100 kHz
- Mature, proven technology

Potentials for significant improvements in both performance and system intergration

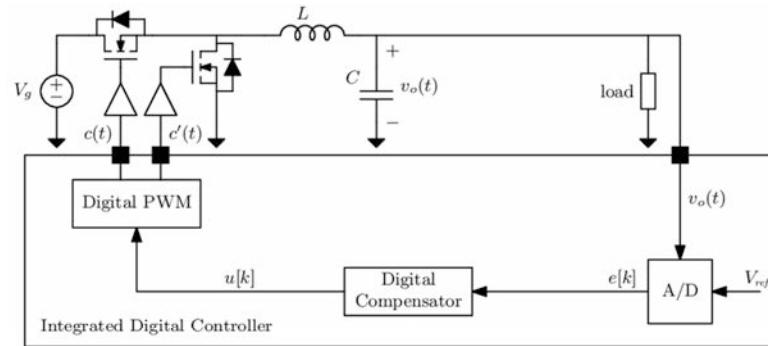


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[65] D. Maksimovic and P. Mattavelli, "Digital Control in Power Electronics: A Power Supply Perspective"

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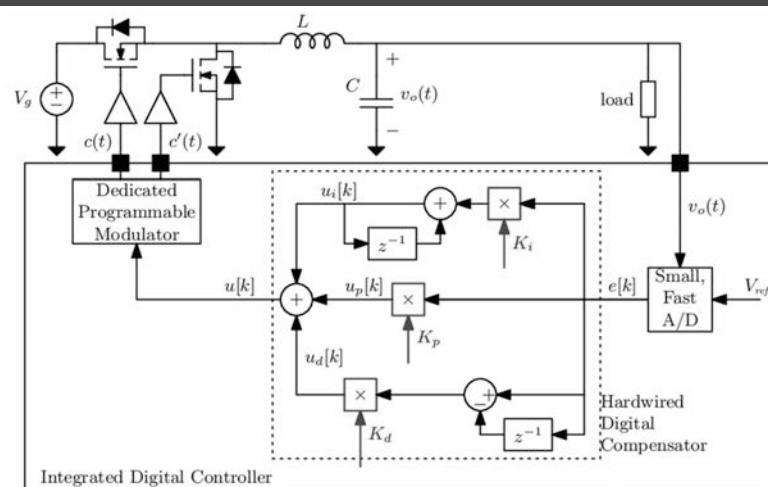
Digitally-Controlled Point-of-Load Converter



L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

9

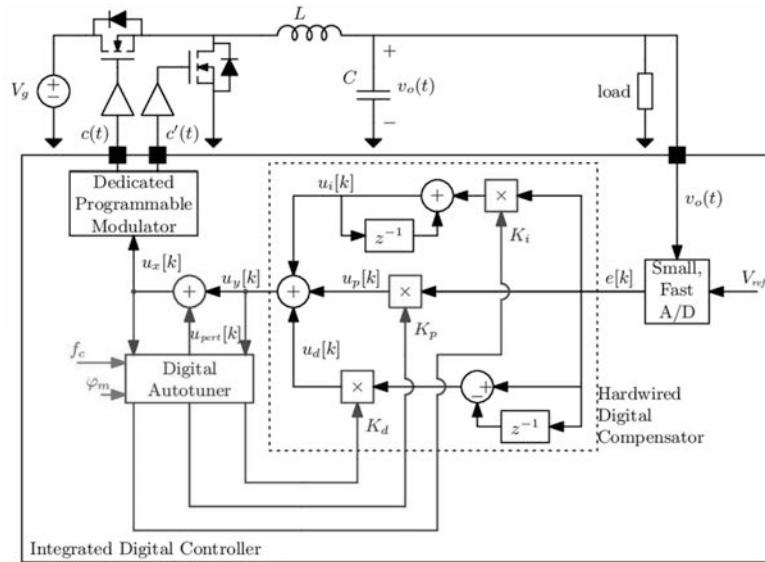
Digitally-Controlled Point-of-Load Converter



L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

10

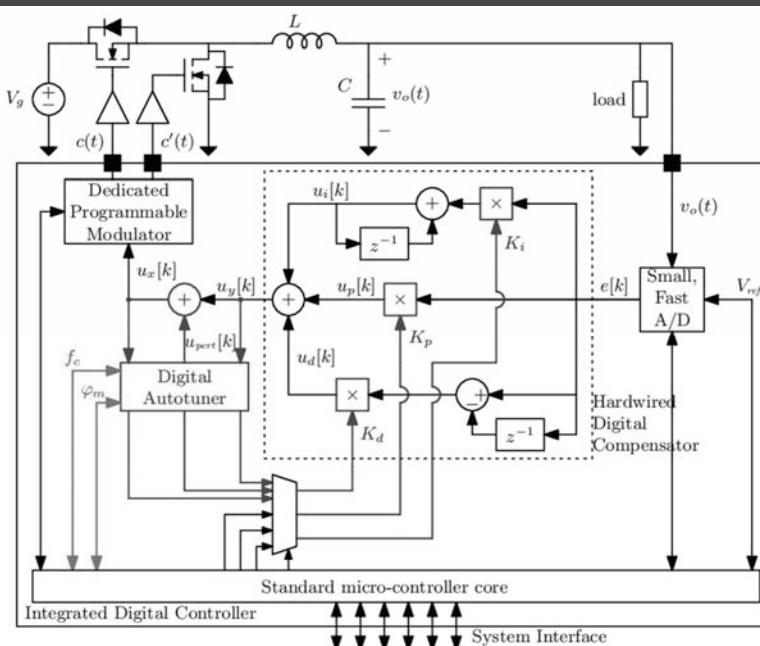
More Features: Digital Autotuning



L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

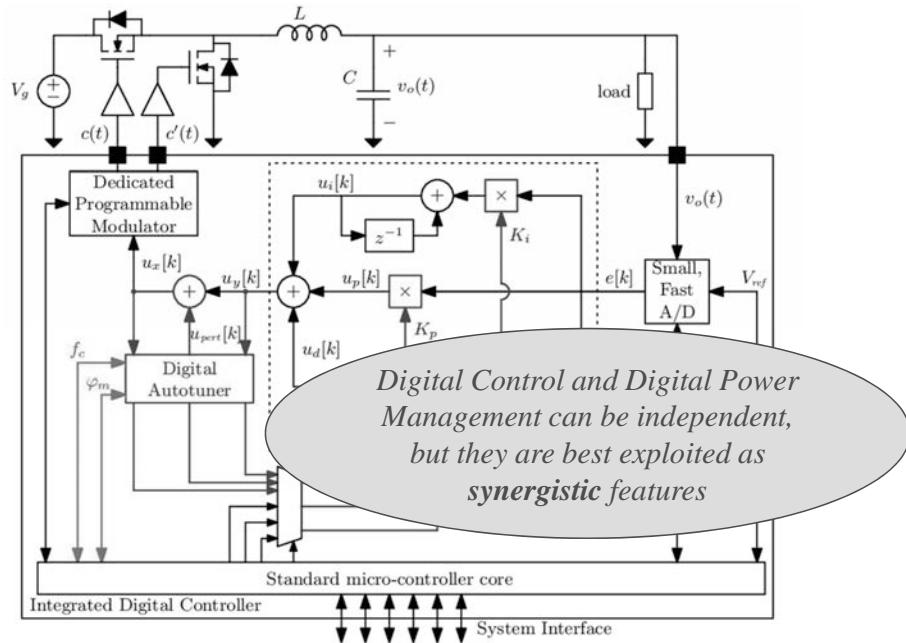
11

From Digital Control to Digital Power Management



L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

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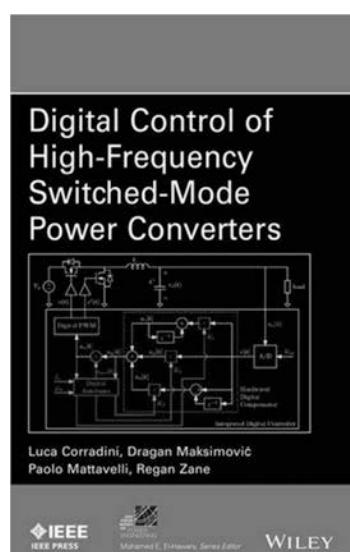


L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

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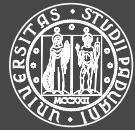
- L. Corradini, D. Maksimović, P. Mattavelli and R. Zane, "Digital Control of High-Frequency Switched-Mode Power converters," 1st ed. Wiley-IEEE Press, 2015
 - Comprehensive treatment of digital control theory for power converters
 - Enables readers to successfully analyze, model, design, and implement voltage, current, or multiloop digital feedback loops around switched-mode power converters
 - Practical examples are used throughout the book to illustrate applications of the techniques developed:
 - Matlab examples and simulations
 - Verilog and VHDL sample codes



<http://eu.wiley.com/WileyCDA/WileyTitle/productCd-1118935101.html>

L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

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Focus on high-performance, low hardware complexity control solutions capable to:

1. Be competitive against well-established analog controllers
2. Offer new features, not available with analog ICs



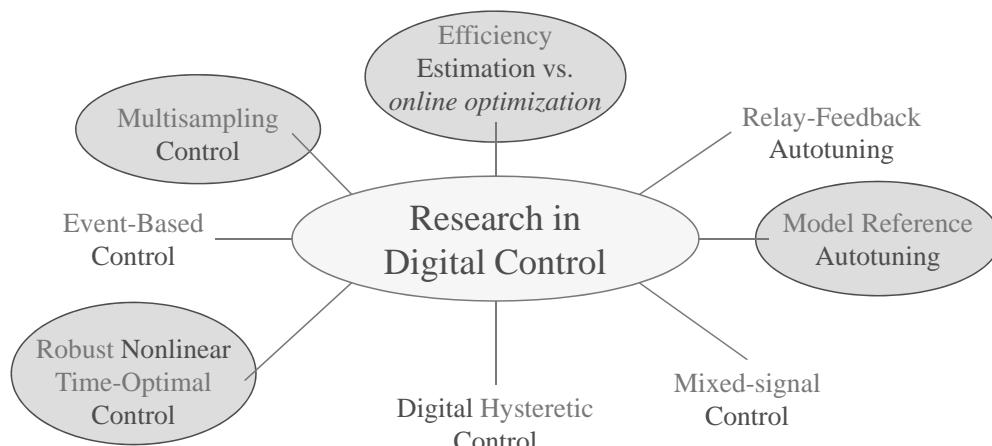
L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

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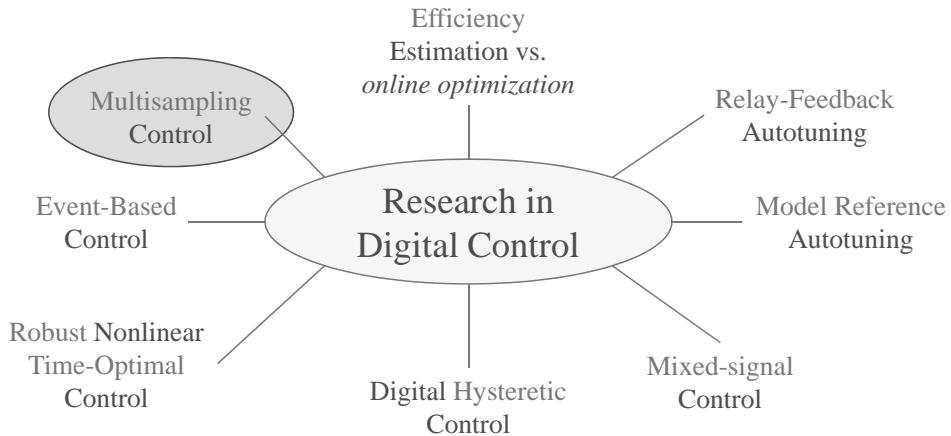
L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

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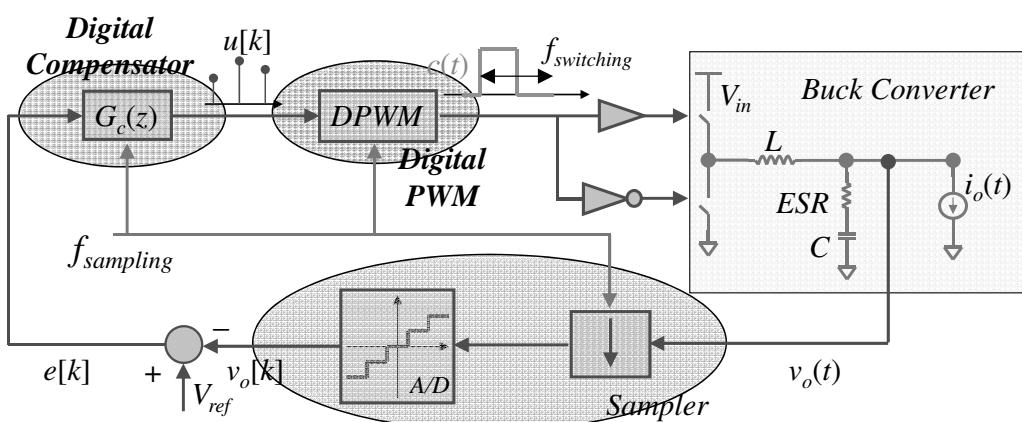
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L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

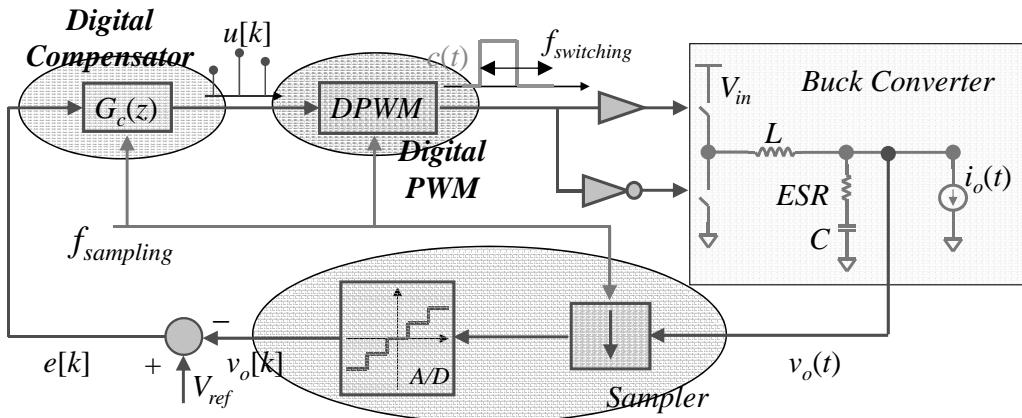
17



- Control operation:
 - The converter output voltage is sampled and quantized
 - A discrete-time compensator processes the error $e[k]$ and outputs the modulating signal $u[k]$
 - A digital pulse-width modulator generates the PWM signal $c(t)$

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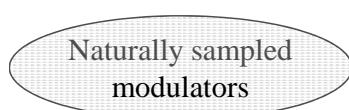
- Loop dynamic performances are constrained by the total loop delay t_d , sum of the following contributions:
 - A/D conversion delay
 - Computational delay
 - Gate drive propagation delay
 - Modulator delay

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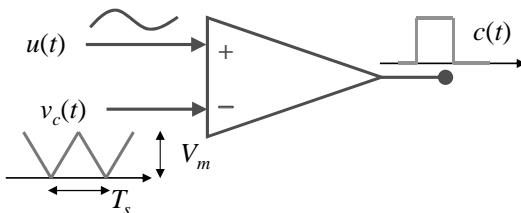


Three families of PWM modulators can be identified:



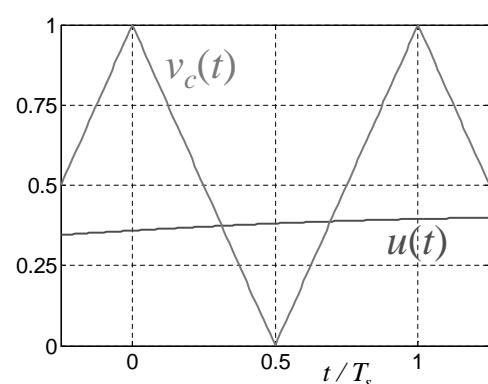
Multiple sampled modulators

Uniformly sampled
(or single-sampled)
modulators



Process an *analog* modulating signal $u(t)$.

They are commonly employed in traditional analog PWM control

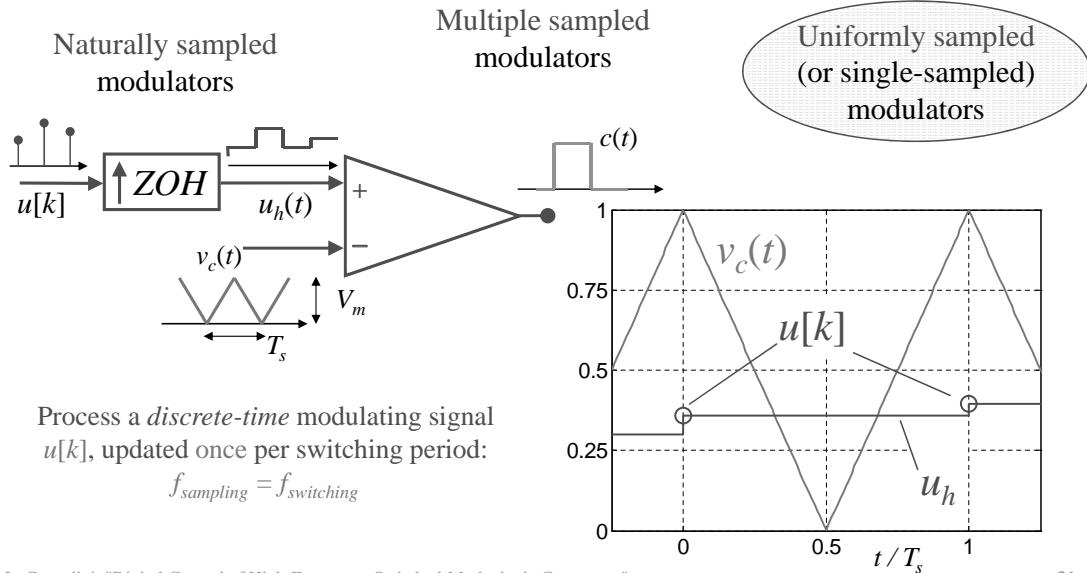


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Three families of PWM modulators can be identified:

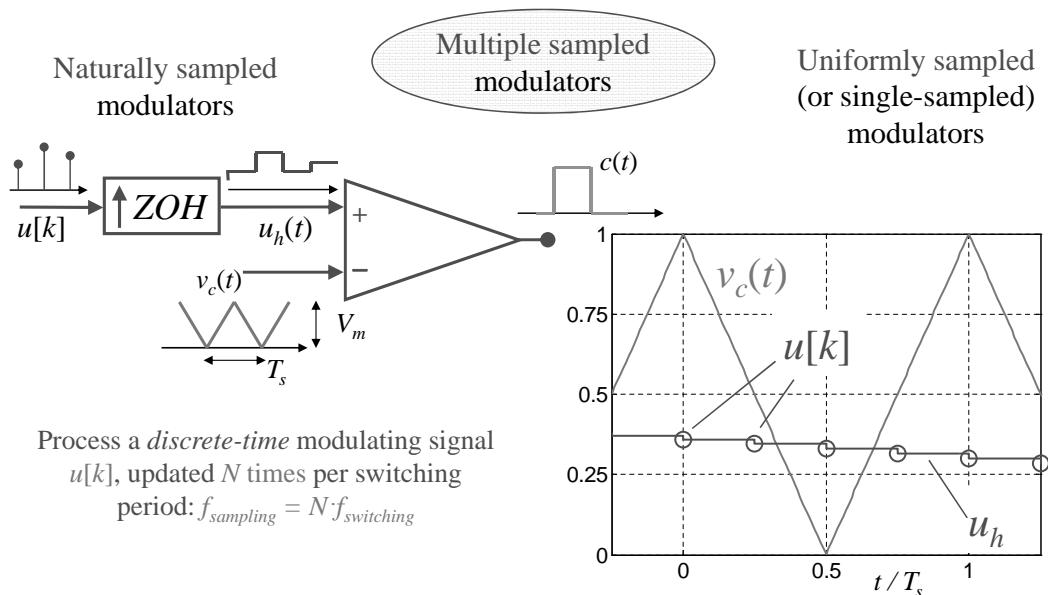


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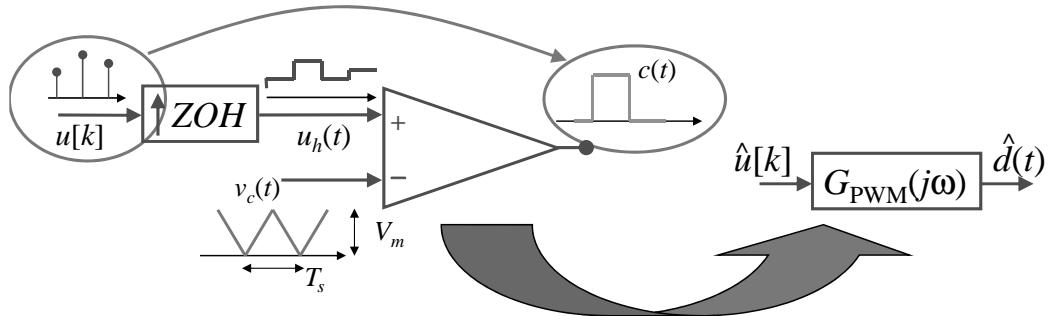


Three families of PWM modulators can be identified:



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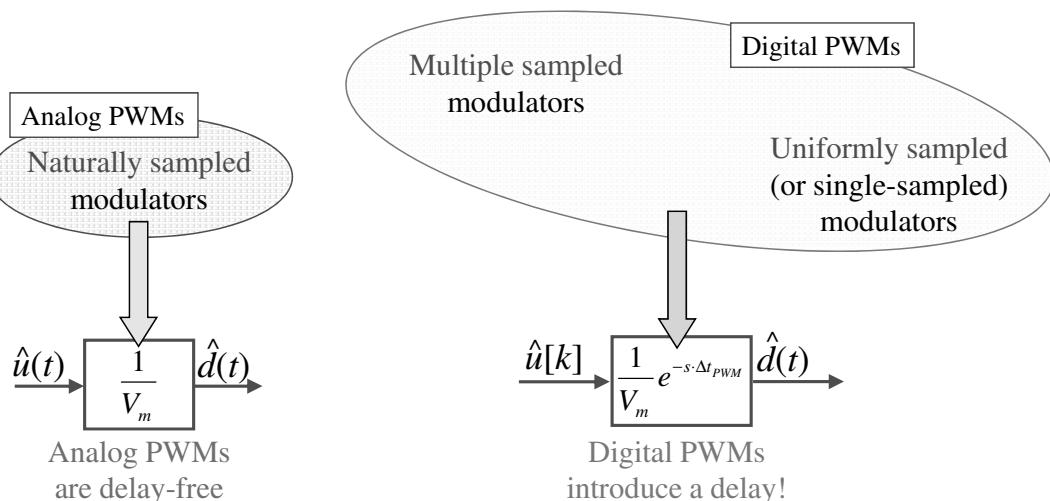
Finding the small-signal frequency response of a pulse-width modulator means [29]:

1. Applying a small sinusoidal perturbation at frequency ω to the modulating signal u
2. Calculating the Fourier component $d(t)$ of the PWM output $c(t)$ at frequency ω
3. Calculating the amplitude/phase relationship $G_{\text{PWM}}(j\omega)$ between d and u at frequency ω

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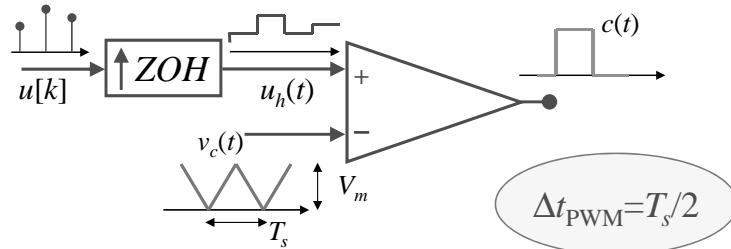
Small-signal PWM analysis – summary of main results



L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

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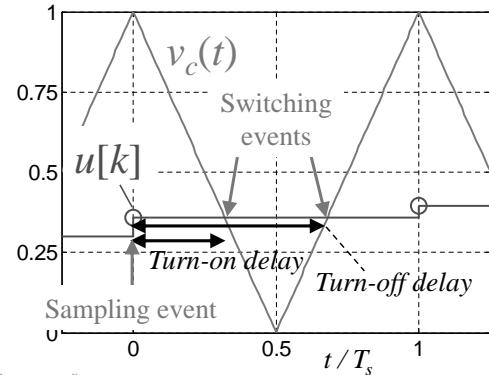
Physical Origin of PWM Delay



Uniformly sampled modulators:
 $d(t)$ is *delayed* with respect to $u[k]$:

$$\hat{u}[k] \rightarrow \frac{1}{V_m} e^{-s \cdot \Delta t_{\text{PWM}}} \hat{d}(t)$$

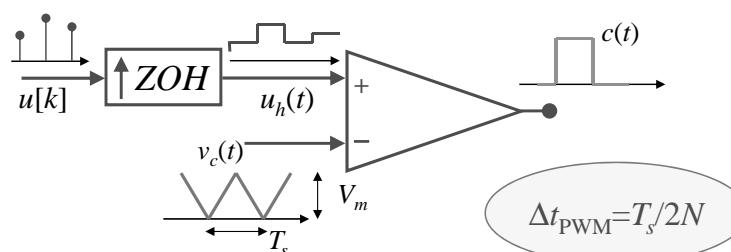
Physical origin of such delay is the difference between the sampling instant and the switching instants



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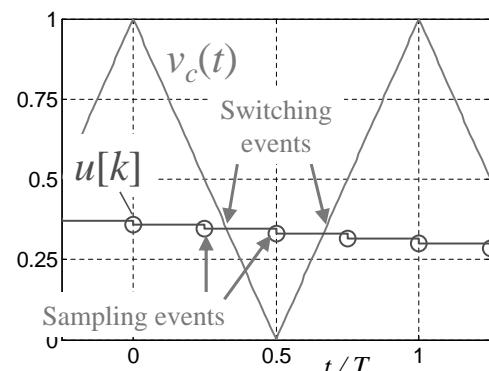
25

Physical Origin of PWM Delay



Multiple sampled modulators:
 $d(t)$ still delayed with respect to $u[k]$, but difference between sampling and switching event is reduced.

➔ In a multisampled modulator, delay is reduced because of the increased sampling rate.

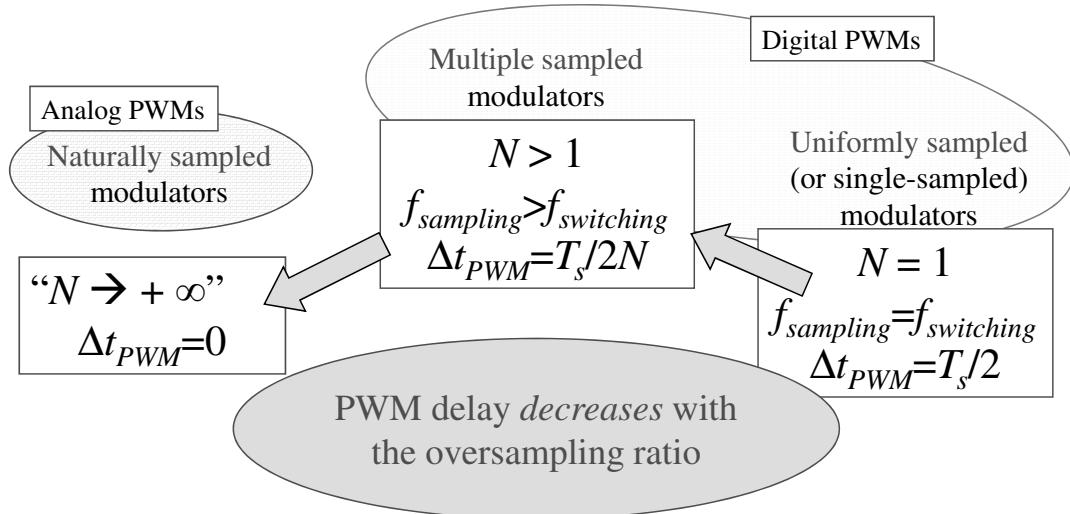


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$N = f_{sampling}/f_{switching}$ represents the number of times the modulating signal is updated within the switching period

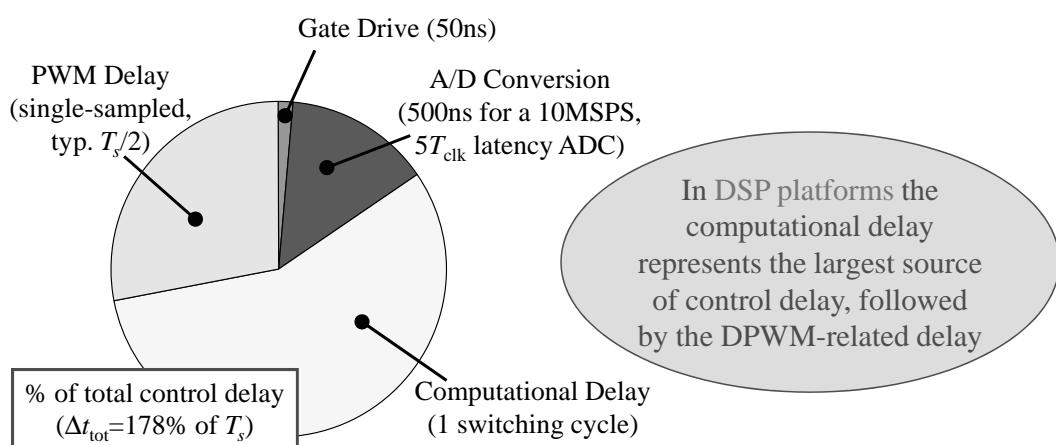


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- Example: $f_{switching} = 500$ kHz application, $f_c = f_s/10$ control bandwidth
- Relative importance of various control delays:

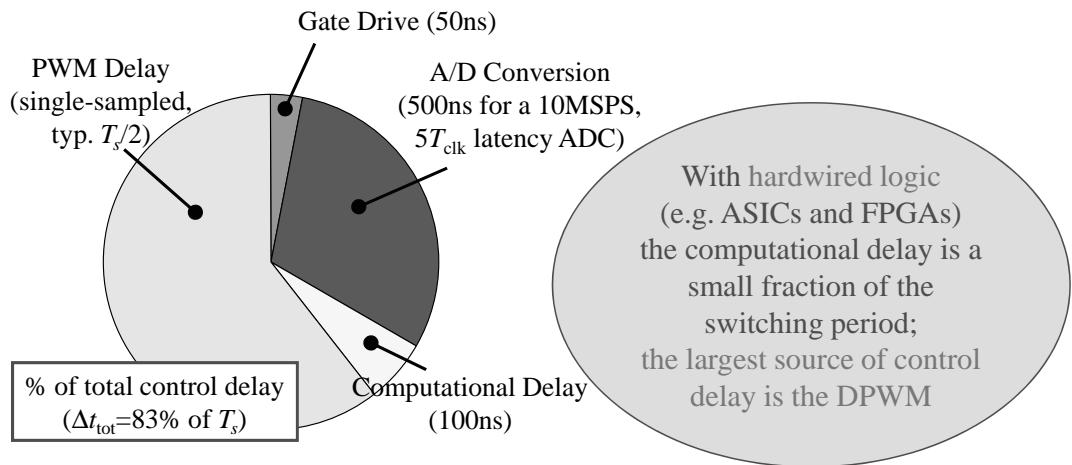


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- Example: $f_{\text{switching}} = 500 \text{ kHz}$ application, $f_c = f_s/10$ control bandwidth
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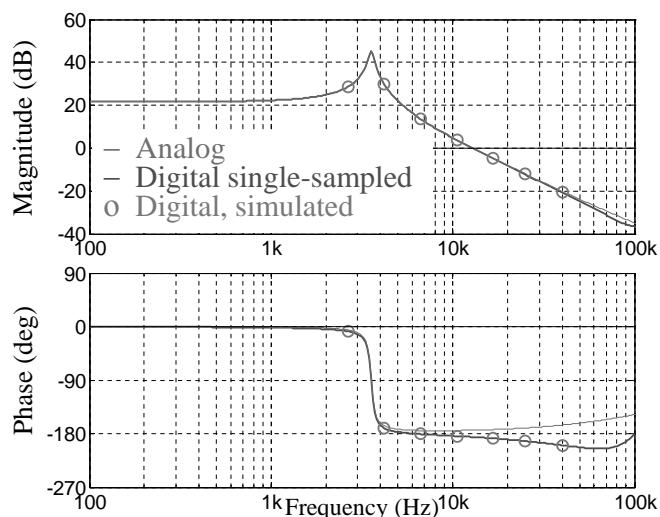
29

Example: Single- vs. Multi-sampled Dynamics



Design example: 12 V–5 V, 50 W synchronous Buck converter

$L=2 \mu\text{H}$, $r_L=2 \text{ m}\Omega$, $C=1 \text{ mF}$, $\text{ESR}=1 \text{ m}\Omega$, $f_{\text{switching}}=200 \text{ kHz} = f_{\text{sampling}}$



Comparison between digital and analog control-to-output transfer function reveals the larger phase lag of the former, due to the PWM delay



Bandwidth limitation!

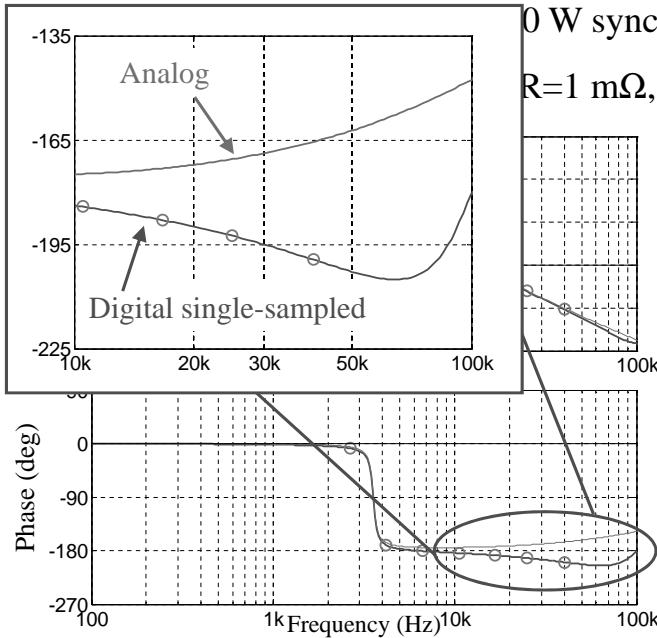
PWM-related delays may severely degrade achievable performances in digitally controlled SMPS!

L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

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Example: Single- vs. Multi-sampled Dynamics



0 W synchronous Buck converter

$R=1 \text{ m}\Omega, f_{\text{switching}} = 200 \text{ kHz} = f_{\text{sampling}}$

Comparison between digital and analog control-to-output transfer function reveals the larger phase lag of the former, due to the PWM delay



Bandwidth limitation!

PWM-related delays may severely degrade achievable performances in digitally controlled SMPS!

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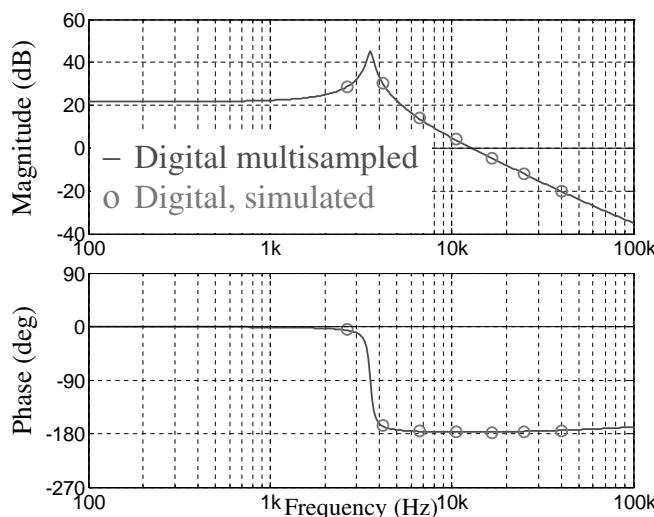


Example: Single- vs. Multi-sampled Dynamics



Design example: 12 V–5 V, 50 W synchronous Buck converter

$f_{\text{switching}} = 200 \text{ kHz}, f_{\text{sampling}} = 4 \times f_{\text{switching}} = 800 \text{ kHz}$



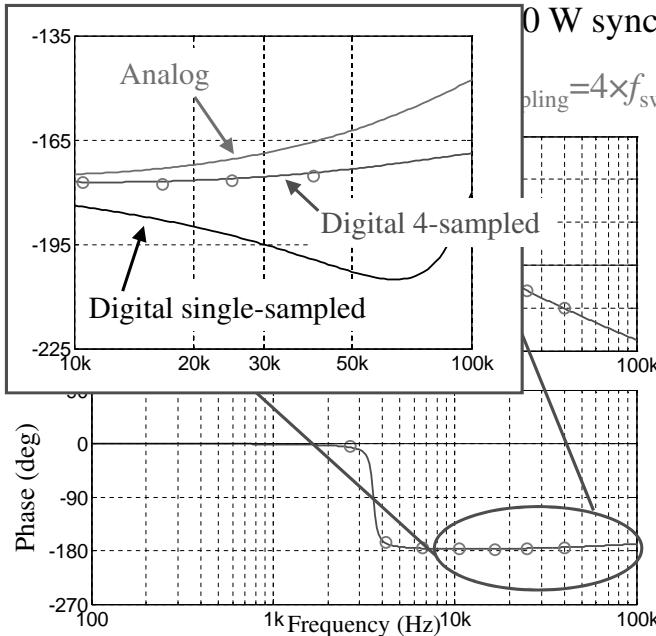
The increased sampling frequency reduces the PWM-related delay by a factor N

System better "approximates" analog behavior

L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

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Example: Single- vs. Multi-sampled Dynamics



0 W synchronous Buck converter

$$f_{\text{sampling}} = 4 \times f_{\text{switching}} = 800 \text{ kHz}$$

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L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

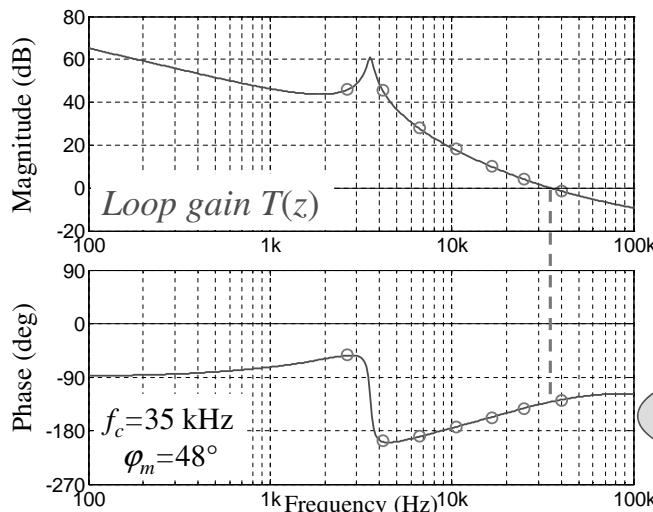
33

Example: Single- vs. Multi-sampled Dynamics



Design example: 12 V–5 V, 50 W synchronous Buck converter

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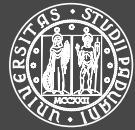
High-bandwidth design!

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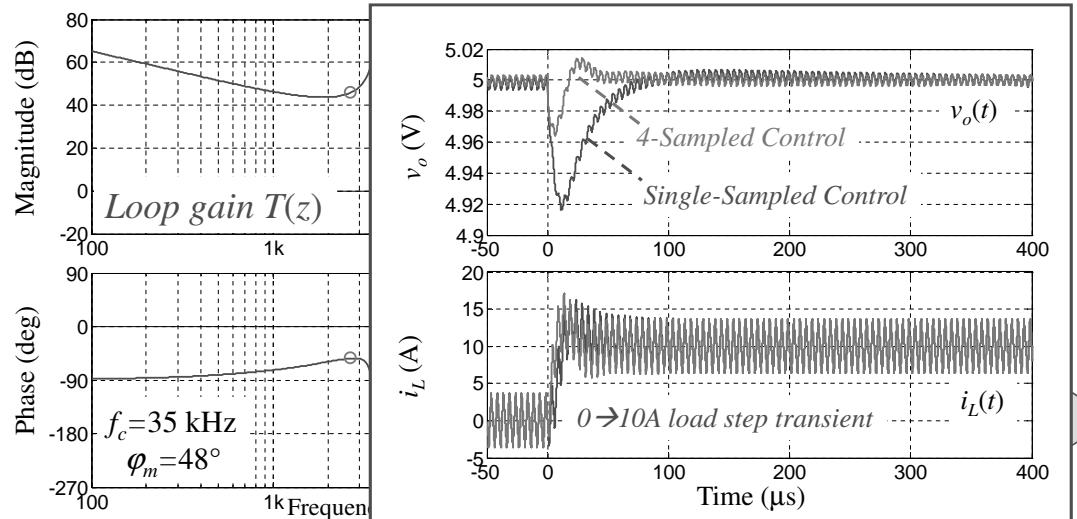


Example: Single- vs. Multi-sampled Dynamics



Design example: 12 V–5 V, 50 W synchronous Buck converter

$$f_{\text{switching}} = 200 \text{ kHz}, f_{\text{sampling}} = 4 \times f_{\text{switching}} = 800 \text{ kHz}$$



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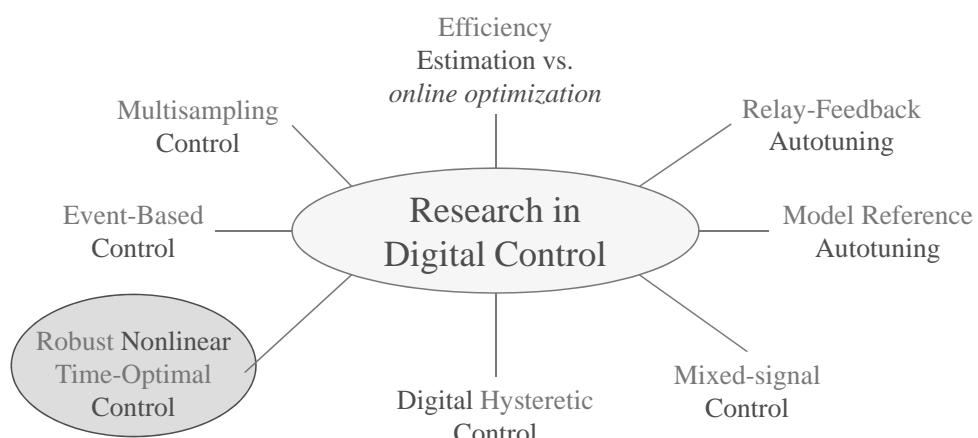


Research in Digital Control of High-Frequency Power Converters



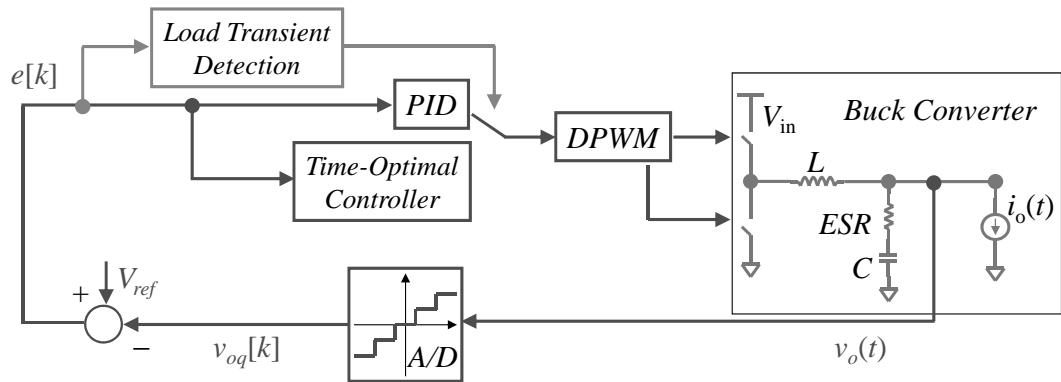
Focus on high-performance, low hardware complexity control solutions capable to:

1. Be competitive against well-established analog controllers
2. Offer new features, not available with analog ICs



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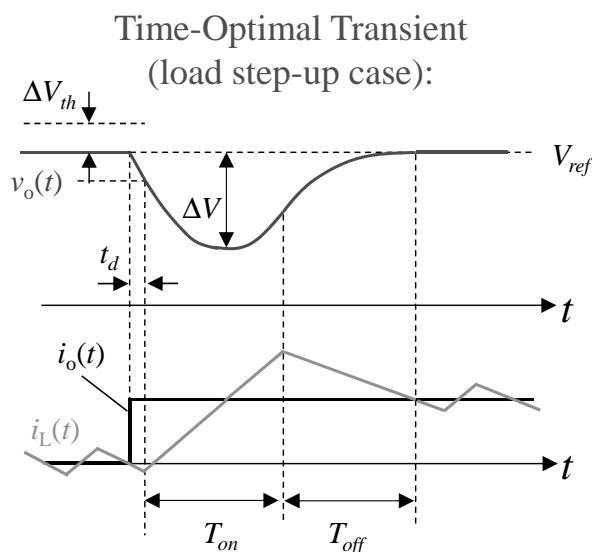
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- A conventional PID controller is active during normal operation
- A nonlinear time-optimal controller (TOC) takes over when a load change is detected
- The TOC control recovers the voltage error with a single on/off switching action

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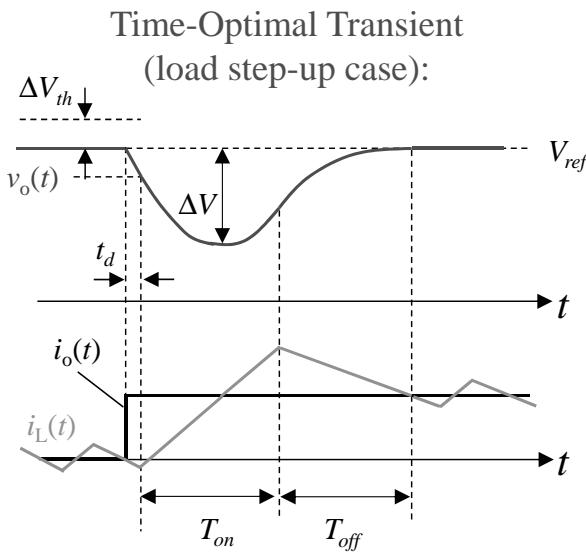


Once the load change is detected:

1. Primary switch is turned on for a time interval T_{on}
2. Primary switch is turned off (and synchronous switch is turned on) for a time interval T_{off}
3. If T_{on} and T_{off} are properly timed, the output voltage is brought back to regulation in minimum time

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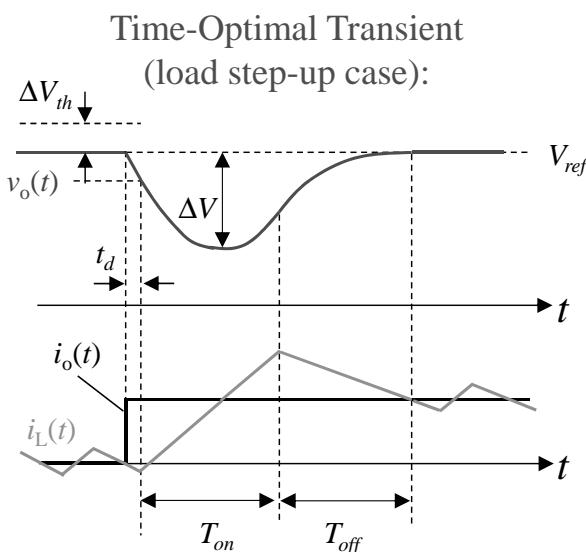
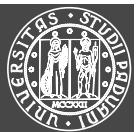


Fastest transient response of a given Buck converter:

- Dynamic capabilities of the converter are exploited to their limit
- Required output filter capacitance is minimized for a given specification on ΔV !

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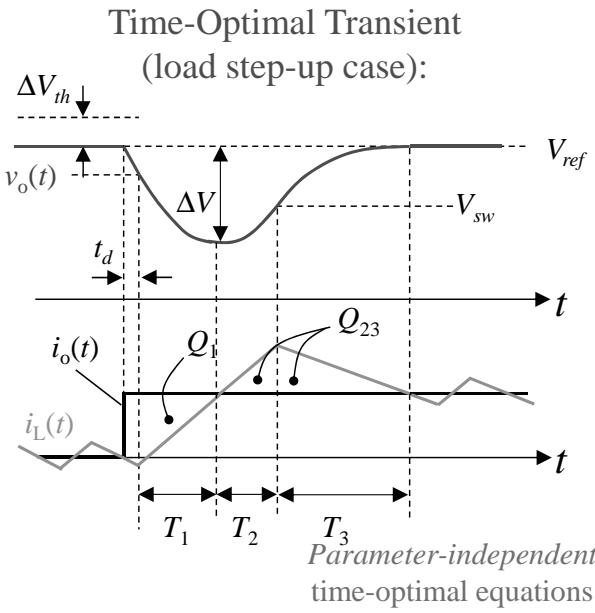
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- Both T_{on} and T_{off} depend on the power stage parameters.
- However, it is possible to realize a Time-Optimal switching sequence without preliminary knowledge of the power stage parameters, as long as times and voltages can be measured "on the fly" during the transient.

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Principles involved (assume $t_d=0$):

$$Q_1 + Q_{23} = 0$$

Charge balance,
does not depend on C

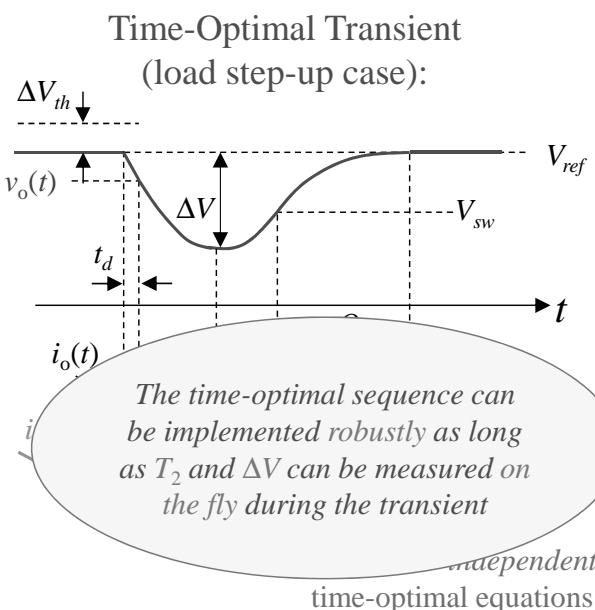
$$i_L(T_1) = i_L(T_1 + T_2 + T_3)$$

Volt-second balance,
does not depend on L

$T_3 = \frac{1-D}{D} T_2$
 $V_{sw} = V_{ref} - (1-D)\Delta V$

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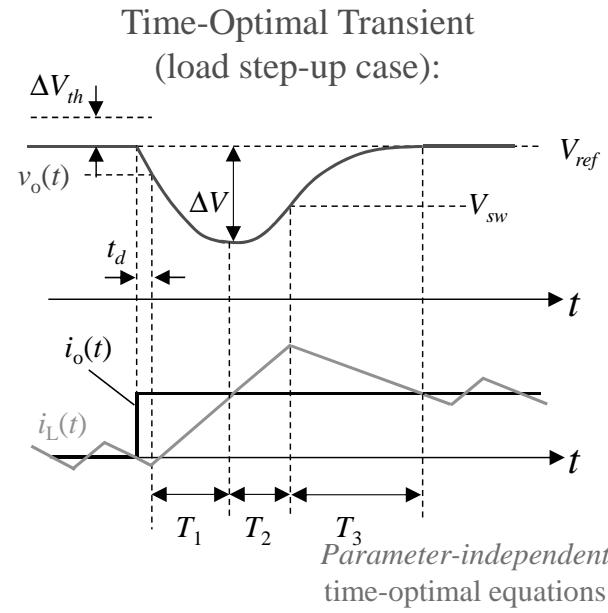
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Robust time-optimal sequence:

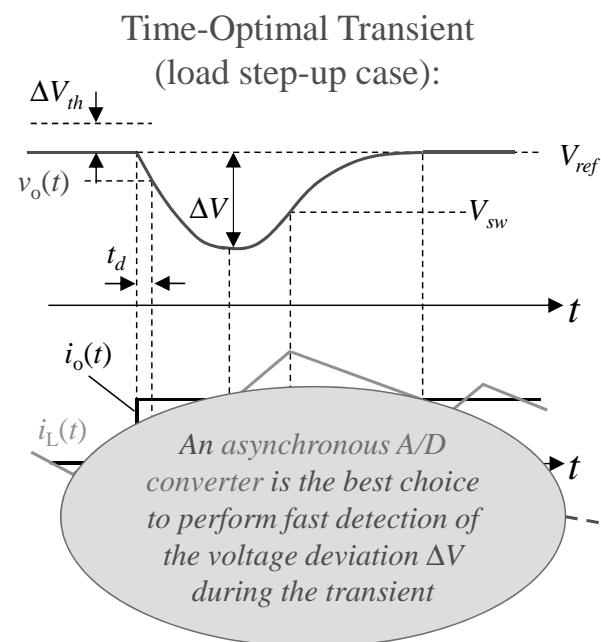
1. Upon transient detection, turn primary switch on
2. At the valley point, measure the value of output voltage deviation ΔV and calculate V_{sw}
3. Measure time interval T_2 as $v_o(t)$ reaches V_{sw}
4. At $v_o(t)=V_{sw}$, turn switch off and calculate T_3
5. At the end of T_3 , return to PID operation

$$T_3 = \frac{1-D}{D} T_2$$

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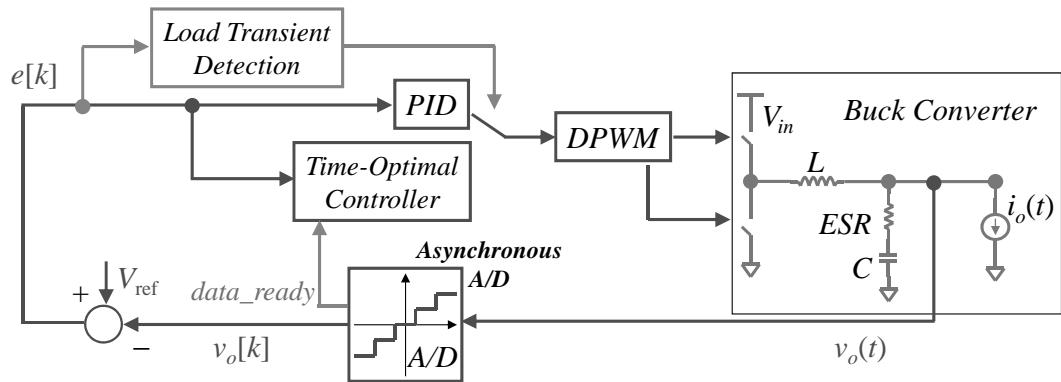
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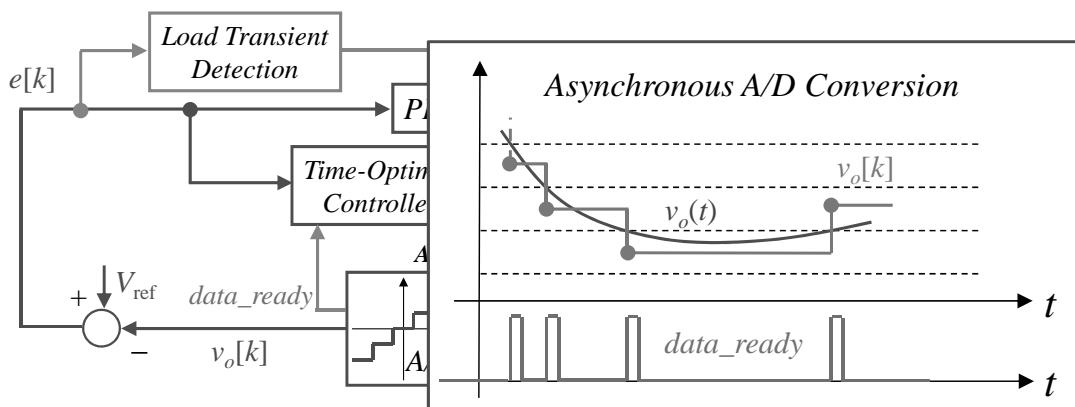
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- An asynchronous A/D converter quantizes the output voltage as soon as it crosses a quantization level
- A *data_ready* flag is asserted upon every conversion
- Viable approach for fast acquisition during the Time-Optimal Transient

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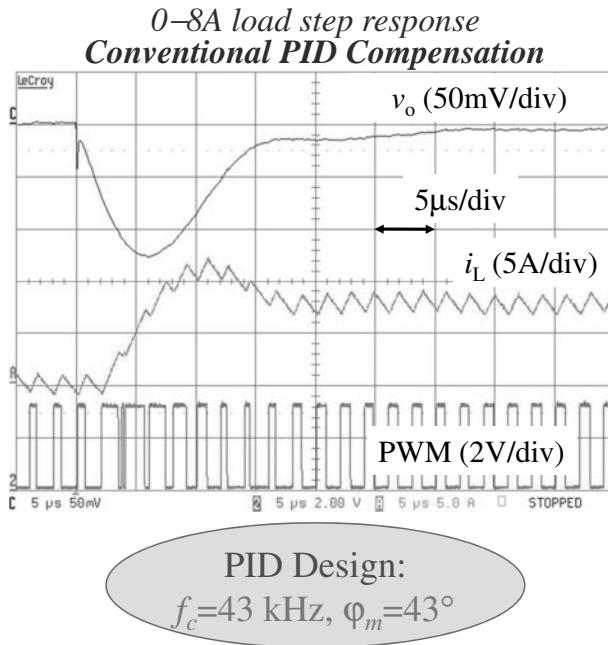


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Experimental Results: Conventional PID Control



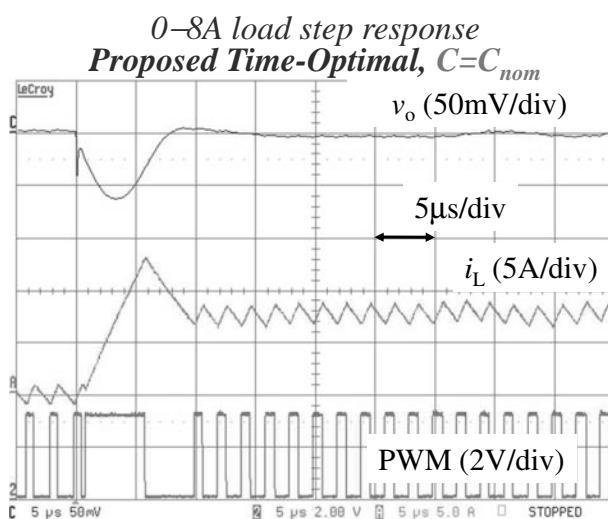
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Experimental case study:

- 5 V – 1.6 V synchronous buck, $f_s=500 \text{ kHz}$, $L=1.1 \mu\text{H}$, $C_{nom}=250 \mu\text{F}$ (ceramic)
- Asynchronous A/D quantization step $\Delta q=3 \text{ mV}$
- Load detection threshold $\Delta V_{th}=12 \text{ mV}$
- Experimental tests:
 - Conventional PID
 - Proposed Time-Optimal, Voltage Based Approach
 - Tests for different values of the output capacitance

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Experimental Results: Time-Optimal Control



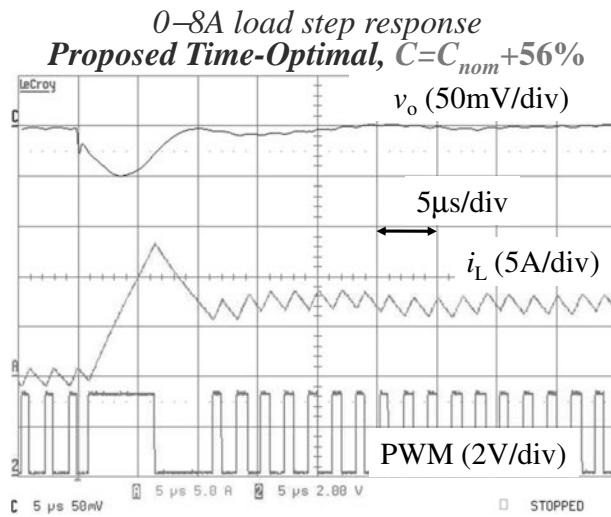
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Experimental Results: Time-Optimal Control



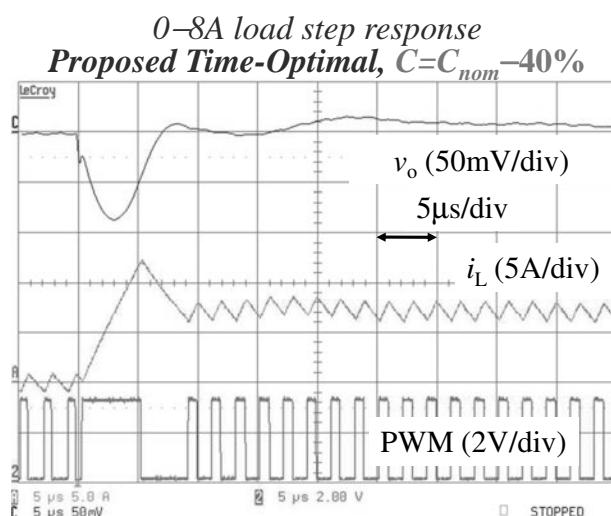
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Experimental Results: Time-Optimal Control

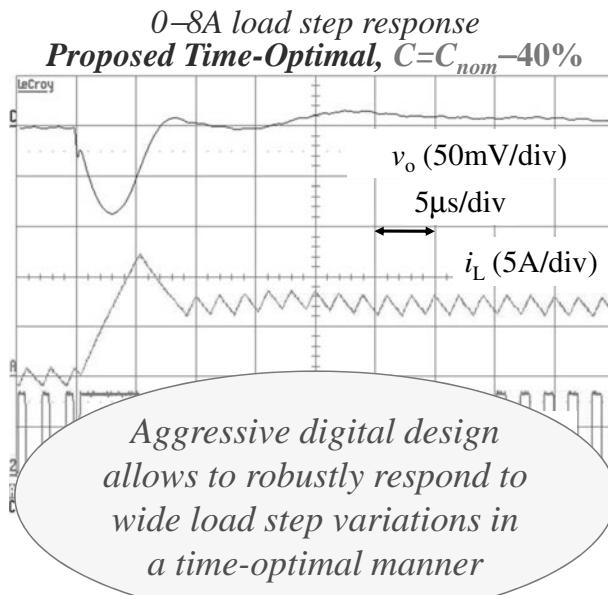
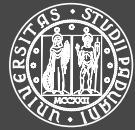


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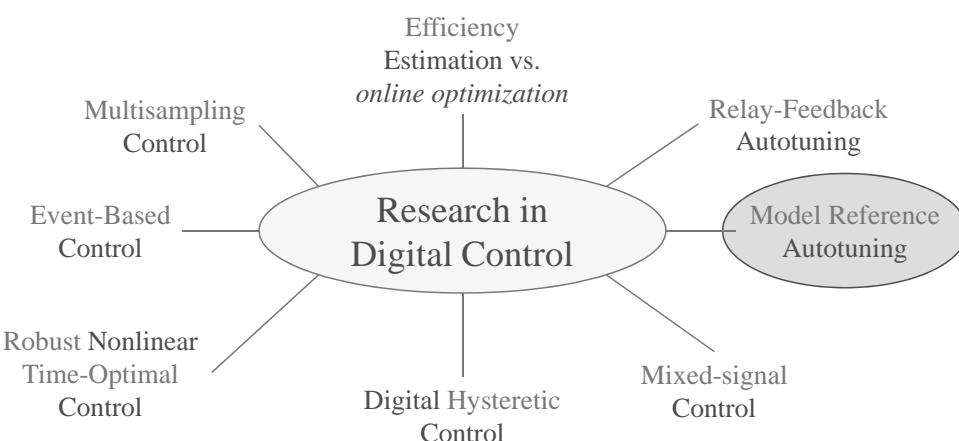
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Focus on high-performance, low hardware complexity control solutions capable to:

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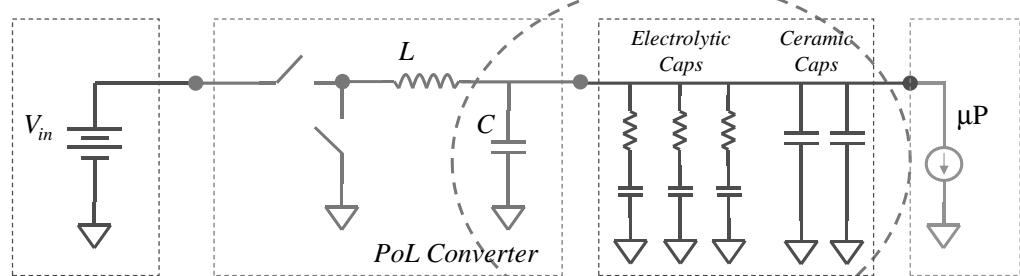


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Digital Autotuning



Design challenges
in Point-of-Load converters:

- Number, types and values of load decoupling capacitors often unknown to the designer
- Component tolerances
- Temperature variations or aging

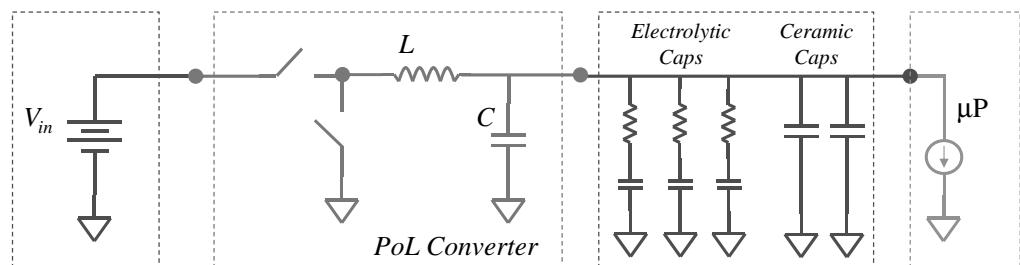
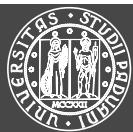
Equivalent capacitance and ESR may vary over orders of magnitude

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Digital Autotuning



Control design approaches

Standard, worst case design:

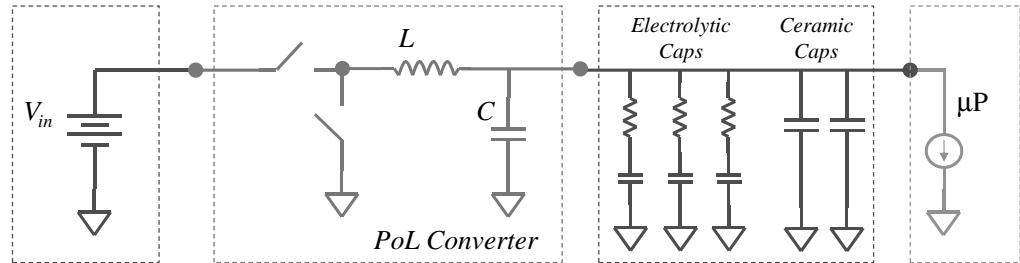
- Must accept significant penalties in closed loop performances
- Unable to track process parametric variations

Self-tuning digital controllers:

- *Optimized* closed loop bandwidth while maintaining proper stability margins
- *Online tuning* is possible to track process variations

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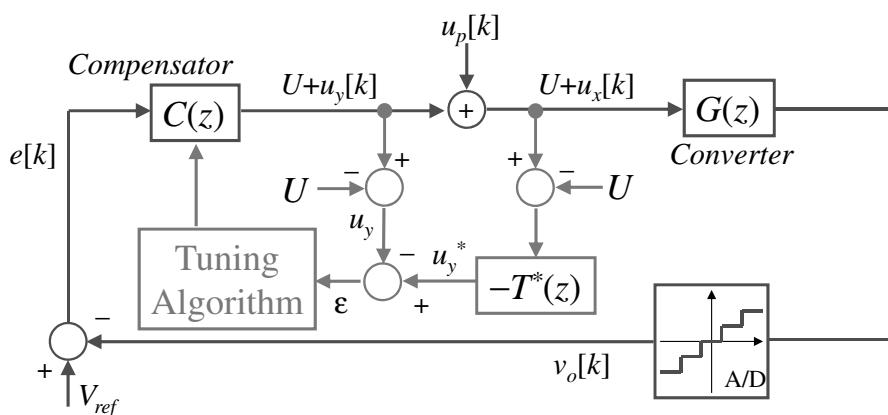


Objectives of the tuning algorithm

- Determine the compensator parameters in order to meet proper stability margins, and ensure adequate dynamic performances.
- Typically:
 - Phase margin $\phi_m = \phi_m^*$
 - Loop gain crossover frequency $f_c = f_c^*$

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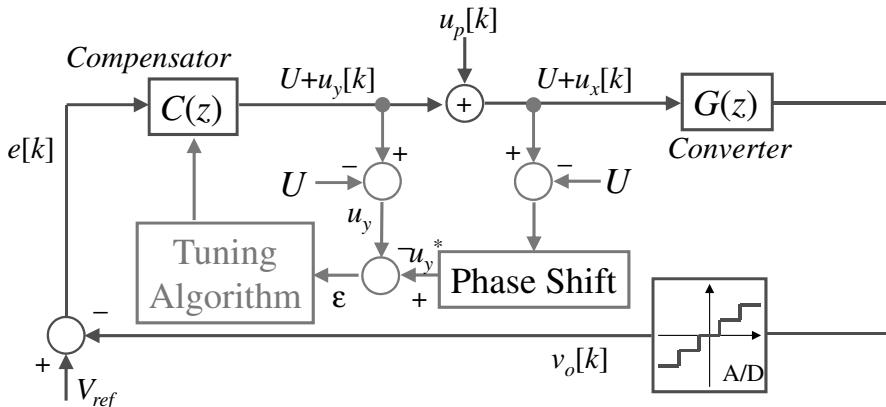
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- In closed-loop configuration, an input perturbation $u_p[k]$ is superimposed to the modulating signal
- The model reference expresses the desired system loop gain: $T^*(z) = C^*(z)G^*(z)$

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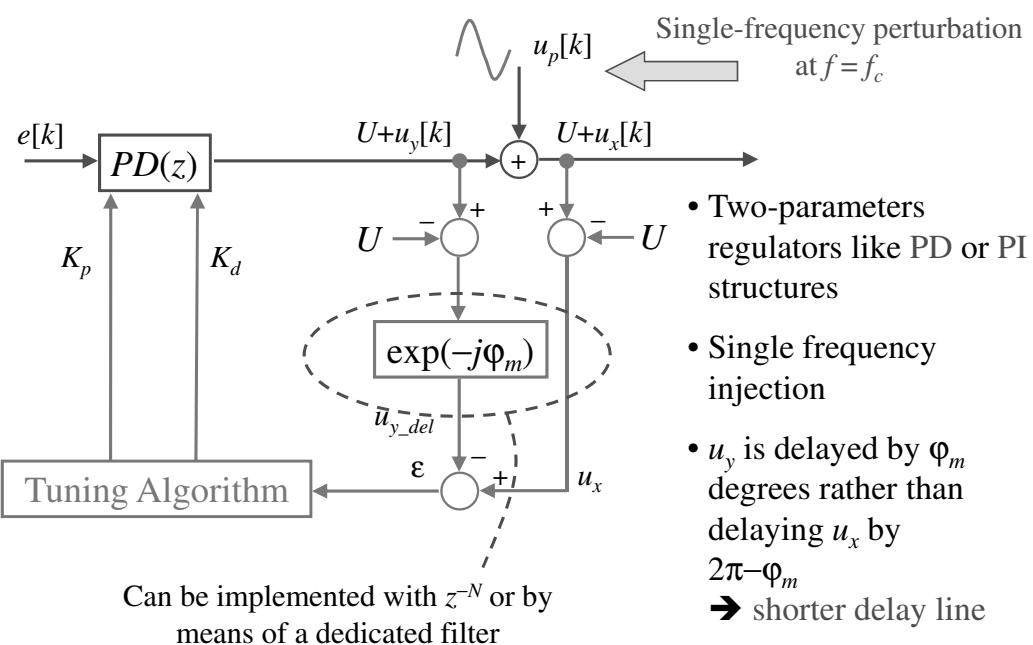


- Rather than forcing condition $T(z) = T^*(z)$ at every frequency, it is imposed only at the desired crossover frequency f_c . Therefore, the model reference reduces to a simple phase shift:

$$T^*(f_c) = e^{-j(\pi - \varphi_m)} = -e^{j\varphi_m}$$

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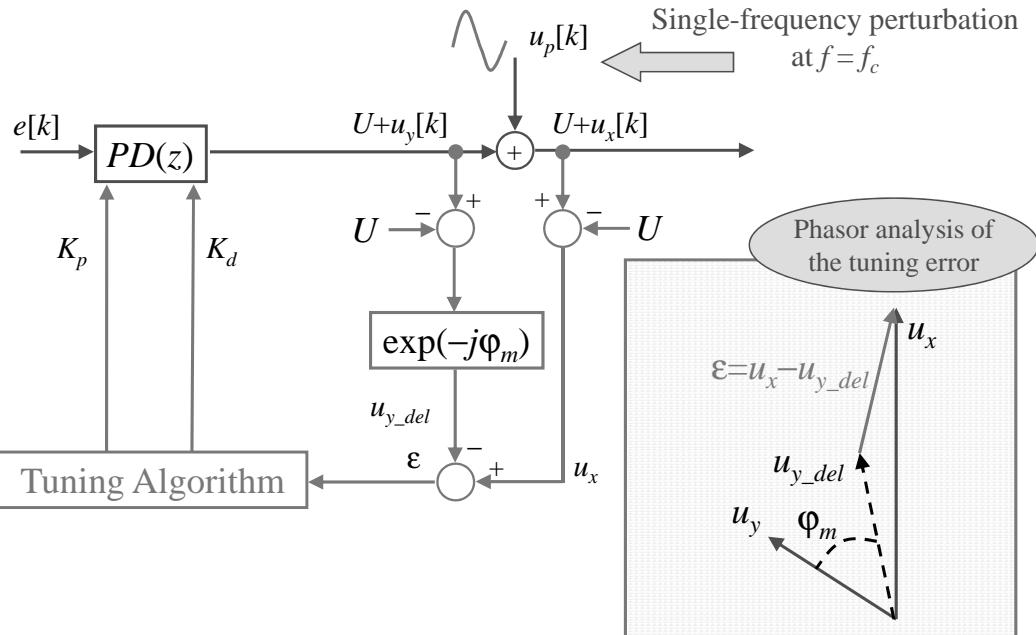
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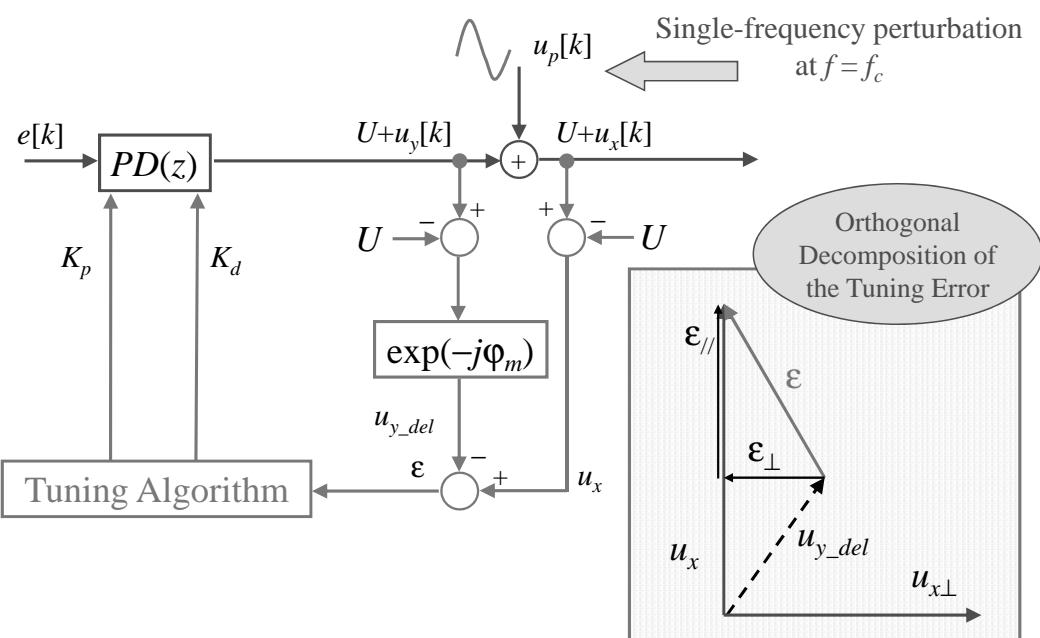
Application to Two-Parameters Regulators (PD or PI)



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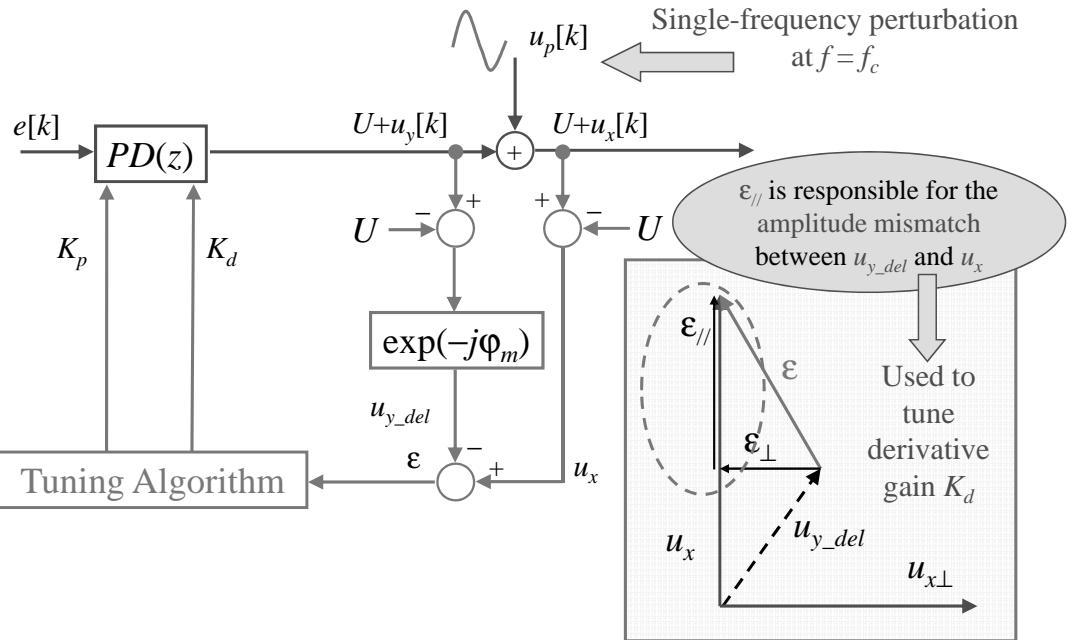
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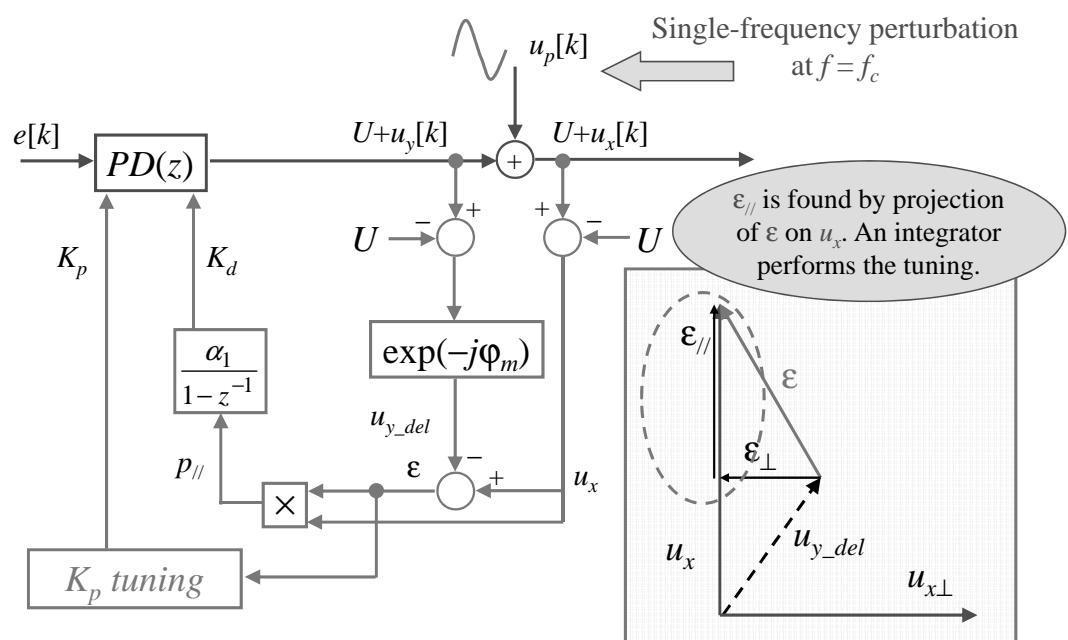
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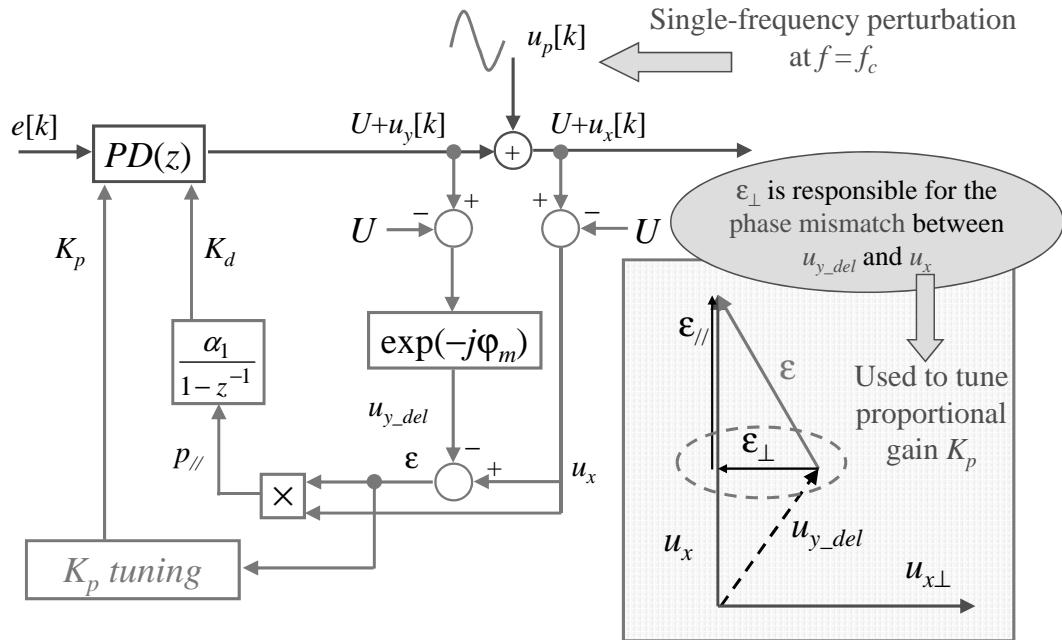
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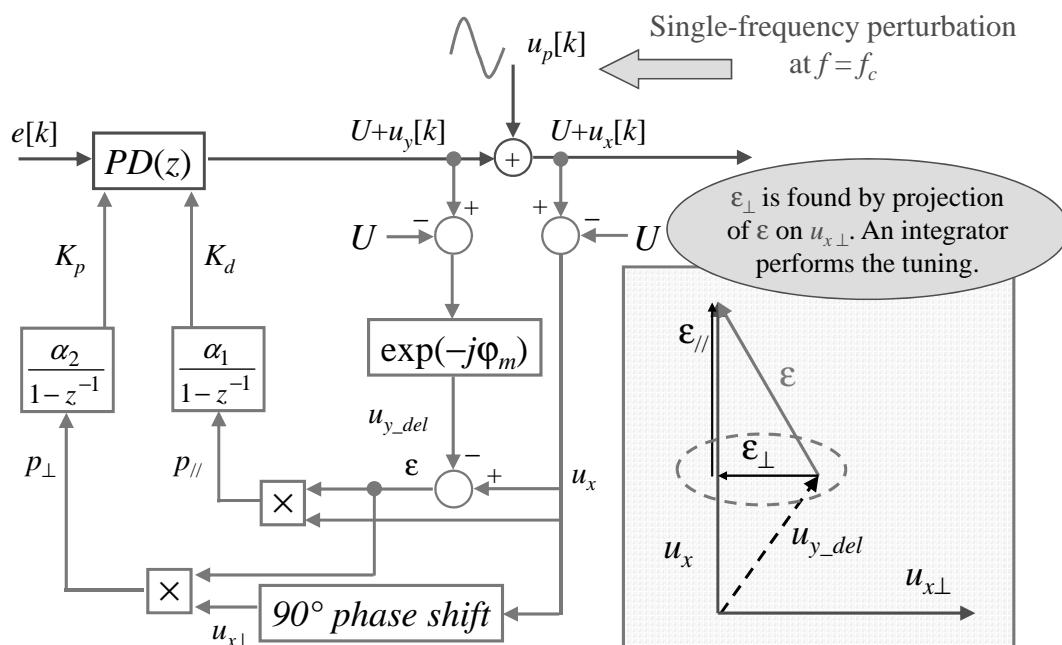
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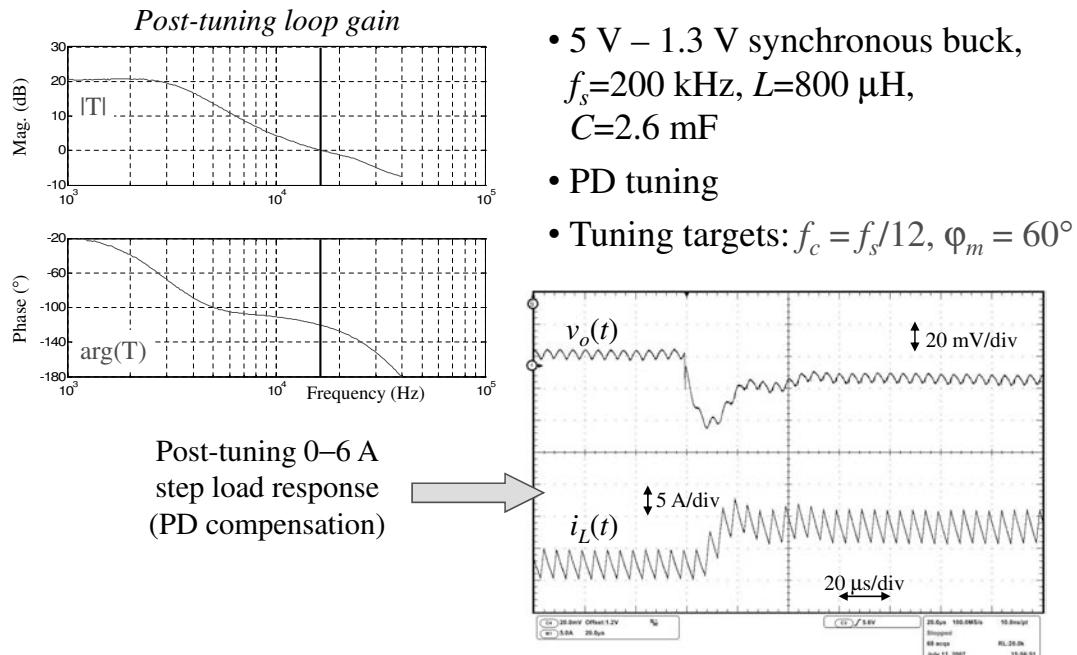
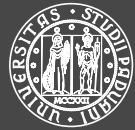
Application to Two-Parameters Regulators (PD or PI)



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Experimental Example



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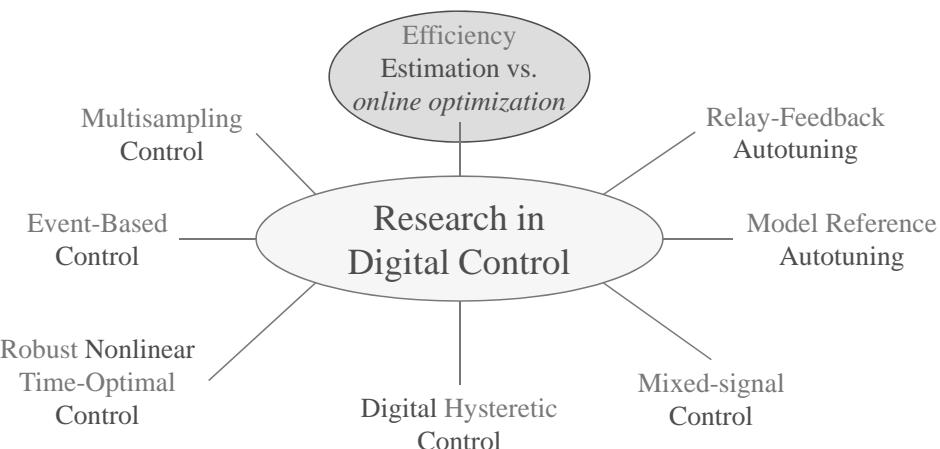
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Research in Digital Control of High-Frequency Power Converters



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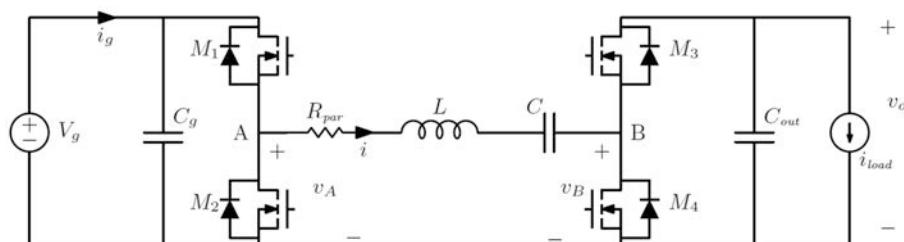
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- Traditional approach to efficiency improvement:
 - "Optimization" carried out during the design phase and limited to a specific operating point or narrow operating range
 - Often topological modifications/ancillary elements are required to mitigate efficiency loss outside the optimal range
 - Fixed modulation scheme → converter capabilities not fully exploited
- Digital online efficiency optimization:
 - Exploit converter degrees of freedom, dynamically adjust operation to reach and track the maximum efficiency point
 - No topological modifications, transfer additional complexity to the controller rather than to the (more expensive) power stage
 - Inherently exploit maximum efficiency of a given topology and for a given operating point (e.g. mixed soft/hard switching operation)
 - Advanced control / modulation strategies facilitated by the digital approach

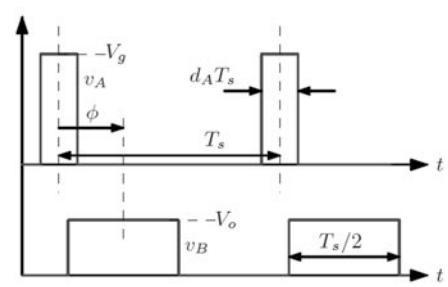
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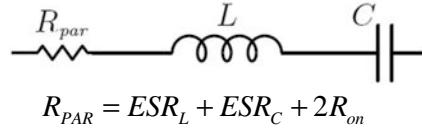
A number of degrees of freedom are offered by the DHB–SRC topology:

- Duty cycle d_A of first leg
- Duty cycle d_B of second leg
- Phase lag ϕ between control signals
- Switching frequency f_s

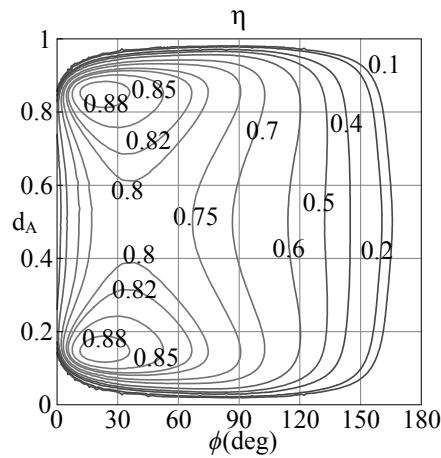
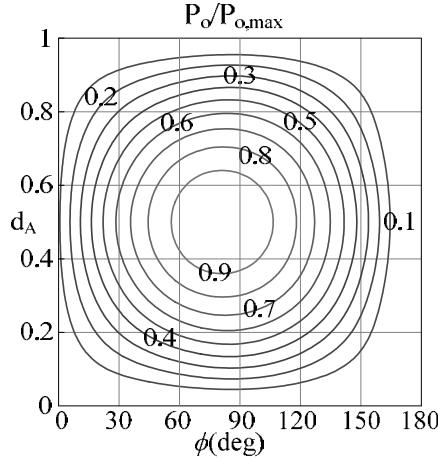


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$$\begin{cases} d_B = 0.5 \\ f_s = \text{constant} \end{cases}$$

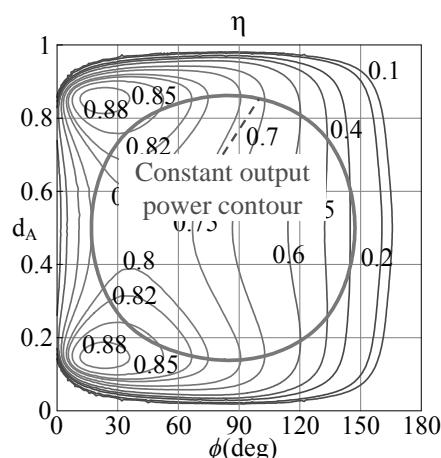
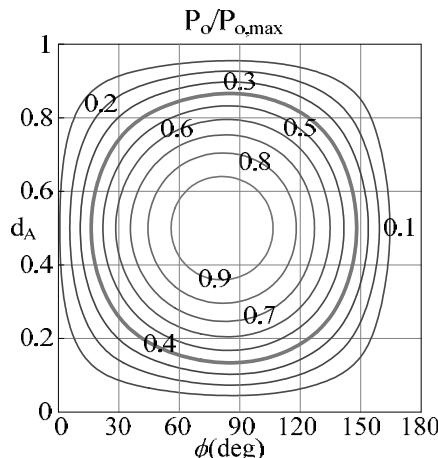


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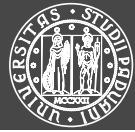


- Infinite (d_A, ϕ) configurations correspond to the *same* output power
- Among these, an optimal control input exists which maximizes efficiency

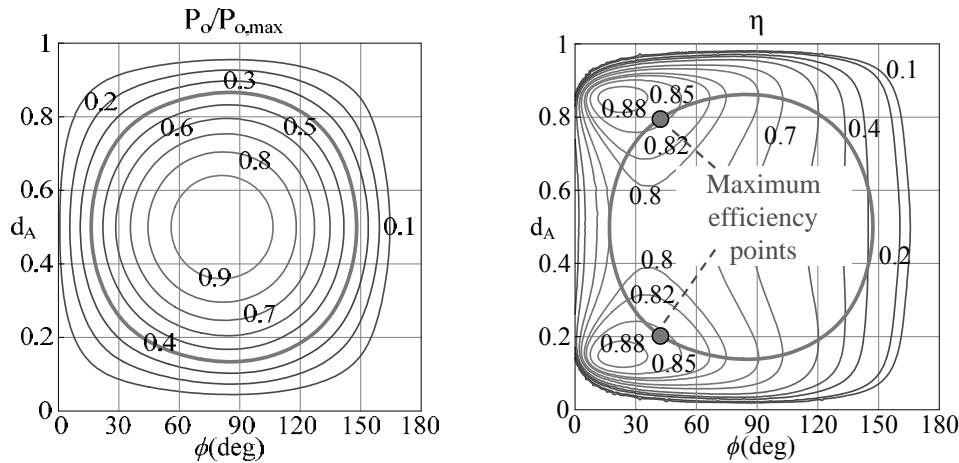


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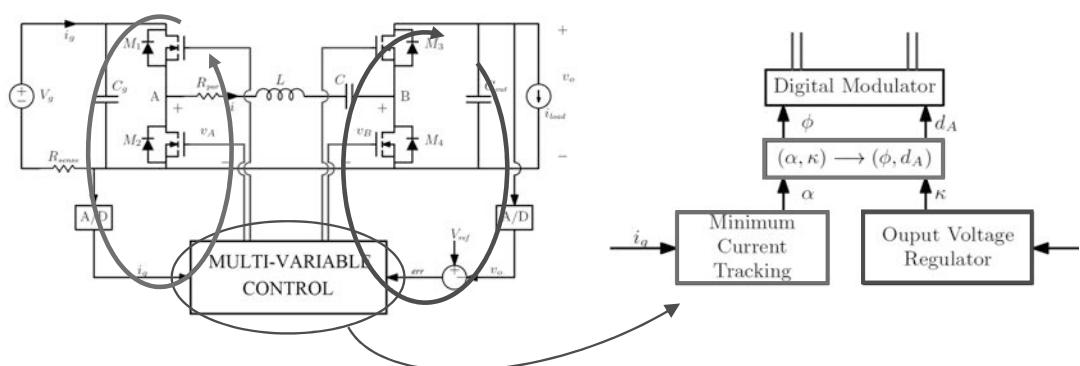


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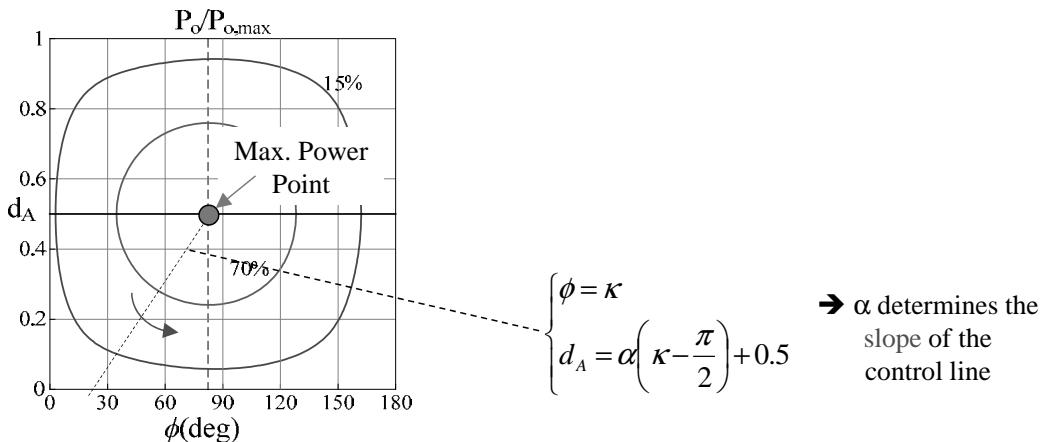
- Two loops:
 - Regulation loop (command κ) regulating the output voltage
 - Slower optimization loop (command α) minimizes the input current using a minimum current tracking algorithm (e.g. Perturb&Observe)
- Choice of the $(\alpha, \kappa) \rightarrow (\phi, d_A)$ map is crucial to the robustness of the control

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Control input is constrained to lie on a straight line passing through the maximum power point:

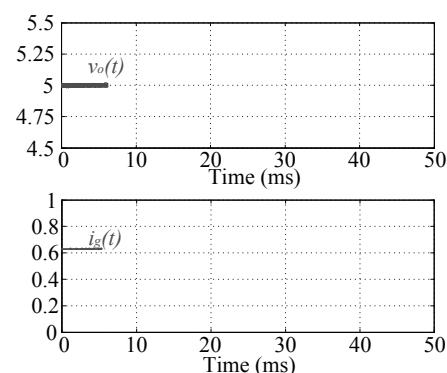
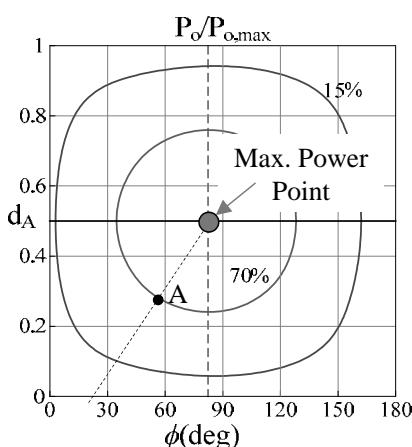


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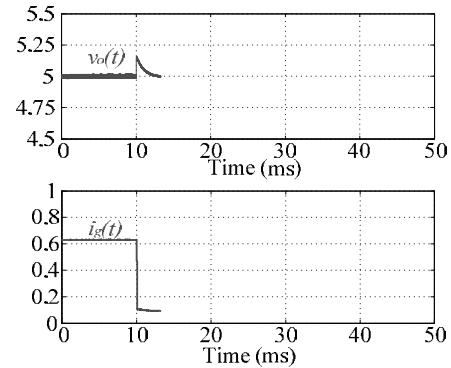
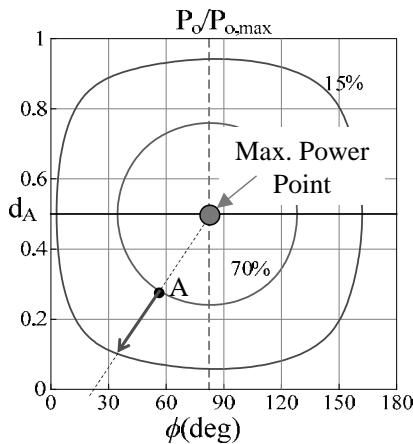
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Investigated Approach for Online Efficiency Optimization



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the maximum power point:



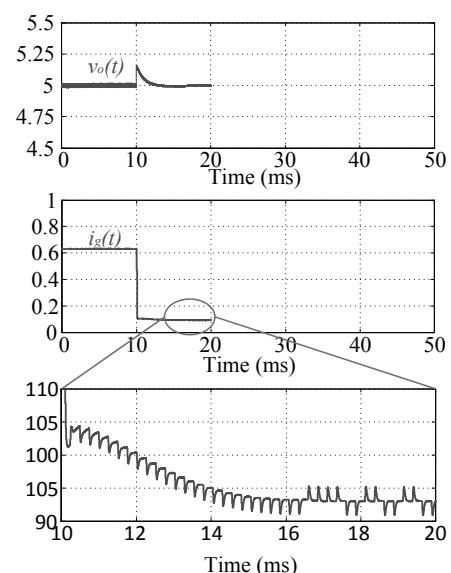
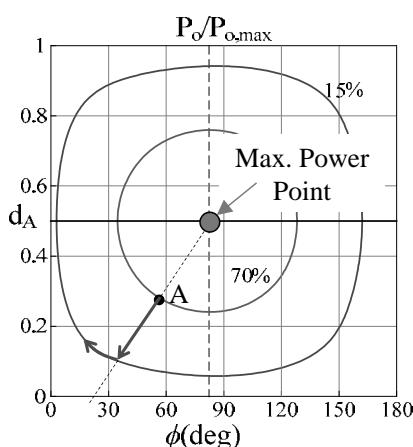
L. Corradini, "Digital Control of High-Frequency Switched-Mode dc-dc Converters"

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Investigated Approach for Online Efficiency Optimization



Control input is constrained to lie
on a straight line passing through
the maximum power point:

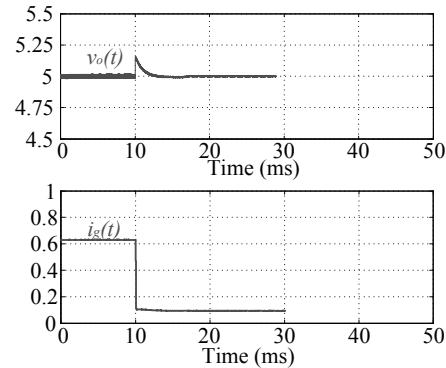
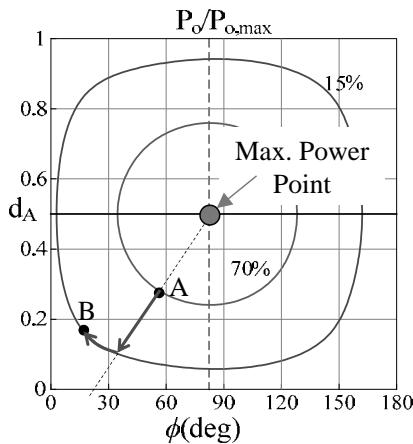


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Control input is constrained to lie on a straight line passing through the maximum power point:

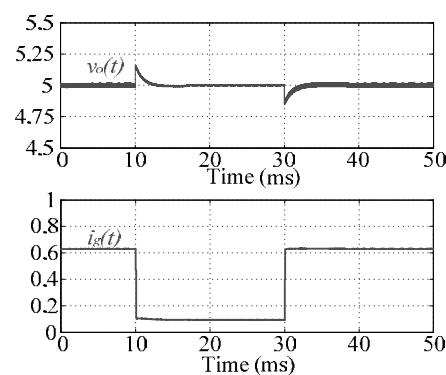
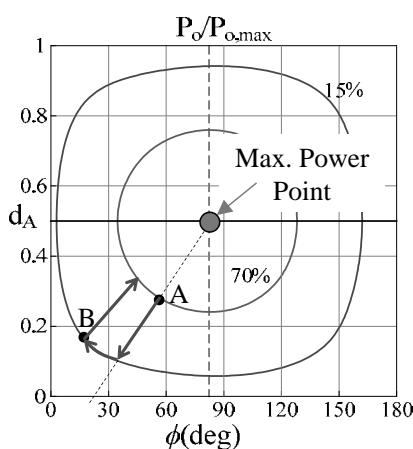


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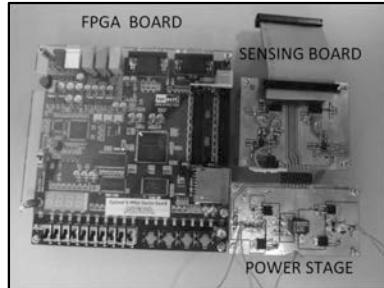
Control input is constrained to lie on a straight line passing through the maximum power point:



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Online Efficiency Optimization: Experimental Results

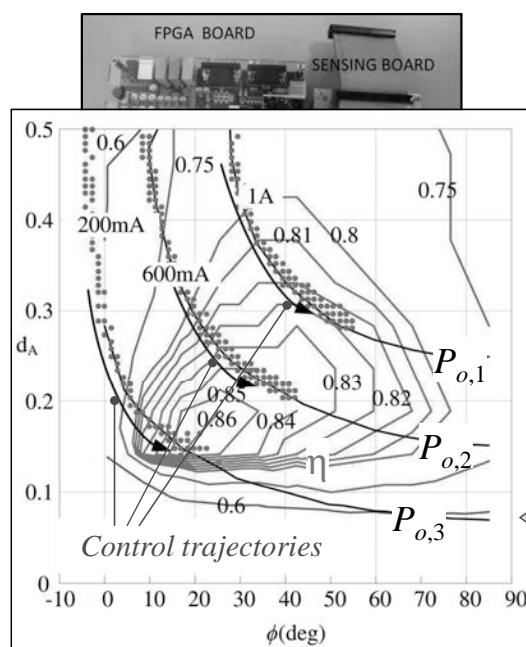


Switching frequency f_s	200 kHz
Input Voltage V_g	12 V
Output Voltage	5 V
Nominal output current	1 A
Tank capacitance	630 nF
Tank inductance	2.1 μ H
Equivalent tank resistance R_{par}	0.22 Ω
Input current sensing resistance	0.2 Ω

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Online Efficiency Optimization: Experimental Results



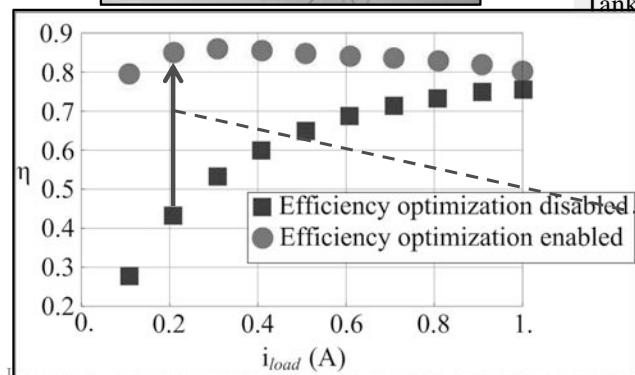
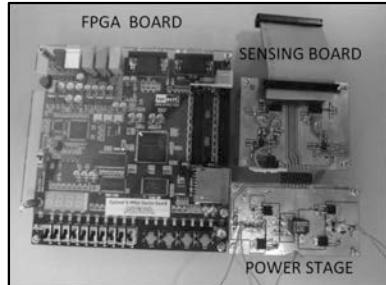
Switching frequency f_s	200 kHz
Input Voltage V_g	12 V
Output Voltage	5 V
Nominal output current	1 A
Tank capacitance	630 nF
Tank inductance	2.1 μ H
Equivalent tank resistance R_{par}	0.22 Ω
Input current sensing resistance	0.2 Ω

Efficiency optimization as
seen on the (d_A, ϕ) plane
(experimental)

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Online Efficiency Optimization: Experimental Results



Switching frequency f_s	200 kHz
Input Voltage V_g	12 V
Output Voltage	5 V
Nominal output current	1 A
Tank capacitance	630 nF
Tank inductance	2.1 μ H
Equivalent tank resistance R_{par}	0.22 Ω
Current sensing resistance	0.2 Ω

Efficiency Improvement

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Thank you for your kind attention!

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How to avoid most common mistakes in DCDC design

Voltage mode PWM fixed frequency

Vadim Ivanov

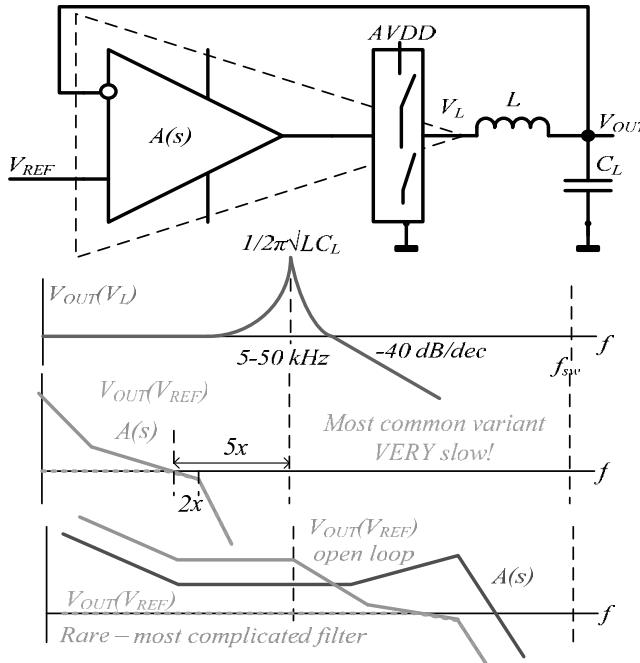
vivanov@ieee.org



Outline

- What is wrong with voltage mode and PWM?
- Customer expectations and external components selection
- Which operation mode to select?
- Structural design method basics.
- Inductor current measurement
- Error amplifiers and comparators
- Switching frequency control
- Conclusions

Voltage mode is a historic mistake



Voltage mode:

- Very slow
- or
- Very complicated

and always

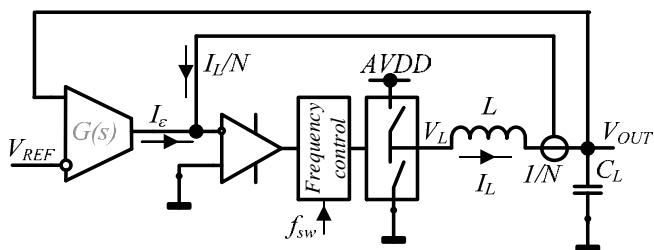
- Plenty of application-specific external compensation RC
- Compensation is sensitive to L and C_L variations

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DCDC control and circuit techniques

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Current mode



Very fast

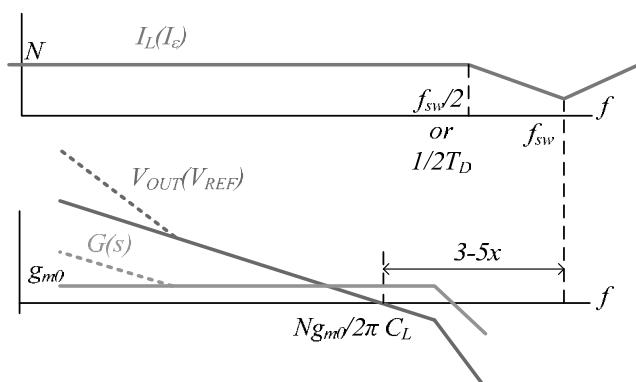
Very simple

No external, application dependent compensation components

Low sensitivity to L or C_L variations

- Need to measure I_L – but it has to be measured anyways

*What is duty ratio?
Who knows. It is just right.*



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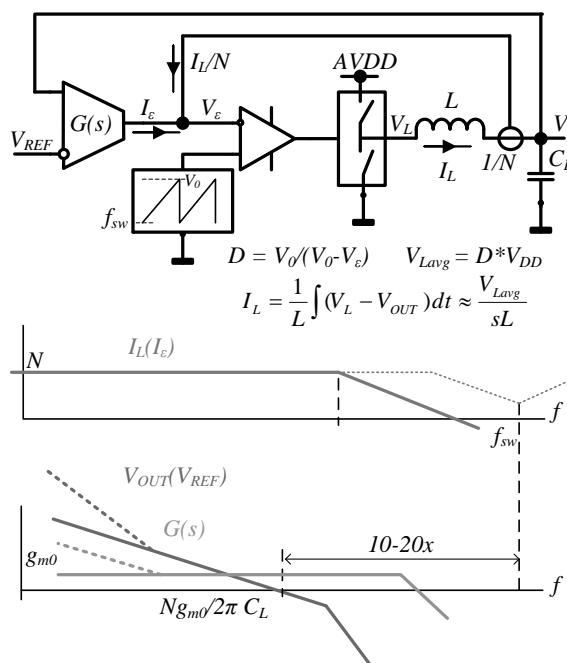
DCDC control and circuit techniques

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Current mode flavors

- Voltage hysteretic (buck converters only)
- Current hysteretic (ripple)
- Fixed T_{ON}
- Fixed T_{OFF}
- Min T_{ON}/T_{OFF}
- Peak current
- Valley current
- Average current per period
- Charge transfer

PWM: “common sense” nonsense



We got an extra pole!

Location depends on $AVDD$, V_0 , L

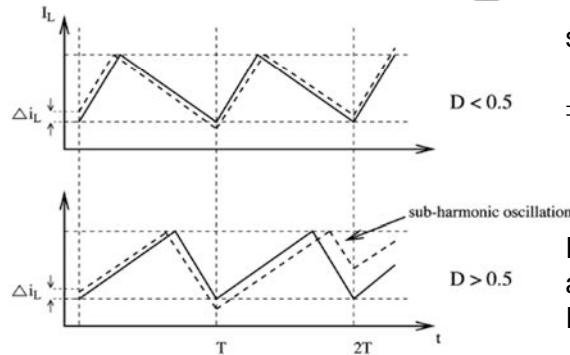
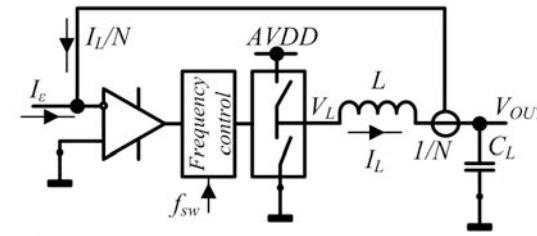
- Extra cell: more complexity, more consumption

- Decreased speed

- Complicated compensation

+ “Common sense”

Forced frequency → chaos



System has its own delays and inherent oscillation frequency

When clock is forced upon it – we can expect problems

These problems manifest as pulse skipping and subharmonic oscillations

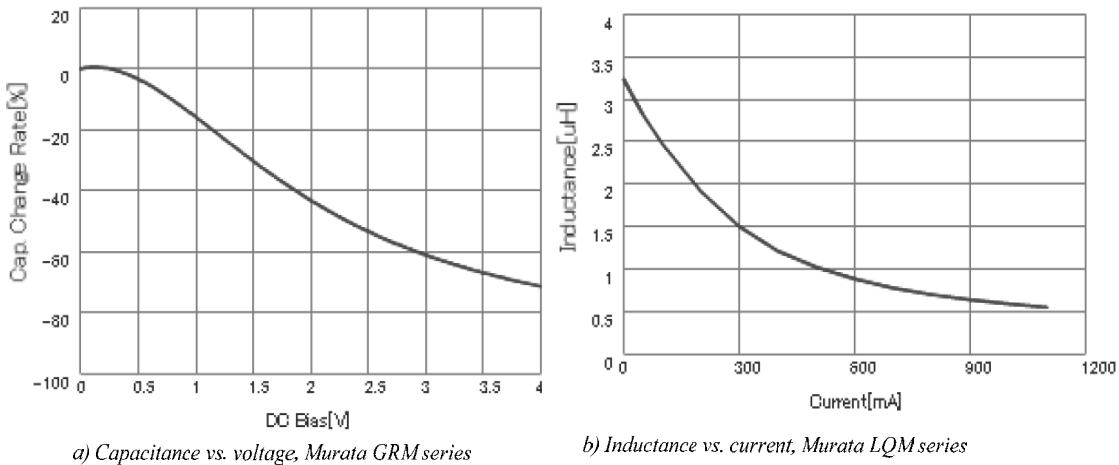
⇒ Say NO to imposed clock. When required, adjust system delays so frequency is what desired

Fixed clock is hardly a requirement in almost any application.
It is just a tradition

Customer expectations

- Cost
 - Cheap (monolithic) inductors
 - Cheap input/load capacitors
 - No other external components aloud
- Solution size
 - Small inductors & caps => high switching frequency
- Interference to surroundings (EMI, RF noise, supply noise)
- Accuracy, V_{OUT} ripples, etc.

Inductors and capacitors nonlinearity



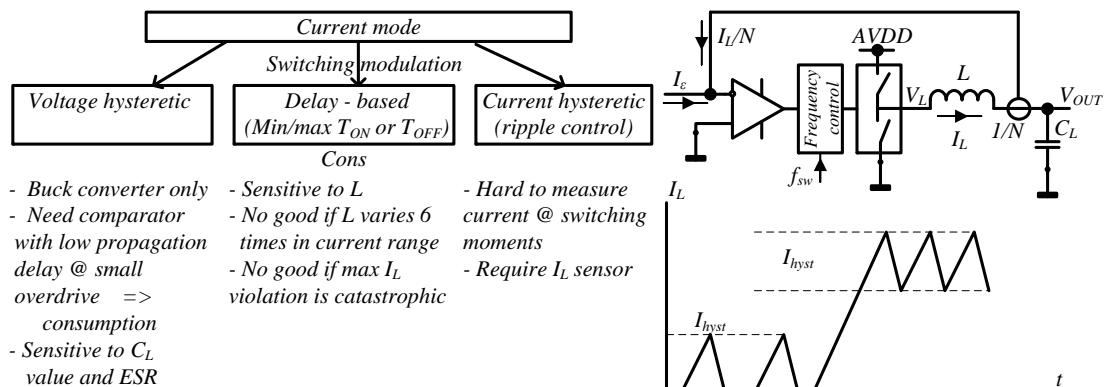
- Capacitor can drop 5 times @ high voltage
- Inductor can decrease 6 times vs. current! → timing modulation schemes are no good

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DCDC control and circuit techniques

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Operation mode choice



Choice is the current hysteretic control with min T_{ON} and T_{OFF} limitations (10-50 ns):

- Not sensitive to L value and nonlinearity
- Not sensitive to C_L ESR and value as long as above min
- Simple implementation

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DCDC control and circuit techniques

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STRUCTURAL DESIGN METHOD

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Circuit design: too many options

- 18,000 amplifiers from 2 transistors – without parametric variations!
- Need a light at the place where decisions are
- Circuit generation procedure
- Instant weeding of the bad solutions

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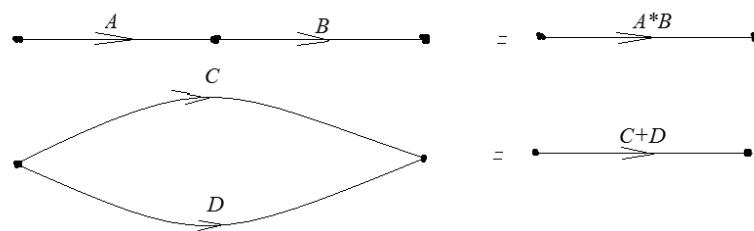
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Design sequence

- Start from graphic system presentation: block diagram or signal flow graph
- Modify it: each important parameter should have a dedicated feedback loop
- Generate set of implementations with elementary cell library
- Choose the one you like

Signal graph advantages

- Formal transformation rules



◆ Faster to draw

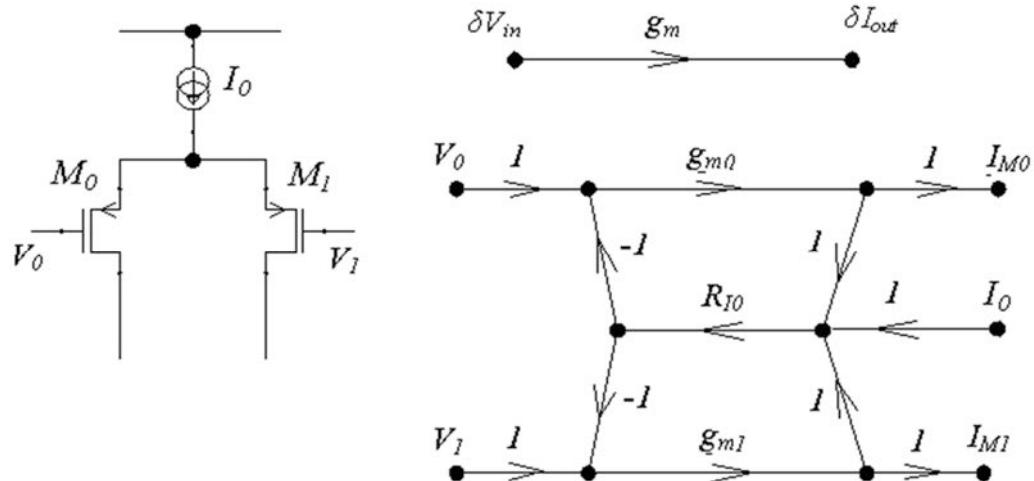
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Graphic high-level system description

- Block diagrams
- Signal flow graphs

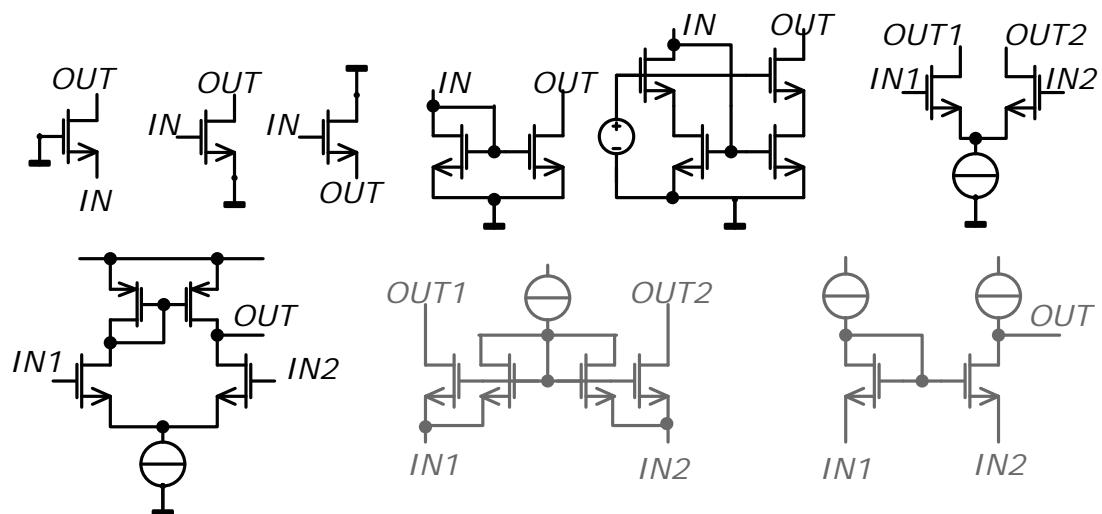


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Elementary cell library

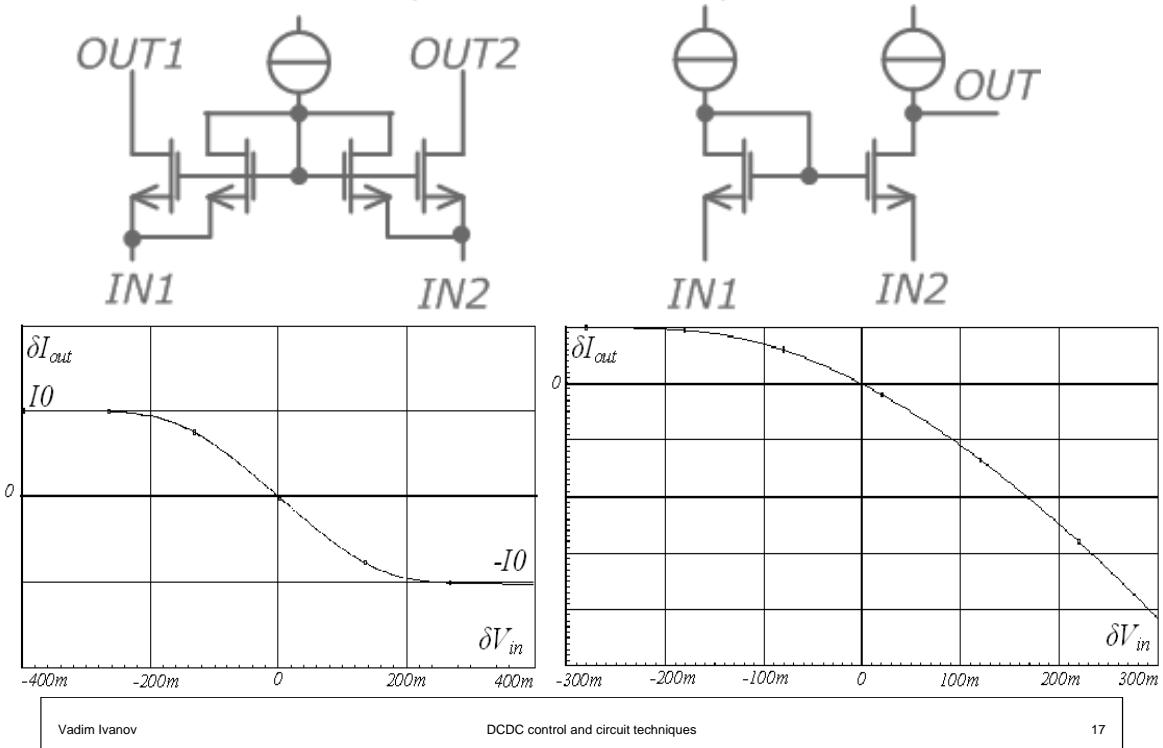


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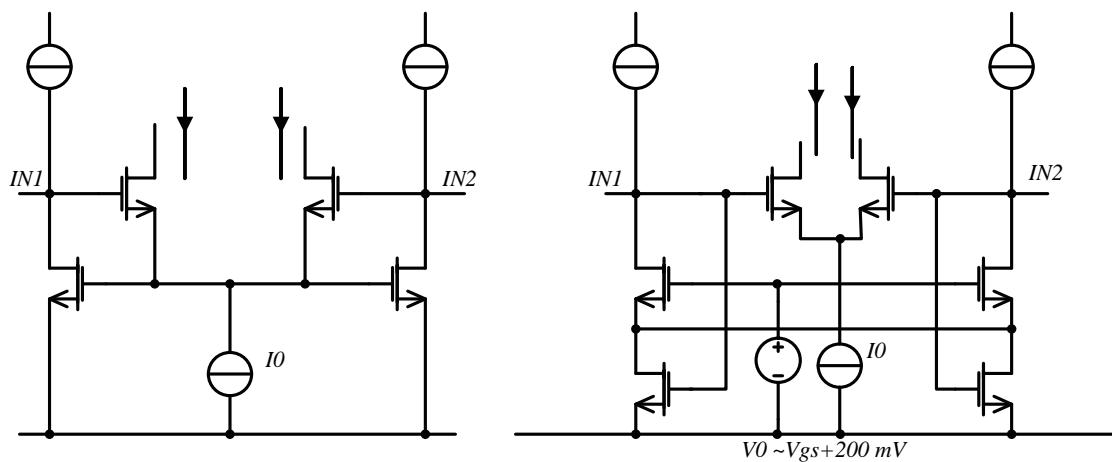
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Elementary cell library - addition

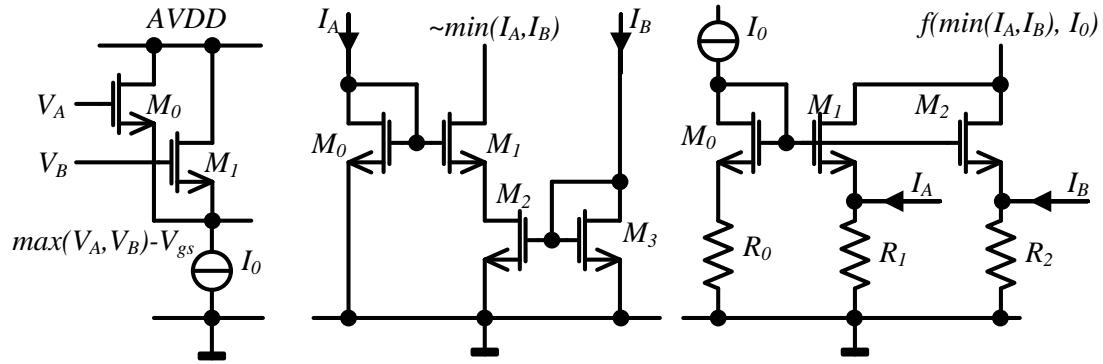


Other amps

- Low common mode – high differential input impedance



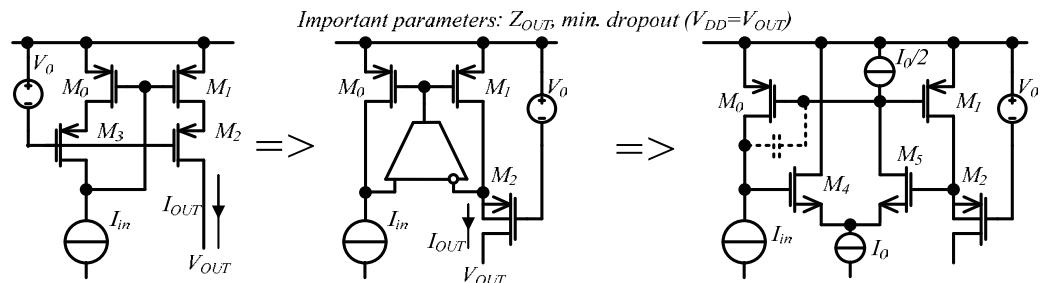
Nonlinear cells



Features of the good circuit

- Has dedicated feedback loops for all important parameters
- Robust to the process and temperature variations
- Dynamically behaves as a second-order system
- Nonlinear effects (start-up, saturation, cutoff) are taken care of
- Insensitive to the substrate noise

Example: improvement of the current mirror

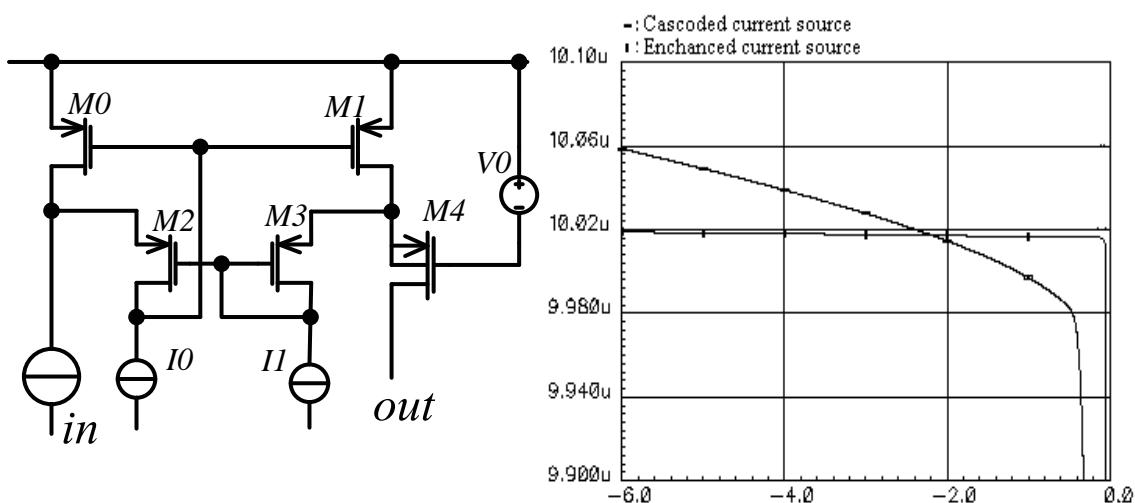


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Current mirror with single-stage amp



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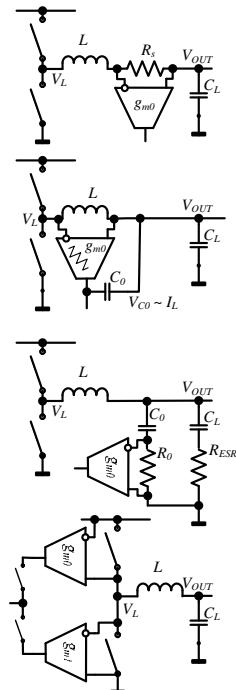
Literature on design methodology

- G. Polya “How to solve it” // Princeton university press, 1971
- J. O’Connor, I. McDermott “The art of systems thinking”// Thorsons, 1997
- G. Altshuller “And Suddenly the Inventor Appeared” // Center for technical innovations, 1996
- V. Ivanov, I. Filanovsky “Operational Amplifier speed and accuracy improvement” // Kluwer, 2004

CIRCUIT TECHNIQUES

Inductor current measurement

- Resistor in series with inductor
 - Customer should be very nice
- Impedance of the inductor
 - No good when L varies 6 times
- ESR resistance of the capacitor
 - No good with ceramic cap
- ON resistance of the power switch
 - Hard to do w external switch

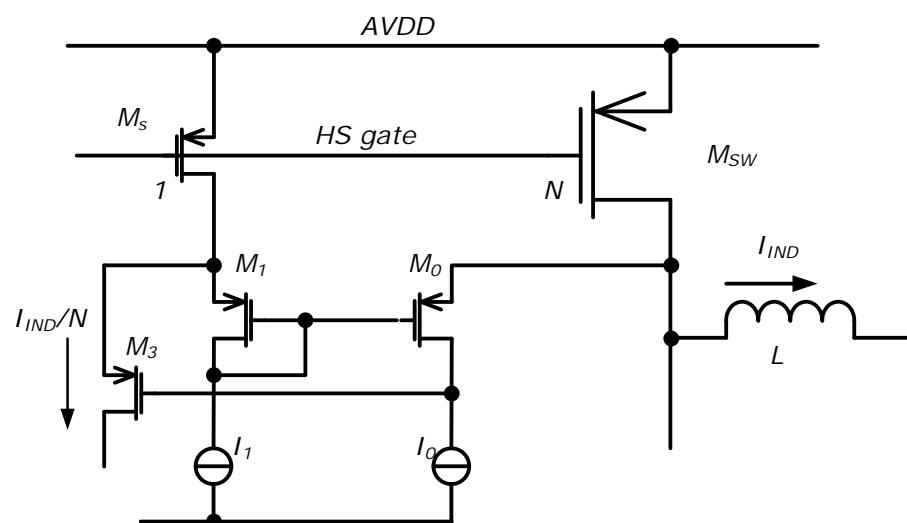


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Sensing in high-side switch using R_{on}



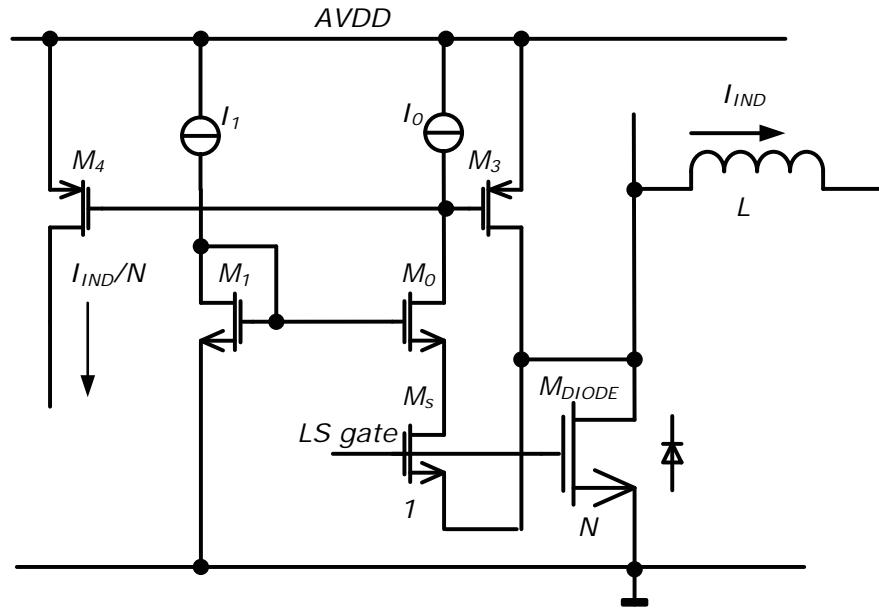
BW ~ 20MHz / 20 μ A Iq @ 0.35 μ m process,
100 MHz / 20 μ A @ 65 nm process

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Sensing in low side rectifier using R_{on}

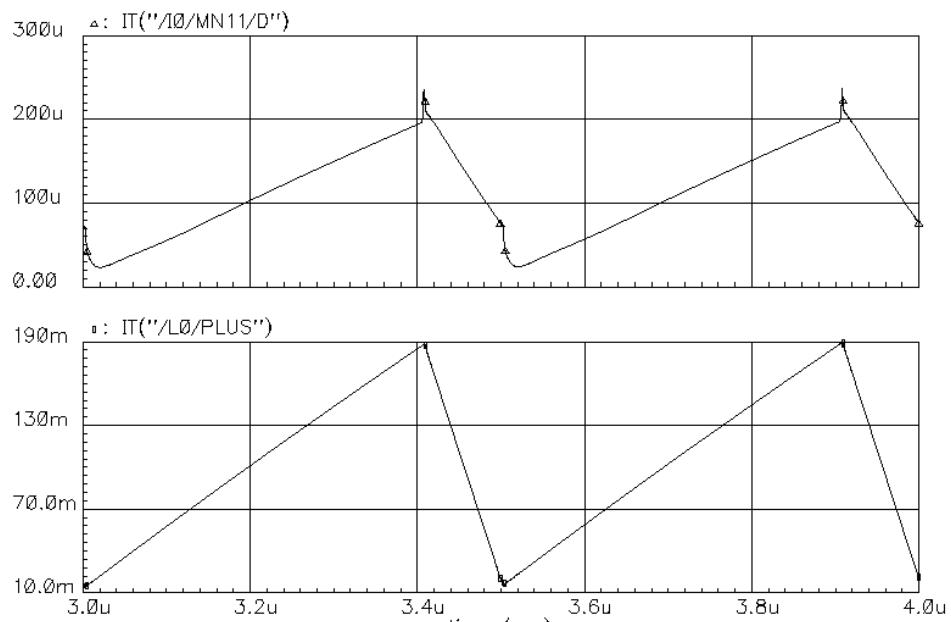


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Inductor vs. output current

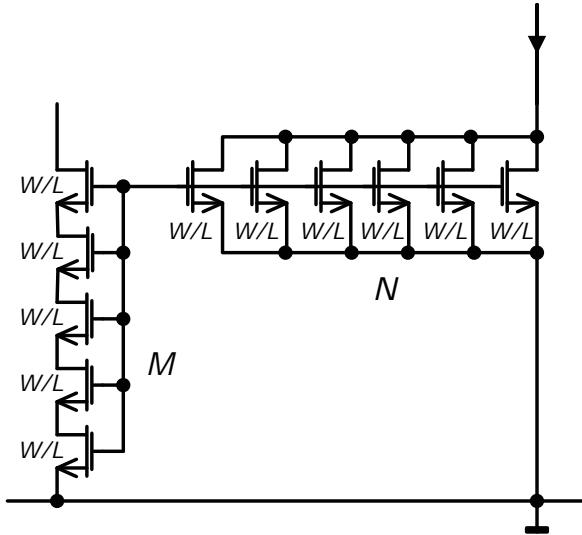


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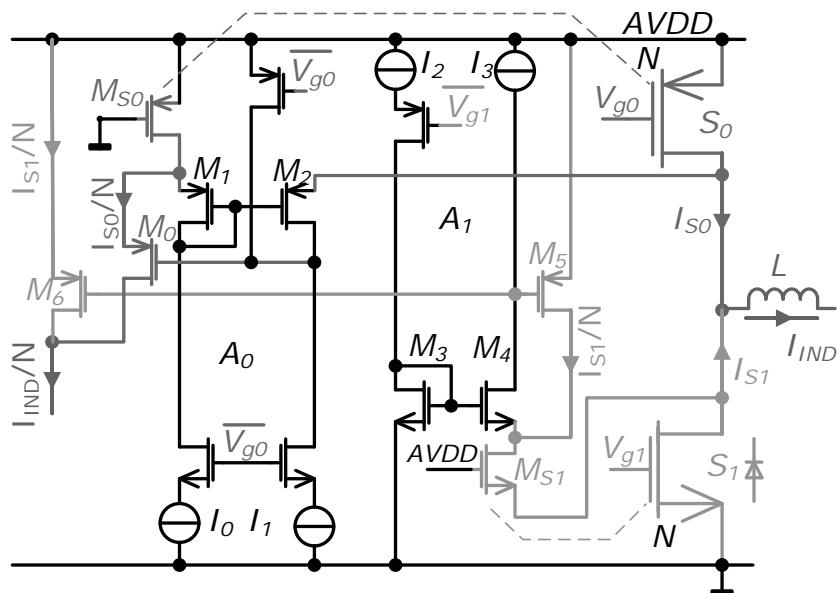
28

Large ratio current sensor



- Good matching if ($V_{ds} \leq V_{gs}$)

Buck DCDC current measurement



10-20% accuracy

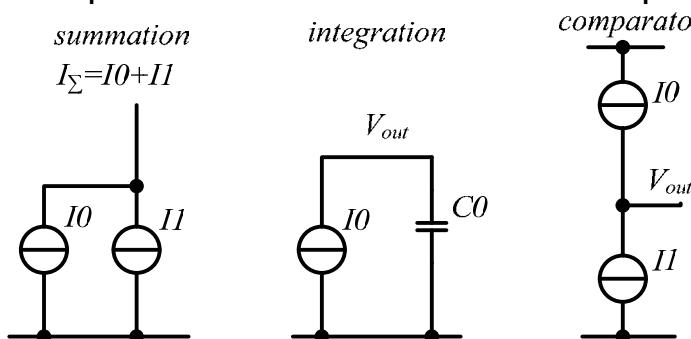
$I_{0/1/2/3} \sim 10 \mu\text{A} \Rightarrow (I_{IND}/N + 20 \mu\text{A})$ consumption when active
No consumption when $I_{IND} = 0$

Error amplifier and frequency compensation

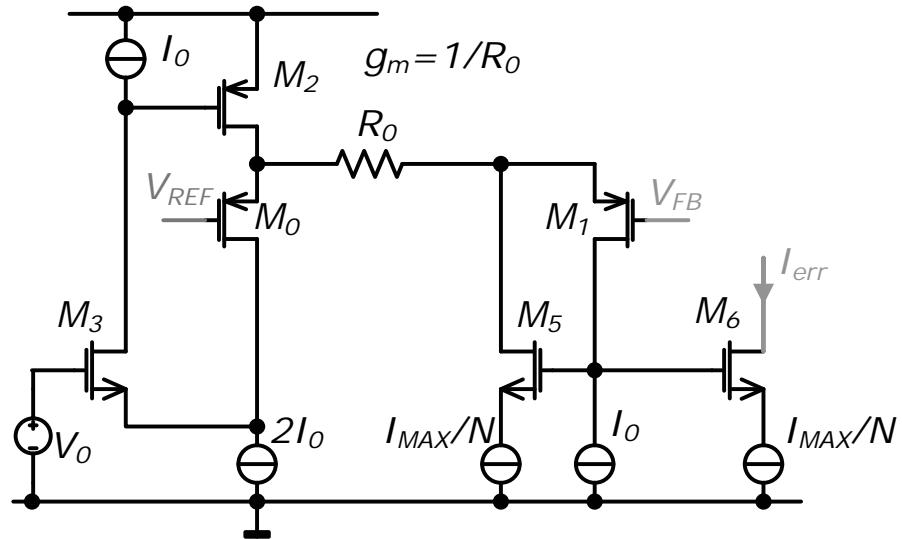
- OpAmps
traditional way
- switch-capacitor techniques
sample/hold circuits are always present
- gm-C techniques
match transistor properties

Current mode advantages (g_m -C)

- ~5x less I_q for the same speed
- Current-mode signal processing is less sensitive to substrate noise
- It is circuit-natural as transistor is a current-output device
- Simple implementation of most common operations:



Error amp for boost DCDC



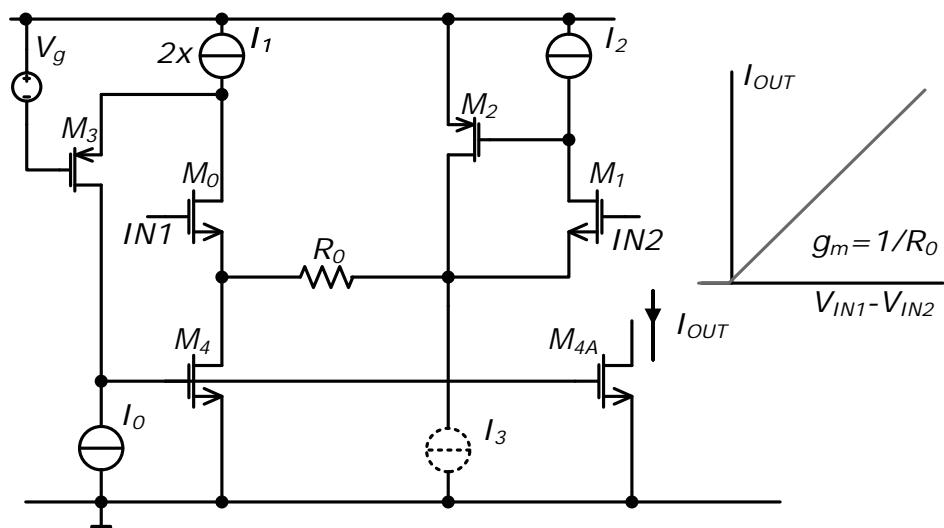
20-30 nA $I_o \Rightarrow$ 50-100 nA I_q

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Constant g_m amp (for buck DCDC)



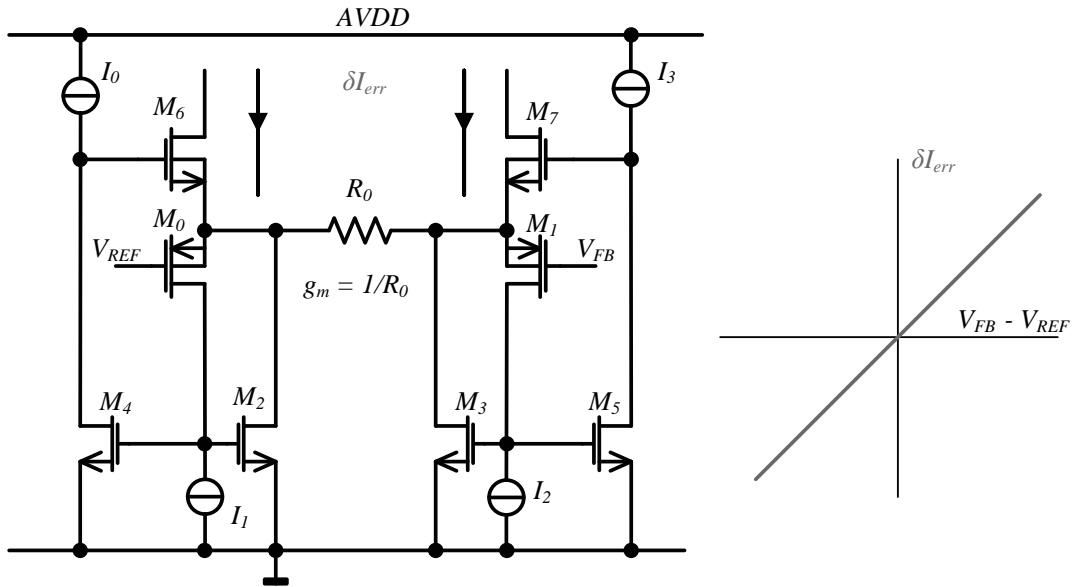
Low I_q (~ 50 nA /10 kHz BW@ 0.35 μm process)
Well-defined g_m & unlimited output current
Input range up to AVDD

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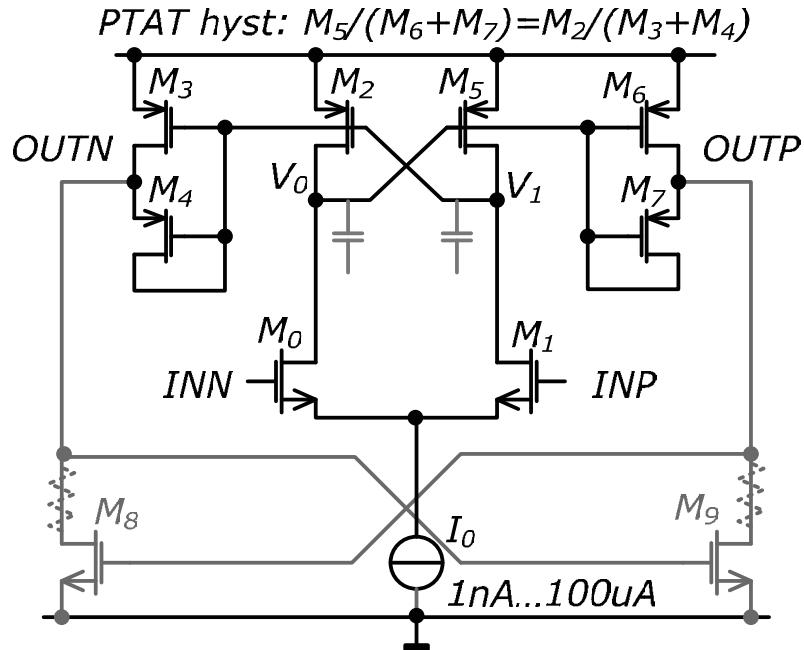
Bidirectional error amplifier



Error comparator

- Offset is not important
- Delay may be proportional to VOUT error
- Freeze output state for 30-50 ns after switching

Scalable Iq / speed comparator

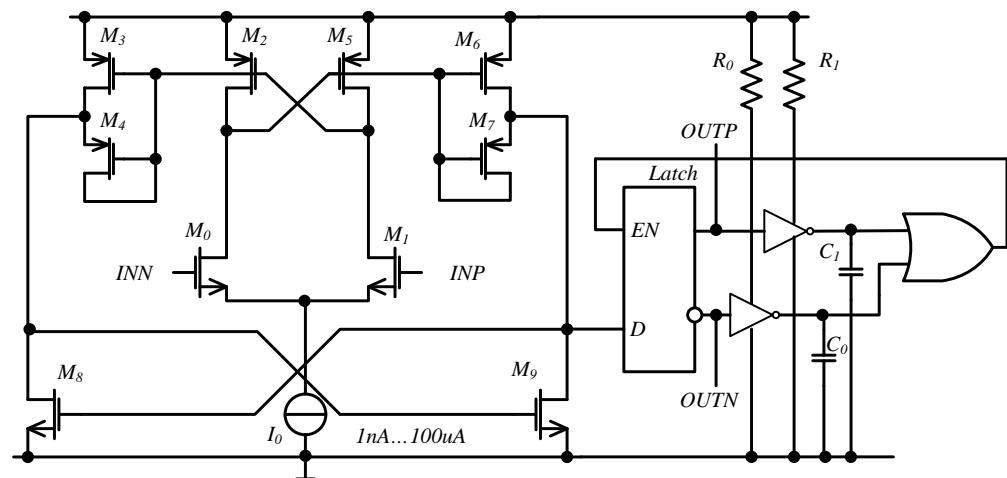


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Comparator with freeze

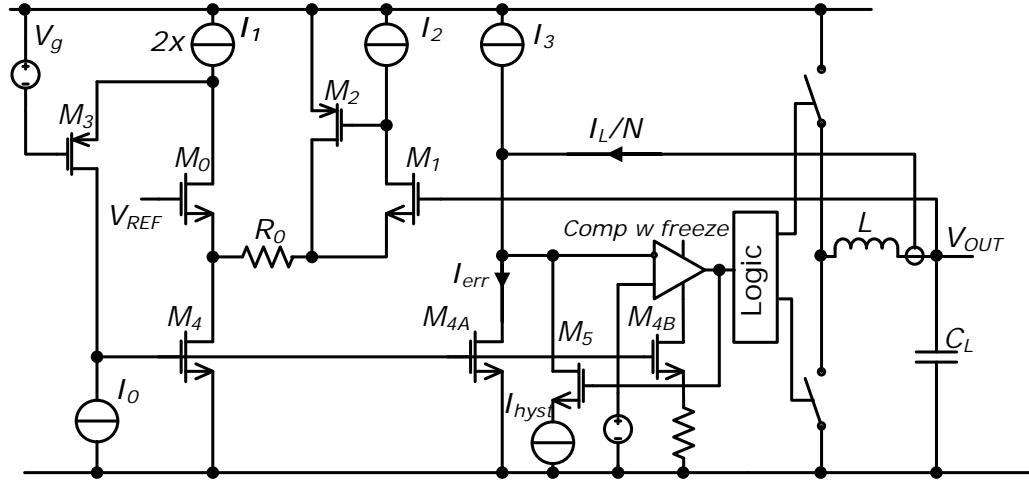


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Current hysteretic DCDC converter

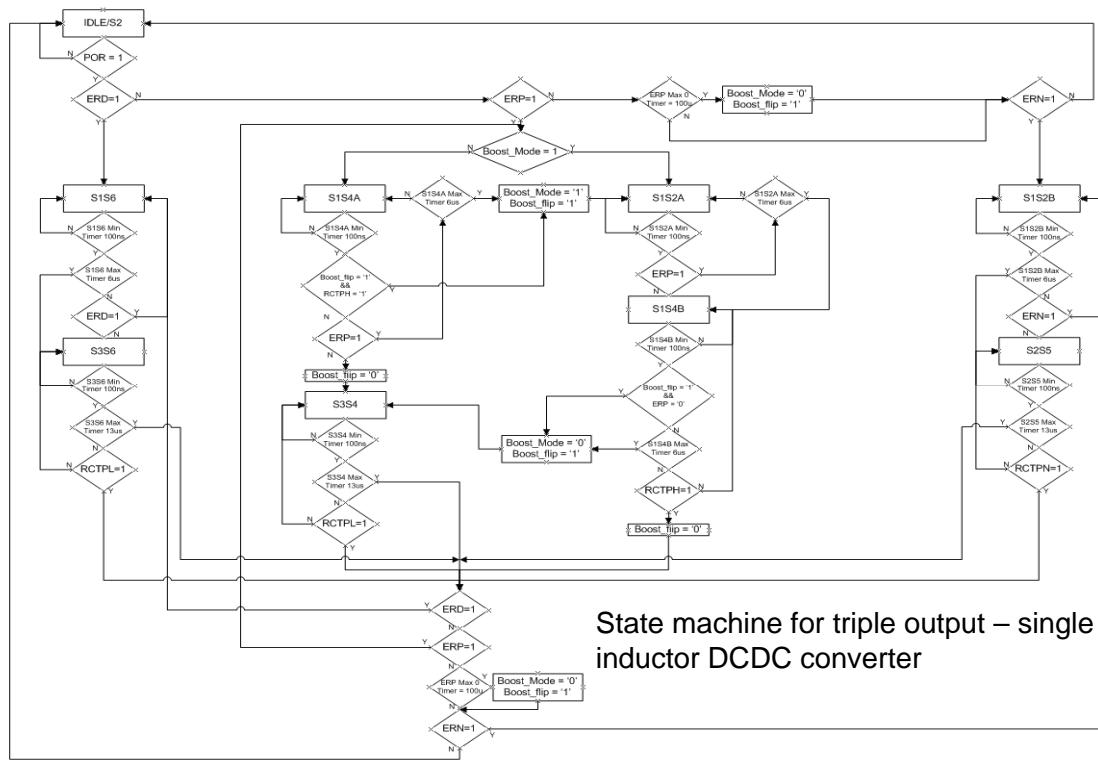


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Logic may be very complicated

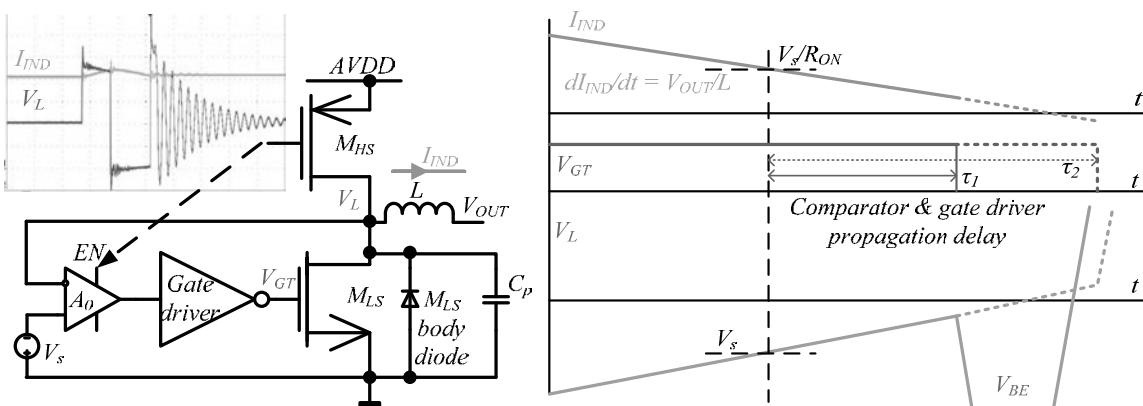


State machine for triple output – single inductor DCDC converter

Logic design

- Error comparator and rectifier switching are asynchronous by nature
- Have to use digital design flow
 - Prevent racing
 - Analog sims of logic take forever
 - Verification
 - Test
- Create short (2-10 ns) pulse at every input event and use as clock for state machine

Synchronous rectifier



Comparators for synchronous rectifier

- Small delay (5-15 ns)
- Low I_q
- Accurate predefined offset

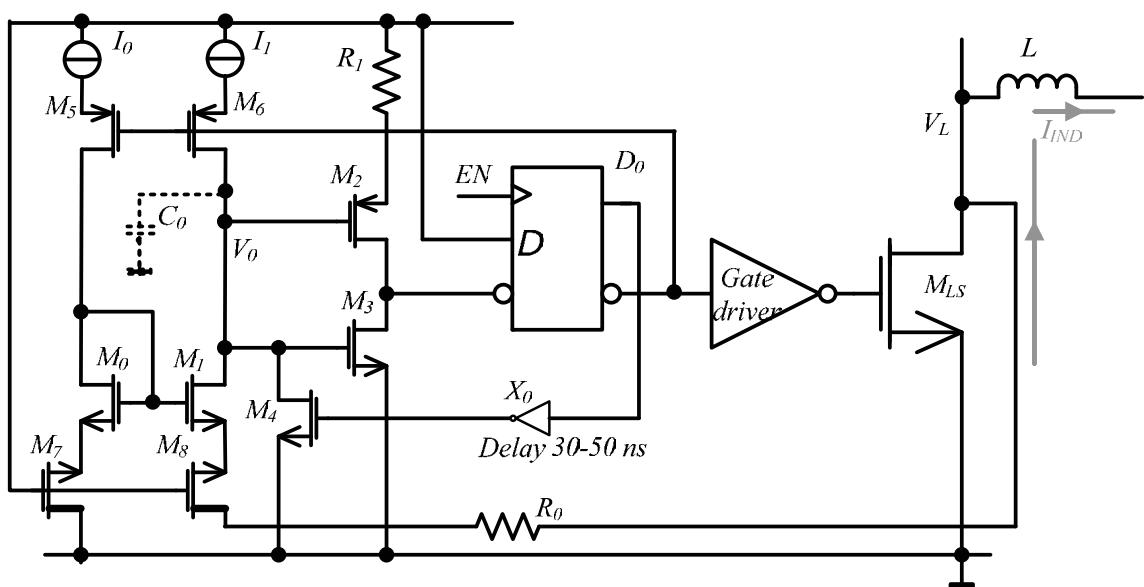
Design basics:

- Current input (>5x faster)
- Low voltage swing at first stage output
- Disable when not needed

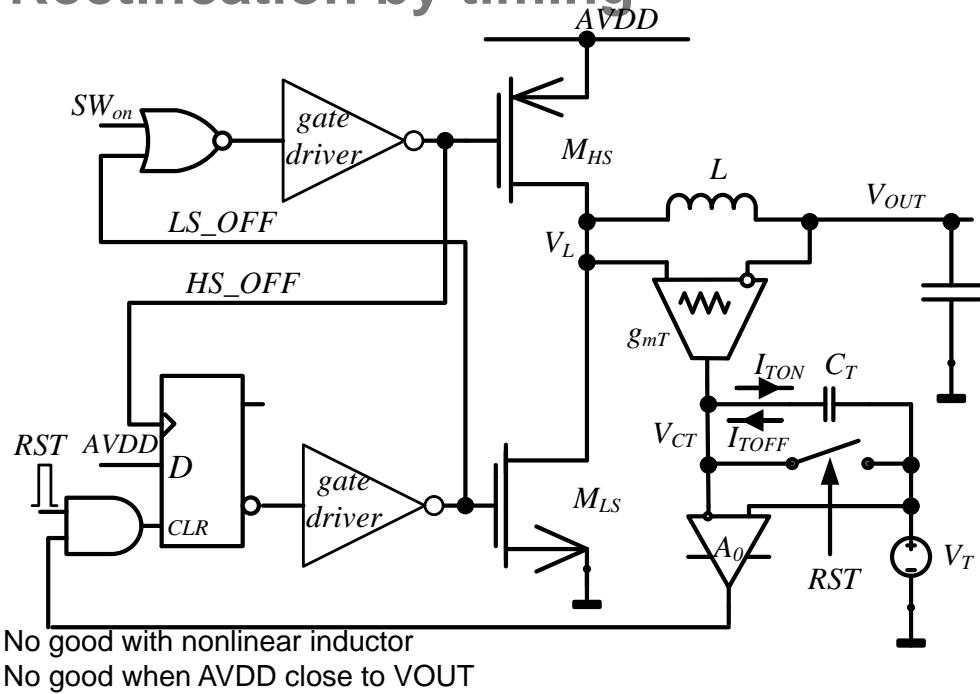
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Low side rectifier comparator



Rectification by timing



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For tight frequency control: PLL

- For delay-based modulators: control T_{ON} / T_{OFF}
- For current hysteretic modulators: control ripple

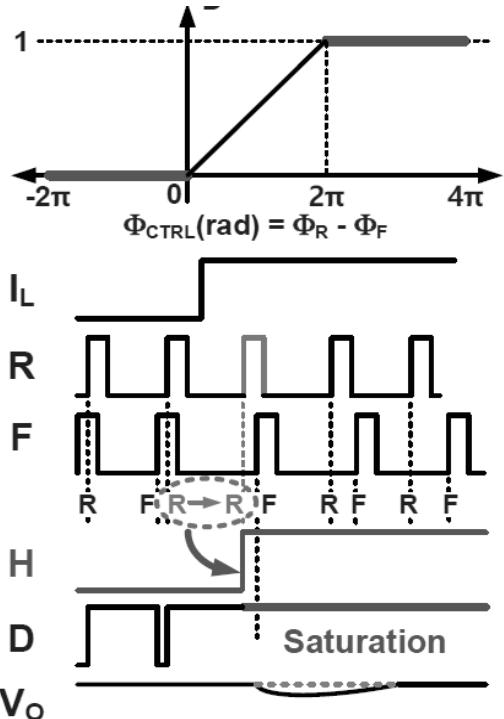
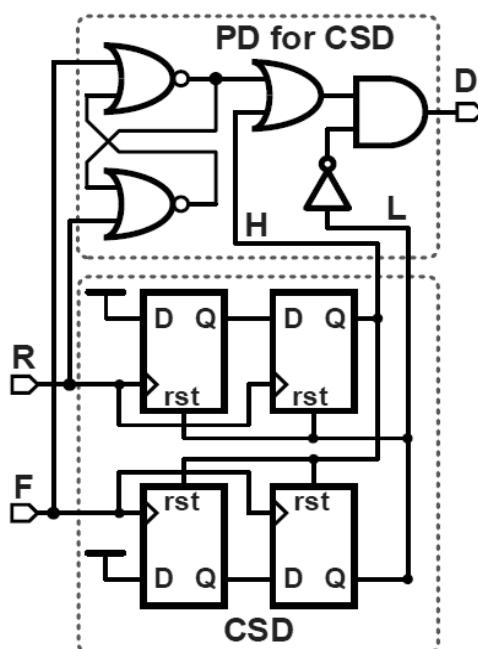
if parameter is important – control it with feedback loop!

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No-slip phase-frequency detector

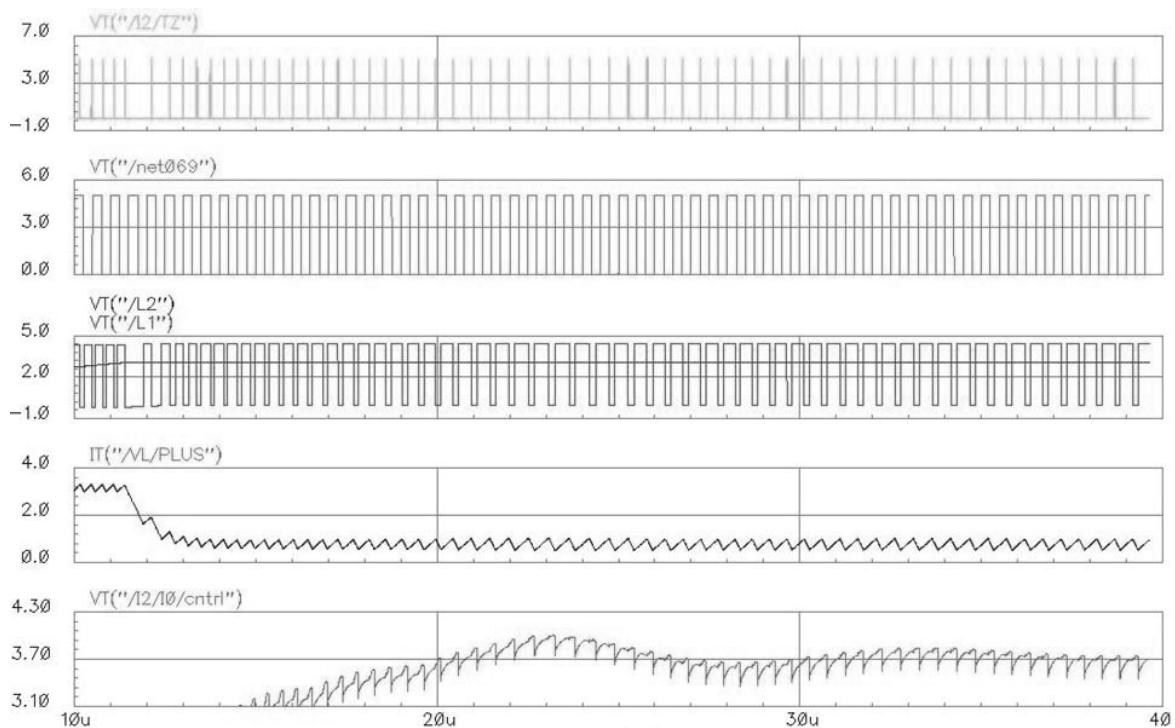


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12.2 : A 1.8V 30-to-70MHz 87% Peak-Efficiency 0.32mm² 4-Phase Time-Based Buck Converter Consuming 3μA/MHz Quiescent Current in 65nm CMOS

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PLL locking process



Conclusions

- Most common design choices: voltage mode, PWM and fixed frequency,- are mistakes
- With structural design we can avoid these and improve stability, consumption and efficiency of DCDC converters while using the cheapest inductors and capacitors