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High Step–up DC–DC Converter Based on Three–Winding Coupled Inductor

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***Abstract*—In this paper a novel topology for high step-up DC–DC converter is introduced. The converter makes use of coupled inductor and voltage multiplier cell to reach the desired high step-up voltage gain. The main advantages of the proposed converter are simple topology, high step-up voltage gain, continuous input current, recycling the energy of the leakage inductance of the coupled inductor, and utilizing only one active switch with reduced voltage stress. Reduced switch voltage stress results in selection of switch with low on-resistance which improves the efficiency. Operational principles of the converter in steady state are studied and an analytical approach is used to attain voltage gain and switch voltage stress. Some of the determinant factors are compared with similar coupled inductor converters. Modular extension of the proposed converter to reach even more step-up voltage gain is also discussed. Finally appropriate performance of the proposed topology is verified by simulating a 30V/400V, 750W converter.**

Keywords—DC-DC boost converter; high step-up; coupled inductor; high voltage conversion ratio

I. INTRODUCTION

Recently the use of step-up DC-DC converters with high voltage ratio has been increased. That is due to the growing usage of this type of converters in a wide range of applications such as fuel cell stacks (FC), photovoltaic (PV) cells, uninterruptable power supplies (UPS), etc. [1]–[4]. In these sorts of applications high step-up converters are used to convert the low level varying primary voltage to the desired regulated high voltage output.

The voltage gain of the conventional boost converter theoretically increases by an increment in switch duty cycle. However, it has to operate with a very large duty cycle to reach the high voltage conversion ratio. Also the voltage stress of the switch in conventional boost converters is equal to the output voltage. Thus high voltage switches with high on-resistance ($R_{DS(on)}$) should be selected. Meanwhile the output diode voltage stress is high which leads to serious reverse recovery problem. As a result a reduction in overall efficiency will happen in large duty cycles which limits the actual voltage conversion ratio [5], [6]. Therefore, simple conventional boost converters cannot be used in applications requiring high output-input voltage ratio.

To practically achieve high voltage conversion ratios several topologies for high step-up boost converters has been proposed. One of the interesting types of these converters is switched capacitor converters [7] – [9]. These converters possess the advantage of having low size and weight. However, the drawbacks are high number of switches and capacitors, high current stress and complexity of control.

Utilizing three state switching cells (3SSC) is another way to reach the high voltage gain which is specially used in power factor correction (PFC) applications [10], [11]. Reducing size and weight is one of the main advantages in these converters. Also in this kind of converters low current of switches results in lower cost. However in each operation state current passes through four semiconductor devices which results in efficiency reduction.

One of the main strategies to achieve high step-up voltage ratio is to utilize voltage multiplier cells in conventional converters. But the step-up ratio reached in this method is not enough. So to get to the desired ratio one should utilize multiple cells, which increases the complexity and overall cost of the converter [12].

Another method to achieve high step-up voltage ratio is to use coupled inductors [13] – [20]. The voltage gain can be

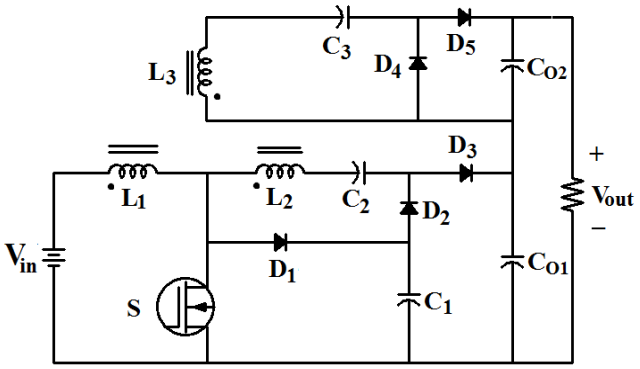

Fig. 1. Circuit configuration of the proposed converter.

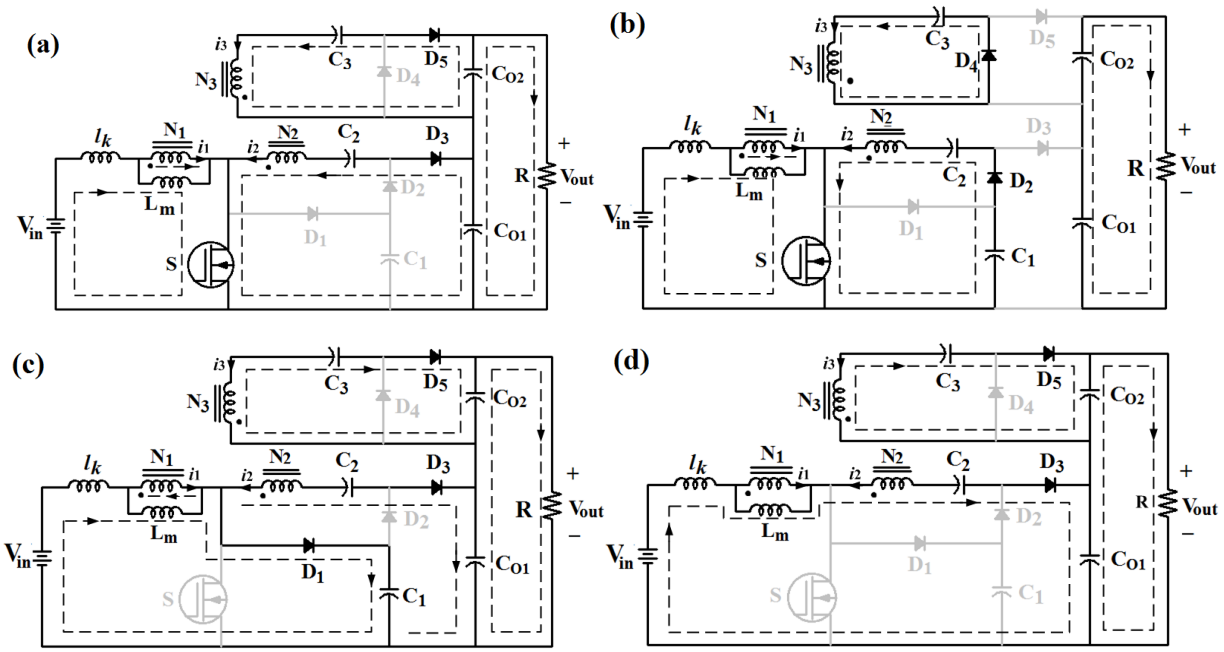

Fig. 2. Circuit topology and current paths in each operation interval (a) Interval 1, (b) Interval 2, (c) Interval 3, (d) Interval 4.

increased by incrementing the coupled inductor turn ratio in these converters. Simplicity of control is another advantage of these converters. However there are some limitations and drawbacks in some topologies proposed for this type of converter. The turn ratio of the coupled inductor could not increase gradually. This is due to increase of leakage inductance which lowers the efficiency. Also the input current of the converter is discontinuous in some topologies which results in high ripple.

In this paper a novel topology for high step-up DC-DC converters is introduced based on coupled inductor. Fig. 1 depicts the circuit configuration of the proposed converter. In the following first we will discuss operating principles of the proposed topology in section II. Next steady state performance of the converter will be discussed in detail in section III. After that in section IV the proposed topology is extended to obtain even more step-up voltage gain using low voltage diodes and capacitors. Simulation results are given in section V to verify the operation of the proposed circuit. Finally a brief conclusion of this study is presented.

II. Operating Principles of the Proposed Converter

The operation principles for the continuous conduction mode (CCM) are explained in this section. The coupled inductor can be modeled by an ideal transformer with primary winding N_1, two secondary windings i.e. N_2 and N_3, a magnetizing inductance L_m and a leakage inductance l_k. Operation of the converter is divided into four intervals and is discussed hereafter. Circuit topology in each interval and the current-flow paths are illustrated in Fig. 2. Fig. 3 shows some of the typical waveforms of the proposed converter.

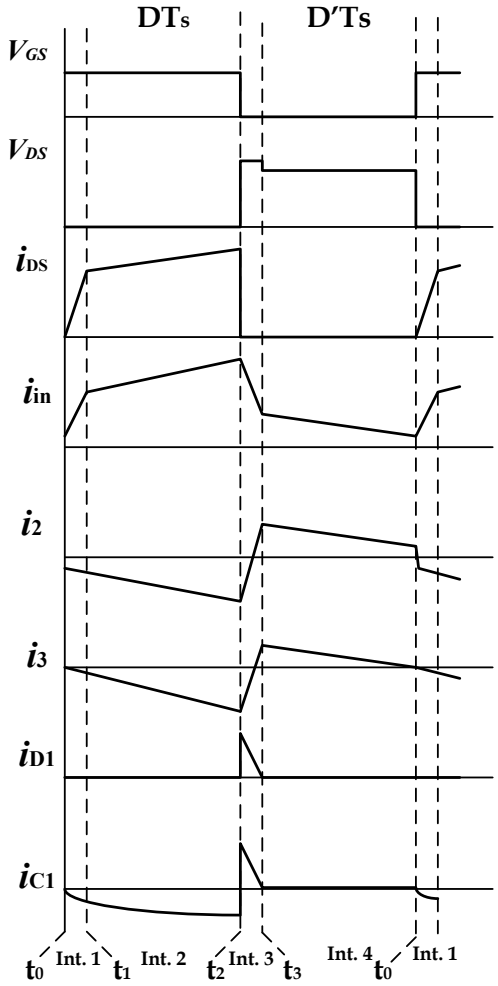

Fig. 3. The key waveforms of the proposed converter in CCM.

Interval 1 [t_0–t_1]: This interval begins with turning the switch *S* on. In this interval which is shown in Fig. 2(a) the voltage across the magnetizing and leakage inductances equals V_{in}. Thus the current in L_m is increasing linearly. This interval is reverse recovery mode of the two diodes D_3 and D_5 and lasts until their currents reaches zero and they stop conducting. In this interval both of the output capacitors C_{O1} and C_{O2} are discharging their energy to the load. This mode is ended at $t=t_1$.

Interval 2 [t_1–t_2]: This interval begins when reverse recovery process of diodes D_3 and D_5 is ended. Unlike the former interval this interval is the main conduction interval when *S* is on. Due to conduction of the switch *S* energy of the input voltage source V_{in} is supplied to magnetizing inductance resulting in linear increase of the L_m current. Diodes D_2 and D_4 are conducting from the beginning of this interval. Thus the energy stored in capacitor C_1, which is the energy of the leakage inductance of the coupled inductor, recycles into the circuit. The load is isolated from input source and the output capacitors are supplying the load. This interval lasts until the switch *S* is turned off at $t=t_2$. Fig. 2(b) shows the current-flow path of this mode of operation.

Interval 3 [t_2–t_3]: This interval begins by turning switch *S* off. Input current, which is equal to leakage inductance current, charges the parasitic capacitor of the switch and builds up its voltage. Thus diode D_1 conducts and the energy of the leakage inductance is stored in capacitor C_1 to avoid occurrence of high voltage spikes on power switch. Voltage of the magnetizing inductor is negative and its current is reducing. Output capacitors C_{O1} and C_{O2} are charging from input source. This interval lasts till C_1 absorbs the energy of the leakage inductance. After that the input current equals the secondary current i_2 and D_1 is reverse biased and turned off in zero current. The circuit topology and path of current are shown in Fig. 2(c). This mode end at $t=t_3$.

Interval 4 [t_3–t_4]: In this interval the switch *S* is still turned off. Magnetizing inductor current is reducing. Diodes D_3 and D_5 are still conducting and feeding load and output capacitors. The input current is equal to secondary current i_2. The input source, primary and secondary windings of the coupled inductor (N_1 and N_2) and capacitor C_2 are connected in series to charge the output capacitor through diode D_3. Finally when the switch *S* is turned on this interval is ended and Interval 1of the next switching cycle begins. The current-flow path of this interval is illustrated in Fig. 2(d).

III. Steady-State Performance Analysis of The Proposed Converter

In this section voltage gain of the proposed boost converter is calculated. For the simplicity of the analysis, leakage inductance of the coupled inductor is neglected. Also all capacitors are large enough. Therefore, their voltages are considered constant.

As it can be seen from Fig. 1 the overall output voltage of the converter is the sum of the voltages across output capacitors C_{O1} and C_{O2}, which is denoted in (1) as follows:

$$V_{out} = V_{CO1} + V_{CO2} \tag{1}$$

In order to obtain the overall gain of the converter the voltage of each output capacitor should be derived as a function of the input voltage V_{in}, coupled inductor turn ratios n_{21} and n_{31}, and switch duty cycle (D). As the first step one should calculate the voltage across C_{O1}. The voltage across magnetizing inductance L_m in switch conduction interval DT_s, can be stated as:

$$V_{Lm}^{DT_s} = \frac{V_{in} + V_{C2} - V_{C1}}{1 + n_{21}} \tag{2}$$

Similarly during interval $D'T_s$ in which the power MOSFET is in off-state, the voltage of the magnetizing inductor L_m is as follows:

$$V_{Lm}^{D'T_s} = \frac{V_{in} - V_{CO1} + V_{C2}}{1 + n_{21}} \tag{3}$$

Using Kirchhoff's law in Fig. 2(b) and Fig. 2(c) one can derive the voltage across capacitors C_1 and C_2 as:

$$V_{C1} = \frac{V_{CO1} - V_{in} - V_{C2}}{1 + n_{21}} + V_{in} \tag{4}$$

$$V_{C2} = V_{C1} + n_{21} V_{in} \tag{5}$$

These two equations can be expressed as follows:

$$V_{C1} = V_{DS} = \frac{V_{CO1}}{2 + n_{21}} \tag{6}$$

$$V_{C2} = \frac{V_{CO1}}{2 + n_{21}} + n_{21} V_{in} \tag{7}$$

The switch-off voltage of the active switch *S*, i.e., V_{DS} is clamped to voltage across C_1. For the same input voltage and voltage conversion ratio, the driven switch voltage stress is lower compared to converter introduced in [18].

Using volt-second balance for magnetizing inductance, results in:

$$\langle V_{Lm} \rangle_{T_S} = DT_s V_{Lm}^{DT_s} + D'T_s V_{Lm}^{D'T_s} = 0 \tag{8}$$

Where $\langle V_{Lm} \rangle_{T_S}$ denotes the average value of the magnetizing inductance voltage in one switching period. Substituting V_{C1} and V_{C2} from (6) and (7) into (2) and (3) and using (8) one can obtain the V_{CO1} as follows:

$$V_{CO1} = \frac{2 + n_{21}}{1 - D} V_{in} \tag{9}$$

In order to obtain an expression for the overall voltage gain of the converter another equation should be achieved for the other output capacitor voltage V_{CO2} in terms of V_{in}.
In switch conduction interval DT_s, V_{C3} can be calculated as:

$$V_{C3} = V_3 = n_{31} V_{Lm}^{DTs} = n_{31} V_{in} \tag{10}$$

where V_3 is the voltage of the secondary winding N_3. Using KVL in interval $D'T_s$ results in (11)

$$V_{CO2} = -V_3^{D'Ts} - V_{C3} \tag{11}$$

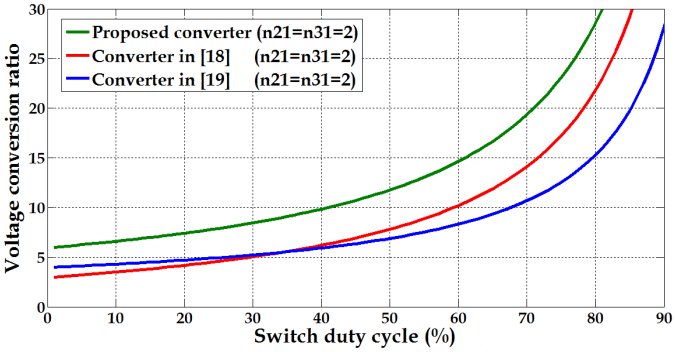

Fig.4. Comparison between voltage gains.

Equation (11) can be rewritten as follows:

$$V_{CO2} = -n_{31} V_{Lm}^{DTs} - V_{C3} \tag{12}$$

Now from Fig. 3(d) and using (9) one can obtain V_{Lm}^{DTs} as follows:

$$V_{Lm}^{DTs} = -V_{in}\left(\frac{D}{1-D}\right) \tag{13}$$

Substituting (10) and (13) into (12) gives the upper side voltage conversion ratio as:

$$\frac{V_{CO2}}{V_{in}} = \frac{n_{31}}{1-D} \tag{14}$$

Finally, using (9) and (14) the overall voltage gain of the proposed converter in CCM can be expressed by:

$$M_{CCM} = \frac{V_{OUT}}{V_{in}} = \frac{n_{31} + n_{21} + 2}{1-D} \tag{15}$$

Fig.4 gives a comparison between voltage gains of the proposed converter and two other similar converters introduced in [18] and [19]. Turn ratios of the coupled inductor are equal to 2 in all converters. As it can be seen from Fig.4 the voltage conversion ratio of the proposed converter is greater than the other two converters in entire range of the switch duty cycle. Also it is shown that high voltage gains can be obtained in reasonably low switch duty cycles. As a result switch conduction loss decreases and the overall efficiency improves.

IV. Extension of The Proposed Topology

In this section an extension of the proposed converter using diode-capacitor voltage multiplier cells is introduced in order to reach even more step-up voltage gain. A simple way to reach more step up gain is to increase turn ratios of the coupled inductor namely n_{21} and n_{31}. However it may increase leakage inductance and ohmic losses. Here is an extension of the proposed topology using only sufficient number of low voltage diodes and capacitors.

In this topology which is depicted in Fig. 5 lower part of the circuit is the same as the basic converter. The upper part of the extended topology includes modular arrangement of "*n*"

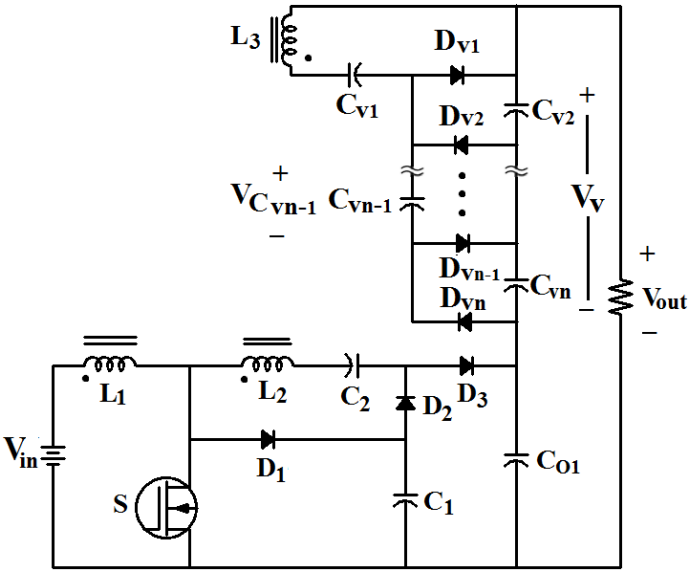

Fig.5. Extension of the proposed converter using modular voltage multiplier cells.

capacitors and diodes which are substituted with the upper part capacitors and diodes of the basic converter. Every two diodes and two capacitors form one voltage doubler cell. Thus the number of cells i.e., K_V is half of the total capacitor and diodes of upper part. So K_V and n are related to each other as:

$$K_V = \frac{n}{2} \tag{16}$$

As it can be seen from Fig.5 overall voltage of the upper part represented by V_V, is the sum of voltages across capacitors with even indices or

$$V_V = \sum_{i=1}^{K_V} V_{C_{V\,2i}} \tag{17}$$

After some calculation the voltage gain of the upper part of the converter can be obtained by:

$$M_V = \frac{V_V}{V_{in}} = \frac{K_V n_{31}}{1-D} \tag{18}$$

According to (18) the voltage gain of the upper stage of the extended topology is K_v times of the corresponding voltage ratio in basic converter which is stated in (14). As a result from (9) and (18) the overall voltage gain of the extended converter can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{2 + n_{21} + K_v n_{31}}{1-D} \tag{19}$$

V. Simulation Results

In order to verify the performance of the proposed

TABLE I. Parameters of the Simulated Converter

Parameter	Value/Part num.	Description
Coupled inductor core	ETD-59	Ferrite core
Coupled inductor turn ratio	1: 2.7: 2.7	
Switch *S*	IRFP2907	Power MOSFET
C_1	22uF	Capacitor
C_2	10uF	Capacitor
C_3	47uF	Capacitor
C_{O1} , C_{O2}	2*22uF	Capacitor
D_1	STPS30100	Schottky diode
D_2 - D_5	BYV27-200	Ultra-fast diode

converter and theoretical analysis, a 30V/400V case is simulated in PSpice circuit simulator. This software contains the actual models of the circuit components. Therefore the results would be very similar to the experimental results of real converter. Maximum output power and operating frequency of the simulated converter are 750W and 100 kHz respectively. Other specifications and parameters used for the simulation are given in Table I.

Steady state simulation results are given in Fig. 6 – Fig. 11. Fig. 6 depicts output, input and output capacitors voltages for the CCM operation of the converter. The input voltage is 30V so the voltage gain is about 13.4. Switch duty cycle is about 0.44 for this voltage conversion ratio.

Simulated voltage and current stresses of the active switch are shown in Fig. 7. As it is can be seen the voltage stress of the switch is about 55V in turn off mode which is very low compared to 400V output voltage. So the other problem of the high step-up converters which is high voltage stress, is alleviated in the proposed converter and verified by simulation results and mathematic equations. Reduction of switch voltage stress allows making use of switch with low on-resistance which leads to loss reduction and efficiency improvement.

Simulated current waveforms for capacitors C_1 and C_2 are illustrated in Fig. 8. For avoiding the large voltage spikes on the MOSFET, Capacitors C_1 should absorb the energy of the leakage inductance of the coupled inductor. Hence at the conducting interval of the diode D_1, it begins to be charged and its current is positive. After completely absorbing the leakage energy, diode D_1 is turned off in zero current (Fig. 9) and the current flow to C_1 is blocked.

Fig. 10 illustrates simulated waveforms of input current, primary and secondary currents (i_2 and i_3) of the coupled inductor. As it can be seen from this figure, the input current has a continuous waveform which is one of the main advantages of the proposed topology compared to converters such as Flyback with discontinuous input current.

In Fig. 9 and Fig.11 voltage and current stresses of diodes D_1 and D_3 are illustrated. Among the power diodes the maximum voltage stress is on D_3. However even in this case the voltage stress is about half of the output voltage.

VI. Conclusion

In this paper a novel topology for high step-up DC-DC converters is presented. It is based on coupled inductor and diode-capacitor voltage multiplier cells. Principles and steady state analysis of the proposed converter in CCM is discussed. Voltage gain of the converter is compared with similar converters. It was shown that the proposed converter exhibits the best performance in voltage convergence among mentioned converters. Simplicity of control and implementation due to utilizing only one active switch is one of the advantages of the proposed topology. Recycling the energy of the leakage inductance of the coupled inductor leads to an improved efficiency. Meanwhile the voltage of the active switch is clamped to a low voltage capacitor which prevents the power switch from high voltage spikes. Reduction of voltage stress for active switch results in use of switch with low on-resistance which leads to further increase in the overall efficiency. The proposed converter can be generalized for achieving more step-up voltage gain using low voltage diodes and capacitors. Extended circuit and its analysis are also given. Simulation results proved the validity of theoretical analysis of the basic proposed converter.

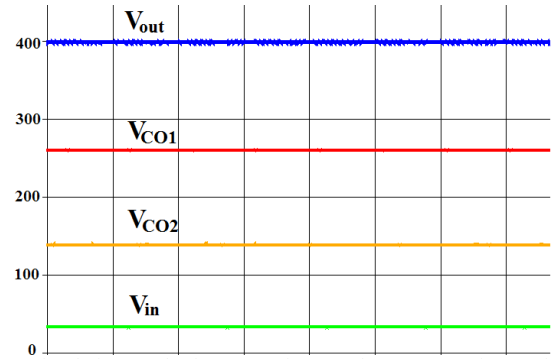

Fig. 6. Simulation results for output, input and output capacitors voltages in CCM of operation

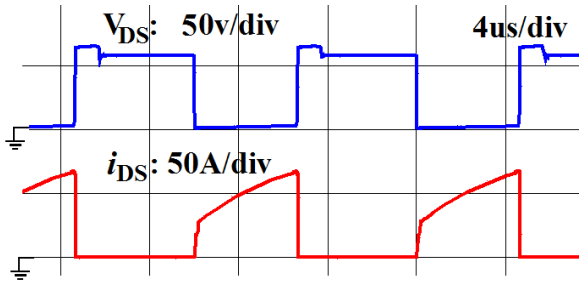

Fig. 7. Current and voltage stresses of the switch *S*.

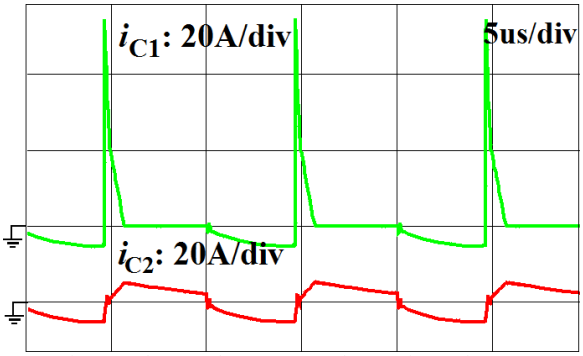

Fig. 8. Voltage and current waveforms of capacitor C_1.

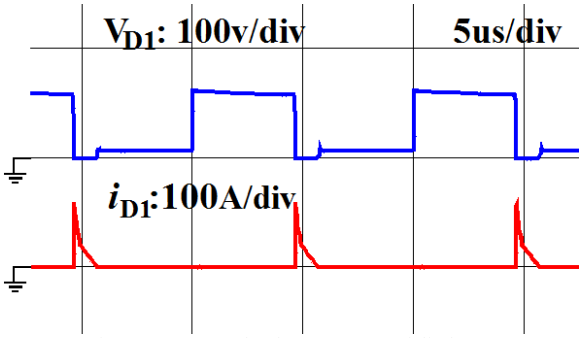

Fig. 9. Current and voltage stresses of diode D_1.

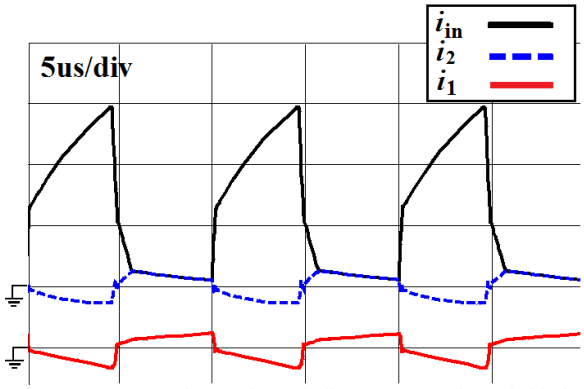

Fig. 10. Input current and secondary windings currents of coupled inductor.

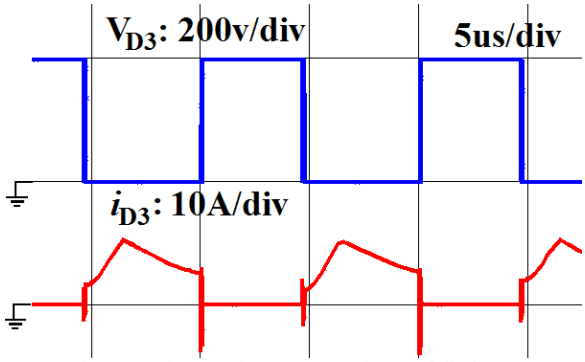

Fig. 11. Voltage and current waveforms of diode D_3.

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