

## ABSTRACT

LEE, MENG-CHIA. Developing Physics-based Models for 4H-SiC High Voltage Power Switches – MOSFET, IGBT and GTO. (Under the direction of Dr. Alex Huang.)

The goal of this dissertation is to develop physics-based equivalent circuit models for 15kV~20kV 4H-SiC power switches. The previous modeling works will be reviewed, and the parameter extraction methodologies will be discussed.

MOSFET is modeled using a voltage-controlled current source for channel current and three nonlinear capacitances for the transient behavior. The high electron saturation velocity and its effect on the saturation current level will also be discussed. Final model has been implemented in Simulink/Matlab, and the execution time for the turn-on and off transient is less than 1 second.

IGBT Analytical model that translate the local excess carrier to the diffusion capacitance will be derived first and implemented in a sub-circuit manner into Simulink/Matlab. A novel parameter extraction technique – Excess carrier density mapping (ECDM) – using inductive switching waveforms is introduced. The execution time of the model is about 7 seconds and 2 seconds for a turn-off and turn-on transient, respectively. IGBTs with two-zone drift region for slowing down the turn-off dv/dt are also proposed based on the developed analytical model.

Finally, 4H-SiC p-GTO model based on the IGBT one is developed. Region-wise lifetimes throughout the drift region was observed when using the proposed ECDM technique. Simulated waveforms using region-wise lifetime have shown better fitting results than the case using constant lifetime. The difference between n-type and p-type ambipolar switches will be discussed and compared using the developed models.

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Developing Physics-based Models for 4H-SiC High Voltage Power Switches – MOSFET, IGBT and  
GTO

by  
Meng-Chia Lee

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## **DEDICATION**

*To my parents,*

*Thank you for always being supportive.*

## **BIOGRAPHY**

Lee, Meng-Chia was born in Yunlin, Taiwan. He received his MS degree in Electronic Engineering from National Tsing Hua University (HsinChu, Taiwan) in 2009. His research focus was lateral 4H-SiC transistors on semi-insulating substrate. In 2010, he enrolled in graduate school at North Carolina State University (Raleigh, NC) for pursuing his PhD degree in Electrical Engineering under the guidance of Dr. Alex Q. Huang. His field of interests includes power semiconductor design, fabrication, simulation, optimization and modeling.

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# Chapter 1

## Introduction

### 1.1 Recent progress on high voltage 4H-SiC power switches

Figure 1-1 are the simplified cross-sections of >10kV 4H-SiC power switches that have been developed over the past decade [1]. Figure 1-2 shows the measurement results of the IV curves at 25°C and 125°C for 15kV device technologies. 4H-SiC GTO has the best conduction characteristics and is insensitive to the temperature, while the conductivity of MOSFET has dropped more than 50% from 25°C to 125°C.

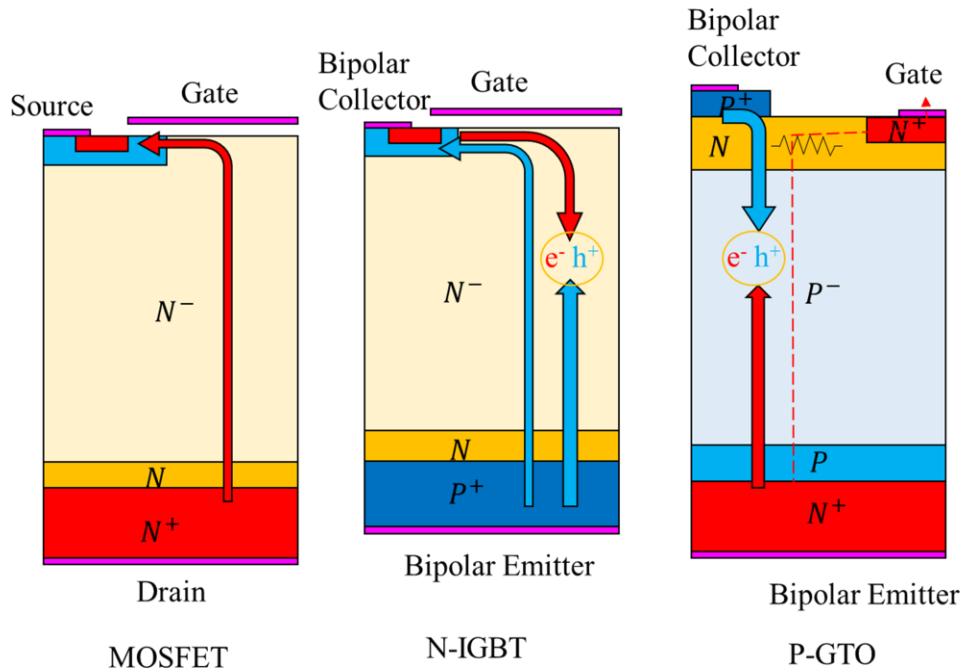


Figure 1-1 Simplified cross-section of MOSFET, IGBT and GTO.

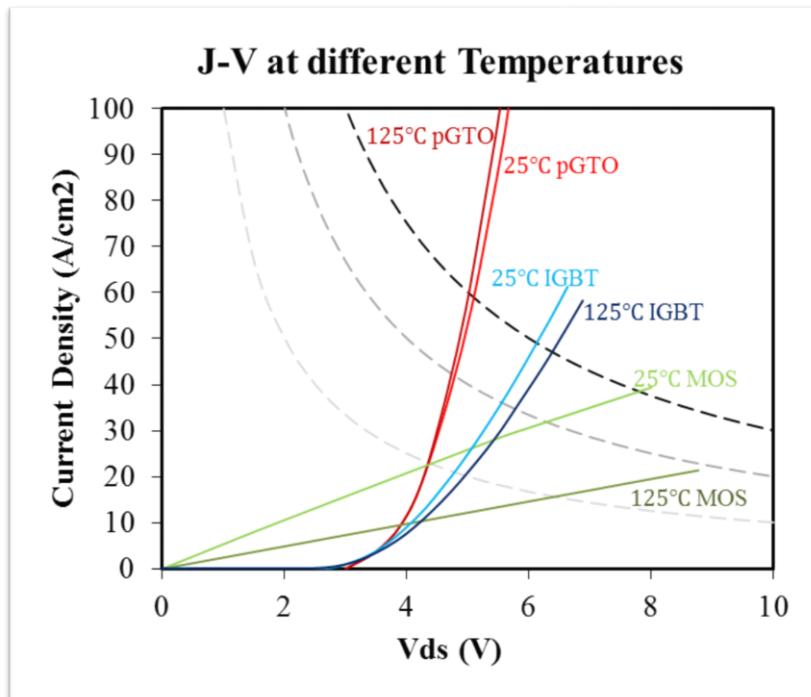


Figure 1-2 IV curves at different temperatures for 15kV 4H-SiC MOSFET, n-IGBT and p-GTO.

Figure 1-3 summarizes the recent >10kV 4H-SiC technologies of ambipolar transistors.

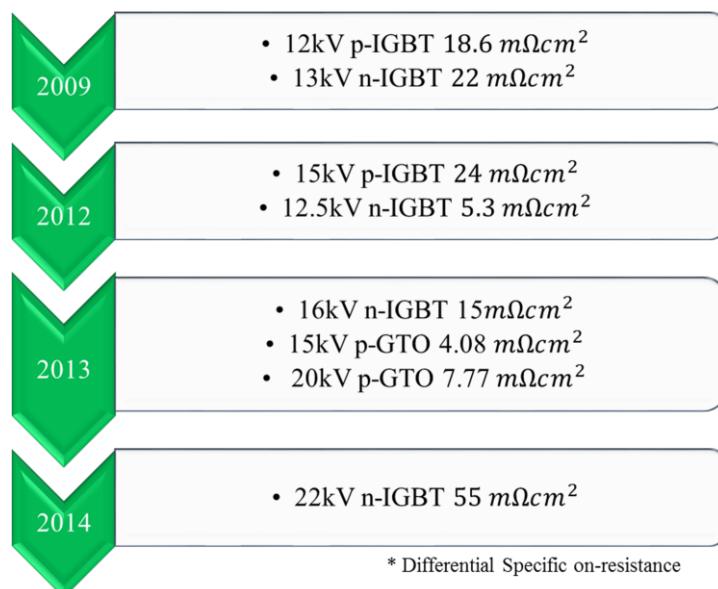


Figure 1-3 Recent progress on 4H-SiC high-voltage ambipolar switches.

From this trend shown in Figure 1-3, n-channel devices seem to be the focus for the future IGBT device technologies. It also has been experimentally [2] and theoretically [3] that n-channel IGBTs can switch faster than p-channel ones. The reason that n-GTO has not been demonstrated might be due to the poor quality of P+ substrate [4].

4H-SiC MOSFETs are strong candidates for the application in solid-state transformer (SST) for future smart grid technology because the faster switching speeds compared to 6.5 kV Si IGBTs [5]. The major advantage is that the lower switching loss due to its unipolar nature allows the device to operate at higher frequency, which significantly reduces the size of the passive components.

4H-SiC IGBTs are gate-controlled devices with conductivity modulation during on-state that can provide smaller conduction loss, and therefore, higher current capability than 4H-SiC MOSFET for the same voltage rating. For distribution level SST with up to tens of kilo watts (2.3~35kVA) [6], however, 15kV MOSFETs seems to be slightly favorable than its IGBT counterparts due to the switching loss for MOSFET is about half of the value of IGBTs [7]. Nevertheless, current trend or preference may be upset by the ongoing improvement and evolving on SiC device technologies. For example, a 16kV SiC injection enhanced n-IGBT (IEGT) [8] and a 22kV SiC n-IGBT have just been introduced in 2014 [9]. At 20kV voltage rating with junction temperature of 125°C, SiC MOSFET technology might suffer from a much higher conduction loss due to its unipolar nature.

For the applications of higher power rating (MVA~GVA) with lower frequency and high current, e.g. FACT and HVDC, SiC GTOs are the ideal candidates for the enabling technologies [6],[10]. Due to the regeneration action [11] during the on-state, the carrier

density profile in a thyristor is similar to a P-i-N diode, providing superior on-state characteristics than IGBTs.

## 1.2 Frequency capability V.S. Device Size (15kV MOSFET and IGBT)

It will be shown in this section that, for the current 15kV SiC device technologies, MOSFETs seem to be more favorable than IGBTs in terms of frequency capability. Based on the measurement results of 15kV devices at 125°C for switching loss (both turn-on and off) and conduction loss in [7], an empirical power loss estimation is provided in Table 1.1.

Table 1.1 Power loss estimation empirical models for MOSFET and IGBT

|                        | $P_{\text{conduct}}(W)$                        | $E_{\text{sw,sq}}(\text{Joule}/\text{cm}^2)$   | Coefficients   |
|------------------------|--|--|--|
| <b>15kV<br/>MOSFET</b> | $I \times I \times \frac{R_{\text{on,sp}}}{A}$ | $E_{\text{sw0,sq\_M}} + \frac{\partial E_{\text{sw,sq\_M}}}{\partial J} \frac{I}{A}$ | $R_{\text{on,sp}} = 0.4432$<br>$E_{\text{sw0,sq\_M}} = 0.0286$<br>$\frac{\partial E_{\text{sw,sq\_M}}}{\partial J} = 0.0014$ |
| <b>15kV<br/>n-IGBT</b> | $I \times (2.7 + k_m \sqrt{\frac{I}{A}})$      | $E_{\text{sw0,sq\_I}} + \frac{\partial E_{\text{sw,sq\_I}}}{\partial J} \frac{I}{A}$ | $k_m = 0.53$<br>$E_{\text{sw0,sq\_M}} = 0.0409$<br>$\frac{\partial E_{\text{sw,sq\_M}}}{\partial J} = 0.0025$                |

The on-state voltage drop for IGBT in the linear region is found to be proportional to  $\sqrt{I}$ . Therefore, the conduction loss is found to be proportional to  $I^{1.5}$ , as opposed to  $I^2$  for MOSFET. The switching loss versus current for both devices can be approximated as a straight line.

For a given power rating, 9kV blocking capability is assumed, the corresponding required current can be calculated. The total power loss of a transistors can be estimated by:

$$P_{\text{total}} = P_{\text{conduct}} \times \delta + E_{\text{sw},\text{sq}} \times f_{\text{sw}} \times A \quad (1.1)$$

Noted that the actual calculation of a power conversion circuitry is far more complicated but is not the focus of this work. The maximum switching frequency as a function of the device area at the 300W/cm<sup>2</sup> limit are given by:

$$f_{\text{max\_MOS}} = \frac{300 - \left(\frac{I}{A}\right)^2 R_{\text{sp,}on} \delta}{E_{\text{sw0,sq\_M}} + \frac{\partial E_{\text{sw0,sq\_M}}}{\partial J} \times \frac{I}{A}} \quad (1.2)$$

$$f_{\text{max\_IGBT}} = \frac{300 - [\frac{I}{A} V_{pn} + k_m \left(\frac{I}{A}\right)^{1.5}] \delta}{E_{\text{sw0,sq\_I}} + \frac{\partial E_{\text{sw0,sq\_I}}}{\partial J} \times \frac{I}{A}} \quad (1.3)$$

where

$$I \equiv \frac{\text{power rating}}{9000 \text{ volts}} \quad (1.4)$$

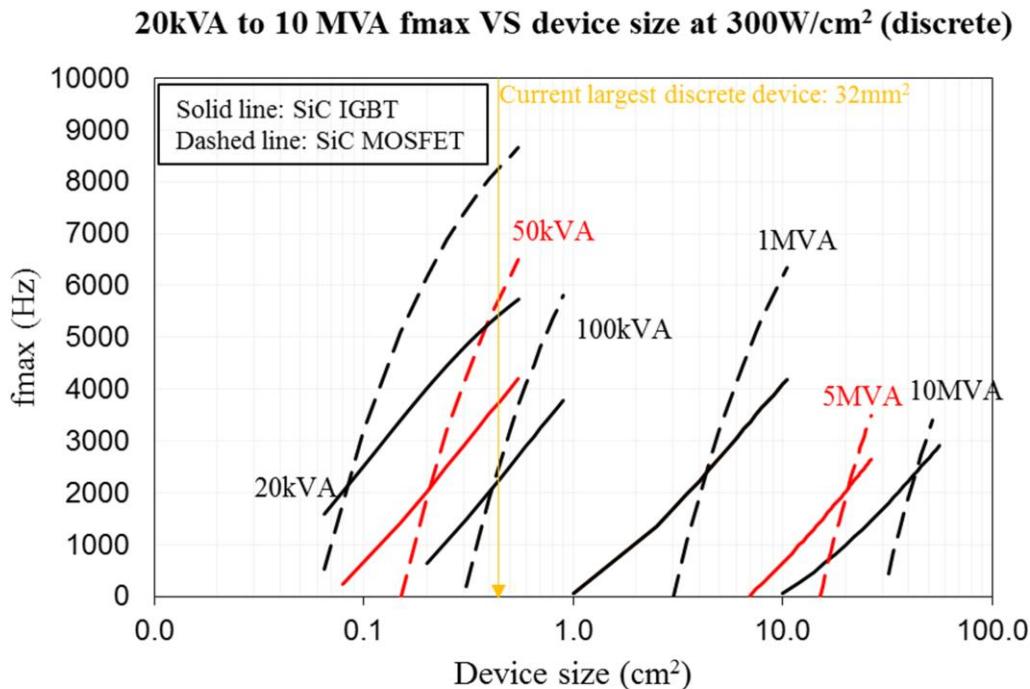


Figure 1-4 Frequency capability V.S. device size for 15kV MOSFET and IGBT at different power rating.

A preliminary assessment between MOSFET and IGBT in terms of frequency capability VS device size for different power rating are shown in Figure 1-4.

It can be observed that, for the current device technology:

- A. 15kV MOSFET seems to be more suitable than IGBT in terms of higher frequency switching for power rating up tens of kilo watts.
- B. Applications with power rating higher than 100kVA have to resort to multiple device paralleling or low frequency high current devices like GTO.
- C. The cross-over frequency is around 2k Hz.

### 1.3 Challenge and Outlook for SiC IGBTs for high frequency operation

Due to the presence of excess carriers in ambipolar switches, the design consideration of IGBTs not only have to include the device dimension and geometry, but also the ambipolar-related parameters and characteristics [12]. For the previous discussion on the 15kV device technology, SiC IGBTs seems to be unfavorable in terms of frequency capability. Also in [10], it has been predicted that SiC IGBT technology is only suitable for the voltage rating between 15kV and 20kV application, in which >20 kV devices are required for the safe operation. Due to the fact the development of SiC IGBTs starts relatively later than its MOSFET counter parts, it is of interest to see the impact of the feasible future improvements of device characteristics on the frequency capability.

Figure 1-5 shows the crossover frequency of 15kV and MOSFTs versus the percentage of improvement on either switching loss or conduction loss by fixing the other.

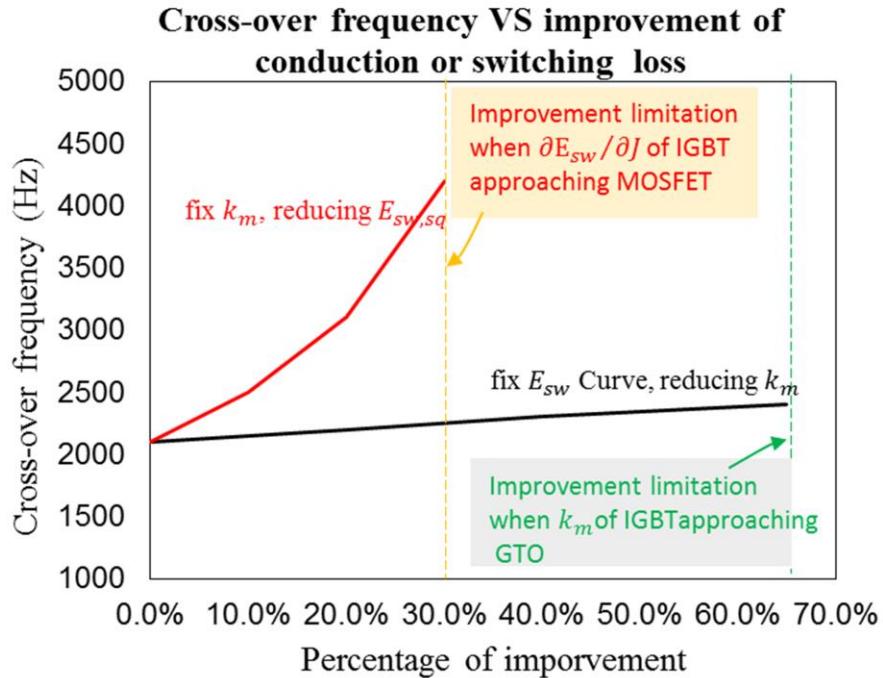


Figure 1-5 Crossover frequency V.S. Improvements in switching or conduction loss.

The improvement of the conduction loss is capped to the on-state voltage drop approaching that of GTOs. The improvement of the switching loss is capped to the case when  $\partial E/\partial J$  of the IGBT is the same as the MOSFET in Table 1.1. Noted that  $k_m$  is a coefficient in the empirical expression of conduction power loss described in Table 1.1. It can be seen that by reducing the switching loss is more efficient than reducing the conduction loss in terms of improving the frequency capability of IGBTs.

Although it seems unlikely to reducing switching loss without compromising the conductivity, it has been suggested that [13] the carrier density profile can significantly affect the switching loss. To be more specific, at a given total excess charge, different carrier profile distributions can have different switching waveforms and therefore different switching loss. The optimum carrier density profile is suggested to be higher close to the bipolar collector and lower to the bipolar emitter. In order to achieve this, except for the insertion of current spreading layer (CEL), the injection from the MOSFET channel has to be increased either by using trench technology or increasing the channel mobility. The channel mobility in a 16kV-4H-SiC IEGT has been demonstrated to be able to increase from 10 ~ 20 to over 100 cm/V.s [8]. Trench MOSFETs including U and V shaped channel have been demonstrated in [14] and [15].

Another issue of the 15kV 4H-SiC IGBT technology is the EMI issue that can be induced by the high  $dv/dt$  during the turn-off and turn-on [16]. The reason is the design of the drift region is not optimized and punch through at much lower voltage. This issue can be solved by optimizing the drift region [17] at the cost of longer epi layer and higher switching loss due to the shape of switching waveform.

## 1.4 The Purpose of this Modeling Work

Simulation is important and necessary for optimization either for device technology or circuit design. It can reduce the numbers of the cycle of learning and, especially for devices fabricated on new and expensive materials, minimizing the risk of destroying the devices during the test. For different purposes, different types of simulation or modeling are required.

Analytical modeling is necessary for the in-depth understanding of device physics [17], parameter extractions, or some preliminary works [18] of device macro models. For discrete device design, simulations based on Finite-Element Method are preferred in order to capture as many device physics as possible. For wide-band gap material, the execution time for steady-state is acceptable. However, transient simulation like double pulse switching including a physical freewheeling diode can take as long as few hours. Convergence problem is also an issue due to the extremely low intrinsic carrier density of wide-band gap materials.

For power conversion circuitry loss estimation, direct power loss calculation or device macro-models (in SPICE or SABER) can be the option. The former one takes shorter time to perform at the cost of lower accuracy compared to the latter one. Direct power loss calculation can be either analytical [19], or using ideal switch with loss lookup table [20]. Estimating loss using macro models may take longer time, but details of the waveform including, overshoots, current tail, ringing can only be observed using the macro models. Some of these phenomenon need to be included in the model in order to investigation of interaction between the transistors and the diodes [21] or to design gate drive circuit or filters for EMI issues [16] [22].

In terms of the focus of this work – high voltage 4H-SiC switches, very few of the aforementioned models are available for the 4H-SiC devices due to the relatively new

technology. Macro device models whose goal are to predict the genuine waveforms can present the unique characteristics, if any, of devices that are fabricated on the new materials. High voltage 4H-SiC IGBT and GTO are known for their two-phase transient, which need to be carefully addressed while building circuits using the components. In addition, as discussed earlier, excess carrier density profile plays an important role in the switching loss and also accurately prediction of dv/dt for EMI issue; therefore, macro models that are capable of emulating the effects of carrier density profile on the switching waveforms are desired. The goals of this work are:

- A. Builds macro model for 4H-SiC MOSFET, IGBT and GTO.
- B. Delivering models that can predict unique characteristics of these switches
- C. Developed models are capable of predicting the waveforms for different carrier density profiles.

## 1.5 Outline of this work

In chapter 1, the latest high voltage 4H-SiC switches have been introduced. Frequency capabilities versus device size have been plotted for IGBT and MOSFETs based on measurement data. The feasible improvement for 15kV IGBT's frequency capability are briefly discussed. Finally, the purpose and focus of this modeling work are listed.

In chapter 2, previous SiC high voltage MOSFET modeling works will be reviewed. The characteristics of high voltage 4H-SiC MOSFET with long drift region will be discussed. The

parameter extractions and fitting techniques will be introduced and followed the implementation of the model into Simulink/Matlab.

In chapter 3, different methodologies of constructing the IGBT model will be reviewed and pros and cons will be addressed. The modified equations for ambipolar devices and an analytical turn-off model that has included the displacement current and local carrier density will be presented. A novel characterization technique – Excess Carrier Distribution Mapping (ECDM) – will be introduced. Finally, the model will be implemented into Simulink/Matlab and will demonstrate its capability to capture the unique features for 4H-SiC IGBTs.

In chapter 4, optimization works for high voltage 4H-SiC IGBTs will be reviewed. With the aid of developed analytical model, feasible concepts of improving the IGBT performance by using today's device technology will be proposed. Then, novel structures in order to achieve these goal will be proposed and investigated using TCAD simulation.

In chapter 5, 4H-SiC GTO model that accurately predicts on-state and transient characteristics will be discussed. It will be shown that the proposed new model for the ambipolar switches are capable of accurately predicting the device behavior even if the ambipolar lifetime is not uniform throughout the drift region.

Chapter 6 will summarize the main contribution of this work.

## Chapter 2

### 10A 15kV 4H-SiC MOSFET Modeling

This chapter will describe the implementation of a 10A 15kV 4H-SiC MOSFET sub-circuit model. Previous modeling works for 4H-SiC MOSFET will be reviewed, and improvement on the existing model will be proposed and incorporated in this model. The modeling focus on ultrahigh voltage SiC transistors will also be addressed. The methodology and parameter extraction procedure of the proposed model is summarized in Figure 2-1.

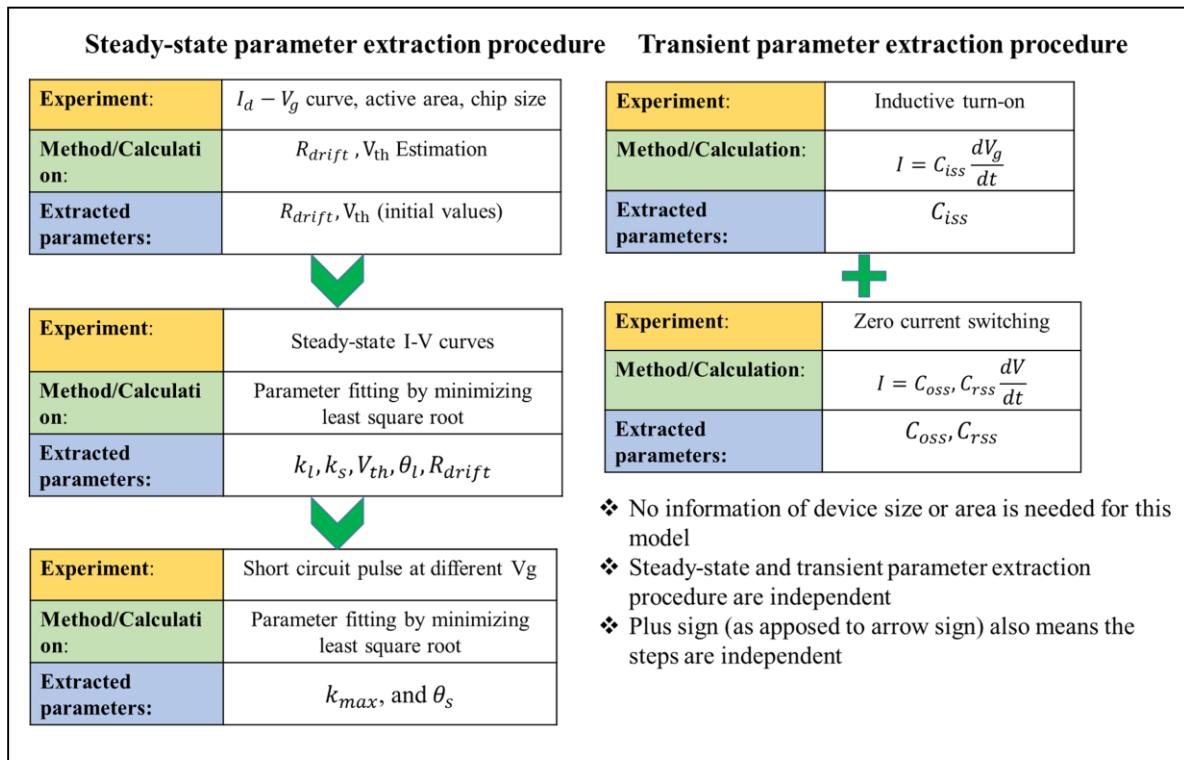


Figure 2-1 The flow chart of parameter extraction of the proposed 4H-SiV 15kV MOSFET.

We will first roughly estimate part of the parameters based on the information of nominal dimension provided by the vendor. Then, MOSFET current equation in different regions will be introduced with parameters that needs to be extracted or fitted. Measurement data from the packaged device will be used to fit or optimized those parameters, such as threshold voltage and transconductance, in the proposed MOSFET equation. Parasitic capacitance  $C_{oss}$ ,  $C_{iss}$  and  $C_{rss}$  will be extracted. The model will be implemented in Simulink/Matlab.

## 2.1 Review of existing models

Ultra high voltage ( $>10\text{kV}$ ) 4H-SiC MOSFET have been developed in recent years for the components used in future smart grid application. Although the commercialized 1200V SiC MOSFET modeling have been proposed in recent years, few high voltage MOSFET modeling works have been reported. The major differences between high voltage 4H-SiC MOSFET and low-to-medium voltage ones are that (a) the drift region is long and (b) current saturation happens at much higher drain bias.

It is well-known in general that the extension of the edge termination is at least 5~6 times of the drift region length. For example, the recent 15kV MOSFET has a  $32\text{mm}^2$  active area but with a  $64\text{mm}^2$  total chip size. This means that the current spreading effect of a high voltage device cannot be ignored. Calculating the drift region resistance using active area may lead to erroneous results based on the discussion above. Although it is possible to still have a compact model by parameter fitting to the measurement results, the model will not be physically legitimate.

The conduction current level in the saturation region is important since the model has to predict the short circuit capability. In addition, during switching transient, the MOSFET is in the saturation region and the channel current need to be correctly modeled. Figure 2-2 and Figure 2-3 are the TCAD simulation IV curve for a medium voltage and high voltage SiC MOSFET, suggesting that the saturation bias is much higher for high voltage SiC than for medium one. This is due to the peak electric field, which is the cause of the velocity saturation, increases slower in high voltage SiC with lower doping drift region according to Poisson equation.

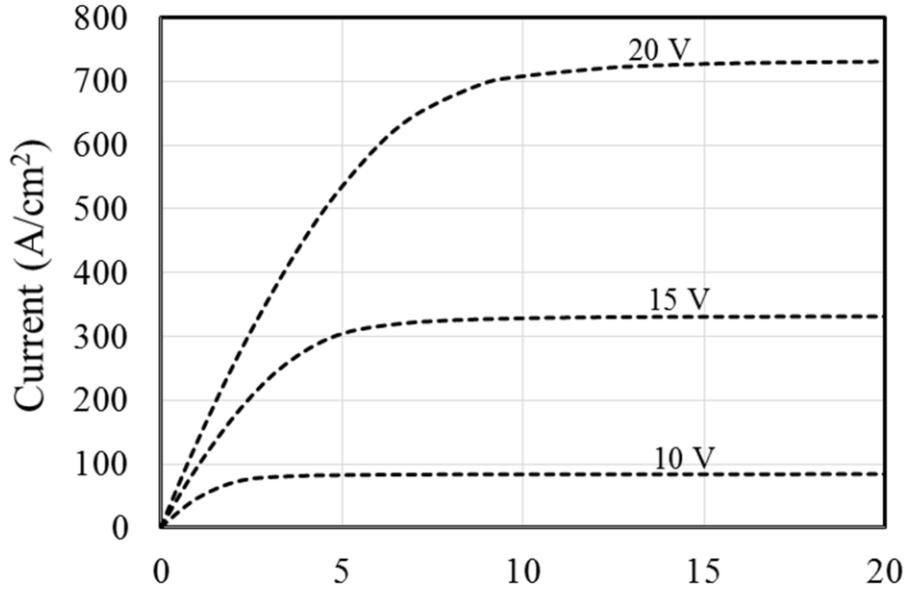


Figure 2-2 Simulated IV curves of 4H-SiC 650 V MOSFET with constant channel mobility

This particular feature of high voltage SiC MOSFET – saturation voltage increases drastically as the gate voltage increases – poses a challenge when it comes to fitting the IV curves with relatively simple equations.

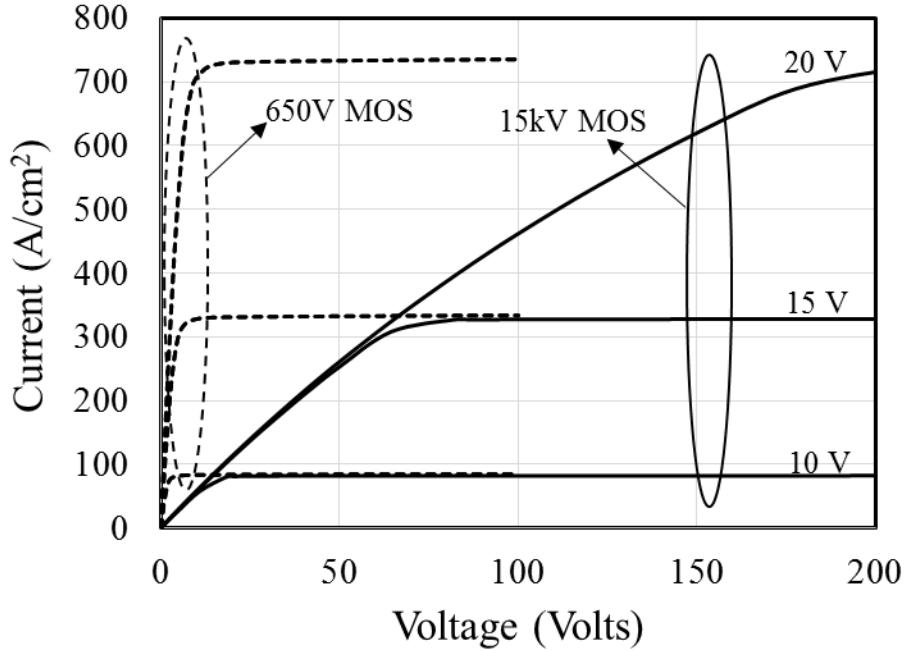


Figure 2-3 Simulated IV curves of 4H-SiC 15 kV MOSFET (overlapped with 650 V) with constant channel mobility.

In 2007, a 2kV SiC MOSFET model [23] has been developed in Saber<sup>TM</sup>. The drift region resistance is calculated based on the doping concentration provided by the vendor and the active area. Although the current spreading effect might not be significant given that it only has 20  $\mu\text{m}$  drift region, using only active area to calculate the resistance for longer drift region (e. g. 100  $\mu\text{m}$ ) might be erroneous. In addition, in order to deal with the fact that the saturation happens at higher drain bias for high voltage SiC MOSFET, the author in [23] propose superposition of  $I_{\text{mosh}}$  and  $I_{\text{mosl}}$  to fit the total current. One component saturate at lower drain bias and another saturate at higher drain bias. This results in more complicated current equations and the number of parameters that need to be extracted might be doubled compared

to the model without superposition of two current components. Finally, the parameter extraction procedure in the paper requires unique software that might not be easily accessible to the public. In 2008, a 10kV MOSFET model in SPICE has been proposed. The MOSFET equations being used are the SPICE level 1 model. The drift region resistance is fitted in a behavior manner, and the saturation current is not discussed. For dynamic switching, a rather complicated sub-circuit is used to describe the non-linear capacitance  $C_{gd}$ . In sum, the goal is to develop a macro device model of 4H-SiC high voltage MOSFET for circuit simulation with fairly simple current equation. The model will have the ability to describe the current in the saturation region and fit the IV curves with the drastic increase of  $V_{d,sat}$  as gate voltage increases.

## 2.2 On-state modeling of the proposed model

### 2.2.1 Drift region resistance

Accurately modeling of the drift region resistance is important especially for the high voltage device with a long drift region. Figure 2-4 shows the simple cross-section of the MOSFET and the simplified equivalent circuit to describe the behavior during on-state.

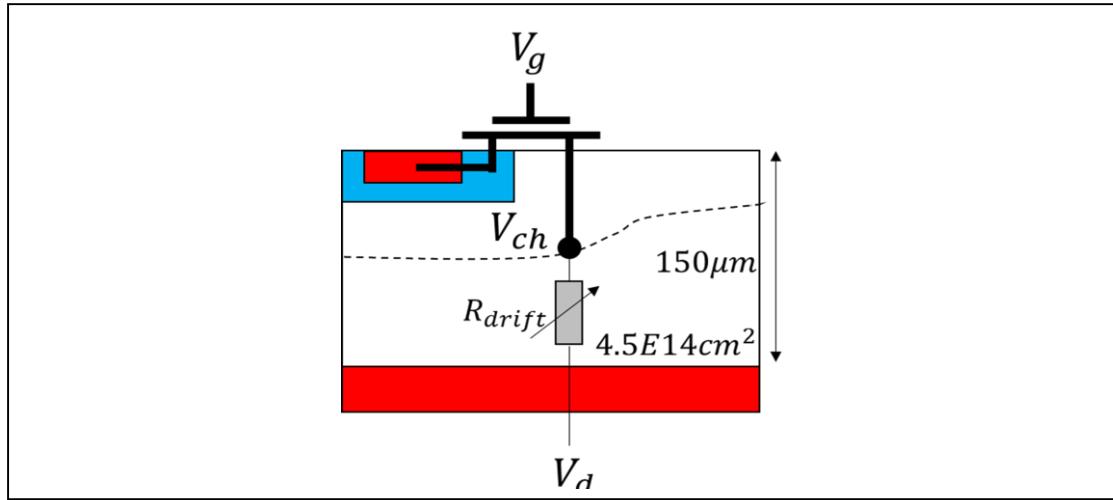


Figure 2-4 Simplified Cross-section and simple equivalent circuit of 4H-SiC 15kV MOSFET.

Figure 2-5 illustrates the current conducting path from the back side to the top active area. The nominal chip size and active area are  $64\text{mm}^2$  and  $32\text{mm}^2$ , respectively. The resistance between the top and bottom metal should be calculating using the effective cross-section marked using the red dashed line in Figure 2-5. Table 2.1 shows that it would be erroneous if calculating  $R_{\text{drift}}$  using the active area of  $32\text{mm}^2$ .

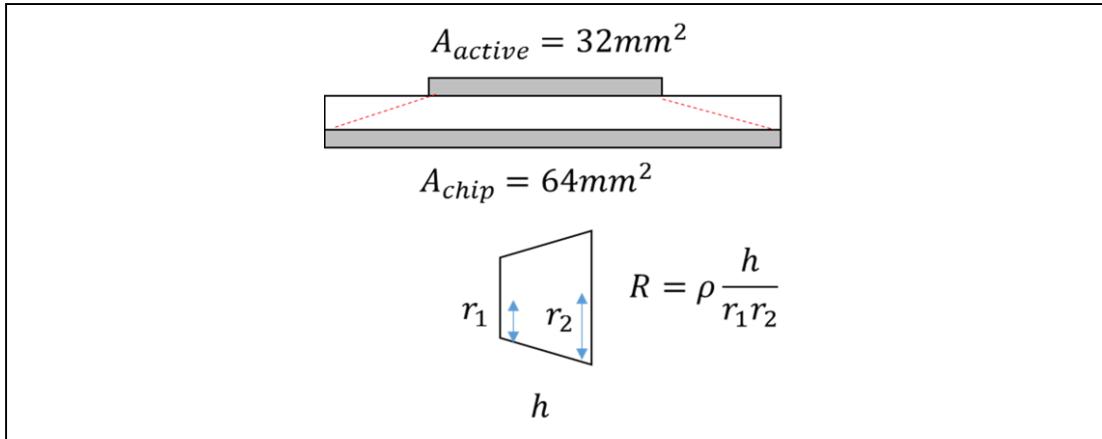


Figure 2-5 Device dimension and resistance estimation of 10A 4H-SiC 15kV MOSFET.

Noted that, however, the actual resistance can be up to 10% lower due to the fact that there will be some fringing current outside the truncated shape indicated by the red dotted line. The active area under low drain bias should be at least  $45.3\text{mm}^2$ . The estimated drift region resistance at room temperature and low drain bias is  $0.488\ \Omega$ . This initial estimated value will be optimized within a 10% range of this estimated value together with other parameters in the model.

Table 2.1 Resistance calculated using different methods.

| <b><math>R_{\text{total}}(25^\circ\text{C})</math><br/>(Measured)</b> | <b><math>R_{\text{drift}}(25^\circ\text{C})</math><br/>(Calculated using active area)</b> | <b><math>R_{\text{drift}}(25^\circ\text{C})</math><br/>(Calculated using effective active area)</b> |
|---|---|---|
| $0.627\ \Omega$   | $0.703\ \Omega$ (not likely)  | $0.488\ \Omega$   |

### 2.2.2 Velocity saturation in the drift region

The velocity saturation in semiconductor power devices happens near the area of high electric field. For vertical power MOSFET, the current saturation mechanism might result from the combination of two: (a) saturation in the channel and (b) saturation in the JFET region, or quasi saturation. For high voltage device with lightly doped drift region, the saturation will happen at higher drain bias, as depicted in Figure 2-6. To reach the peak electric field that causes the velocity saturation, device with lightly doped drift region has to apply more voltage to reach that value according to Poisson equation.

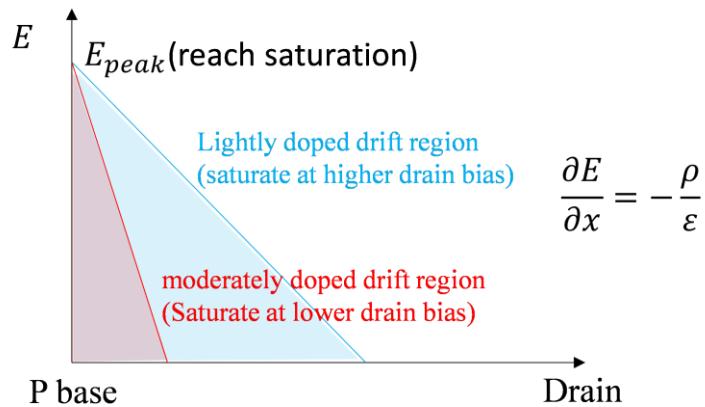


Figure 2-6 The illustration of the difference between E field in low and high doping drift region

Figure 2-7 and Figure 2-8 plot electron velocity at varied drain bias for two SiC MOSFETs with 4.5E15 and 1E15 cm<sup>-3</sup> doping, respectively. At relatively low drain bias, the channel as well as the JFET region for 650 V MOSFET already reach velocity saturation, whereas 15kV MOSFET does not have velocity saturation at relatively high drain bias.

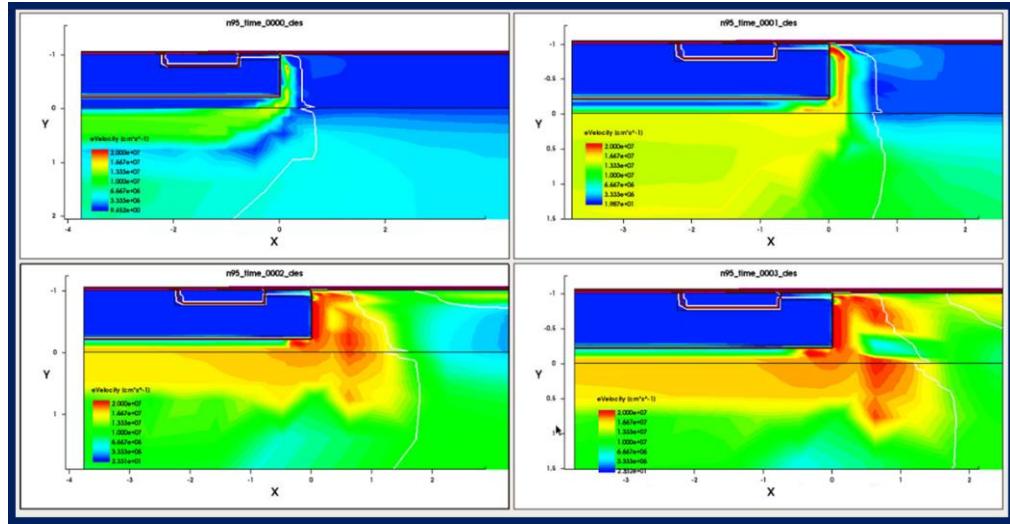


Figure 2-7 Electron velocity plots of SiC MOSFET with  $ND=4.5E14 \text{ cm}^{-3}$  at  $Vg=15$  volts and  $Vdd= 45, 100, 150, 170$  volts. Current start to saturate at  $Vdd=150$  volts.

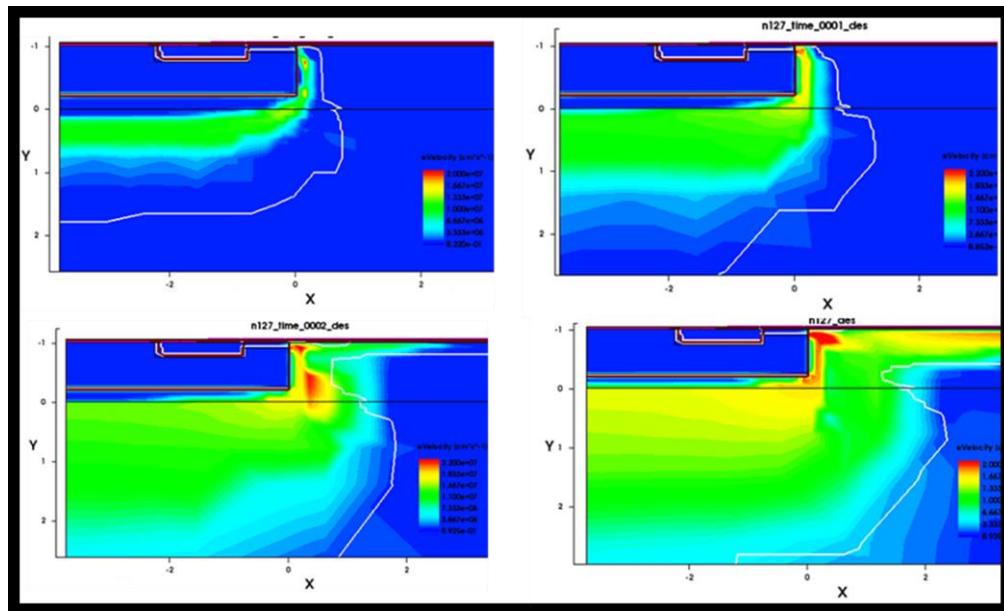


Figure 2-8 Electron velocity plots of SiC MOSFET with  $ND=4.5E14 \text{ cm}^{-3}$  at  $Vg=15$  volts and  $Vdd= 1, 4, 6, 7.5$  volts. Current start to saturate at  $Vdd=4$  volts.

Figure 2-9 is the electron velocity versus the electric field in 4H-SiC, which indicates that the velocity starts to saturate after the electric field of 1E5V/cm. Later in the derivation of MOSFET current equation, the peak electric field of 1E5 V/cm is assumed to be the criteria of velocity saturation.

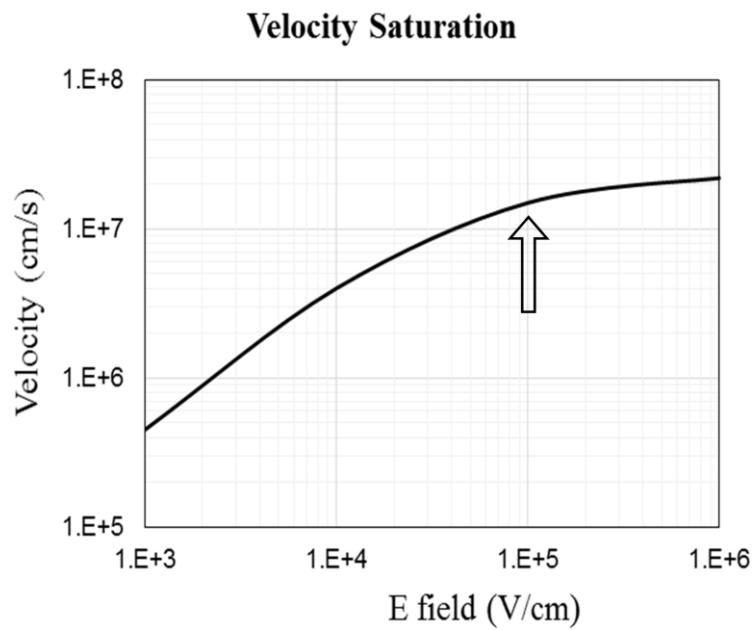


Figure 2-9 Electron velocity V.S. electric field for 4H-SiC

### 2.2.3 MOSFET current equation and its parameters

*Linear region ( $k_l$ ,  $k_s$ ,  $\theta$ ,  $V_{th}$ ):*

The equation that describes voltage-current relationship in the linear region is given in tab. III. The transconductance in the linear region at smaller drain bias is  $k_l$ , and  $k_s$  serves as a correction term to gradually modulate the transconductance as the drain bias increases. The effect of channel mobility as a function of vertical electric field in the channel is modeled by the parameter  $\theta_l$ . These parameters will be directly fitted later using the measurement results. The threshold voltage  $V_{th}$  can be estimated using  $V_{gs} - I_d$  curve and will be optimized later along with the other parameters.

Table 2.2 MOSFET current equations for steady-state

| MOSFET Equation   |   |
|---|---|
| $I_{d,lin} = \frac{k_l \times [(V_g - V_{th}) \times V_{ch} - \frac{1}{2} \times V_{ch}^2 \times \frac{k_l}{k_s}]}{1 + \theta_l (V_g - V_{th})},$ | $V_{ch} < (V_g - V_{th}) \frac{k_l}{k_s}$ Linear region |
| $I_{d,trans.} = \frac{V_{dh} - V_{dl}}{I_{dh} - I_{dl}} V_{ch} + I_{dl},$   | $V_{dl} \leq V_{ch} \leq V_{dh}$ Transition region      |
| $I_{d,sat} = \frac{\frac{1}{2} k_{max} (V_g - V_{th})^2}{1 + \theta_s (V_g - V_{th})},$   | $V_{ch} \geq V_{dh}$ Saturation region                  |
| $I_{d,off} = 0,$  | $V_g \leq V_{th}$ cut-off region                        |
| $V_{dh} = \frac{\varepsilon E_{corner}^2}{2qN_D} + V_g - V_{th},$   | $E_{corner}(4H - SiC) \cong 1E5 (\frac{V}{cm})$         |
| $V_{dl} = (V_g - V_{th}) k_l / k_s$   |   |
| $I_{dl} = I_{d,lin} (V_{ch} = V_{dl})$  |   |
| $I_{dh}(V_g)$ is constants at different $V_g$ , measured by a short gate pulse at 2kV bias  |   |
| KVL   |   |
| $V_d = V_{ch} + R_{drift} \times I_d$   |   |
| $R_{drift} = \frac{1}{qN_D \mu_n} \frac{L}{\sqrt{A_{active} \times A_{chip}}},$ where $L = W_D - \sqrt{2\varepsilon V_{ch}/qN_D}$                 |   |

Figure 2-10 shows that the Vds-Id curve at low gate bias at different temperature, and clearly the threshold voltage decreases with temperatures. The estimated threshold voltage ranges from 5.3 volts at room temperature to 3.5 volts at 125°C. After the initial estimation of some parameters, the fitting is conducted in EXCEL by finding the sum of the least square root between the calculated and measured data points, as shown in Figure 2-11. The initial estimation is necessary to avoid the iteration of finding the minimum ending up converging to local minimum instead of global minimum.

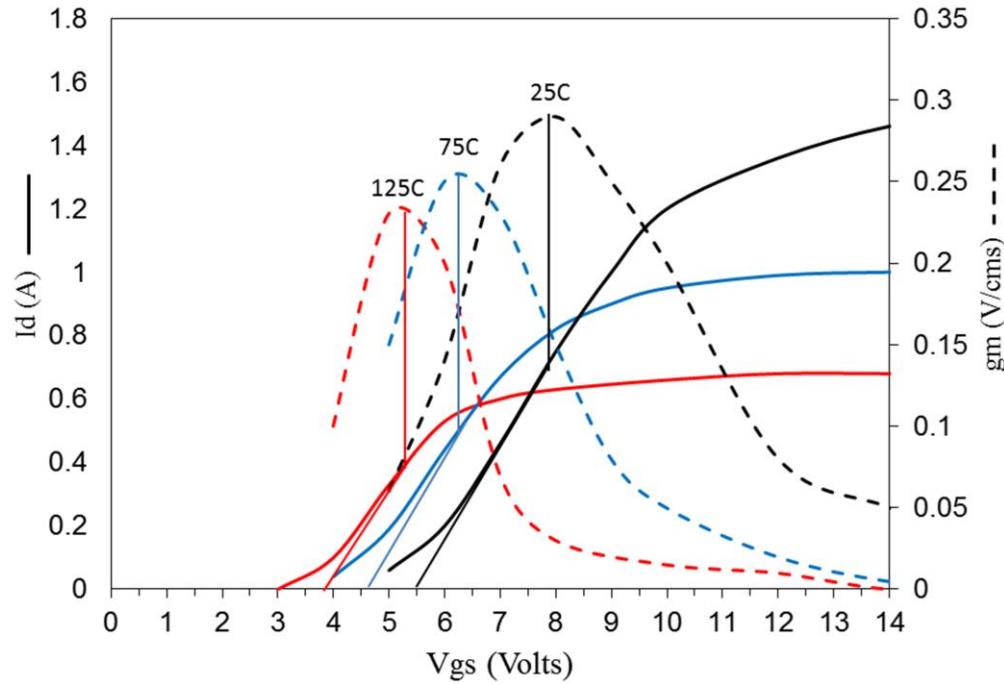


Figure 2-10 Threshold voltage extraction at different temperatures.

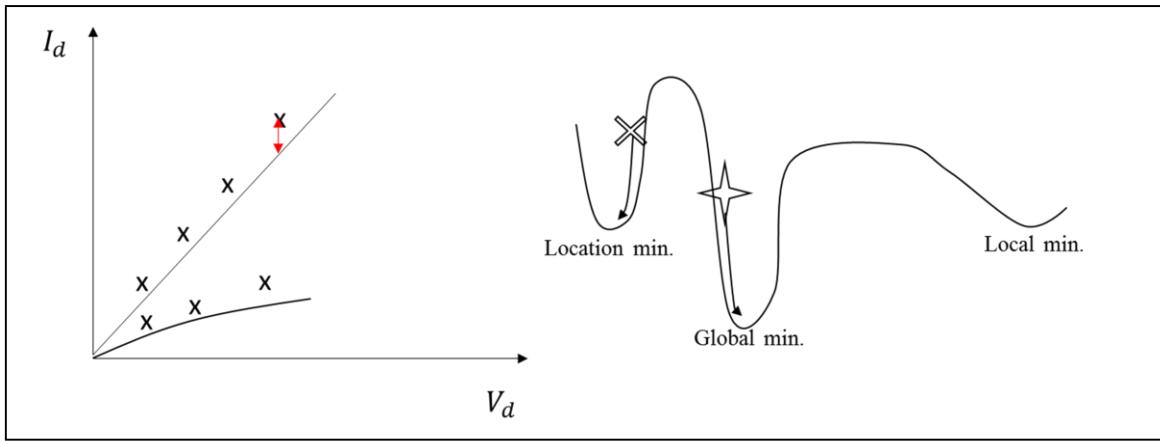


Figure 2-11 Parameters optimization by iterating to find the minimum sum of least square root.

Figure 2-12 shows the simulated and measured I-V curve at different gate voltage at room temperature.

Figure 2-13 shows the model can predict that the on-state conductance is lower at elevated

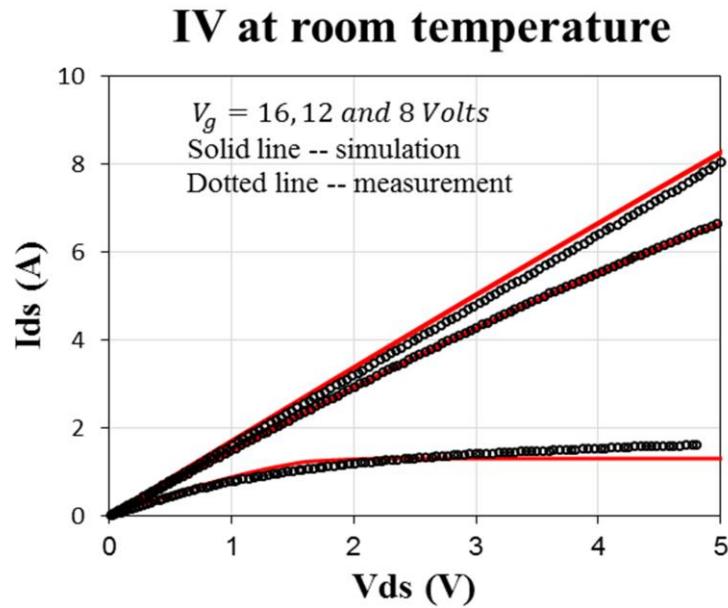


Figure 2-12 Simulated and measurement results for 15kV MODFET at lower bias.

temperature. Figure 2-14 is the extracted threshold voltage and transconductance as a function of temperature.

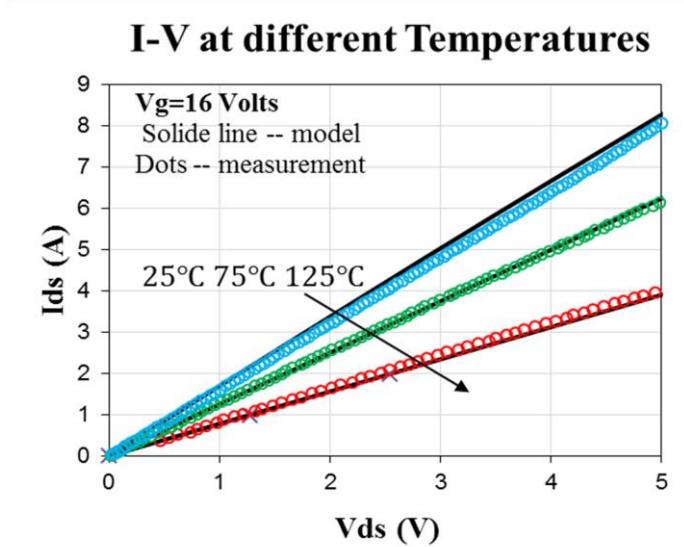


Figure 2-13 Simulated and measurement IV curves of 15kV MOSFET at different temperatures.

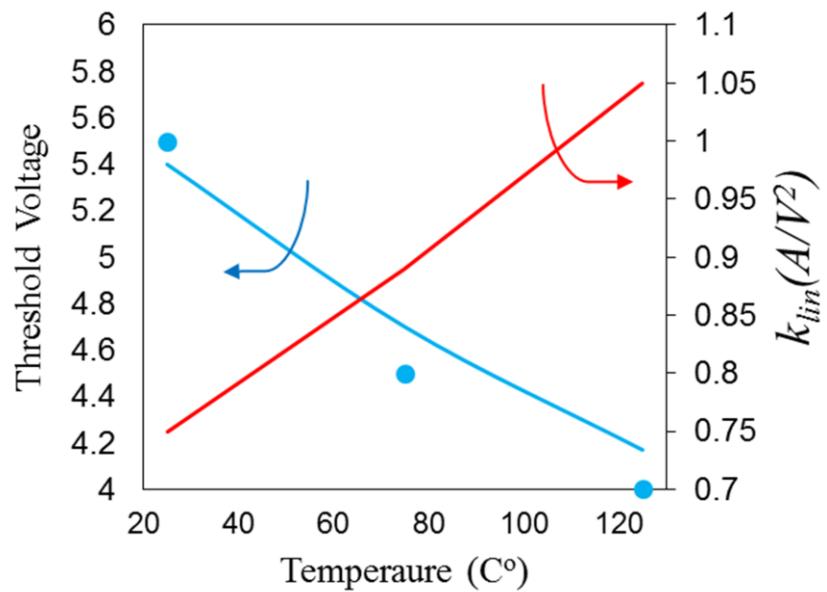


Figure 2-14 Transconductance in the linear region and threshold voltage as a function of temperature.

*Saturation region ( $k_{max}, \theta_s$ ):*

MOSFET current at higher bias is assumed to be a constant in this model. The saturation region is defined as the peak electric field exceeds  $1E5$  V/cm, as pointed out in Figure 2-6. The illustration of the difference between E field in low and high doping drift region. The measured saturation current level at different gate bias is obtained by giving a gate pulse at  $V_d=2k$  [7]. The equation in this region is provided in tab. III. By using the same parameter optimization manner introduced earlier, the fitted transconductance in the saturation region and  $\theta_s$  are shown in Figure 2-15.

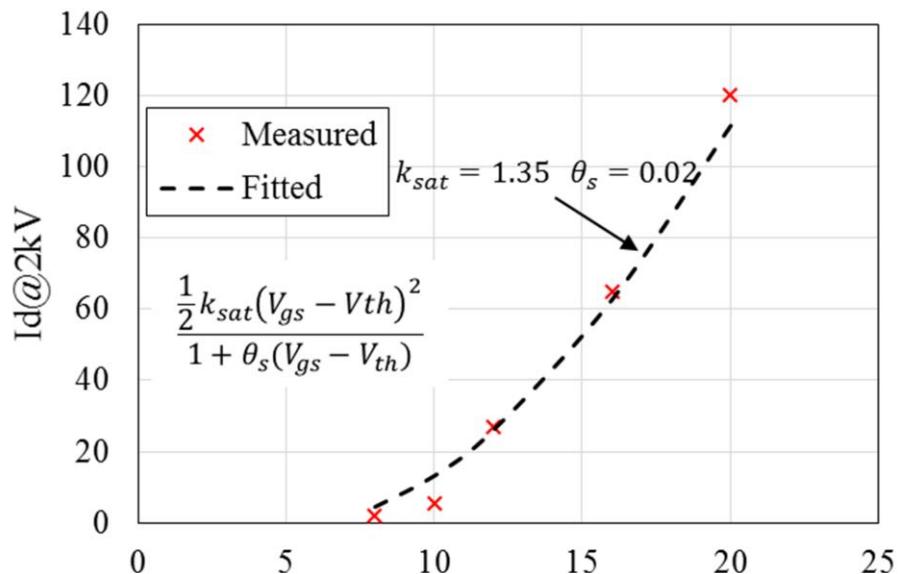


Figure 2-15 Transconductance in saturation region and saturation current vs gate voltage

For low-to-medium voltage MOSFET behavior modeling, using only two region can smoothly fit the model with the measurement results for a wide gate bias range. However, it is difficult for high voltage SiC MOSFET due to the fact that the difference between the saturation voltage at high gate bias and low bias is too large, as evidenced in **Error! Reference source not found.** and **Error! Reference source not found.** (15kV and 650kV) plotted using TCAD simulator, in which the parameter file in the channel region of the software are identical. This make it difficult to fit the curve using only linear and saturation region in a wide range of gate bias. Therefore, a transition region must be introduced between the linear and saturation region. This region also known as quasi-saturation region [24], in which the voltage drop across the depletion region prevent the end of the channel from perceiving the high electric field. Nevertheless, the current (and the electron velocity) will still gradually saturate due to the velocity saturation in the depletion region of the drift region.

*Transition region (quasi-saturation):*

In [23], two current components  $I_{mosh}$  and  $I_{mosl}$ , are superposed in the linear region to smoothly connects the linear region and saturation region. In this proposed model, a simpler way of describing this region is to connect the linear region and the saturation region with a straight line. Although losing certain fidelity in this region is inevitable, from a practical point of view, this region is insignificant in real circuit operation.

The boundaries between linear/transition region ( $v_{dl}$ ) and transition/saturation region ( $v_{dh}$ ) have to be defined. The linear region at corresponding gate voltage ends when the derivative of the I-V curve is zero. The saturation region starts when the peak electric field in the drift region reaches  $1E5$  V/cm $^2$ . The equations and relations are provided in Table 2.2, and the final IV curves across three regions are shown in Figure 2-16.

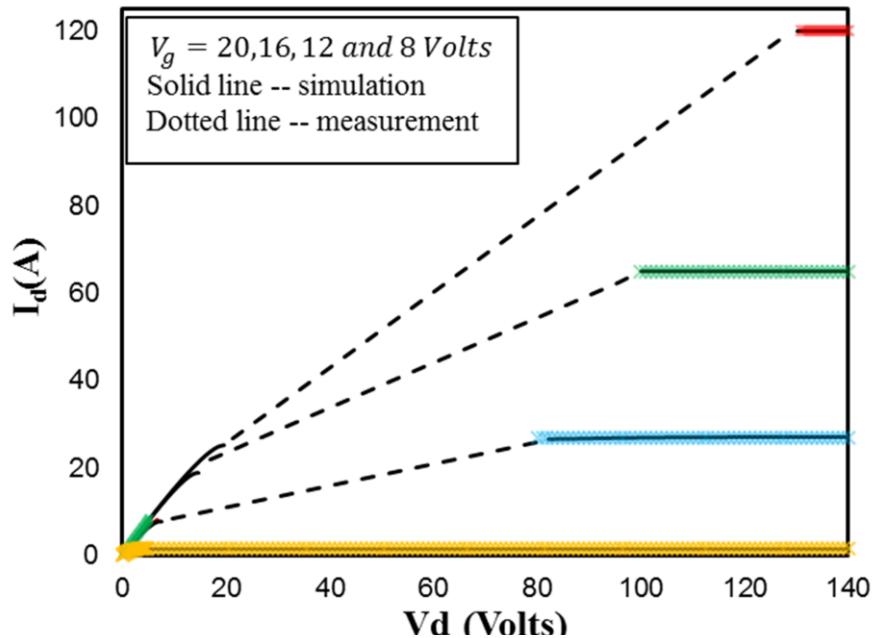


Figure 2-16 Modeled IV curves of 15kV MOSFET in linear, transition, and saturation region.

## 2.3 Dynamic switching modeling

### 2.3.1 Switching dynamics during turn-on

Figure 2-17 shows three phases during turn-on transient and the current flows. Figure 2-18 shows the corresponding voltage and current waveforms.

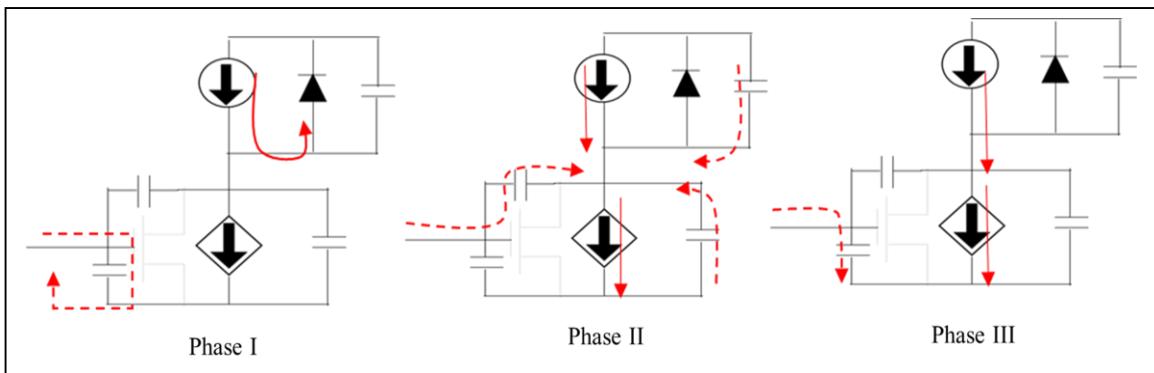


Figure 2-17 Turn-on transient and current flows. Solid and dashed lines are the conduction and displacement current, respectively.

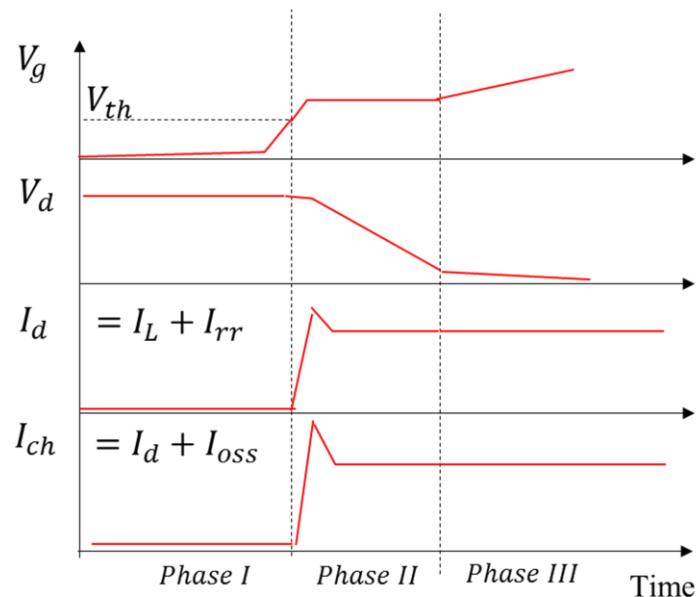


Figure 2-18 Typical turn-on waveforms of a MOSFET with a freewheeling diode.

### *Phase I:*

This phase is defined before the gate voltage reaches the threshold voltage. The gate current is charging the  $C_{gs}$  through gate resistances. The non-linear  $C_{gs}$  will decrease from its maximum capacitance  $C_{max}$  at negative gate voltage to its minimum capacitance value  $C_{min}$  when the gate voltage increases toward threshold voltage. Therefore, the gate voltage charging trajectory is slow (delay) and then fast. The channel remains off during this phase while the load current floating through the freewheeling diode.

### *Phase II:*

Once the gate voltage rises above the threshold voltage, the channel starts to turn-on, and the channel current rises. When the gate voltage reaches the “Millar plateau,” the drain voltage will start to rise, while gate current will flow mostly through  $C_{gd}$ . Noted that due to the  $dv/dt$  presents at the drain node, there will be displacement current flow from the capacitance of the diode. Also noted that the total current that flow through the channel is the sum of  $i_{oss}$ ,  $I_L$  and  $I_{rr}$ . The displacement current that discharge the output capacitance ( $i_{oss}$ ) is an internal current that cannot be measured at the drain node. But this current component will contribute to the total turn-on loss.

### *Phase III:*

After the drain voltage decrease to the on-state voltage drop at the gate plateau voltage, the gate current stops flowing through  $C_{gd}$  and starts to further overdrive  $C_{gs}$  until the gate voltage reaches the input gate signal.

### 2.3.1 Switching dynamics during turn-off

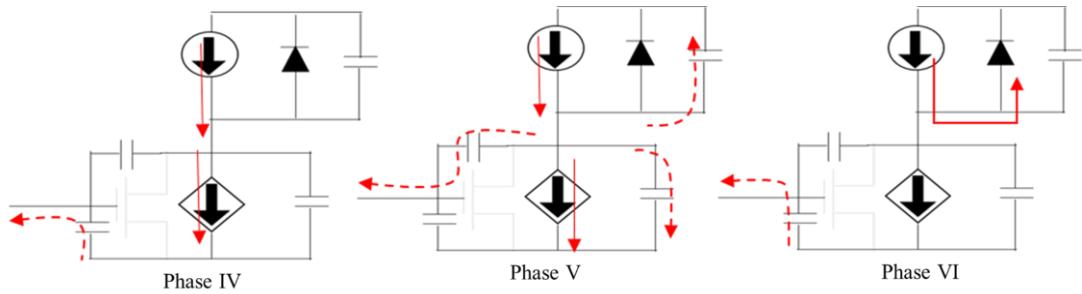


Figure 2-19 Turn-on transient and current flows. Solid and dashed lines are the conduction and displacement current, respectively.

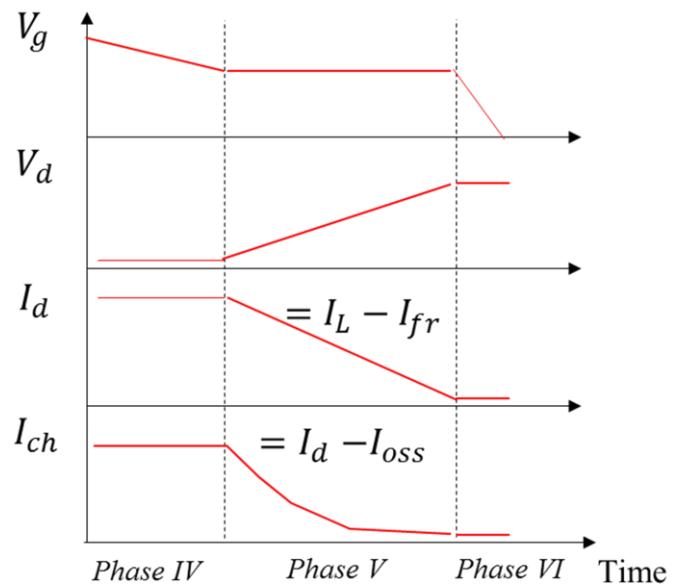


Figure 2-20 Typical turn-on waveforms of a MOSFET with a freewheeling diode

#### Phase IV:

The gate current slowly discharges  $C_{gs}$  before the gate voltage reaches the Miller plateau. The drain voltage will slightly increase due to the increase of channel resistance.

#### Phase V:

When the gate voltage reaches certain value (plateau), the channel current is not large enough to carrier all the load current. Part of the load current will start to charge the capacitance seen by the drain node – output capacitance of the MOSFET as well as the diode. The current measured at the drain node will decrease since part of the load current has been stolen by the diode output capacitance due to the presence of  $dv/dt$ . Noted that, internally, the current flowing through the channel is even smaller and is equal to the drain current minus the current that charging the MOSFET output capacitance.

#### Phase VI:

When the drain voltage exceeds the bus voltage plus the forward voltage of the diode, the diode starts to turn on. The drain voltage will remain constant and the gate current will equal to the current that discharging  $C_{gs}$

### 2.3.2 Extraction of parasitic capacitance

*Output capacitance ( $C_{oss}$ ):*

The output capacitance is composed of  $C_{ds}$  and  $C_{gd}$ . It can be obtained by giving a current pulse and directly measuring the  $dv/dt$  with the gate and source shorted. Alternatively, one can switch two parallel devices with the DUT's gate and source connecting to the ground. The output capacitance of the DUT can then be obtained by dividing the current flowing through it by  $dv/dt$ .

Since the device active area ( $32\text{mm}^2$ ) and chip size ( $64\text{mm}^2$ ) are known, it is interesting to compare the calculated and extracted results, as shown in Figure 2-21. Surprisingly, even calculated using the total chip size area, the calculated output capacitance is still two times smaller than the actual measured results. The difference of the capacitance value may come from package capacitance, fringing effect and 2-D effect while the depletion region expanding/retrieving in the edge termination area. In other words, these secondary effect makes it harder to charge/discharge the overall capacitance than a 1-D ideal capacitance, and therefore, the real capacitance value is expected to be higher.

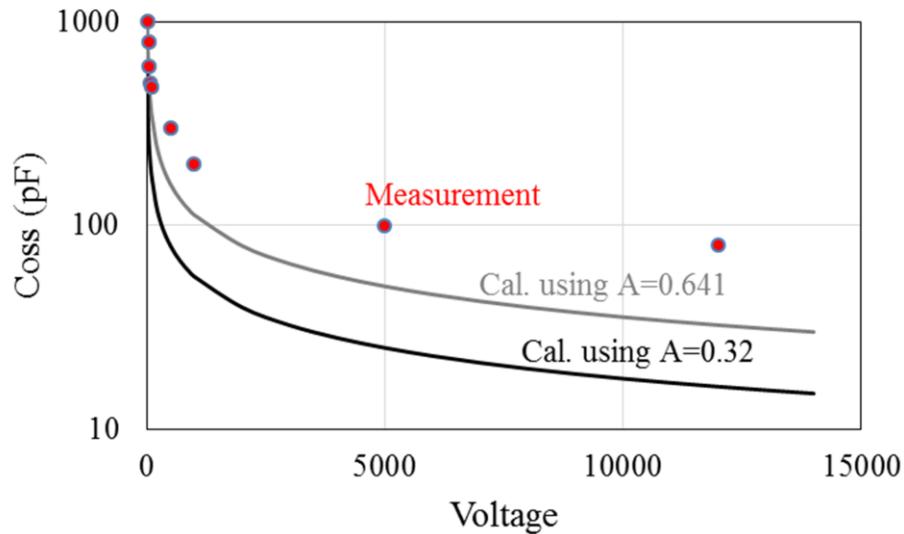


Figure 2-21 The measured output capacitance of the 15kV MOSFETs compared to calculated values.

*Crss (reverse transfer capacitance):*

Also known as the gate-to-drain capacitance, this capacitance can be extracted by dividing the gate current during the Miller plateau by the dv/dt during turn-on.

*Ciss (input capacitance)*

This capacitance consists of  $C_{gd}$  and  $C_{gs}$ . Since  $C_{gd}$  has been extracted, we will only discuss the extraction of  $C_{gs}$ . A typical  $C_{gs}$  as a function of gate voltage is depicted in Figure 2-22. The  $C_{max}$  is extracted by using the  $V_g-t$  curve in phase III during turn-on. The  $C_{min.}$  is extracted by using the  $V_g-t$  curve in phase I during turn-on.

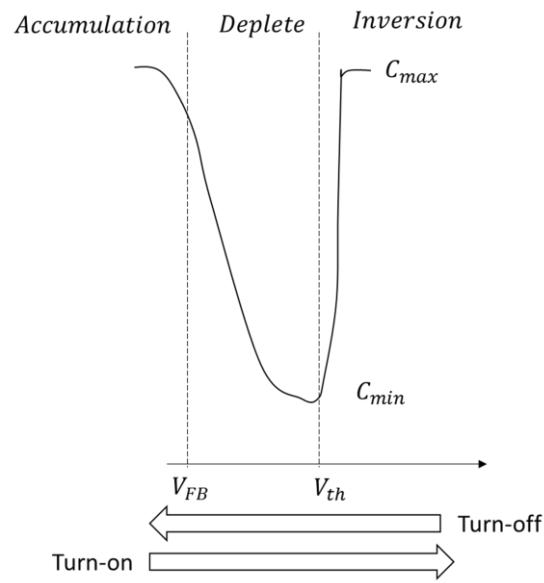


Figure 2-22 Typical CV curve for the input capacitance of a MOSFET.

The C-V curves for the 10A 15kV 4H-SiC MOSFET with a 32mm<sup>2</sup> active area is shown in Figure 2-23.

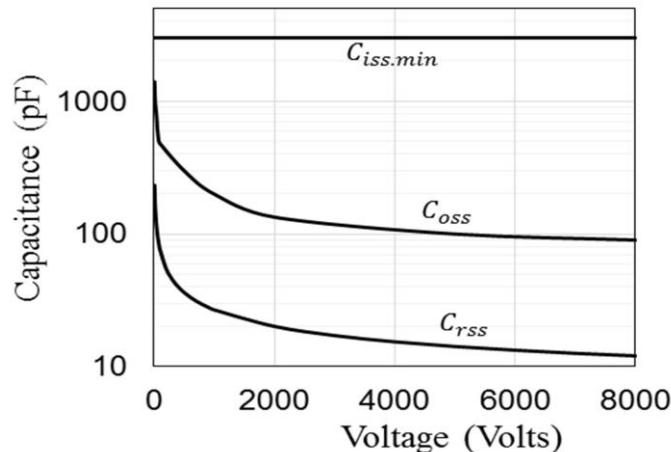


Figure 2-23 Extracted Coss, Ciss and Crss for the 15kV MOSFET.

## 2.4 Model implemented in Simulink/Matlab

Simulink/Matlab is a powerful software that allows model developer to write the equations in the user-defined box to describe the device behavior. For example, the MOSFET equation in tab. III are directly written in the user-defined box to serve as a voltage-controlled current source. The implementation of non-linear capacitance can be done by building a look-up table, in which the capacitance as a function of the voltage can be directly plotted. This means no cumbersome equation is needed to account for the secondary effect of the capacitance (for example 2-D effects). The capacitor implementation is shown in Figure 2-24, in which the 1-D look up table is where the user can directly draw or key in the capacitance value as a function of voltage.

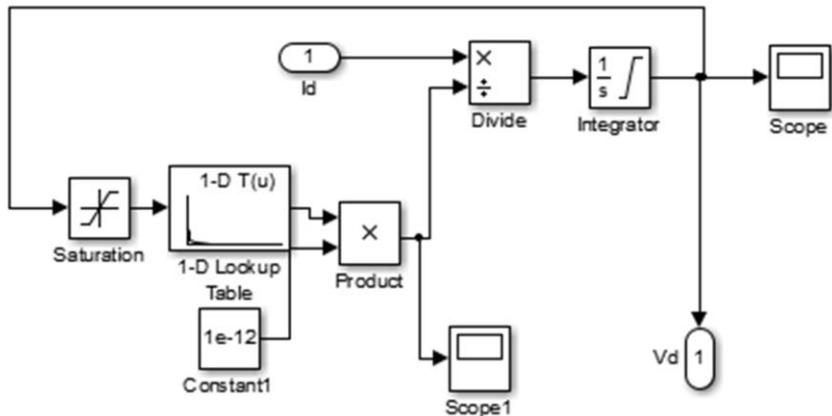


Figure 2-24 Non-linear capacitance implementation in Simulink/Matlab. Measured C-V curve can be put into the look up table.

The final model is shown in Figure 2-25.

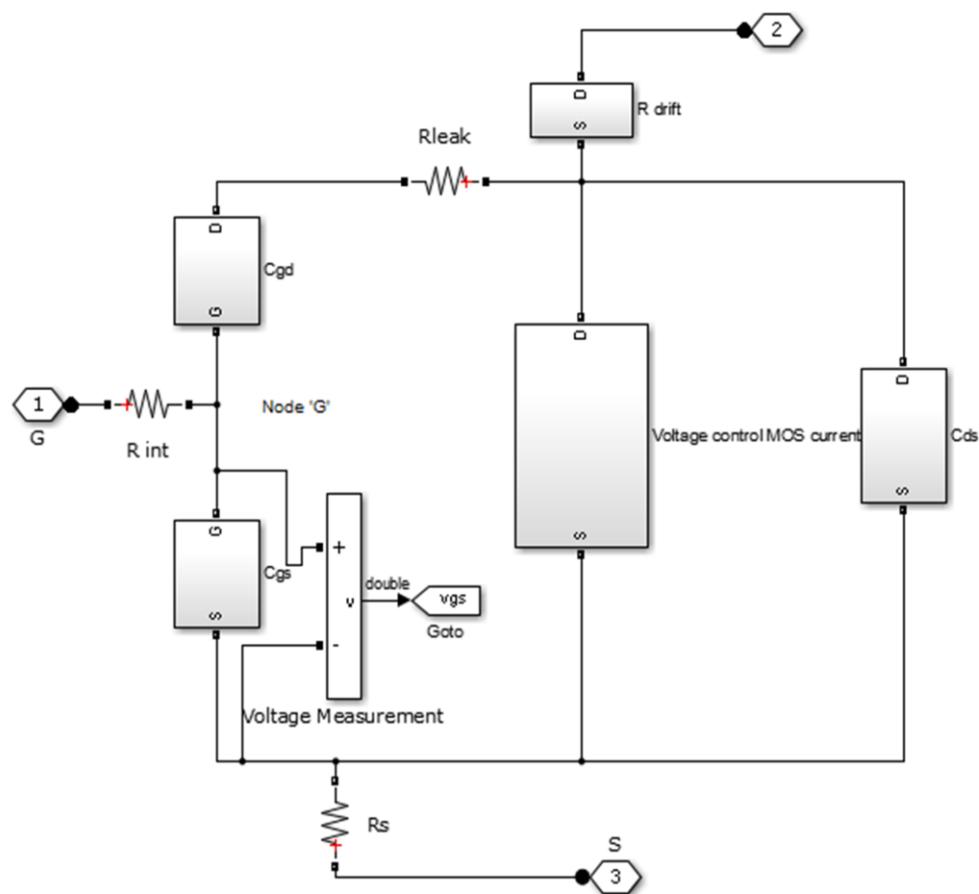


Figure 2-25 A 15kV MOSFET model in Simulink/Matlab.

Figure 2-26 shows the simulation setup of double pulse test circuit. Ode 15 is used for simulation in the Simulink/Matlab to get fast and easy-to-converge result.

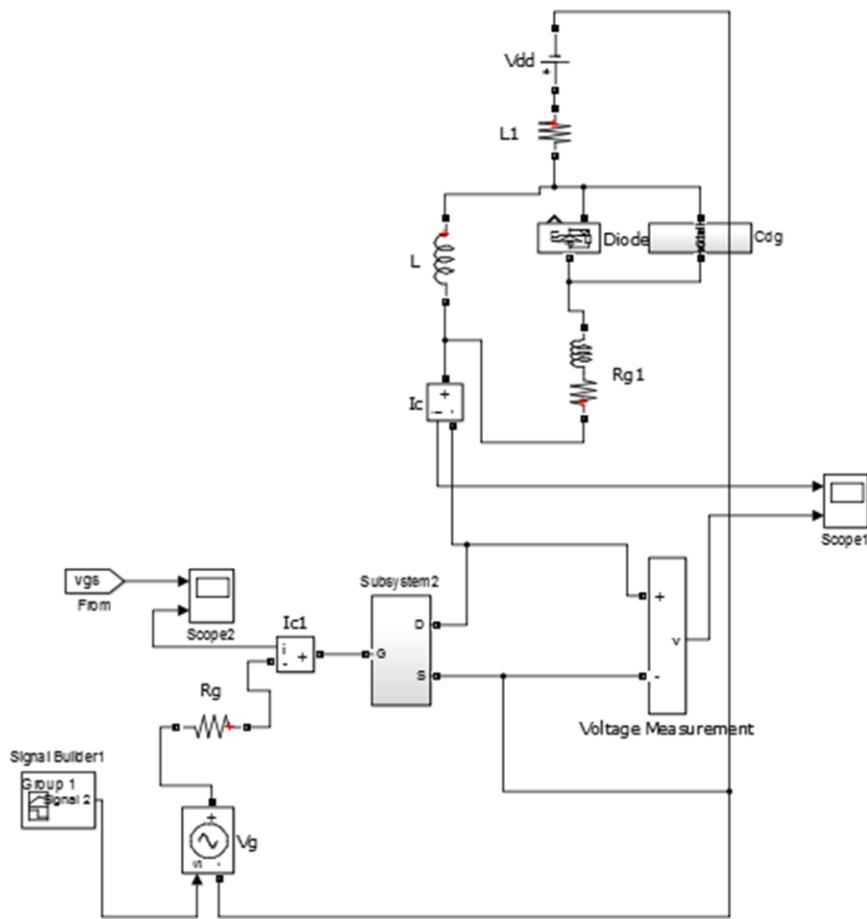


Figure 2-26 Inductive load switching of the 15kV MOSFET with a simplified Schottky diode model.

## 2.5 Model validation

The simulated results will be compared to the measurement results for inductive switching for both turn-on and turn-off. The circuit simulation will also include a simple Schottky diode model, whose parameters are extracted from a real device that is used in the measurement. Figure 2-27 and Figure 2-28 are the turn-off and turn-on result comparison, respectively.

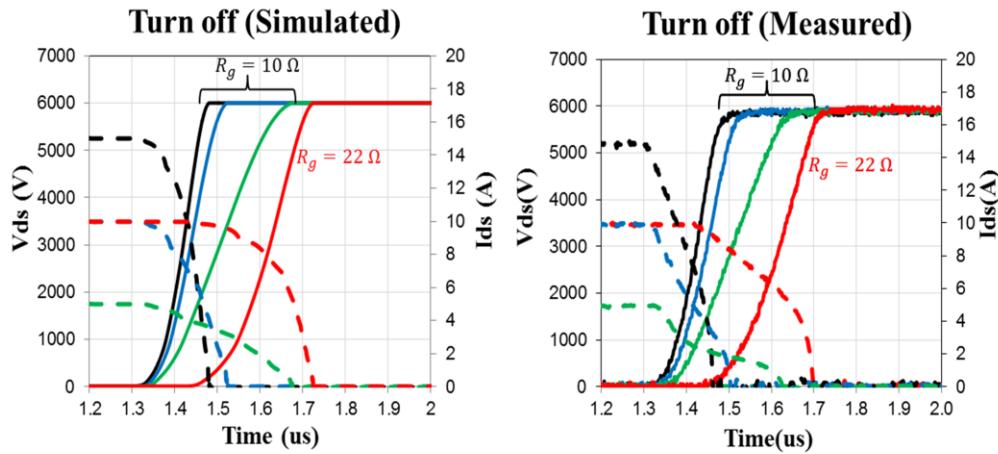


Figure 2-27 Simulated and measured turn-off waveforms of the 15kV MOSFET for different current level.

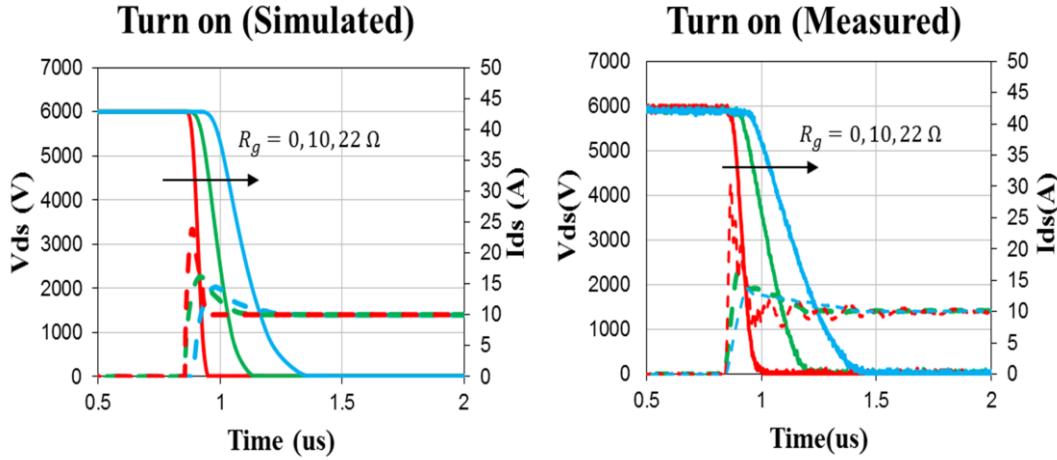


Figure 2-28 Simulated and measured turn-on waveforms of the 15kV MOSFET for different gate resistance.

The turn-on energy loss as a function of current predicted by the proposed model is shown in Figure 2-29. Most importantly, this model accounts for the loss related to energy stored in the output capacitance, as discussed in section 2.3.1. Also known as Eoss, this loss cannot be directly measured and is important to include when estimating the turn-on loss. Since the charge and discharge of the capacitance do not consume power, it is the current that flows through the resistors, such as channel resistance or partially depleted drift region during the switching transient that generate joule heat. More detail description can be found in [7, 25]

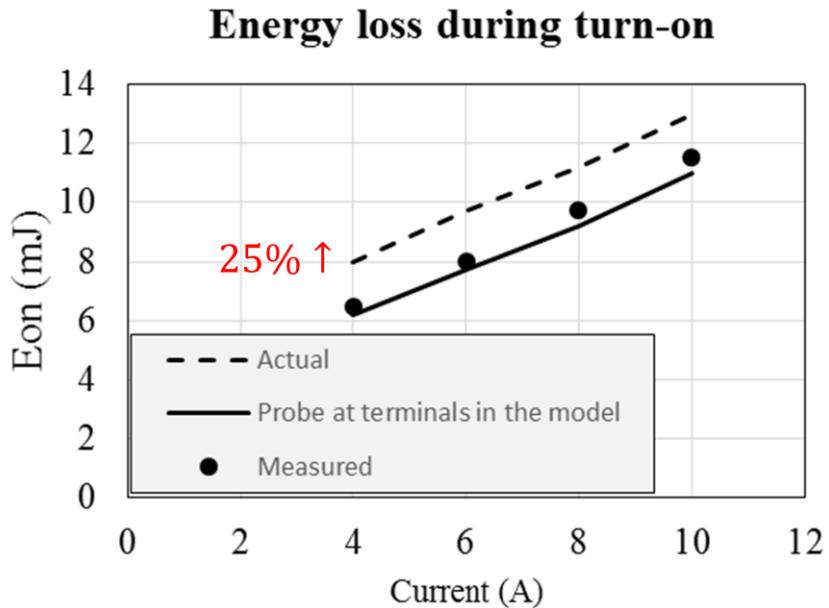


Figure 2-29 The actual turn-on loss is 25% percent higher than the measured loss. VDD= 6kV.

Figure 2-30 and Figure 2-31 show the model's prediction of the energy loss as a function of current at 25°C and 125°C, respectively. The DC bus voltage is 9kV and the gate resistance is 10 ohm. Notice that these simulated results do not include the Eoss but simply the power calculated using the terminal current and the voltage of the device.

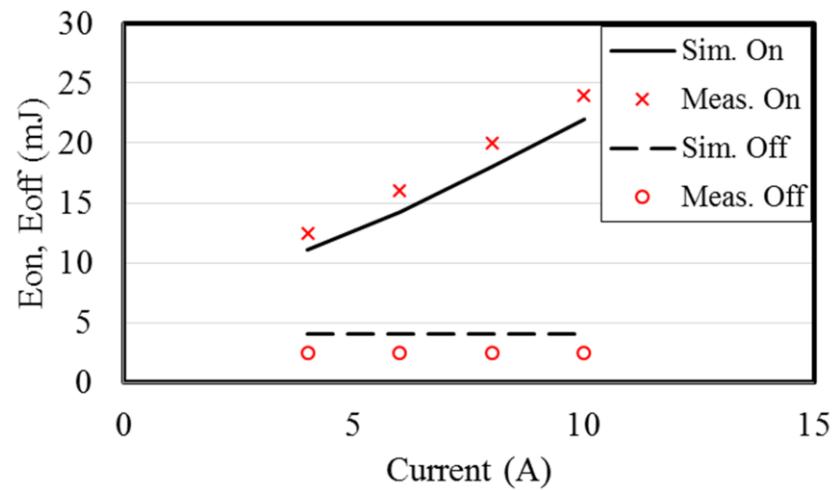


Figure 2-30 Energy loss versus current prediction at  $25^{\circ}\text{C}$ . VDD=9kV.

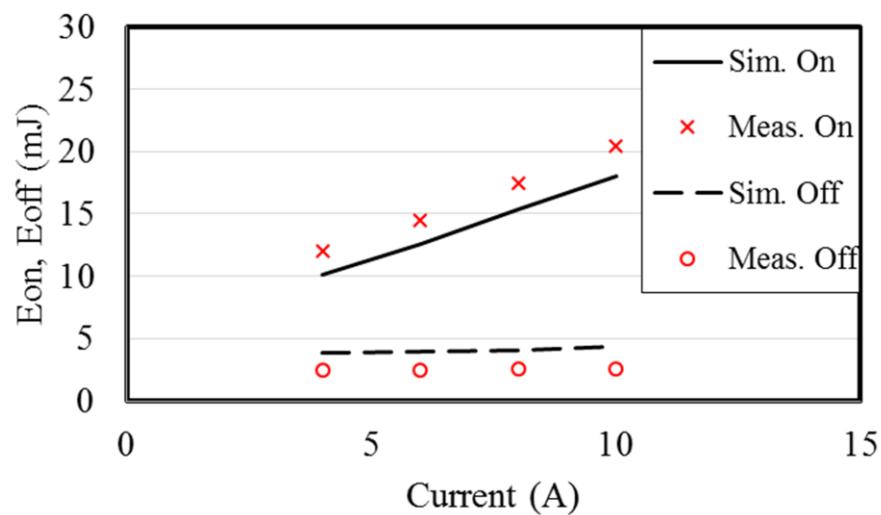


Figure 2-31 Energy loss versus current prediction at  $125^{\circ}\text{C}$ . VDD=9kV.

Figure 2-32 is the total switching loss prediction by the model, showing excellent match between the simulated and measured results.

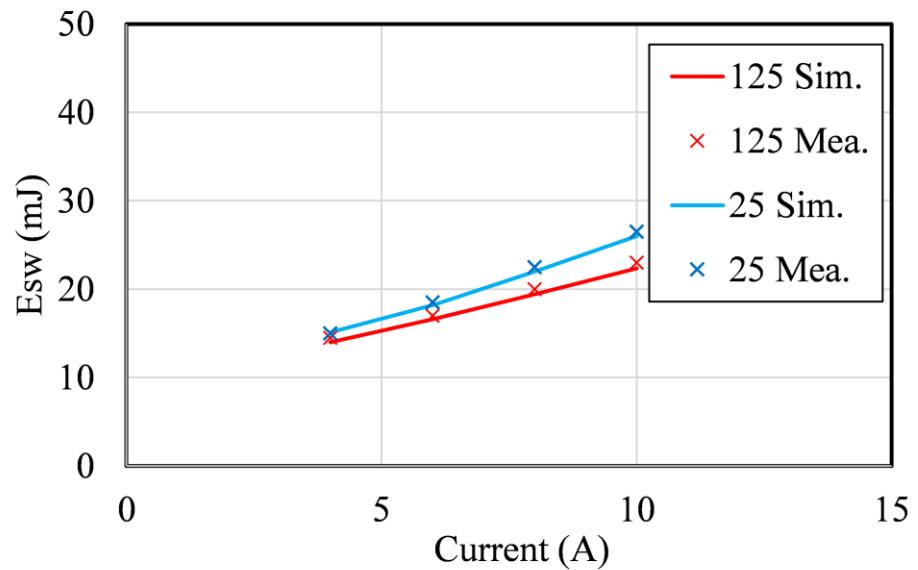


Figure 2-32 Total switching loss at 25 and 125°C. VDD=9kV.

# Chapter 3

## 20A 15kV 4H-SiC n-IGBT Modeling

### 3.1 Review of IGBT model

Due to the presence of the excess carrier, modeling ambipolar devices is more challenging than unipolar devices. In general, IGBT model can be categorized in two ways: the manner of implementing the model and handling the excess carriers in the drift region. It is summarized in Table 3.1.

Table 3.1 Ambipolar model categories

|                            |  |
|----------------------------|--|
| <b>Equivalent (E)</b>      | Utilize the KCL and KVL that are inherently built in the software by connecting the components that can reflect the real device's structure and geometry |
| <b>Mathematical (M)</b>    | Solving sets of physics-based equations in the script and return the value to corresponding ports  |
| <b>Dynamic charge (DC)</b> | <i>Target:</i> total minority charge in the lightly doped region   |
|                            | <i>Approach:</i> Solving the charge continuity equation (1 <sup>st</sup> ODE.).  |
| <b>Lumped Charge (LC)</b>  | <i>Target:</i> lumped charge deployed in the critical location of the semiconductor  |
|                            | <i>Approach:</i> Mass action law and discretized continuity equation   |
| <b>Discretized (D)</b>     | <i>Target:</i> multiple discretized lumped charge in the drift region.   |
|                            | <i>Approach:</i> finite difference method.   |
| <b>Continuous (C)</b>      | <i>Target:</i> approximation of carrier density profile  |
|                            | <i>Approach:</i> approximate solution of Fourier series to describe the dynamic carrier profile  |

### 3.1.1 Hefner's model (E.D.C)

The most classic modeling work is proposed by Hefner in [18] and later implemented in saber [26]. This work can be categorized as an E.D.C (equivalent-circuit dynamic charge) model according to the definition in Table 3.1. The equivalent circuit model is depicted in Figure 3-1.

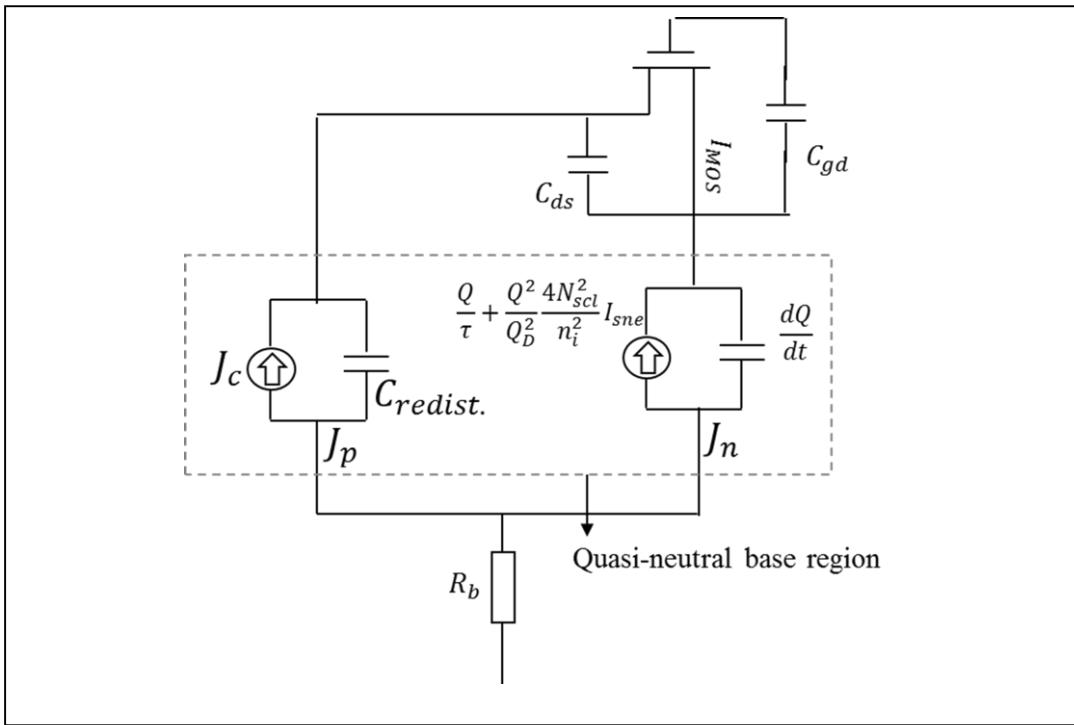


Figure 3-1 Equivalent circuit in Hefner's model.

Noted that an IGBT model will become a MOSFET model when the quasi-neutral base region in Figure 3-1 is removed. The left leg of the model is the hole current path while the right one is the electron current path. It can be seen that the amount of the current that charges the  $C_{gd}$  and  $C_{ds}$  are smaller in IGBT than in MOSFET. This is because the current that actually goes to  $C_{gd}$  and  $C_{ds}$  in IGBT is total current minus the current flow through collector current ( $J_c$ ) and redistribution current ( $C_{redist} \cdot dV/dt$ ).

The center-piece of Hefner's model is the redistribution capacitance  $C_{redist}$ , or  $C_{cer}$ . The origin of this capacitance is depicted in Figure 3-2 and the detail derivation is in [18].

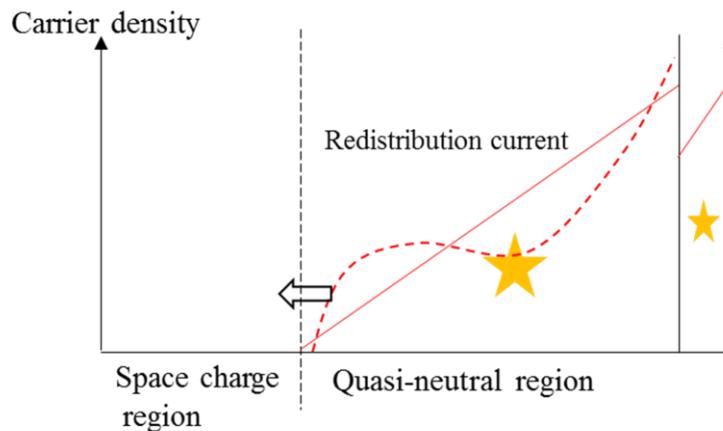


Figure 3-2 Illustration of the redistribution current induced carrier density profile.

It basically describes that when the depletion boundary pushes the excess carrier plasma, there will be a counter-force that slows down the retreating of the depletion boundary due to the presence of excess carrier plasma.

In D. C. (dynamic charge) model, there is only one big node being placed in the drift region and another in the buffer layer. The equation that governs the charge dynamic is based on charge continuity equation and Boltzmann's Junction Law. For non-punch through, the equation is given by:

$$\frac{dQ}{dt} = -\frac{Q}{\tau} - \frac{Q^2}{Q_D^2} \frac{4N_{scl}^2}{n_i^2} I_{sne} + i_d + I_{MOS} \quad (3.1)$$

Once the total charge is obtained, the carrier is assumed to be linear, as the solid line shown in Figure 3-2. This assumption is somehow valid if the depletion region is not moving, for example, during the current decaying phase; however, if the boundary is moving (pushing the excess carrier into quasi-neutral base region), according to Hefner, there will be a redistribution carrier profile component that will be superposed on this linear carrier. The redistribution carrier profile is then lead to an extra current component and can be modeled using a redistribution capacitor  $C_{redis}$ :

$$C_{redis} = C_{bcj} \frac{Q(t)}{3qN_D A(W - x_d)} \quad (3.2)$$

It is reported in [27, 28] that this capacitance might be the cause of the unrealistic ringing of the model. This capacitance is even abruptly incorporated in other model [27, 28] to account for this phenomenon.

In fact, if enough nodes were placed throughout the drift region to modeled the dynamic carriers especially near the boundary between quasi-neutral base and space charge region, this

redistribution component would not have to be included in the model. However, placing too much nodes may significantly slow down the computation speed of the model.

The KCL of this model is given by [18]:

$$I_T = \frac{1}{1+b} I_T + \frac{2D_a}{W^2} A Q(t) + C_{\text{redist}} \cdot \frac{dV}{dt} + I_{\text{MOS}} + i_{gd} + i_{ds} \quad (3.3)$$

In the latter section, the proposed model will be compared to this classic IGBT model.

### 3.1.2 Lumped charge model (E. L. C.):

One way of modeling the ambipolar devices, including PiN [29], GTO [30] and IGBT [27], is the lumped charge model. All the lumped charge models in recent years have been added the displacement current in the continuity equations in the models. The methodology is to deploy charge nodes at critical position in a device. This model type can be categorized in E. L. C in Table 3.1. For a non-punch through structure, it only takes 5 nodes – three in the drift region and two nodes at the junction in the emitter and the collector. However, only one ODE has to be solved in the drift region. Figure 3-3 depicts the carrier dynamics at low and high reverse bias during turn-off.

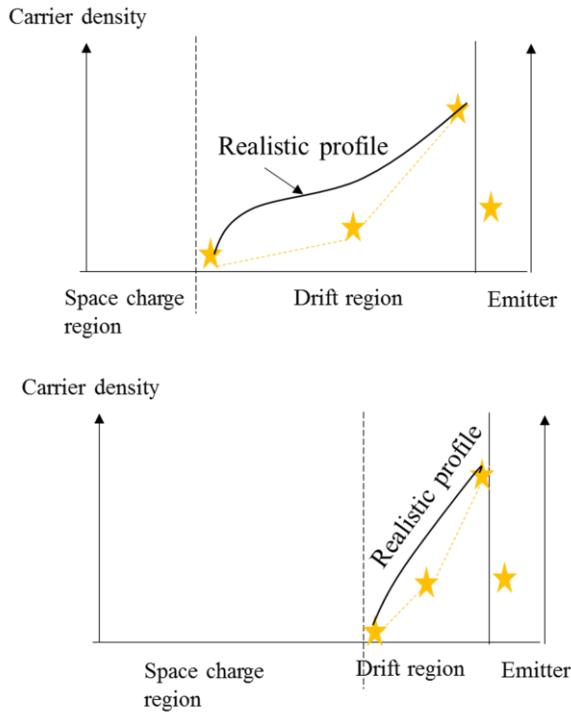


Figure 3-3 Illustration of the carrier dynamics in a lumped charge model.

From Figure 3-3, it can be observed that using three nodes along is not sufficient to model the boundary of the carrier density profile near the depletion region, especially when the quasi-

neutral base is long at low reverse bias. This will lead to erroneous calculation of the hole current entering from quasi-neutral base region to the depletions region. In this sense, devices with long drift region (high voltage) are not suitable for this modeling technique. Although using the parameter fitting techniques might lead to decent match of the switching waveform, the carrier dynamics and the physical parameters might be totally different from the real case in order to compensate the insufficiency of this model in predicting carrier dynamics.

For current high voltage 4H-SiC IGBT technology, the punch through happens around half of the DC bus voltage [31]. In addition, the buffer layer in the structure not only serves as a field stop layer but also a valve to adjust the carrier injection. This means that in order to model the high voltage 4H-SiC IGBT, it requires at least 8 nodes deployed in the structure – three in the drift, three in the buffer (has to be so in order to model recombination in the buffer) and two in the emitter and the collector. Moreover, the carrier dynamic during the transition right before and after punch through can be complicated to handle.

### *3.1.3 Fourier-series-based model:*

The techniques of this model is to use the Fourier-series as a solution of PDE that describe the carrier density profile. The boundary conditions of the profile are from the currents that enter/leave the quasi-neutral base region. This method is first proposed in [32]. In 2007, an IGBT model has been developed using this techniques [22]. This model is depicted in Figure 3-4, and it can be categorized as a M. C. (mathematical continuous) model.

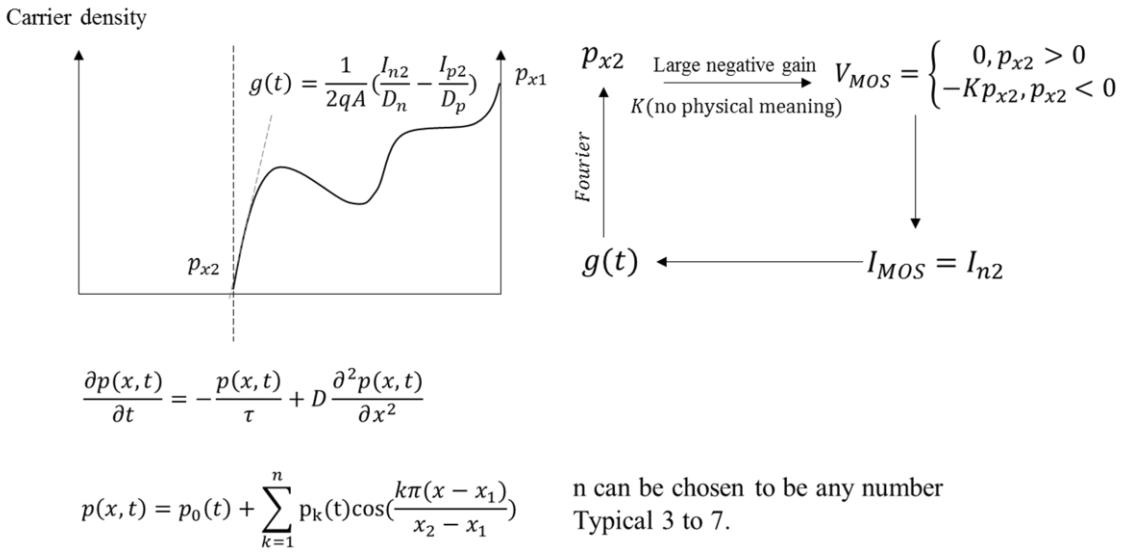


Figure 3-4 The Fourier-series-based solution for carrier density profile and its algorithm.

Notice that this model also emulates the contraction of the carrier profile during turn-off near the drift region. This is a similar feature captured in Hefner's model, in which he uses the "redistribution current" or the redistribution capacitance (Ccer) [18] to achieve this feature. Since Fourier-series-based model already capable of predicting the sharp bend of the carrier density profile near the depletion region using Fourier-series, and therefore, do not require any imaginary component like redistribution current to describe this transition region.

The mathematical nature of this techniques, however, may limit the implementation of the model into software such as PSPICE. In addition, mathematical models are proprietary to the developers and can be complicated to develop, especially for engineer with circuit background, mainly because equivalent circuit model is more systematically connected by utilizing the KCL and KVL that is inherently embedded in most of the software such as Simulink, PSPICE and Saber. Moreover, few mathematical tricks and techniques have to be done to avoid the

convergence issues [22]. In determining the depletion region, a large negative feedback loop that has no physical meaning, as shown in Figure 3-4, is used to constantly keep the boundary carrier density near the depletion region ( $p_{x2}$ ) to be zero while the depletion voltage is generated. While other models need the depletion width and voltage first to calculate the new carrier profile for each time step, this model backwardly calculate the carrier profile first and then use the trick mentioned above to obtain the voltage across the depletion region.

Based on the discussion above, equivalent-circuit model seems to be preferable to the mathematical model. This means the Fourier-series-based model is opted out toward developing a high-voltage SiC MOSFET model.

## 3.2 IGBT theory and principle

Figure 3-5 and Figure 3-6 summarize the preliminary theories in the quasi-neutral base region that will be used in the on-state modeling of IGBTs.

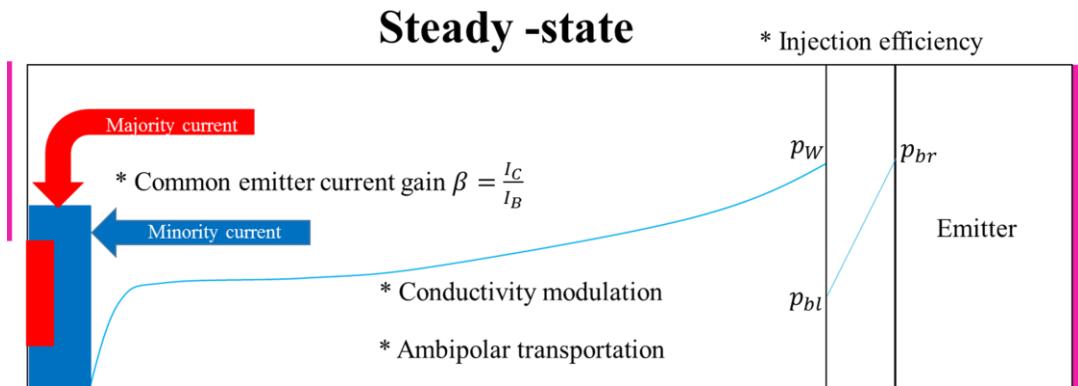


Figure 3-5 Device physics during on-state that will be discussed in the section.

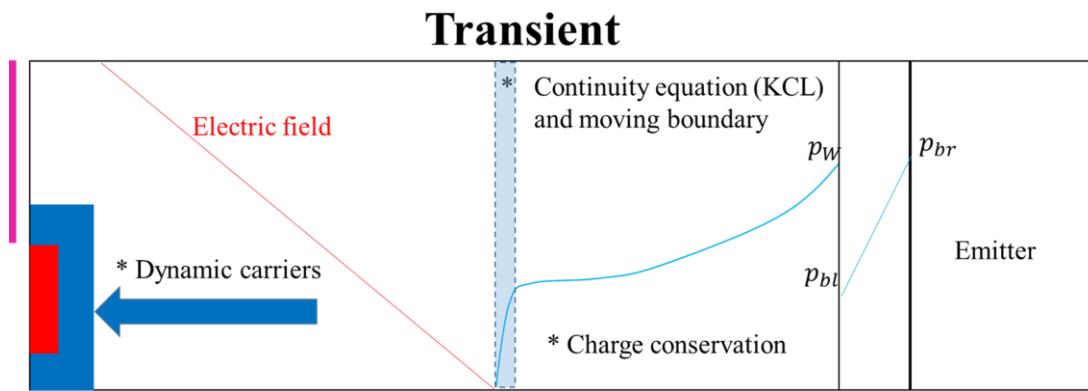


Figure 3-6 Device physics during switching transient that will be discussed in the section.

### 3.2.1 Ambipolar diffusion equation at arbitrary injection level

Ambipolar transportation is used to describe the electron and hole current in the presence of each other. The derivation of the expression of the current under the high-level injection can be found in [11]. Here the ADE under more general cases are provided under arbitrary injection level.

For n channel device:

$$J_n = \frac{b(1+\lambda)}{1+b(1+\lambda)} J_T - q \frac{2+\lambda}{2} \frac{1+b}{1+b(1+\lambda)} D_a \frac{\partial p(x)}{\partial x} \quad (3.4)$$

$$J_p = \frac{1}{1+b(1+\lambda)} J_T + q \frac{2+\lambda}{2} \frac{1+b}{1+b(1+\lambda)} D_a \frac{\partial p(x)}{\partial x} \quad (3.5)$$

For p channel device:

$$J_n = \frac{b}{1+b+\lambda} J_T - q \frac{2+\lambda}{2} \frac{1+b}{1+b+\lambda} D_a \frac{\partial n(x)}{\partial x} \quad (3.6)$$

$$J_p = \frac{1}{1+b+\lambda} J_T + q \frac{2+\lambda}{2} \frac{1+b}{1+b+\lambda} D_a \frac{\partial n(x)}{\partial x} \quad (3.7)$$

$$\lambda(x) = \frac{\text{back ground doping}}{\text{local minority carrier}(x)} \quad (3.8)$$

Eq. (3.4) -Eq. (3.7) will reduce to high-level injection case when  $\lambda$  is much smaller than unity.

### 3.2. 2 Analytical expression of on-state voltage drop along the drift region

The long drift region in high voltage SiC IGBT lightly doped. During on-state, the conductivity modulation will help lowering the voltage drop across the drift region. The carrier density distribution can be approximated as:

$$p(y) = K_1 \exp\left(\frac{y}{L}\right) + K_2 \exp\left(-\frac{y}{L}\right) \quad (3.9)$$

Where

$$K_1 = \frac{P_W - P_0 \exp\left(-\frac{W}{L}\right)}{\exp\left(\frac{W}{L}\right) - \exp\left(-\frac{W}{L}\right)} \quad (3.10)$$

$$K_2 = \frac{P_0 \exp\left(\frac{W}{L}\right) - P_W}{\exp\left(\frac{W}{L}\right) - \exp\left(-\frac{W}{L}\right)} \quad (3.11)$$

$P_W$  and  $P_0$  are the carrier densities at the drift region/buffer layer boundary and at the accumulation layer near MOSFET, respectively.

The voltage drop across the drift region is given by [11]:

$$V_{\text{drift}} \cong \frac{I_T}{qA(\mu_n + \mu_p)} \int_0^W \frac{1}{K_1 \exp\left(\frac{y}{L}\right) + K_2 \exp\left(-\frac{y}{L}\right)} \quad (3.12)$$

An analytical expression can be found as:

$$V_{\text{drift}} = \frac{I_T L}{qA(\mu_n + \mu_p)\sqrt{K_1 K_2}} \left[ \tan^{-1} \left( \sqrt{\frac{K_1}{K_2}} \exp \left( \frac{W}{L} \right) \right) - \tan^{-1} \left( \sqrt{\frac{K_1}{K_2}} \right) \right] \quad (3.13)$$

### 3.2.3 Injection efficiency as a function of total current density

This section will introduce the explicit relationship among terminal current, injection efficiency, the boundary carrier density  $p_W$ , which can be used to estimate the total excess charge in the drift region during on-state. We will then show that injection efficiency can be extracted by examining the amplitude of the sudden current drop during the short-circuit turn-off. Injection efficiency is a measure of how efficient the minority carrier current injects into the drift region to modulate the resistance of the drift region. It is defined as:

$$\gamma_E = \frac{J_{\min} \cdot (x = W_D)}{J_T} \quad (3.14)$$

The analytical expression using parameters in the emitter and the drift region is given in [4]. However, it is pointed out [3] that the injection efficiency is not intuitive to indicate the excess carrier being stored in the drift region. In fact, compared to its p-type counterpart, n-IGBT has much smaller injection efficiency but higher excess carrier stored in the drift region. A new indicator called injection capacity is defined in [3] and is equal to the injection efficiency at certain current density minus the theoretical minimum value of the injection

efficiency. The total excess charge is calculated by integrating the carrier density profile along the drift region:

### N-IGBT

$$Q_h = (\gamma_{En} - \gamma_{En,min}) J_T \tau_H \left( 1 - \frac{1}{\cosh(\frac{W}{L})} \right) \quad (3.15)$$

where

$$\gamma_{En,min} = \frac{1}{1+b} \quad (3.16)$$

### P-IGBT

$$Q_e = (\gamma_{Ep} - \gamma_{Ep,min}) J_T \tau_H \left( 1 - \frac{1}{\cosh(\frac{W}{L})} \right) \quad (3.17)$$

where

$$\gamma_{Ep,min} = \frac{b}{1+b} \quad (3.18)$$

The expression of injection efficiency as a function of total current density is given in [11]. It can be extracted by performing the short circuit turn-off at different current densities [3] shown in Figure 3-7 and is given by:

$$\frac{I_T^+}{I_T^-} = \frac{\gamma_E \left(1 + \frac{1}{b}\right) - \frac{1}{b}}{\cosh(W/L)} \quad (3.19)$$

For n-type IGBT and

$$\frac{I_T^+}{I_T^-} = \frac{\gamma_E (1 + b) - b}{\cosh(W/L)} \quad (3.20)$$

For p-type IGBT.

$I_T^+$  and  $I_T^-$  are defined in Note that it is recommended to perform the extraction at relatively high voltage or the  $J_T^+$  will be very small due to the large denominator in Eq. (3.19) and Eq. (3.20). The validation is detailed in [3] using 10kV n- and p-IGBT in TCAD.

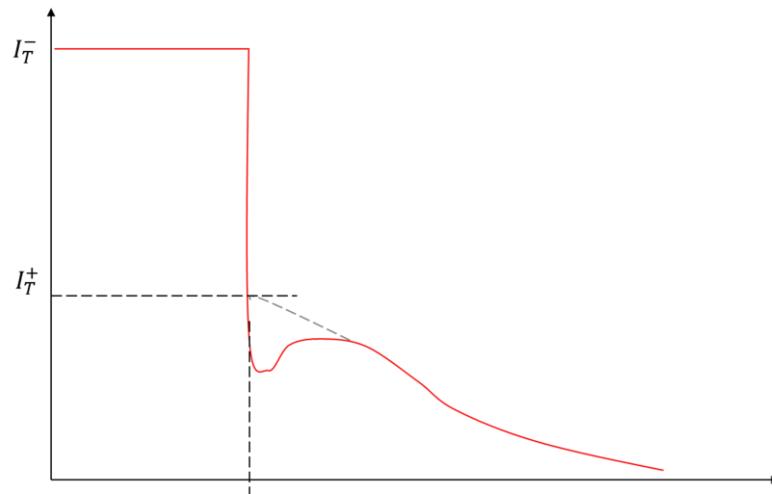


Figure 3-7 Illustration of the sudden current drop after the IGBT gate turnoff.

### *3.2.4 Common emitter current gain $\beta$*

The common emitter current gain will not be explicitly calculated in the model. Nevertheless, it is of interest to discuss the value in SiC IGBT. The  $\beta$  in IGBT is approximately the ratio between the majority and minority mobility. In 4H-SiC n-IGBT, the current that goes into channel is about 8 times larger than the bipolar collector current that goes into the p-well. In contrast, the ratio between channel current and collector current in 4H-SiC p-IGBT is 1/8. In general, this will make n-channel device switches faster than p-channel devices. This conclusion also applies to Thyristors. It is worth pointing out that, although around 88% of the total current is majority current in n-IGBT, the conductivity modulation in n-IGBT is still stronger than p-IGBT, as discussed in last sub-section.

### *3.2.5 Dynamic carrier density in the depletion region*

The dynamic carriers in the depletion results from the carriers that entered space charge region and being swept by the electric field throughout the space charge region. For n-channel MOSFET, the dynamic carrier type is electrons. For n-channel IGBT, the dynamic carrier type is holes. The dynamic carriers in n-IGBT will result in an effective ionized charge that is greater than the original value  $N_D^+$ . Not only the capacitance calculated using Poisson equations will be changed, but also the punch-through voltage will be larger than the value calculated by the background doping. For 15kV 4H-SiC, the background doping is typically  $2e14 \text{ cm}^{-3}$ .

For high voltage ambipolar devices with this lightly doped drift region, it is important to accurately estimate the dynamic carriers in the space charge region that can be significant

compared to the background ionized charge. A conventional way of estimating the dynamic carrier density is given by:

$$N_{\text{dyn}}(x) \approx \frac{J_T}{qV_{\text{sat},p}} \quad (3.21)$$

However, this will lead to the underestimation of the ionized charge in the space charge region, as shown in Figure 3-8. The reason is that the electric field is a triangle shape, and the assumption that all the current is drift carriers traveling at a constant saturation velocity in high electric field is erroneous.

In [16], it also shows that the punch through voltage ( $V_{\text{pt}}$ ) is around 5000 Volts, which results from an effective back ground doping of  $2.8\text{E}14 \text{ cm}^{-3}$ . Both experiment results and simulation suggest that the effective dynamic carriers will be underestimated if using the conventional estimation.

The blue line is the effective space charge density deduced from the punch-through voltage, which is about 4816 Volts at the current density of  $62.5 \text{ A/cm}^2$  (20A for  $0.32\text{cm}^2$  device). This gives a better approximation than the conventional estimation in Eq. 3.22:

$$N_{\text{sc,eff}} = \frac{2\varepsilon_{\text{SiC}} V_{\text{pt}}(I)}{qW_D^2} \quad (3.22)$$

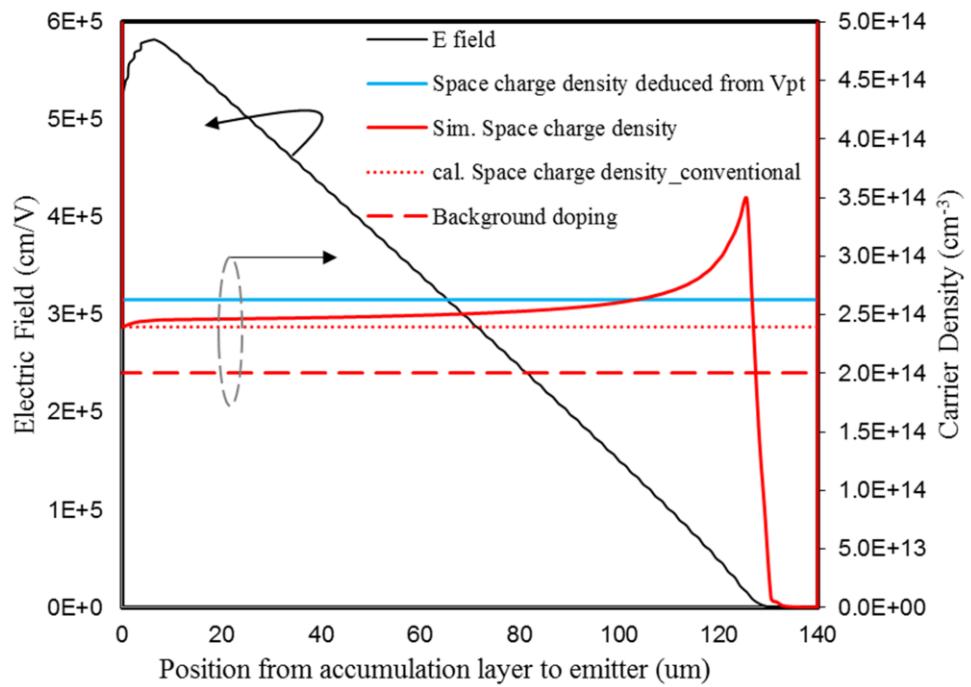


Figure 3-8 Hole carrier densities before punch-through during turn-off.

### 3.2.6 Diffusion capacitance/redistribution capacitance/charge removal capacitance

These three capacitances are fundamentally the same for describing the effect of excess carrier during the switching. It converts the change rate of the excess carrier to the change rate of the depletion boundary, which corresponds to  $dv/dt$ . In this manner, the presence of the excess carrier can be modeled as a capacitance. It can be seen as a diffusion capacitance because it describes the change rate of the charge [33]. In [18], the effect of the local excess carrier during the moving of depletion boundary is described as a redistribution action.

In this work, we will model the dynamic of the local excess carrier as described in [34]. The depiction of the charge removal capacitance is shown in Figure 3-10. The amount of charge in slice that is being removed by the difference of the hole current flux.

$$Q(x_d) = p(x_d)\Delta x \quad (3.23)$$

And the change rate of this local excess charge can be related to the  $dv/dt$  as depicted in Figure 3-10. This charge removal action can then be modeled as a capacitance and is given by:

$$C_q = \frac{p(x_d)}{N_D} C_{oss} \quad (3.24)$$

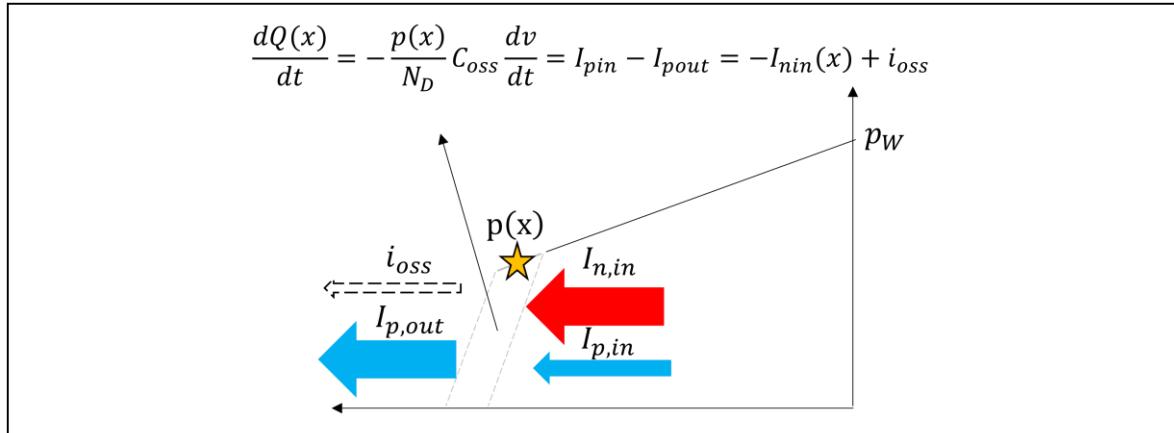


Figure 3-9 The slice of charge marked by the dashed line and the expression of its change rate.

It is important to point out that, although modeled as a capacitance, the current that is coming in and out of this capacitance is actually hole current, not displacement current like  $C_{gd}$  or  $C_{ds}$ .

### 3.3 The proposed IGBT charge-carrier model

Figure 3-10 provides a visual preview of the steps during the model is in action.

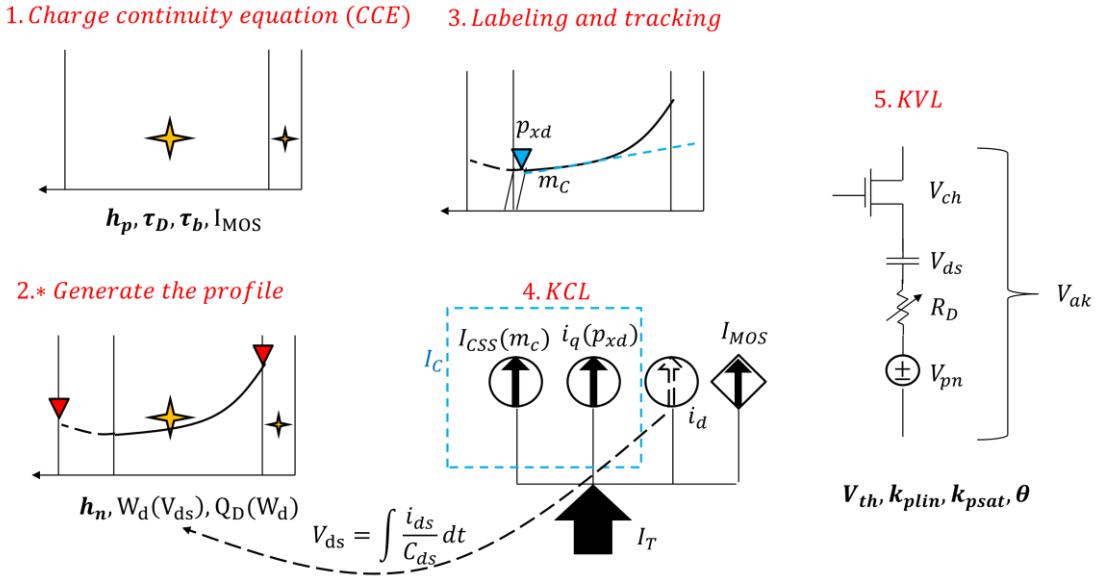


Figure 3-10 Figurative steps of the proposed IGBT model.

These five steps are discussed as follows.

#### 3.3.1 Charge continuity equation (CCE)

The excess carrier in IGBT as a function of time can be calculated in real time using CCE.

The relationship between the excess carrier in the drift region and buffer layer can be described

using Boltzmann Junction's Law. The change rate in the drift region and buffer layer can be solved by the following two equations.

$$\frac{dQ_T}{dt} = -\frac{Q_D}{\tau_D} - \frac{(Q_T - Q_D)}{\tau_B} - h_p(Q_T - Q_D) \frac{Q_H}{d^2} + I_{MOS} + i_{dg} + i_{ds} \quad (3.25)$$

$$Q_T = Q_D + \frac{Q_D^2}{Q_H} \left( \frac{d}{L\alpha} \right)^2 + \frac{d^2}{2D_{pb}} \frac{I_T}{1+b} \quad (3.26)$$

, where

$$\alpha = \frac{\cosh\left(\frac{W}{L}\right) - \cosh\left(\frac{W-x_d}{L}\right)}{\sinh(W/L)} \quad (3.27)$$

Eq. (3.25) is the CCE that has two unknowns: QD and QT (=QD+QB). QH is the background charge of the buffer layer and is equal to the product of NH and d (buffer layer thickness). Eq. (3.26) is the relationship between QT and QD based on Boltzmann junction's law, and the second term of Eq. (3.26) is QB.

Noted that at this point we still do not know where the depletion region boundary is. The parameter  $h_p$  and  $\tau_B$  together determine the total lumped charge in the drift region as well as in the buffer layer.

### 3.3.2 Generate the carrier density profile

After the total charge is calculated, the next step is to use the information of total charge, position of the depletion boundary, and the boundary condition of the carrier profile to generate the carrier density profile. The parameter  $h_n$  determines the imaginary carrier density at the MOS accumulation layer ( $p_0$ ).

$$p_0 \approx \sqrt{\frac{b}{1+b} I_T}{q h_n} \quad (3.28)$$

The dashed line in the depletion region in Figure 3-10 means that all the total charge is within the quasi-neutral base region. The function of this  $p_0$  is to merely generate this abrupt carrier density profile with all left excess carrier profile remained unchanged, as shown in Figure 3-11 during inductive switching.

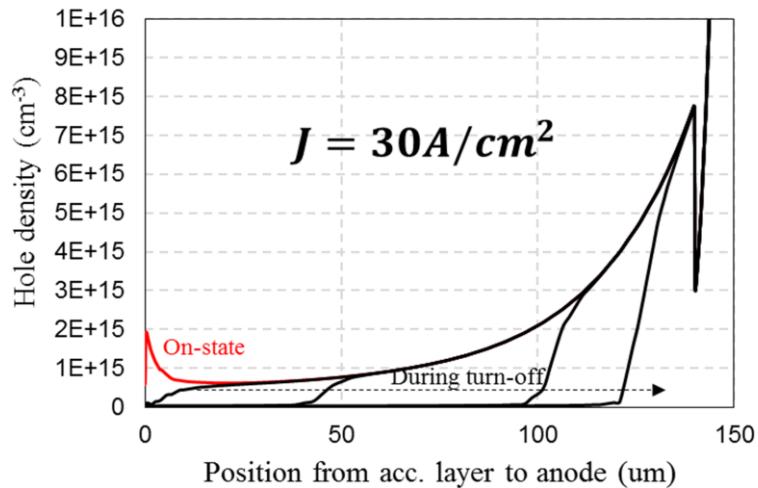


Figure 3-11 Simulated snapshots of carrier density distribution during the inductive turn-off of 4H-SiC IGBT.

### 3.3.3 Tracking the local carrier information

It is now the boundary properties that is of interest. The value on the tip of the excess carrier profile boundary that is labeled as  $p_{xd}$ , and the value of its first derivation ( $m_c$ ), as shown in Figure 3-10. The position of the depletion boundary is used to track these two values at every moment of the simulation.

$$p(x_d) = K_1 \exp\left(\frac{x_d}{L}\right) + K_2 \exp\left(-\frac{x_d}{L}\right) \quad (3.29)$$

Where

$$K_1 = \frac{P_W - P_0 \exp\left(-\frac{W_D}{L}\right)}{\exp\left(\frac{W_D}{L}\right) - \exp\left(-\frac{W_D}{L}\right)} \quad (3.30)$$

$$K_2 = \frac{P_0 \exp\left(\frac{W_D}{L}\right) - P_W}{\exp\left(\frac{W_D}{L}\right) - \exp\left(-\frac{W_D}{L}\right)} \quad (3.31)$$

and

$$P_W = \frac{Q_D \left[ \exp\left(\frac{W_D}{L}\right) - \exp\left(-\frac{W_D}{L}\right) \right]}{qAL \left[ \exp\left(\frac{W_D}{L}\right) + \exp\left(-\frac{W_D}{L}\right) - 2 \right]} \quad (3.32)$$

$$- P_0 \frac{\left[ \exp\left(\frac{W_D}{L}\right) + \exp\left(-\frac{W_D}{L}\right) - 2 \right]}{\left[ \exp\left(\frac{W_D}{L}\right) + \exp\left(-\frac{W_D}{L}\right) - 2 \right]}$$

The slope  $m_c$  can easily be found using Eq. (3.29). These two information will be used to calculate the total collector current ( $I_C$ ) that flow into the depletion region and collected by the p-base. The first component of the collector current  $I_C$  is related to  $p_{xd}$  and is known as the

charge removal current ( $i_q$ ). It is responsible for removing the excess holes at the boundary of the body of excess carriers when the depletion region is moving. It is similar to Hefner's redistribution current [18]. The second component is steady-state collector current  $I_{css}$ , and it accounts for the hole current drifting and diffusing from the quasi-neutral base region into the depletion region. The expression of these two collector current component will be derived in the next subsection.

### 3.3.4 KCL

KCL is the most important element of a model, for it serves as a guide of how the sub-circuit is being connected. The KCL can be found by writing the continuity equation around the slice of the body of excess carrier, as shown in Figure 3-9. This derivation is an extension of the work in [34] by including the displacement current.

The continuity equation of the hole states that:

$$\frac{dQ_p(x)}{dt} \cong I_{p,in} - I_{p,out} \quad (3.33)$$

Where the  $Q_p(x)$  is the slice depicted in Figure 3-9.

$I_{p,out}$  is equal to  $I_T - i_{oss}$  during turn-off after the MOS current is cut-off. In general,  $I_{p,out}$  is equal to  $I_T - i_{oss} - I_{MOS}$ . The recombination is ignored since the difference of the flux of coming and leaving is much stronger than the recombination in this transition region. By

rewriting (9) with the approximation of the change rate of the slice  $Q_p(x)$  equals to  $q \times p_{xd} \times$

$\frac{dx}{dt}$  [34], the total current flowing out of the quasi-neutral base region is then given by:

$$I_T = i_C + i_d + I_{MOS} \quad (3.34)$$

Where  $i_C = I_{CSS} + i_q$  and  $i_d = i_{gd} + i_{ds}$ , with

$$I_{CSS} = \frac{1}{1+b} I_T + q D_a m_c \quad (3.35)$$

And

$$i_q = \frac{p_{xd}}{N_D} \times i_d \quad (3.36)$$

The equivalent circuit can now be constructed based on Eq. (3.34), (3.35) and (3.36), as shown in Figure 3-12. The block on the right leg of the model contains CCE inside to calculate the charge using the base current,  $I_b$ , including MOS current and displacement current. This block will be further explained in the latter section.

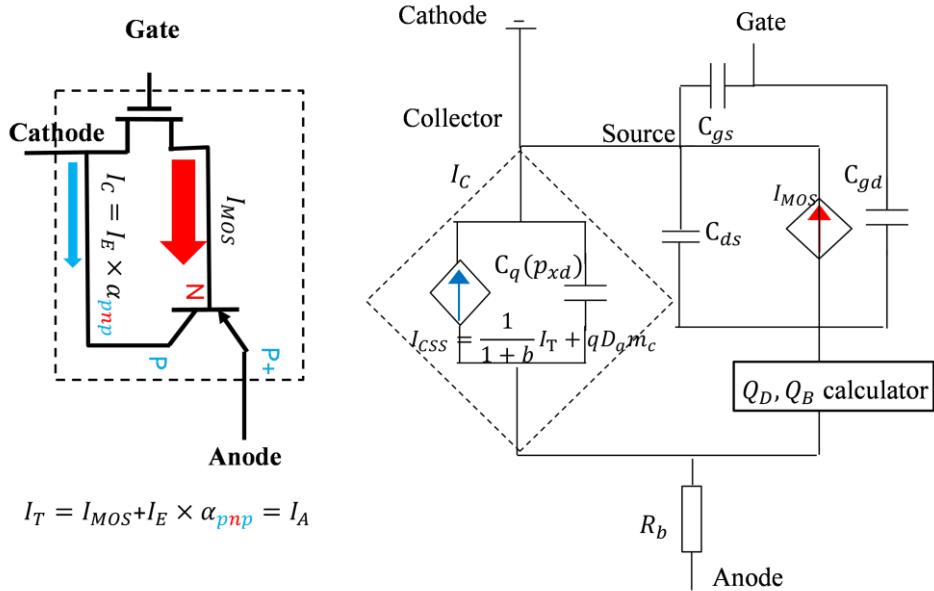


Figure 3-12 The simplified equivalent circuit (left) and the proposed equivalent circuit (right) based on derived KCL.

From the above derivation, one can see that the charge removal current  $i_q$  can be related to the displacement current  $i_d$  and modeled as a capacitor with the value of  $\frac{p_{xd}}{N_D} C_{oss}$ . It is worth pointing out that under two circumstances the charge removal current is zero: (i) during steady-state and (ii) during the current decaying phase. During the current decaying phase, the depletion boundary is not moving and, as a result, no displacement current as well as the charge removal current  $i_q$  according to Eq. (3.36). After the mathematical derivation, it is of interest to take a closer look at the physics of these components, as shown in Figure 3-13.

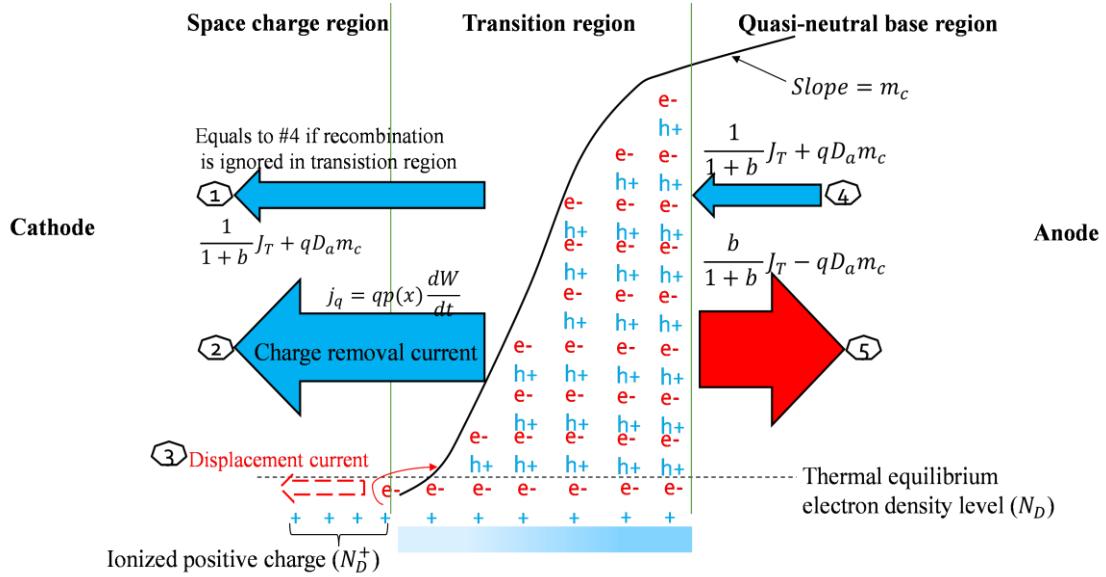


Figure 3-13 Detailed illustration of the current components going in and coming out of the transition region.

There are 3 components that enters the depletion region during the turn-off process and that is: steady-state collector current  $I_C$ , the charge removal current at the boundary  $i_q$ , and finally the displacement current whose origin is the sweeping of majority carriers (electron) and leaving the positive ionized charge behind to block the voltage. Noted that this work does not require the information of the slope in the highly non-linear transition region that is needed in other carrier-based modeling works [22, 35]. By utilizing the continuity equation, this model, although its carrier-profile-based, circumvents the highly non-linear transition region.

### 3.3.5 KVL

The total voltage drop is to sum up all the components in series from anode to cathode. Since this model calculates the carrier density profile, the voltage drop across the drift region has an explicit expression can is given by:

$$V_{\text{drift}} = \frac{I_T L}{qA(\mu_n + \mu_p)\sqrt{K_1 K_2}} \left[ \tan^{-1} \left( \sqrt{\frac{K_1}{K_2}} \exp \left( \frac{W}{L} \right) \right) - \tan^{-1} \left( \sqrt{\frac{K_1}{K_2}} \right) \right] \quad (3.37)$$

Where  $K_1$  and  $K_2$  are given in Eq. (3.30) and (3.31).

### 3.4 IGBT model implementation in Simulink/Saber

This work is an equivalent circuit model in a lumped-charge manner while keeping the information of carrier profile deducing from the total charge at given boundary conditions. The advantage of the model is as the followings: (i) the model is capacitance-based, including charge-removal capacitance that accounts for the minority carriers in the drift region, (ii) this model consider injection from both anode and the accumulation layer, (iii) this model takes the information of carrier density profile into account for both on-state and switching.

#### 3.4.1 Connect the components using the derived KCL

The proposed model constructed based on KCL and implemented in Simulink/Matlab is shown in Figure 3-14.

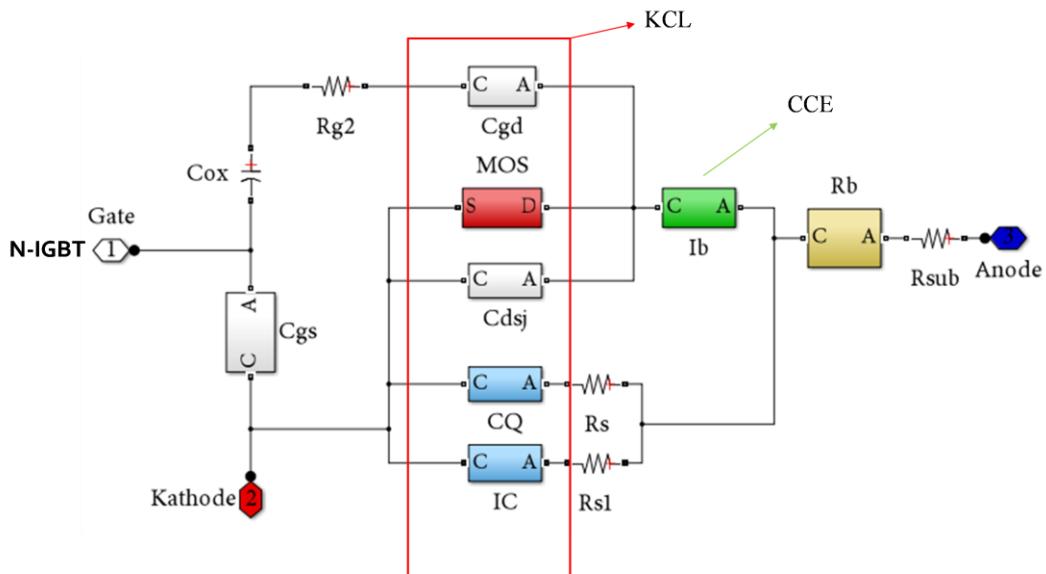


Figure 3-14 Proposed IGBT model implemented in Simulink/Matlab.

### 3.4.2 CCE

The excess charge in the drift region and buffer layer are calculated in the CCE box shown in Figure 3-14. Figure 3-15 shows the inside of the CCE block.

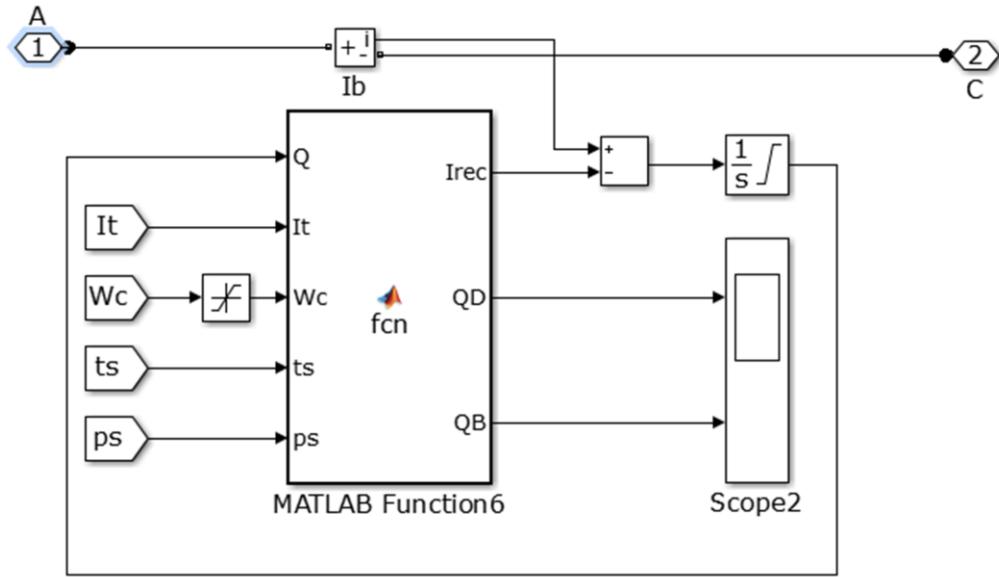


Figure 3-15 Charge continuity equation block in Simulink/Matlab for dynamic charge calculation.

This block will detect the base current ,including  $I_{MOS}$ ,  $i_{ds}$  and  $i_{gd}$ , and calculate the charge by the following equation based on Eq. (3.25):

$$Q_T = \int i_b - i_{rec} \quad (3.38)$$

Where

$$i_{rec} = -\frac{Q_D}{\tau_D} - \frac{Q_B}{\tau_B'} \quad (3.39)$$

Noted that  $\tau_B'$  is given in Eq. (3.39) includes the recombination in the buffer layer and the back injection into the emitter [18].

### 3.4.3 The Voltage-dependent capacitances

In Simulink/Matlab, the user can use the lookup table to directly create a C-V curve to model a capacitor, as shown in Figure 3-16. The capacitor is modeled as a current-controlled voltage source.

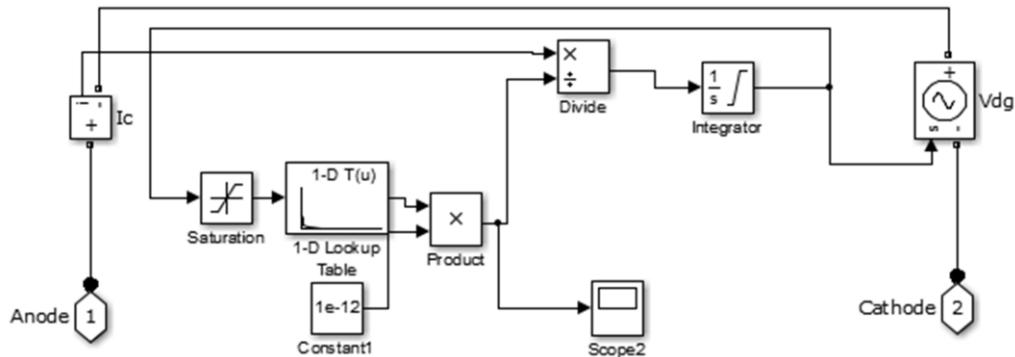


Figure 3-16 The implementaion of non-linear capacitance in Simulink/Matlab.

### 3.4.4 The drift region resistance

The voltage drop of the drift region can be calculated using Eq. (3.37). It is modeled as a current-controlled voltage source, as shown in Figure 3-17.

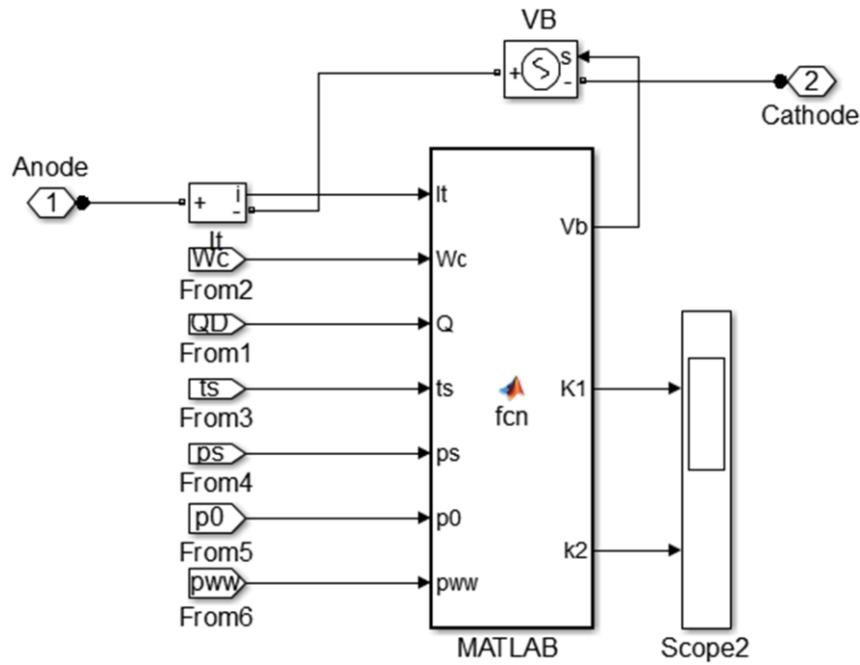


Figure 3-17 The drift region voltage drop calculator in Simulink/Matlab.

## 3.5 Parameter extraction procedure

A systematic way of parameter extraction is proposed in this work for the model. All the parameters will be extracted at temperature 25, 75 and 125 °C, and the temperatures within the range will be interpolated. It takes only 2 experiments setups, including I-V measurement and inductive switching, and 5 steps of calculation for each temperature. There are 16 parameters in total that need to be extracted for the proposed model.

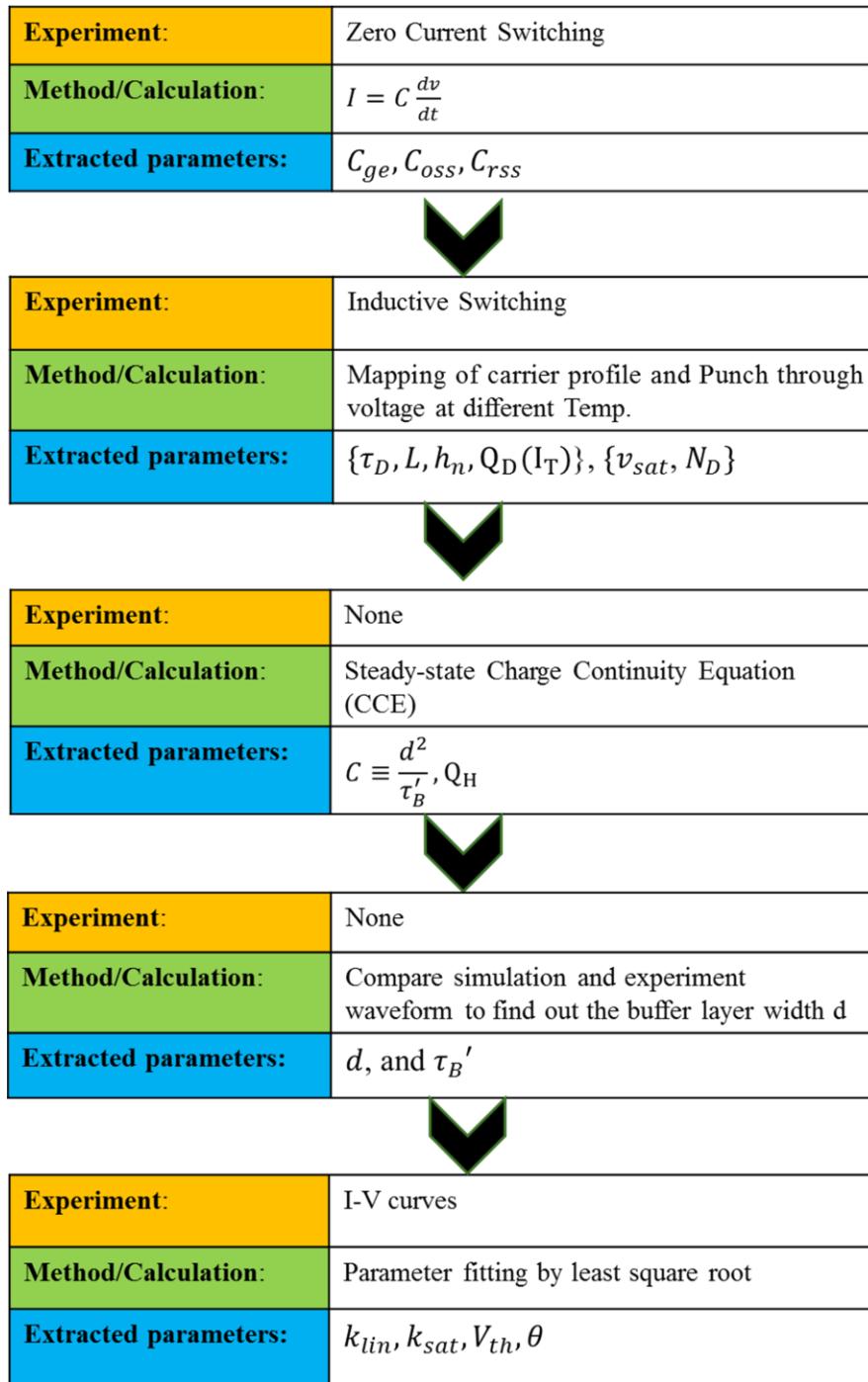


Figure 3-18 Proposed parameter extraction procedure for 4H-SiC IGBT. There are five steps and requires only two experiments.

### 3.5.1 Excess carrier distribution mapping

A new characterization techniques called “Excess carrier distribution mapping” (ECDM) is proposed along with this modeling work. It is generally known that the larger the local excess carrier, the smaller the  $dv/dt$  during turn-off. The proposed technique allows one to obtain the explicit relation between  $dv/dt$  and its corresponding local excess carrier density based on the derived KCL. During the inductive switching turn-off, the MOSFET current should be zero before the voltage rising. If further ignoring the diffusion term of the collector current, the KCL in Eq. (3.34) becomes:

$$I_T \approx \frac{1}{1+b} I_T + \frac{p_{xd}}{N_D} i_d + i_d \quad (3.40)$$

For inductive switching, the total current is known, and the  $i_d$  can be obtained by calculating  $C_{oss} dv/dt$ . The only unknown in Eq. (3.40) is the local carrier density  $p_{xd}$ . By calculating a few  $p_{xd}$  at different positions that can be calculated using the voltage, the spatial carrier density can then be mapped by connecting the dots.

TCAD simulation is used to verify this techniques, since the carrier density profile can be directly observed in the software. By performing the inductive switching for two IGBT with low and high ambipolar lifetime in the drift region, the results of mapping the carrier density profile are shown in Figure 3-19.

It is worth pointing out that this new technique relies on the  $dv/dt$  of the switching waveforms rather than the amplitude and decaying of the current tail, which is too small for high voltage 4H-SiC n-IGBT at room temperature. With this characterization techniques, most

of the parameters related to the transient behavior can be extracted. In addition, it provides insights of not only the total charge but the carrier distributed at given current density for an IGBT.

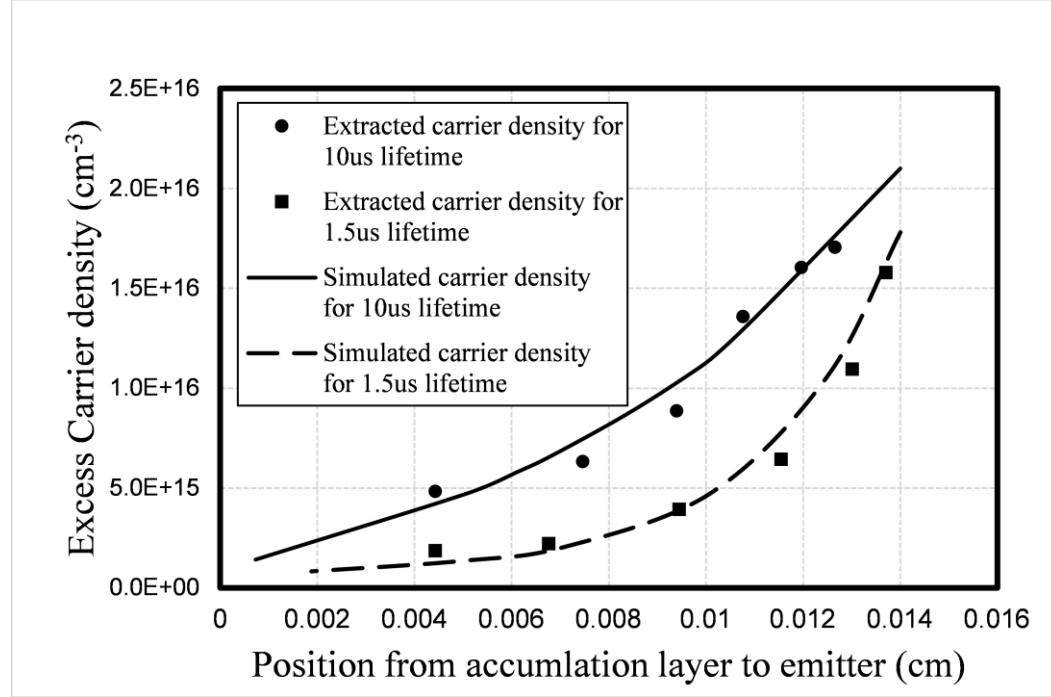


Figure 3-19 Validation of proposed direct mapping technique using simulation.

### 3.5.2 Extract $N_D$ and $v_{sat,p}$

The drift region doping and the hole saturation velocity can be extracted by observing the punch-through voltage at different current level during inductive switching. The relationship between punch-through voltage and the current level can be expressed as:

$$W_D = \sqrt{\frac{2\varepsilon V_{Pt}}{q(N_D + n_{dyn})}} \quad (3.41)$$

Where

$$n_{dyn} = \frac{I}{q \times A \times v_{sat,p}} \quad (3.42)$$

By plotting the  $N_D + n_{dyn}$  versus the current,  $N_D$  can be obtained by extrapolating the line back to  $I=0$ , as shown in Figure 3-20. The effective hole saturation velocity can be calculated using Eq. (3.41) and (3.42). Noted that the purpose of this “effective” saturation velocity is to accurately calculate not only the punch through voltage but also the dynamic carriers, as illustrated in Figure 3-8.

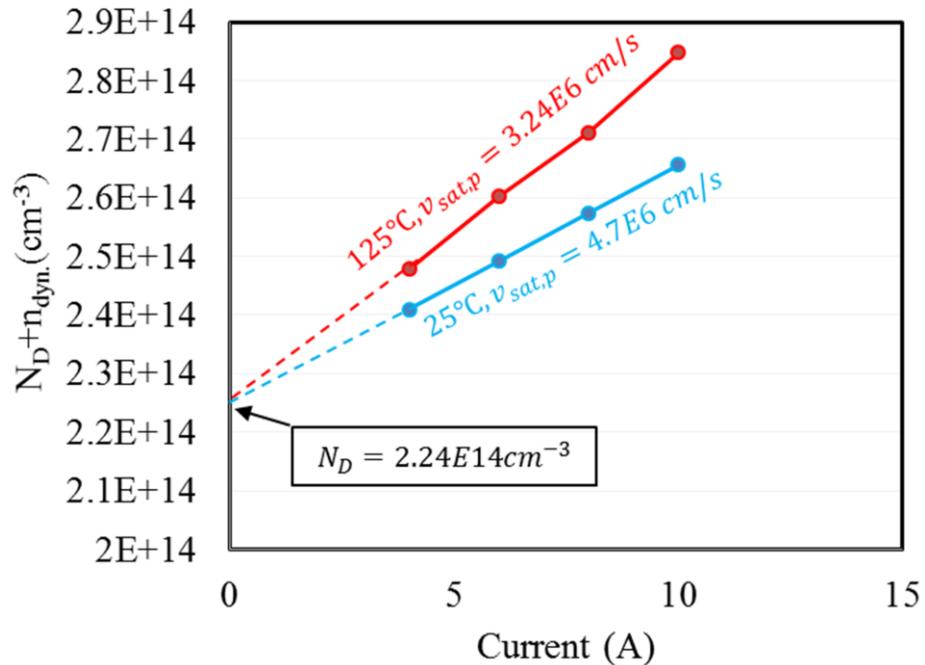


Figure 3-20 Dynamic carrier and the effective saturation velocity. The background doping  $N_D$  can be obtained by extrapolating the curve to current=0.

### 3.5.3 Extract $\tau_D$ and $h_n$

The next step of parameter extraction is to use the proposed carrier profile mapping technique to find out the ambipolar lifetime in the drift region and the parameter  $h_n$  that accounts for the injection from the MOSFET. The experiment required for this step is inductive switching. The high-level lifetime can be obtained by fitting the carrier density distribution obtained by the direct mapping techniques using exponential expression. The parameter  $h_n$  can be calculated using Eq. (3.28) if  $p_0$  is known.  $P_0$  can be obtained by extrapolating the fitted carrier density profile to  $x=0$ . The fitting results for different temperatures are shown in Figure 3-21. The extracted  $\tau_{HL}$  and  $h_n$  are plotted in Figure 3-22.

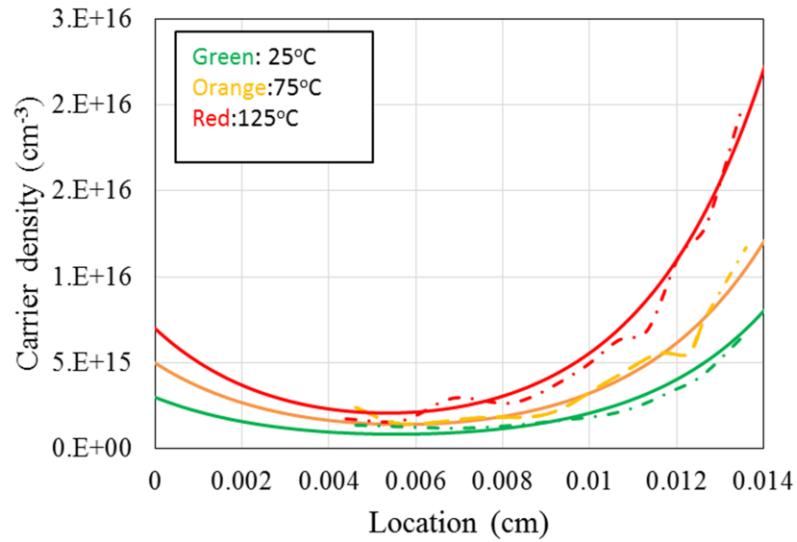


Figure 3-21 The result of direct mapping of carrier density profiles at different temperatures for the 10A 4H-SiC n-IGBT. Dashed line: extracted. Solid line: fitting using exponential expression ( $A \cdot \text{Exp}\left(\frac{x}{L}\right) + B \cdot \text{Exp}\left(-\frac{x}{L}\right)$ ).

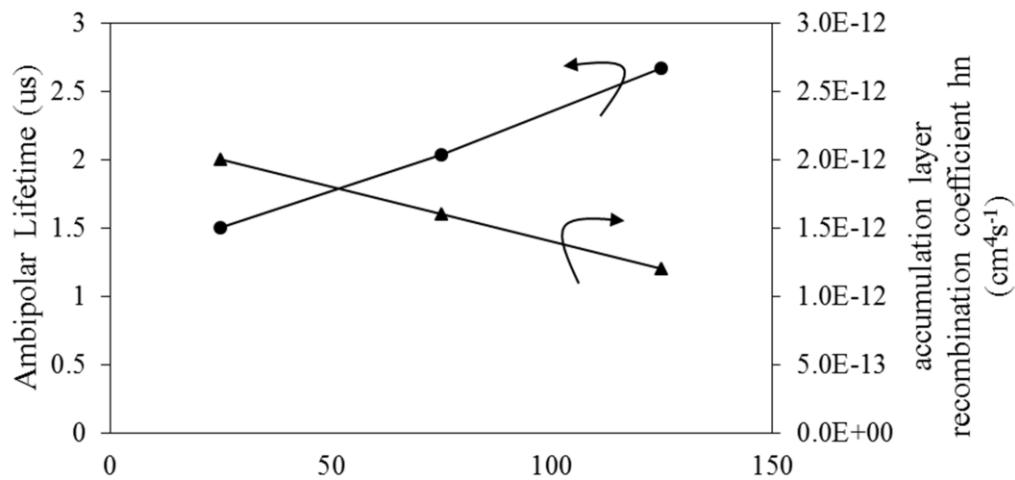


Figure 3-22 Extracted ambipolar lifetime and  $h_n$ .

### 3.5.4 Extract $d^2/\tau_B'$ and $Q_H$

Steady-state CCE and voltage rise time during turn-off will be used to obtain these two parameters. The second (recombination) and third term (back injection) in Eq. (3.25) are combined together as a new parameter  $\tau_B'$ .

$$\frac{dQ_T}{dt} = -\frac{Q_D}{\tau_{HL}} - \frac{(Q_T - Q_D)}{\tau_B'} + I_{MOS} + i_{dg} + i_{ds} \quad (3.43)$$

, where

$$\tau_B' = \tau_B \parallel \frac{d^2}{h_p Q_H} \quad (3.44)$$

, and d is the buffer layer thickness. The physical meaning of combining the two parameters is that there are infinite combination of  $h_p$  and  $\tau_B$  that leads to the same excess carrier injection in the drift region. For example, high injection from the BJT emitter and low buffer layer lifetime (more recombination through buffer layer) will result in the same excess carrier in the drift region as the case in which the injection is poor but with high buffer layer lifetime (no recombination).

During steady state, the change rate of the charge is zero in Eq. (3.43), the channel current is given by Eq. (3.45) using Eq. (3.26):

$$I_{MOS} = \frac{Q_D}{\tau_{HL}} + \frac{d^2}{\tau_B'} \left[ \frac{Q_D^2}{Q_H} \left( \frac{1}{L\alpha} \right)^2 + \frac{I_T}{2D_{pb}(1+b)} \right] \quad (3.45)$$

Then, the channel current for n-type IGBT can also be approximated as:

$$I_{\text{MOS}} \approx \frac{b}{b+1} I_T \quad (3.46)$$

Combining Eq. (3.45) and Eq. (3.46):

$$C \left[ \frac{1}{Q_H} + \frac{\frac{IT}{2Dpb(1+b)}}{\left(\frac{Q_D}{L\alpha}\right)^2} \right] = \frac{\frac{b}{1+b} I_T - \frac{Q_D}{\tau_H}}{\left(\frac{Q_D}{L\alpha}\right)^2} \quad (3.47)$$

, where  $C \equiv d^2/\tau_B'$ .

Noted that  $Q_D$  and  $L$  can be obtained using the direct mapping of carrier profile technique at given current. The unknowns in Eq. (3.47) now are  $Q_H$  and  $C$ . These two variables can be solved at different current levels, since they do not change as the current changes. However, the number of combination of these two parameters is still infinite. That is, as long as the combination of  $d$  and the  $\tau_B'$  result in a constant  $C$ , the carrier density profile will be the same. The extracted constant  $C$  is plotted in Figure 3-23) at different temperatures.

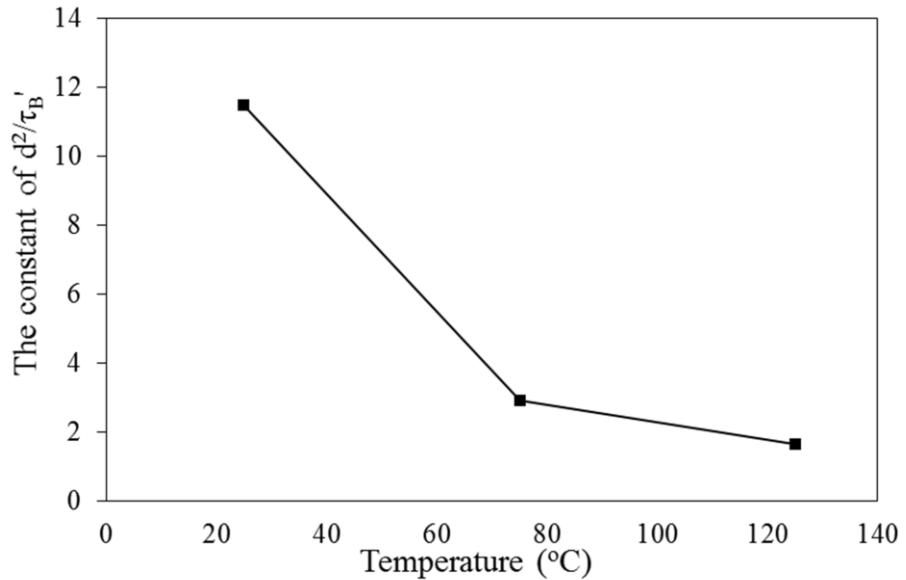


Figure 3-23 Extracted constant of  $\frac{d^2}{\tau_B'}$  at different temperature.

### 3.5.5 Extract $d$

The buffer layer thickness,  $d$ , can be extracting by varying the value and find the best fit between the simulated and measured turn-off current waveforms. It is found that, at room temperature, the sweeping of different values of  $d$  leads to almost the same current waveforms. This is due to the excess carrier in the buffer are too low to tell the difference even at different value of  $d$ . The solution is to extract  $d$  at elevated temperature, such that the current tail can be used to pin down the buffer layer thickness. The reason to vary  $d$  instead of  $\tau_B'$  is that  $d$  would not change with the temperature. At this step of the parameter extraction, not only the combination of the  $d$  and  $\tau_B'$  results in a specific excess carrier distribution at a given current density, but also will match the current tail of the measurement results.

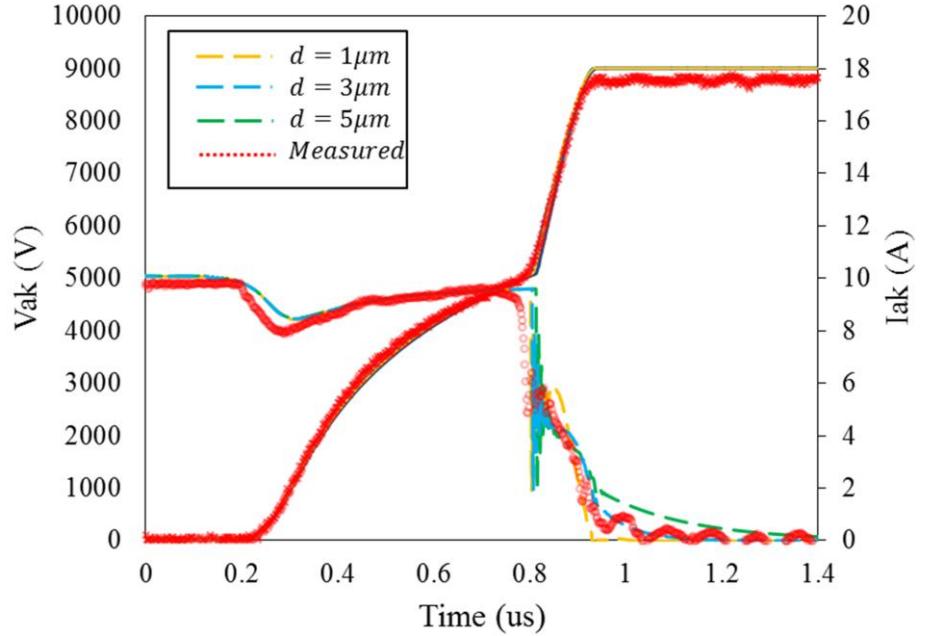


Figure 3-24 Simulated turn-off waveforms for different buffer layer thickness at fixed  $C \equiv \frac{d^2}{\tau_B}$ .

### 3.5.6 Extract parameters related to MOS channel

The MOSFET equation of the IGBT model is provided in Tab. I with other essential equations that have been introduced in the previous sections. The parameters used in the mosfet equation can be obtained by minimizing the least square error between simulated and measured IV curves with good initial guess the parameters. The results are summarized in Table 3.3. The

steady-state total current of the IGBT is the sum of the MOS current and the steady-state collector current  $I_{css}$  given in Eq. (3.35).

Table 3.2 Summarized equations used in the proposed model.

|   |   |
|---|---|
| <b>MOSFET</b><br>$I_{mos,lin} = \frac{K_{p,lin} \left[ (V_{GS} - V_{th})V_{ds} - \frac{1}{2} \frac{K_{p,lin}}{K_{p,sat}} V_{ds}^2 \right]}{1 + \theta(V_{gs} - V_{th})}$ <i>Linear region</i><br>$I_{mos,sat} = \frac{\frac{1}{2} K_{p,sat} (V_{GS} - V_{th})^2}{1 + \theta(V_{gs} - V_{th})}$ <i>Saturation region</i><br>$I_{mos,off} = 0$ <i>Cut-off region</i><br><br><b>Drift Region</b><br>$V_B = \int_0^W \frac{J_T}{q(\mu_n + \mu_p)p(x)}$ $p(x) = K_1 \exp\left(\frac{x}{L}\right) + K_2 \exp\left(-\frac{x}{L}\right)$ $K_1 = \frac{p_w - p_0 \exp(-\frac{W}{L})}{\exp(\frac{W}{L}) - \exp(-\frac{W}{L})}$ $K_2 = \frac{p_0 \exp(\frac{W}{L}) - p_w}{\exp(\frac{W}{L}) - \exp(-\frac{W}{L})}$ | <b>PN</b><br>$V_{pn} = \frac{kT}{q} \ln(p_0 p_w / n_i^2)$<br><br><b>KVL</b><br>$V_{AK} = V_{ds} + V_{PN} + V_{drift}$<br><br><b>KCL</b><br>$I_T = \frac{1}{1+b} I_T + q A D_a m_c + i_d + i_q + I_{MOS}$ $i_d = (C_{gd} + C_{ds}) \frac{dV_{AK}}{dt}$ $i_q = \frac{p_{xd}}{N_D} i_d$<br><br><b>CCE</b><br>$\begin{cases} \frac{dQ_T}{dt} = -\frac{Q_D}{\tau_D} - \frac{Q_T - Q_D}{\tau_B'} + I_{mos} + i_{gd} + i_{ds} \\ Q_T = Q_D + \frac{Q_D^2}{Q_H} \left( \frac{d}{L\alpha} \right)^2 + \frac{d^2}{2D_{pb}} \frac{I_T}{1+b} \end{cases}$ |
|---|---|

Table 3.3 Extracted parameter inputs of the proposed model at different temperatures.

|   |                              |              |
|---|------------------------------|--------------|
| Chip size   | $A_{chip}(cm^2)$             | 0.64         |
| Active Area   | $A_{active}(cm^2)$           | 0.32         |
| Drift region width                                    | $W_D(\mu m)$                 | 140          |
| Buffer layer width                                    | $d(\mu m)$                   | 3            |
| Drift region doping                                   | $N_D(cm^{-3})$               | $2.2E14$     |
| Buffer layer dose                                     | $Q_B(cm^{-2})$               | $1.03E13$    |
| Ambipolar lifetime in the drift region at 25°C        | $\tau_{D25^\circ C}(\mu s)$  | 1.5          |
| Ambipolar lifetime in the drift region at 125°C       | $\tau_{D125^\circ C}(\mu s)$ | 2.67         |
| Effective minority lifetime in the buffer at 25°C     | $\tau_{B25^\circ C}(ns)$     | 7.86         |
| Effective minority lifetime in the buffer 125°C       | $\tau_{B125^\circ C}'(ns)$   | 62           |
| Effective hole saturation velocity at 25°C            | $v_{sat,p,25^\circ C}$       | $4.7E6$      |
| Recombination constant at accumulation layer at 25°C  | $h_{p,25^\circ C}(cm^4/s)$   | $6.15E - 12$ |
| Recombination constant at accumulation layer at 125°C | $h_{p,125^\circ C}(cm^4/s)$  | $1.21E - 12$ |
| Effective hole saturation velocity at 125°C           | $v_{sat,p,125^\circ C}$      | $3.24E6$     |
| Threshold voltage at 25°C                             | $V_{th,25^\circ C}(V)$       | 4            |
| Threshold voltage at 125°C                            | $V_{th,125^\circ C}(V)$      | 3            |
| Transconductance in the linear region at 25°C         | $k_{lin,25^\circ C}(A/V^2)$  | 2.5          |
| Transconductance in the saturation region at 25°C     | $k_{sat,25^\circ C}(A/V^2)$  | 0.6          |
| Transconductance in the linear region at 125°C        | $k_{lin,125^\circ C}(A/V^2)$ | 4            |
| Transconductance in the saturation region at 125°C    | $k_{sat,125^\circ C}(A/V^2)$ | 1            |
| Transverse electric field parameter                   | $\theta(V^{-1})$             | 0.02         |

## 3.6 Model Validation

### 3.6.1 On-state IV

The parameter fitting for on-state IV curve is similar to the manner used in 15kV MOSFET modeling work in Chapter 2. Figure 3-25 shows that the IV curves can be well fitted using the equations provided in Table 3.2.

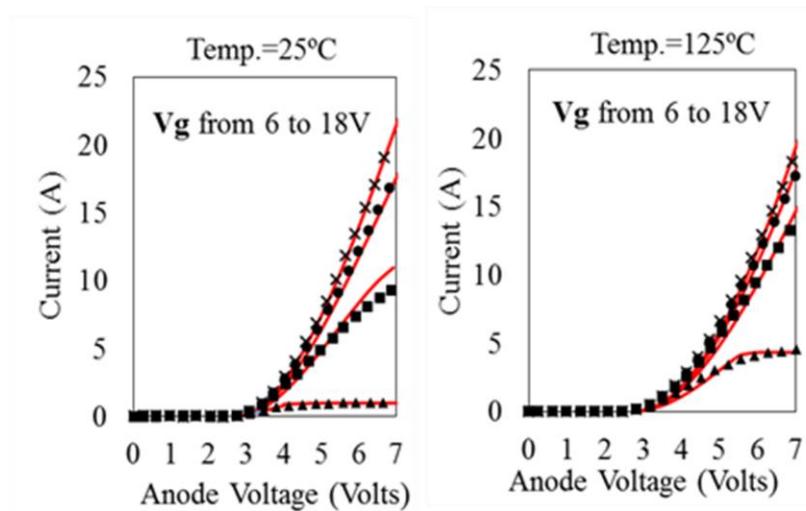


Figure 3-25 Modeled and measured IV curves of 15kV 4H-SiC at different temperatures.

The transconductance and the threshold voltage as a function of temperature is shown in Figure 3-26.

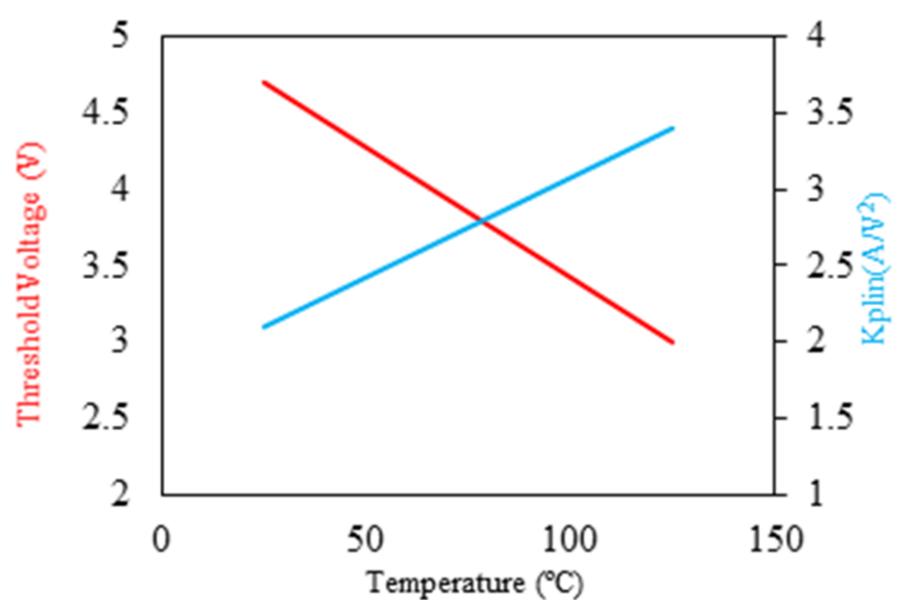


Figure 3-26 The extracted threshold voltage and transconductance as a function of temperature.

During the on-state (steady-state), all the components that associate with time, such as  $dQ/dt$  or  $dV/dt$  will not activate, as shown in Figure 3-27.

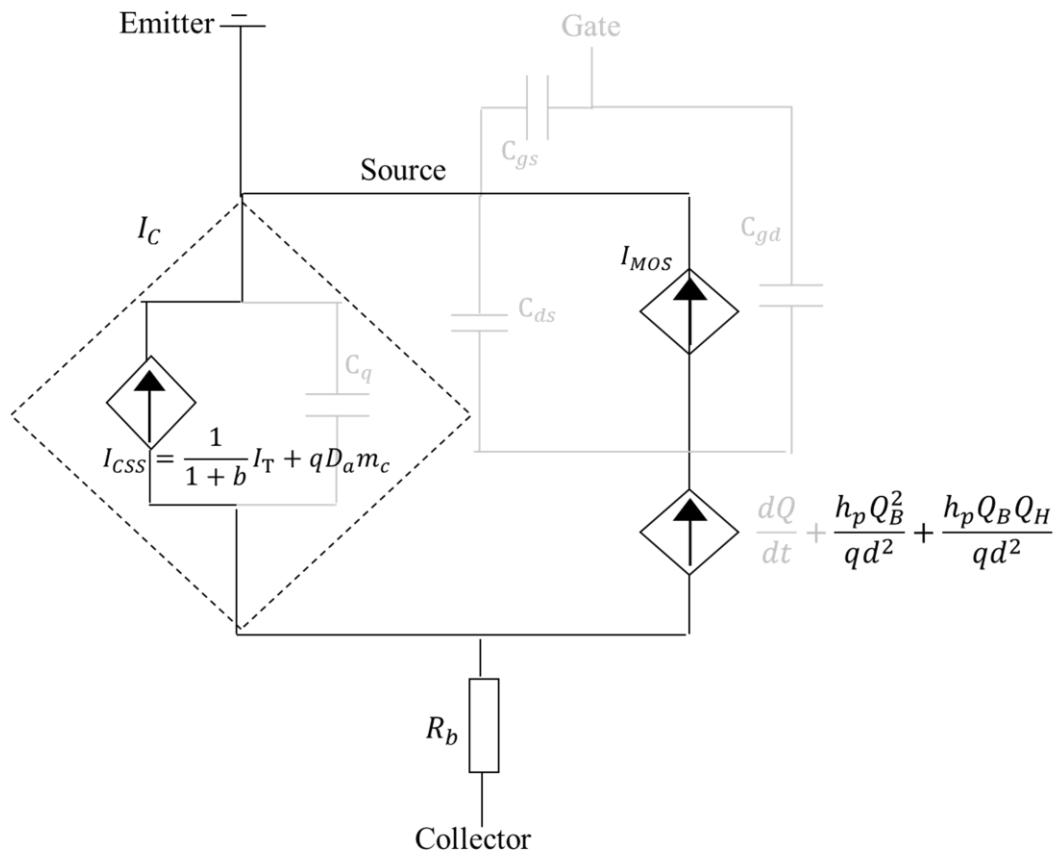


Figure 3-27 The equivalent circuit model during the steady-state.

### 3.6.2 Transient modeling

The simulated results in the Simulink/Matlab will be compared to the measurement of inductive switching at 10A, 9kV. A simple schottky diode model will be used in the simulated circuit, as shown in Figure 3-28. The full cycle execution time for turn-on and turn-off is about 40 seconds for a 20  $\mu$ s simulation using ODE 15 solver. During the voltage rise/fall time, the execution time is about 5 seconds. The turn-off measured and simulated waveforms are shown in Figure 3-31 and Figure 3-32, respectively.

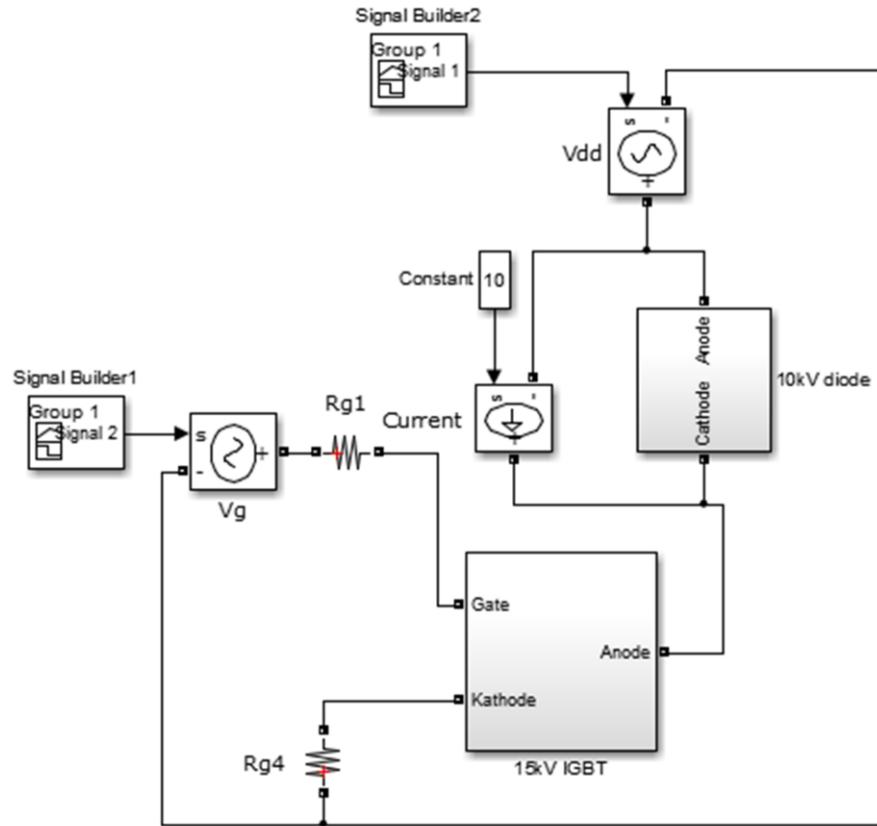
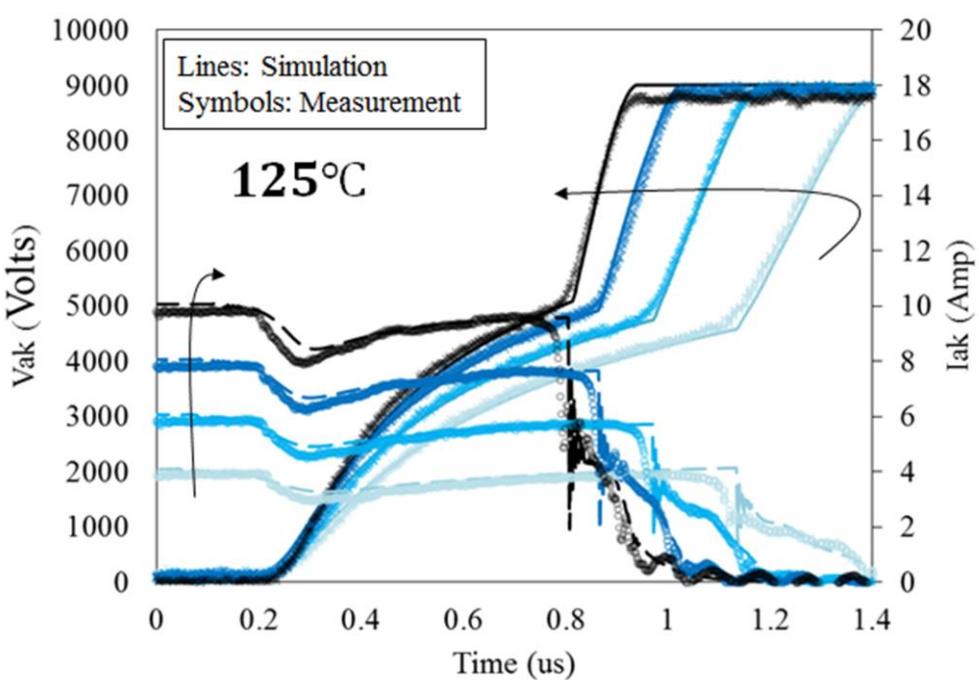
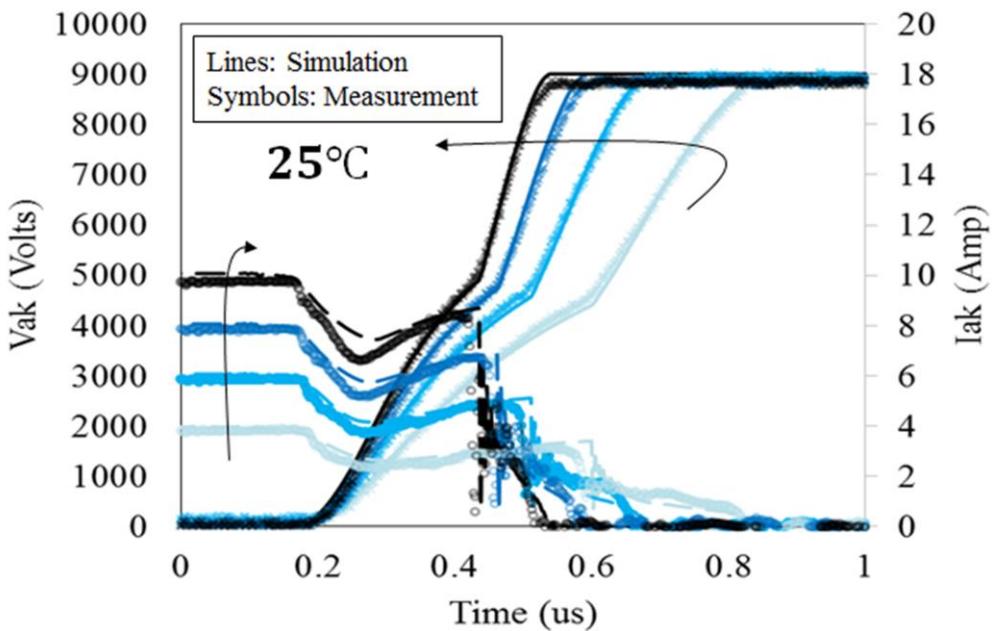


Figure 3-28 15kV IGBT modeled in an double pulse switching circuit in Simulink.



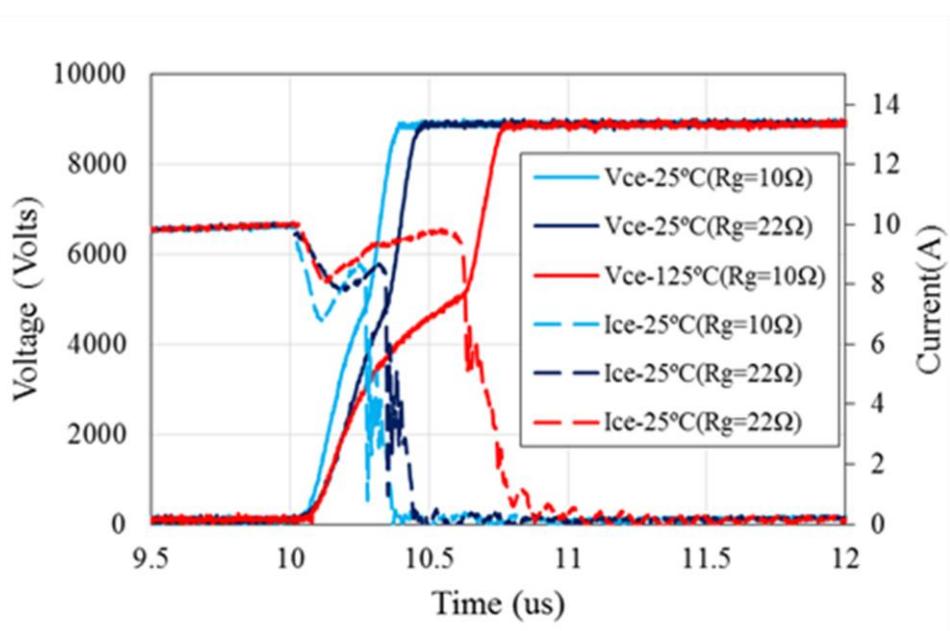


Figure 3-31 Measured 15kV 4H-SiC turn-off waveforms under different conditions.

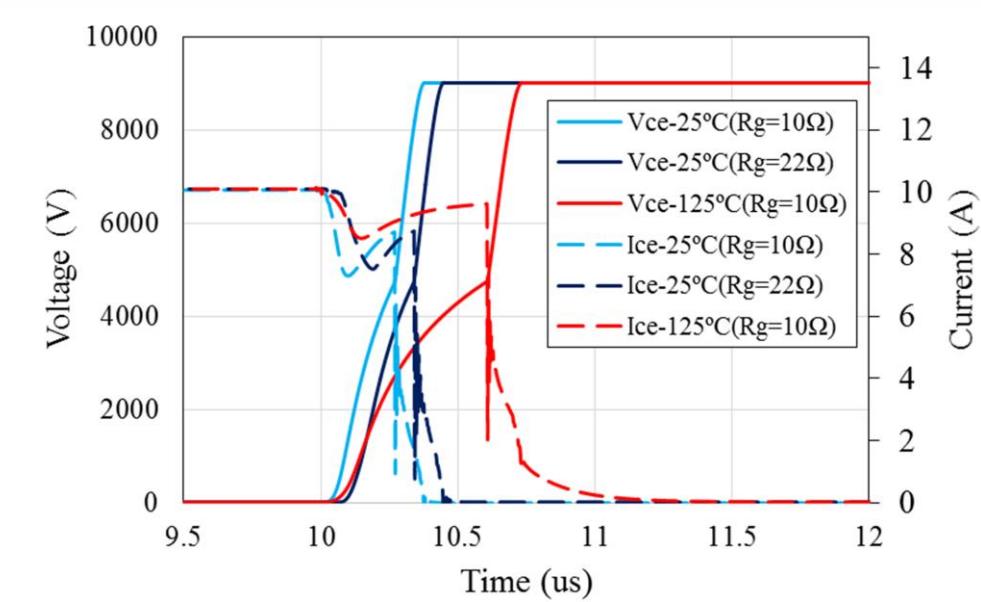


Figure 3-32 Simulated 15kV 4H-SiC turn-on waveforms under different conditions.

The turn-on measured and simulated waveforms are shown in Figure 3-33 and Figure 3-34.

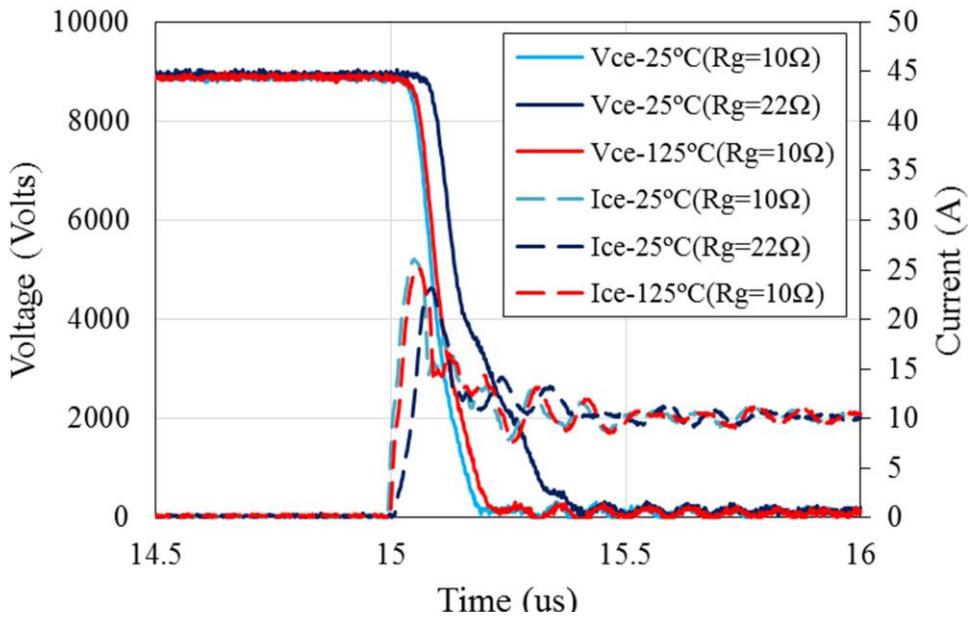


Figure 3-33 Measured 15kV 4H-SiC turn-on waveforms under different conditions.

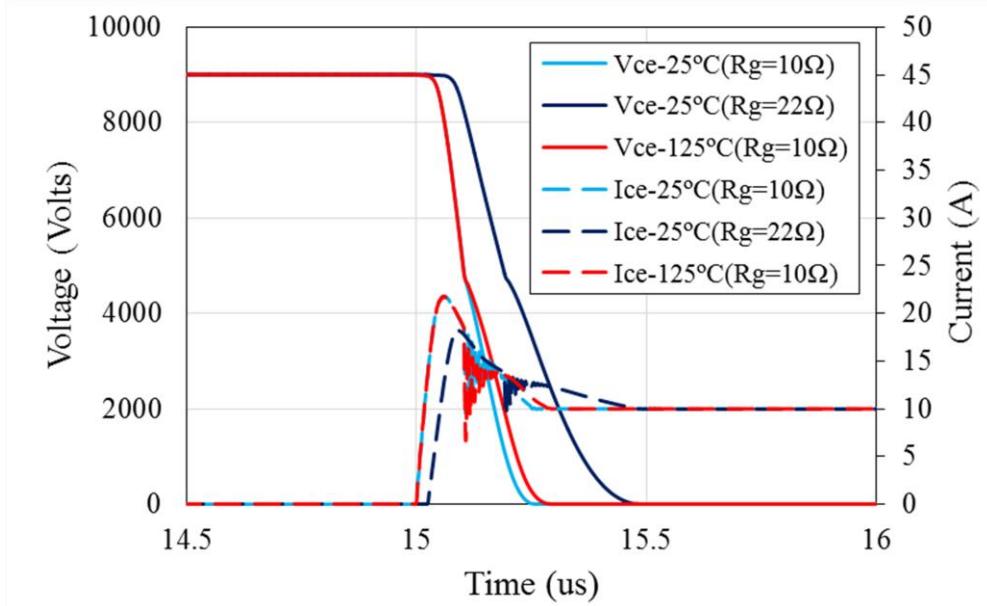


Figure 3-34 Simulated 15kV 4H-SiC turn-on waveforms under different conditions.

### 3.6.3 Charge dynamic during the switching

*Turn-off discussion:*

The physics quantities such as effective capacitance and charge are plotted in Figure 3-35 to understand what is happening in each period during inductive switch turn-off.

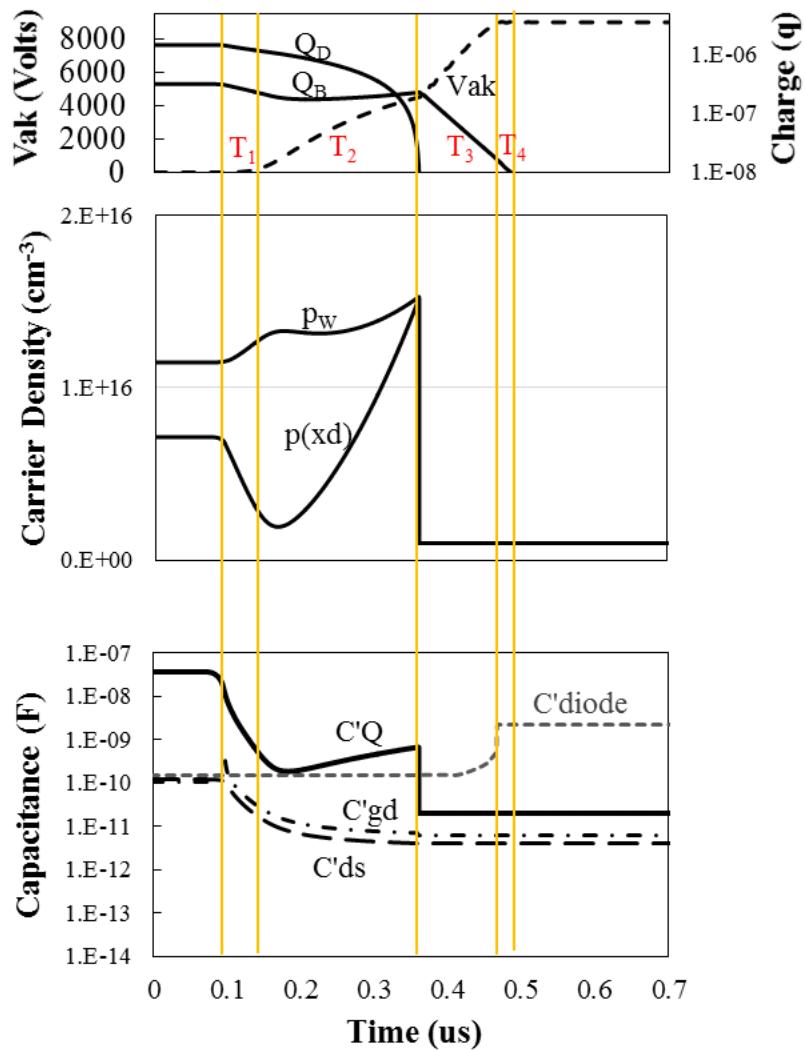


Figure 3-35 Instantaneous physical quantities during turn-off plotted in the Simulink.

(a) Turn-off period T1:

MOS current is decreasing, and therefore the charge starts to decrease from on-state. The voltage rising is not obvious since the carrier density is still high at the MOS side.

(b) Turn-off period T2:

Voltage starts to increase as the channel current is totally cut-off. The depletion boundary, while retreating, “sees” local carrier density at different locations, and CQ is changing with the local carrier density (equation is in Table II). Notice that unlike MOSFET, the output capacitance of 4H-SiC IGBT actually increase as the voltage increase due to the dominate effect of CQ.

(c) Turn-off period T3:

The IGBT is punch-through. The charge in the drift region is zero while the charge in the buffer layer, QB, starts to decrease. The dv/dt is determined by the amount of charge left and the doping in the buffer layer.

(d) Turn-off period T4:

If significant amount of QB still present, there will be tail current.

*Turn-on discussion:*

The physics quantities such as effective capacitance and charge are plotted in Figure 3-36 to understand what is happening in each period during inductive switch turn-on.

(a) Turn-on period T4:

Before the depletion region can be recovered in the drift region, the charge in the buffer layer has to increase to an amount at which the electric field is pushed back to the drift region – from a trapezoidal to triangle shape.

(b) Turn-on period T5:

The  $dv/dt$  is large since there is no charge in the drift region. It is mainly determined by the gate drive circuitry.

(c) Turn-on period T6:

The  $dv/dt$  starts to slow down since the depletion boundary starts to “see” carriers. The charging of the drift region is fast since the total current is high due to the reverse recovery current from the Schottky diode.

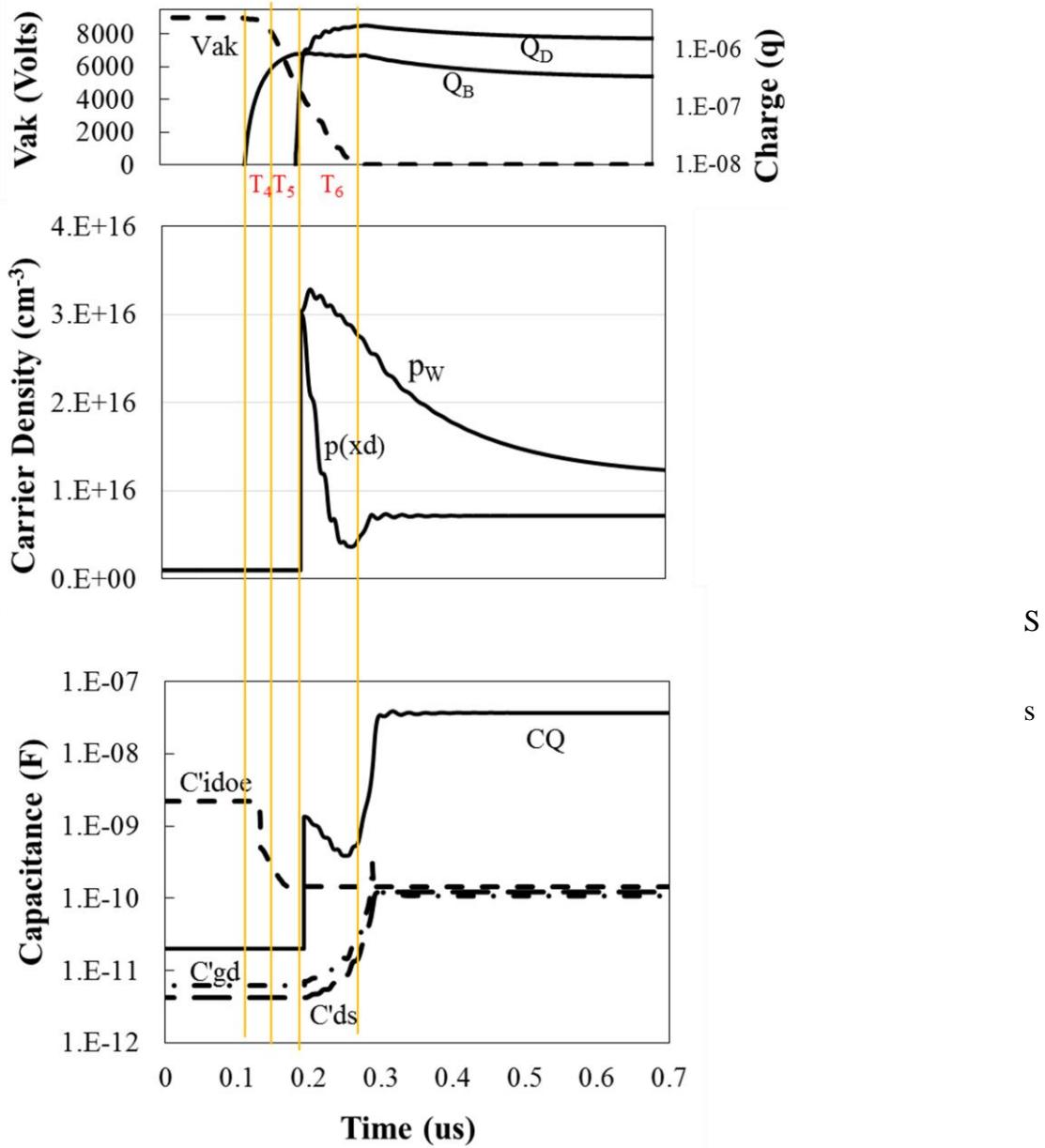


Figure 3-36 Instantaneous physical quantities during turn-on plotted in the Simulink.

### 3.7.4 Switching energy as a function of current

Figure 3-37 and Figure 3-38 are the energy loss predicted by the model at 25°C and 125°C, respectively.

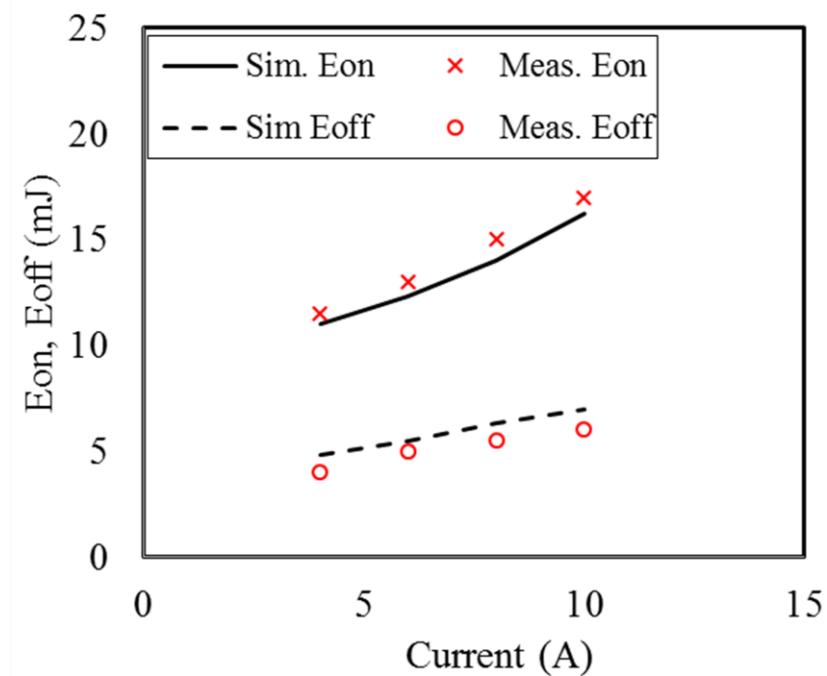


Figure 3-37 Energy loss during turn-off and turn-on at 25°C. VDD=9kV, Rg=10ohm.

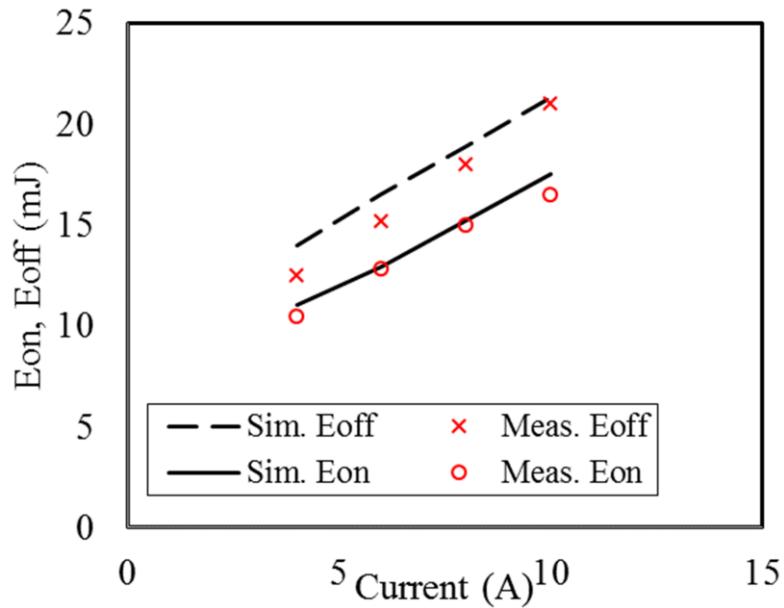


Figure 3-38 Energy loss during turn-off and turn-on at 125°C. VDD=9kV, Rg=10ohm.

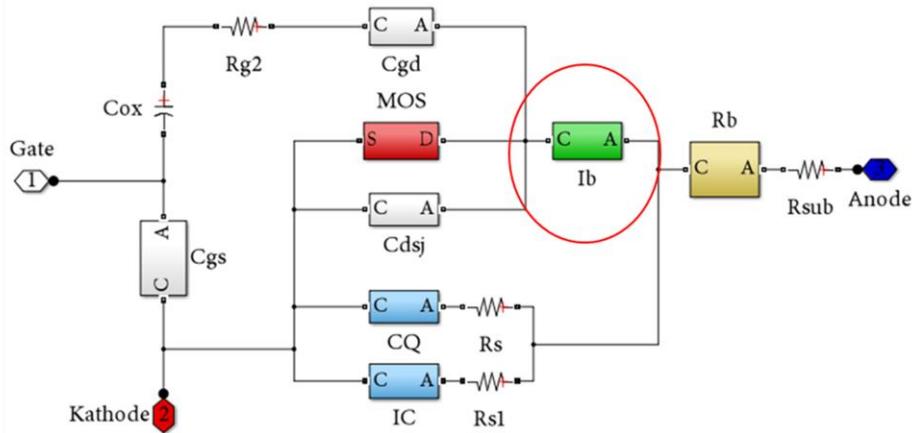
### 3.7 Comparison between Hefner's model and the proposed model

Hefner's model is built for 32mm<sup>2</sup> 4H-SiC n-IGBT to compare with the proposed model.

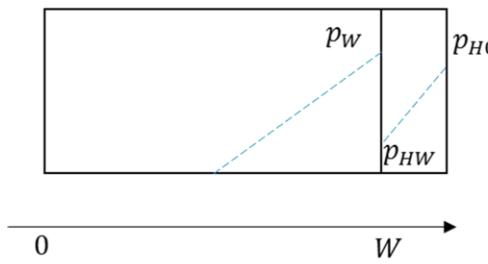
There are four major difference when implementing two models. The parameter extraction methodology and the simulation results will be compared.

#### 3.7.1 Difference I – Charge Continuity Equation

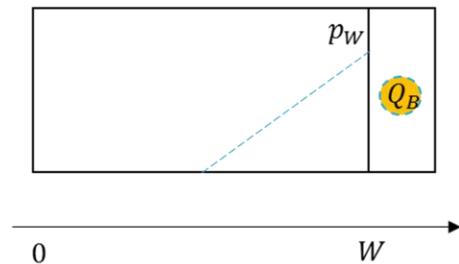
The proposed model lumped the recombination and the back injection in the buffer layer in order to have simpler parameter extraction. The difference is illustrated in Figure 3-39.



**Hefner's model**



**The proposed model**



Recomb. Back injection

$$\frac{dQ_T}{dt} = -\frac{Q_D}{\tau_D} - \frac{Q_B}{\tau_B} - \frac{I_{sne}}{n_i^2} p_{H0} N_H$$

Recomb.+Back injection

$$\frac{dQ_T}{dt} = -\frac{Q_D}{\tau_D} - \frac{Q_B}{\tau_B'}$$

Figure 3-39 Side-by-side comparison of the charge continuity equation between Hefner's and the proposed model.

### 3.7.2 Difference II – Charge Continuity Equation

As shown in Figure 3-40, the proposed model incorporates  $p_0$ , the carrier concentration in the accumulation layer while calculating the drift region resistance.

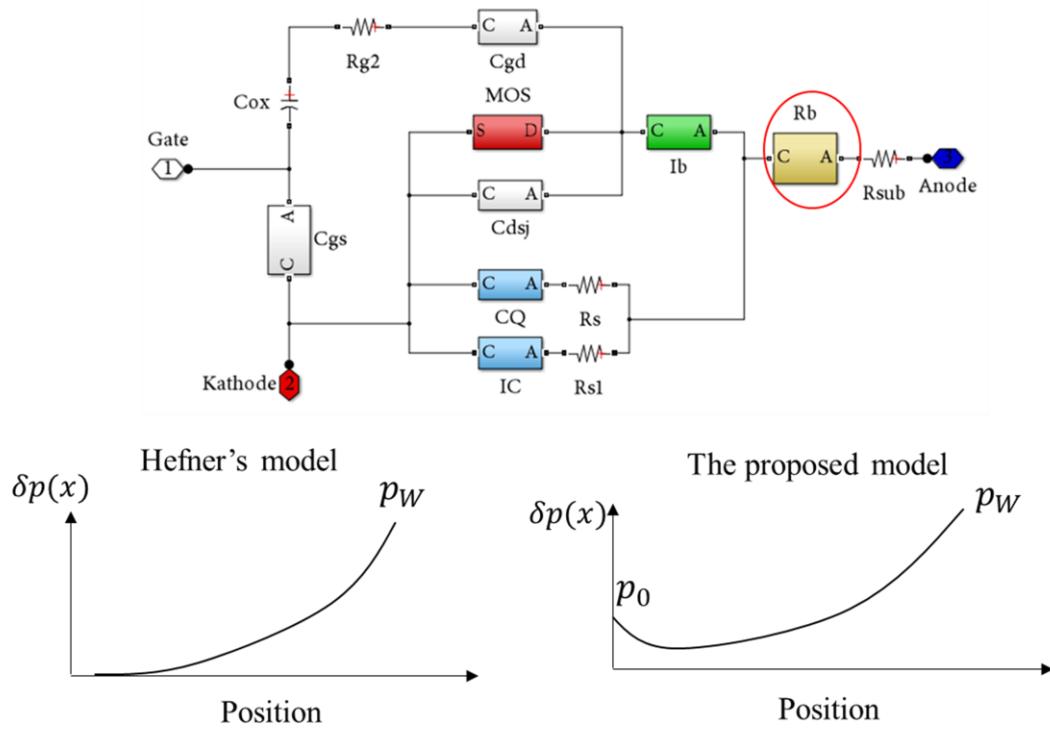


Figure 3-40 Side-by-side comparison of the calculation of the drift region resistance between Hefner's and the proposed model.

### *3.7.3 Difference III – Collector current*

During the turn-off process, the excess holes are being removed and swept through the depletion region and collected by the p-well before further depletion region can be formed. This component is part of the collector current that is associated with  $dv/dt$ , or with the moving boundary of depletion region. While Hefner's model use a mathematical approximation – redistribution current – to account for the effect of moving (depletion) boundary on the total excess charge, the proposed model directly tracking the local excess carrier at each time step of calculation. The directly tracking of the local excess carrier allows the proposed model to translate the local  $\delta p(x_d)$  directly to the instantaneous Charge Removal Capacitance  $C_Q$  and then to  $dv/dt$ , as shown in Figure 3-41.

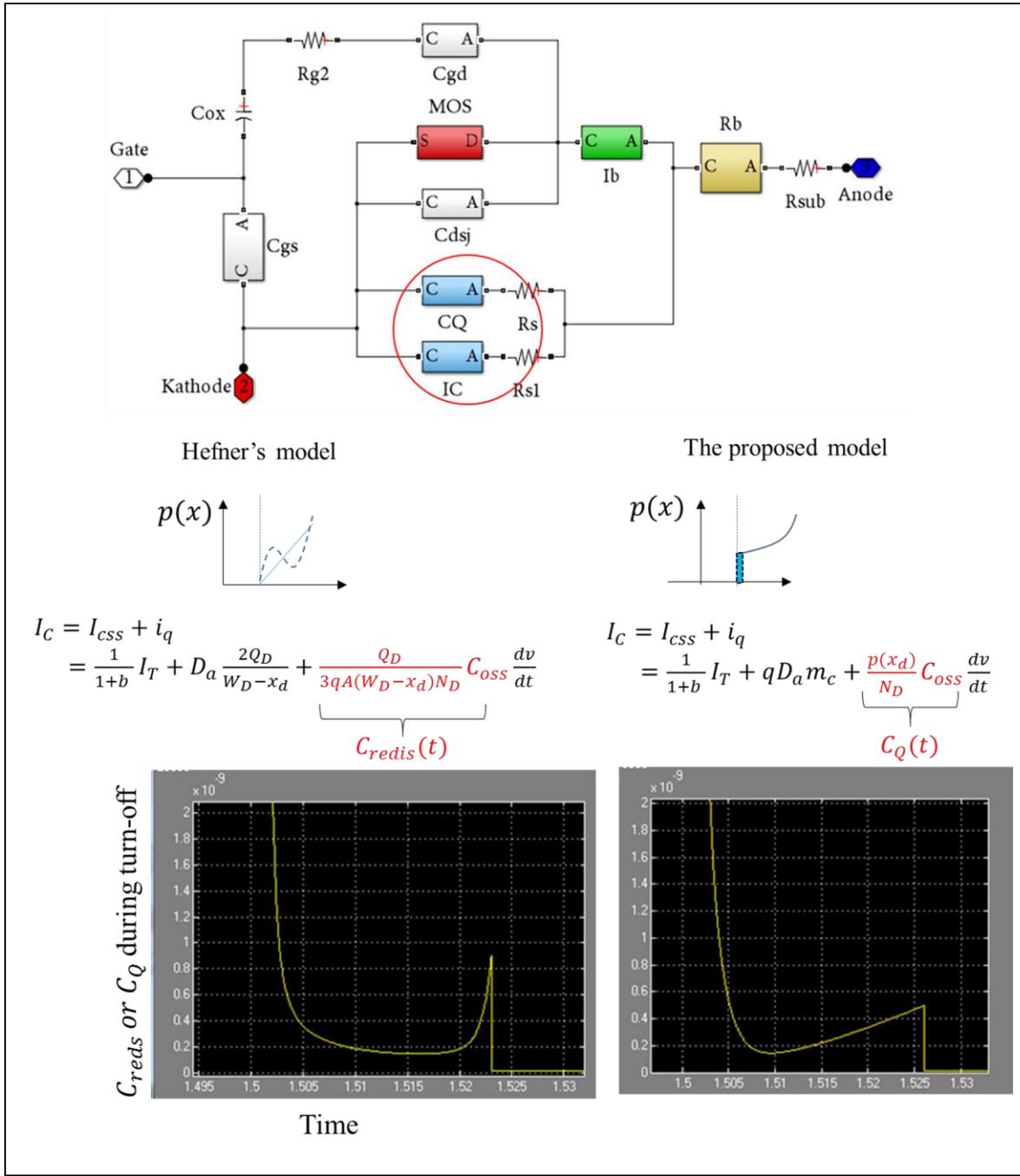


Figure 3-41 Side-by-side comparison of the diffusion capacitance between Hefner's and the proposed model.

### 3.7.4 Difference IV – Ambipolar parameter extraction

While the Hefner's model use the current tail to extract the ambipolar lifetime in the drift region and the buffer layer, the proposed model use the voltage rise waveform to direct extract the carrier density at different location as the voltage rising before punch through, as depicted in Figure 3-42. However, SiC IGBT is known for its absence of the current tail, especially at room to medium temperature [2]. Using current tail to extract the lifetime may result in the poor fitting results at room temperature as well as at low current density [36]. On the contrary, using the proposed excess carrier mapping technique can directly translate the  $dv/dt$  to a local carrier density even there is no current tail.

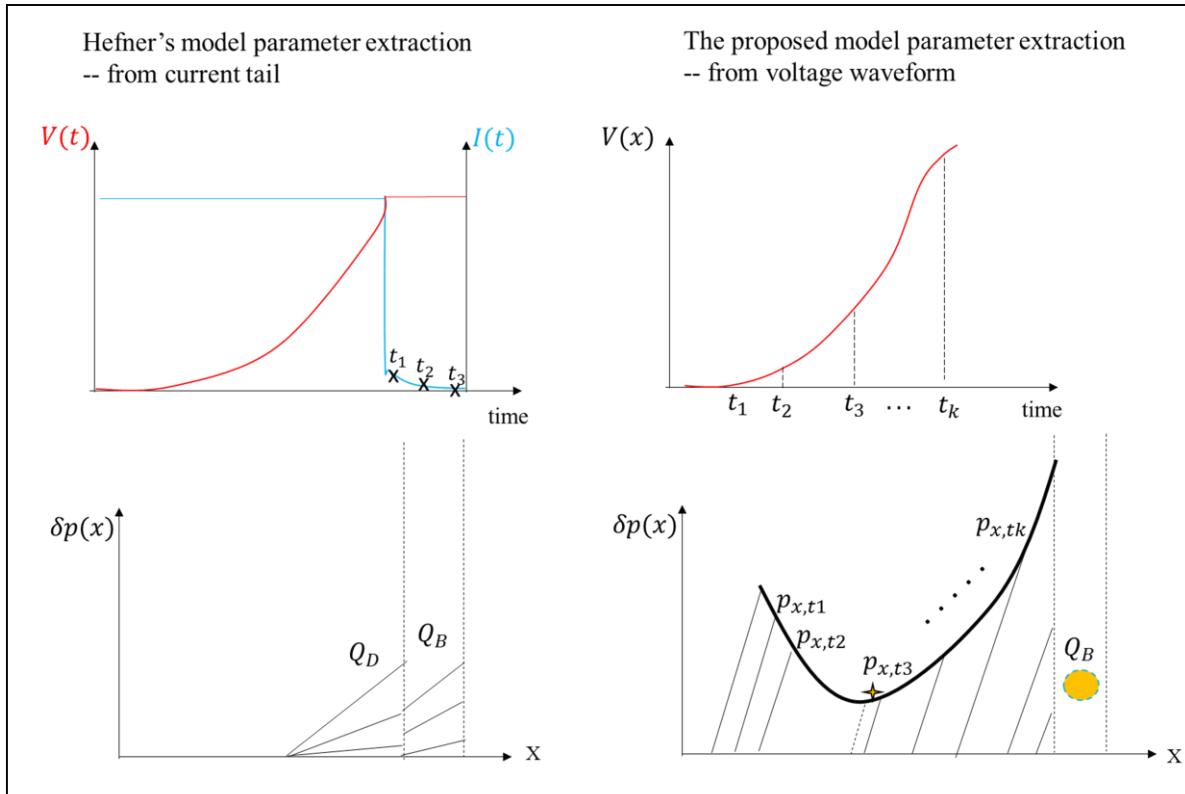


Figure 3-42 Difference between Hefner's and the proposed model in terms of lifetime extraction methodology.

### 3.8.5 Switching simulation comparison between Hefner's model and the proposed model

Figure 3-43 and Figure 3-45 are the simulation results of Hefner's and the proposed model. It can be seen that Hefner's model has less accurate result at lower current level. In addition, although the voltage rise time can be fitted, the voltage waveform is less accurate than the proposed model. The proposed model, on the other hand, can make good predictions of the voltage rise waveform, since the model faithfully translate the information of carrier to  $dv/dt$  for each  $v(t)$ . Figure 3-44 shows that the waveform error for the proposed model is much less than that of Hefner's model.

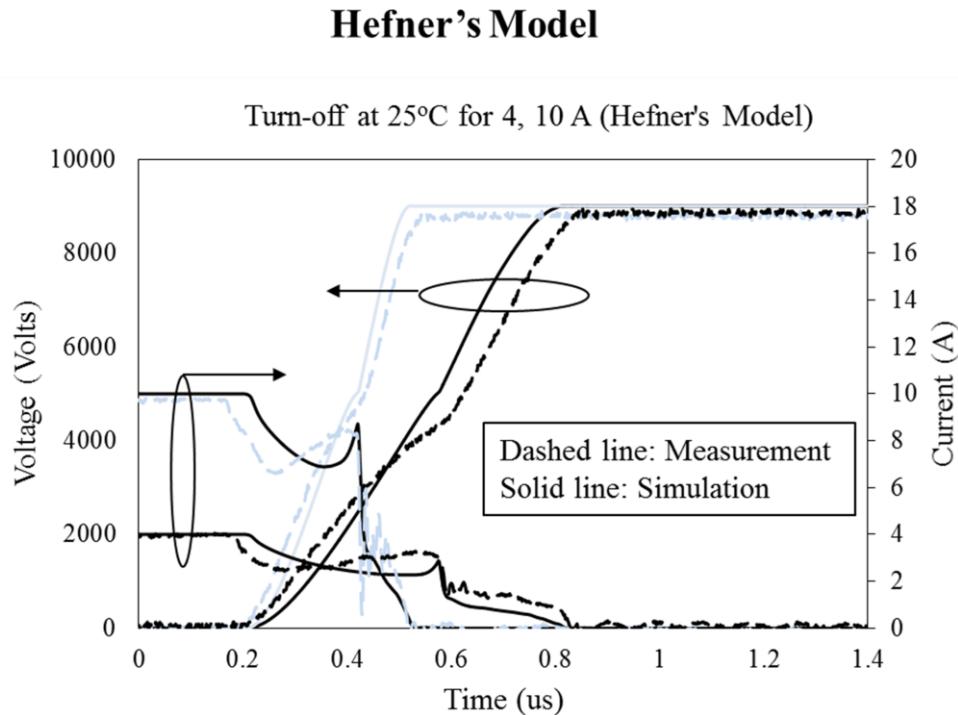


Figure 3-43 Hefner's model compared with the measurement results.

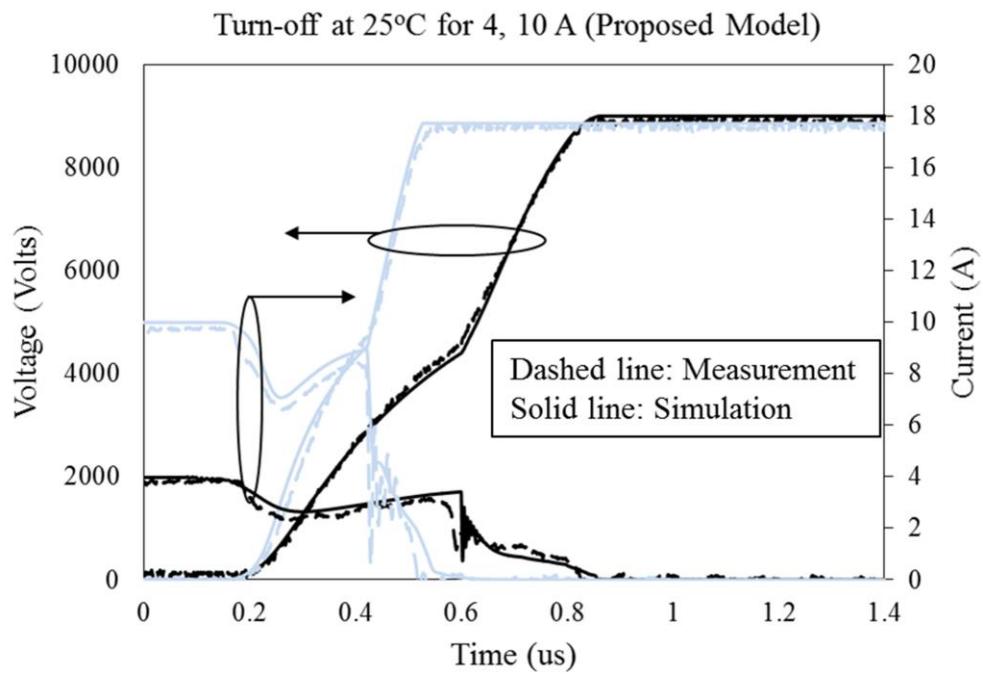


Figure 3-45 The proposed model compared with the measurement result.

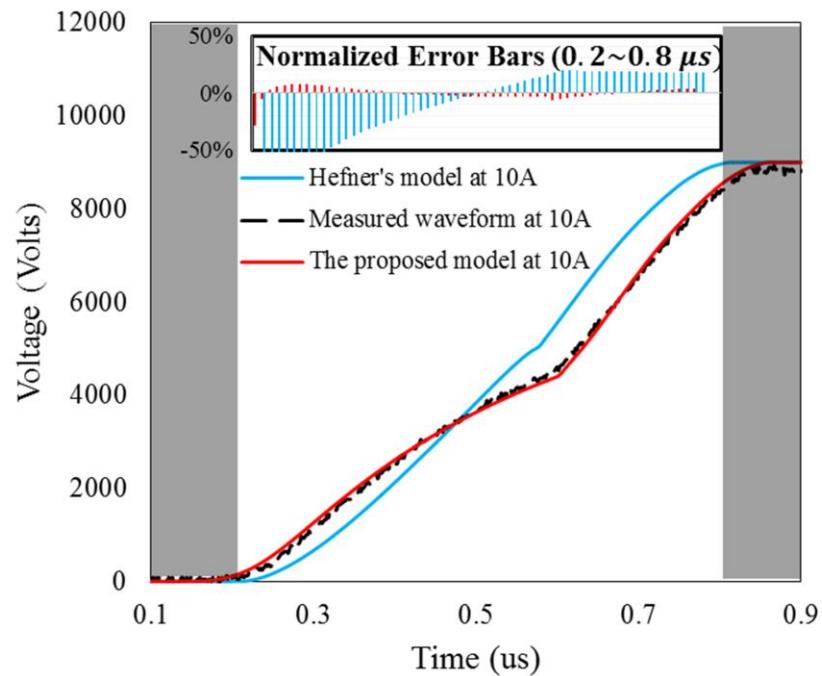


Figure 3-44 Side by side comparison of voltage waveforms and normalized error bars for the proposed and Hefner's model.

### 3.8 Computational speed

The solver used in the model is “ODE15,” a solver that has good convergence and fast speed especially for stiff problems. However, the simulation speed is still slow using ode 15 due to the numerical oscillation when calculating certain values of, for example, voltage, current, or charge. While more sophisticated solution might be possible, a more simple way of improving the numerical calculation in Simulink/Matlab is to insert a second order low pass filter at the output of the value before feeding into the next calculation block. Noted that the cut-off frequency must be much higher than the transient response of the device/circuit. For example, the cut-of frequency of 1GHz should be more enough to filter out the numerical oscillation without compromising the signal fidelity. Figure 3-46 illustrates the improvement of the simulation speed after incorporating the low-pass filter in the model. Figure 3-47 shows the low-pass filter block being used in the model.

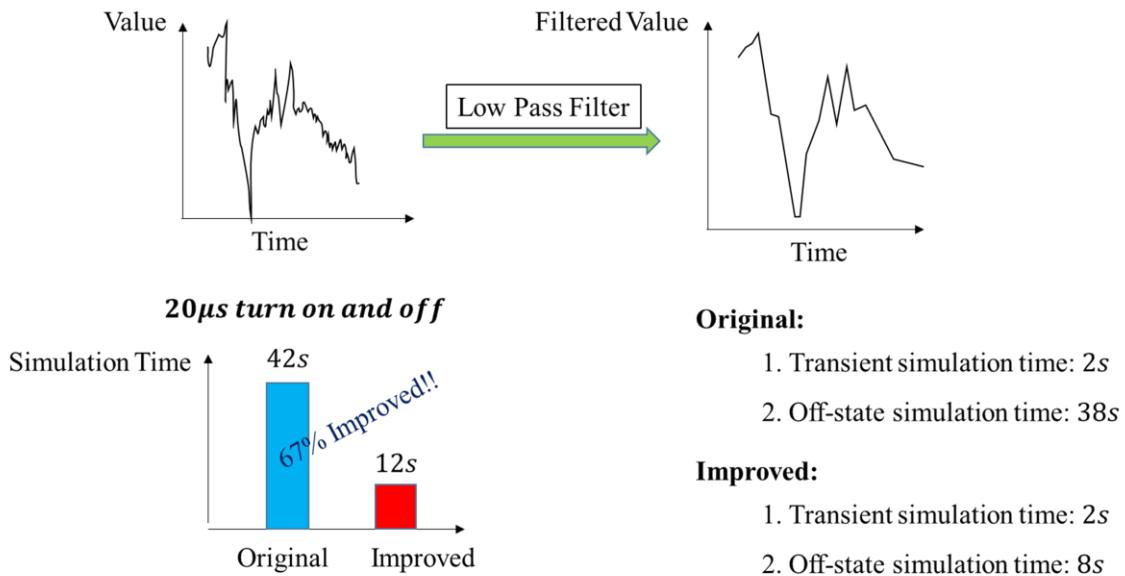


Figure 3-46 Improving the computational speed by inserting the low pass filter.

A turn-off and turn-on transient takes 8 second and 2 second respectively after including the low-pass filter – that is 67% improvement of the case without the low pass filter.

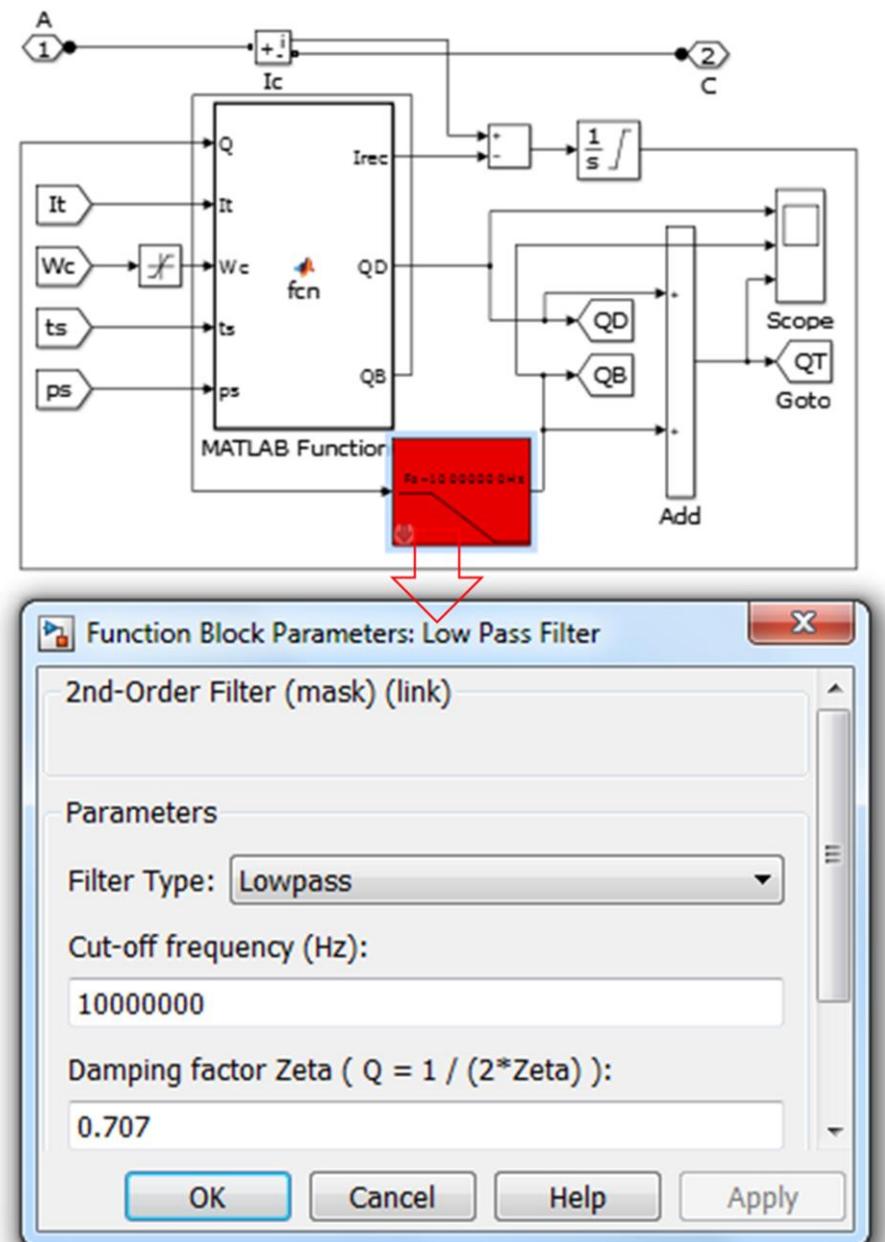


Figure 3-47 The low pass filter in the Charge Continuity Equation (CCE) block.

# Chapter 4

## Novel Structure for High Voltage 4H-SiC IGBT

This chapter will review the optimization studies of IGBT parameters and propose practical approaches with viable technology to achieve the goals suggested by the literatures with the aid of the proposed analytical model. Figure 4-1 shows parameters of an IGBT that can be designed to have different device characteristics. To achieve the best trade-off between conduction and switching loss, one has to find the optimum carrier density profiles [13]. Then, the parameters in the JFET region and the buffer layer [12] can be adjusted to achieve a certain profile. The relationship between the parameters (which is difficult to engineer) in P+ emitter and injection capability have been analytically discussed in [4], in which a clear-cut conclusion is drawn that the quality of the emitter should be as good as possible, and the buffer layer can then be designed to control the injection.

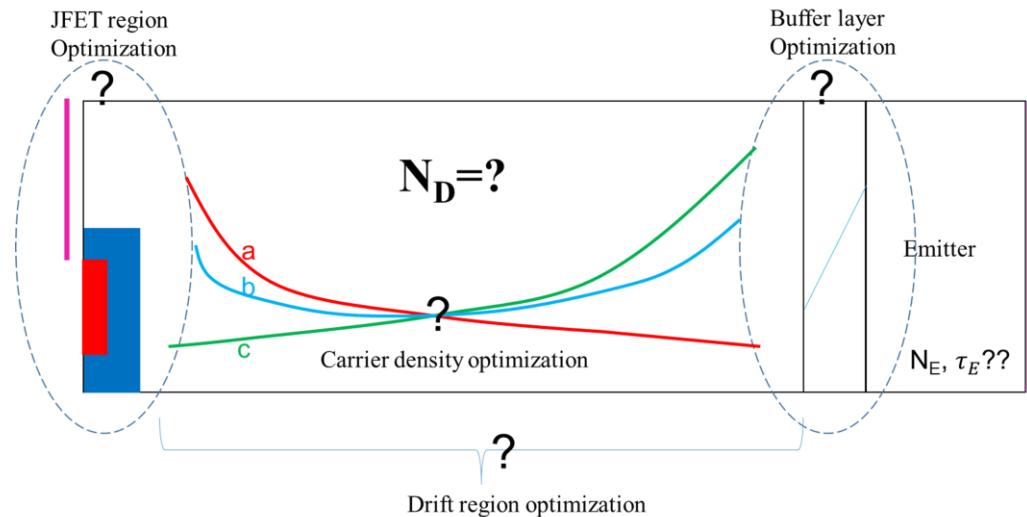


Figure 4-1 IGBT optimizations and theories that will be discussed in this chapter.

## 4.1 Review of 4H-SiC IGBT optimization works

### 4.1.1 Optimum carrier density profile

The theoretically proven that the optimum carrier density profile [13] is the blue carrier profile shown in Figure 4-2. The reason is that this type of profile will not result in voltage rising until the carriers near accumulation layer are removed. By the time the carriers near this region are removed, the amount carriers left in the drift region is very little, resulting in fast dv/dt toward higher anode voltage.

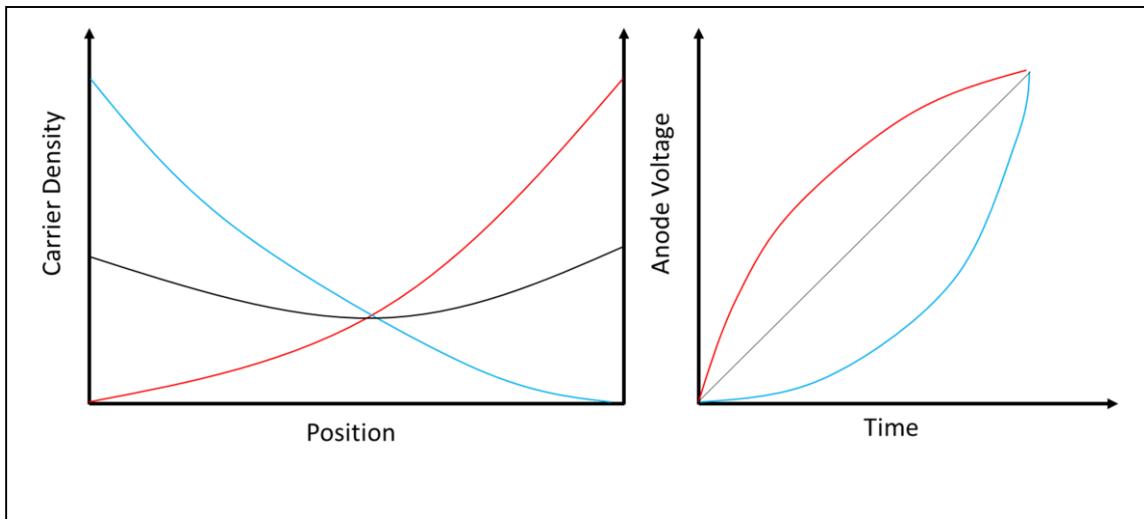


Figure 4-2 Three different types of carrier density profile and their corresponding turn-off waveforms.

Figure 4-3 shows the simulated response of turn-off loss and drift region voltage drop to the increase of  $p_W$  or  $p_0$ . It is clear that increasing  $p_0$  has the better trade-off between conduction and switching loss.

However, it is not likely for 4H-SiC IGBT to achieve such carrier profile. In order to enhance the injection from the channel, one has to (i) increase the doping the JFET region to

facilitate major current spreading and (ii) make trench structure to increase the cell density. The first approach has its limit in order to maintain desired BV rating, while the trench technology is not mature in 4H-SiC due to poor channel mobility along the trench wall.

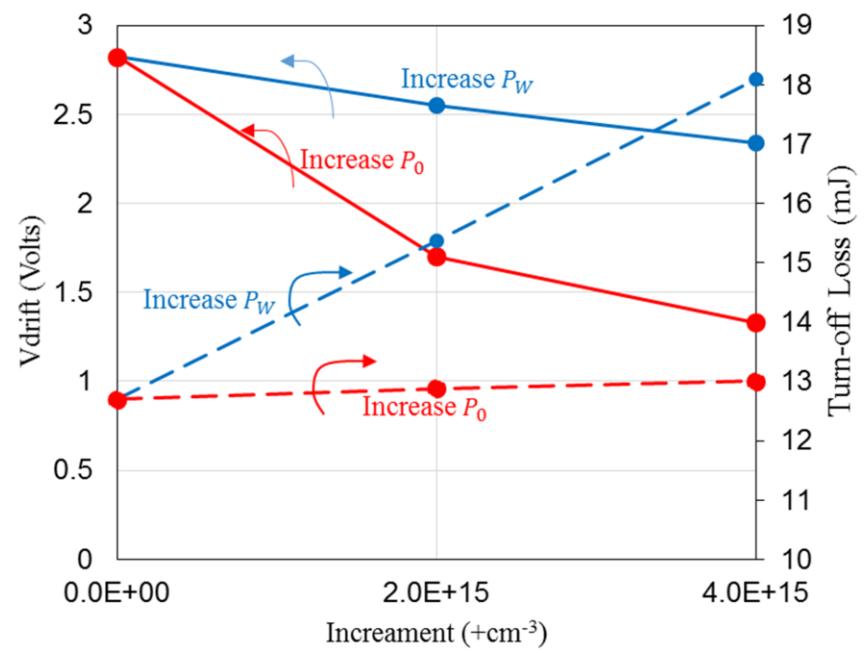


Figure 4-3 Turn-off loss and Vdrift V.S. increment of the boundary carrier densities.

#### 4.1.2 Current enhancement layer

The concept of current enhancement or current spreading layer was first introduced in [37]. The function of the CEL has three folds: (i) facilitates the majority current spreading from the channel. (ii) serve as a hole barrier (kills the PNP gain) (iii) hold back the depletion region from the p-base that will otherwise narrow the JFET region. In [38], it is pointed out that the insertion of CEL can improve up to 30% of conduction loss with a little reduction of BV. For 10kV to 22kV IGBT, the optimized CEL parameter is found to be about 1um thick with  $8\text{E}15$

doping. However, there is still a certain amount of hole current will enter the p-base without coupling with the electron current from the channel to efficiently build up excess carrier density efficiently near the JFET.

#### *4.1.3 Buffer layer optimization*

Buffer layer in a punch-through IGBT serve as a field stop layer as well as a valve to reduce the injection from the emitter. The thickness of the buffer layer should be calculated such that (i) the electric field reaches no farther than 1/10 of the total buffer width at the BV rating and (ii) it is punch through at DC bus voltage. Under these two conditions, the thickness and the doping of the buffer layer can be varied and results in different recombination rates.

However, it is difficult to determine the optimized buffer layer parameters in terms of both switching and conduction loss. This is due to (i) lifetime control techniques in the buffer layer of 4H-SiC are not available or have not been reported (ii) lifetime as a function of the doping, temperature and injection-level (high-level or moderate level injection) in the buffer layer is still unknown. In [12], the optimization of 4H-SiC 20kV pIGBT has been investigated by plotting the trend of parameter variation vs the switching loss (not including conduction loss). It is shown a lightly-doped and thicker buffer layer is preferred if the goal is to reduce switching loss. This is because this type of buffer layer will result in a case in which the ambipolar diffusion length for the minority carrier is much shorter than the buffer layer thickness – meaning more recombination through the buffer layer and therefore less excess carriers. This conclusion is supported in [31], in which 10 um buffer layer has higher voltage drop than the 2um case. Higher voltage drop means less excess carrier in the drift region and faster switching during turn-off.

#### *4.1.4 Drift region optimization avoiding high dv/dt*

It is reported in [16] that different buffer designs all yield high dv/dt in the second phase of turn-off after punch-through even with high gate resistance, and this high dv/dt may cause EMI issue. It is suggested in [17] that the optimum drift region doping and thickness should be the one that is punched through at DC bus voltage. The optimum value suggested in [17] has a  $>4e14 \text{ cm}^{-3}$  doping in a 167 um long drift region, which results in a waveform that avoid the high dv/dt with the cost of higher switching loss than the original design in [39]. In other words, the original design is unfavorable only when the high dv/dt issue is concerned. Therefore, one should look into how to lower this high dv/dt to an acceptable value suggested by the application requirements.

## **4.2 Two-zone drift region for moderate dv/dt**

A 4H-SiC IGBT with two-zone drift region is proposed to limit the high dv/dt below its desired value based on Eq. 3.31. The drift region parameters are co-determined by given maximum dv/dt, breakdown voltage, and punch through voltage.

The switching characteristics of 15kV IGBTs [4] and gate driver circuit have been investigated in [40], suggesting that the second phase of dv/dt cannot be controlled by the gate resistance and depends on the buffer layer parameters. Baliga in [17] suggested that the optimum design to prevent EMI issues should be design the drift region of IGBT to be punch through right at the DC bus voltage. From switching loss point of view, this shape switching waveform actually has smaller loss due to a big chunk of instantaneous power is truncated due to the fast-slow-fast turn-off waveform.

This work propose a two-zone drift region that will have: (a) fast ramping when the depletion region is within Zone 2 that is close to the bipolar emitter, (b) shorter total drift region length and reduction of on-state voltage drop compared to single zone design, and (c) maximum dv/dt that can be designed to be no greater than the desired value.

To achieve at least 15kV blocking capability, 18kV of planar plane blocking voltage is considered with the punch through voltage of 10kV. Figure 4-4 shows that the electric field will terminate at the edge of zone 2 before reaching into buffer layer to avoid high dv/dt.

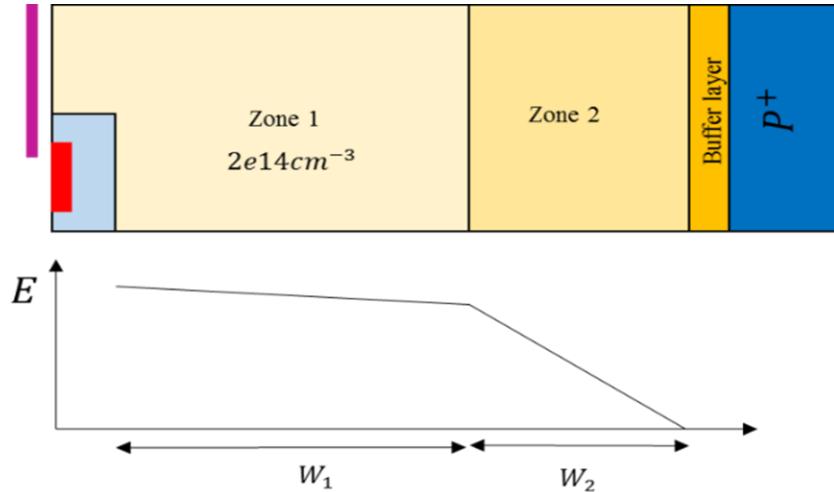


Figure 4-4 Proposed two-zone IGBT. The electric field will be terminated before the maximum voltage rating. Higher doping in zone 2 will result in faster voltage ramping during turn-off.

Noted that in addition to the insertion of zone 2, every design has the same buffer layer with Cree's 15kV n-IGBT. The buffer layer in this design is only for lowering the injection efficiency and providing fast recombination during the current tail phase. According to [13], the optimized carrier density profiles in terms of the switching loss that lead to a "concave up"

voltage ramp is to have a strong injection from the MOS side. Generally speaking, this means that the doping in zone 1 should be kept as low as possible. The doping concentration in zone 1 is then chosen to be  $2\text{e}14\text{cm}^{-3}$ , the lowest value ever reported so far.

The selections of lengths and dopings of the zone1 and zone2 are determined by (a) the desired breakdown voltage of the IGBT (Eq. **Error! Reference source not found.**), (b) the unch through voltage of the IGBT at DC bus voltage (Eq. **Error! Reference source not found.**), and (c) the ion integral equal to unity at breakdown voltage (Eq. **Error! Reference source not found.**).

$$BV = E_C(W_1 + W_2) - m_1 W_1 W_2 - \frac{1}{2} m_1 W_1^2 - \frac{1}{2} m_2 W_2^2 \quad (4.1)$$

where

$$E_C = \frac{BV + \frac{1}{2} m_1 W_1^2 + m_1 W_1 W_2 + \frac{1}{2} m_2 W_2^2}{W_1 + W_2} \quad (4.2)$$

$$V_{pt} = \frac{1}{2} m_2 W_2^2 + m_2 W_1 W_2 + \frac{1}{2} m_1 W_1^2 \quad (4.3)$$

The equation of the Ion Integral along the drift region equals to unity is given by:

$$\int_o^{W_1} C \times E(x)^g + \int_{W_1}^{W_2} C \times E(x)^g = 1 \quad (4.4)$$

, where C and g is given by 4E-48 and 8 [41], respectively. The electric field distribution at breakdown can be expressed in terms of Ec, m1, W1, m2, W2, as specified in **Error! Reference source not found..**

$$\begin{aligned} & \frac{C}{m_1(g+1)} [E_C^{B+1} - (E_C - m_1 W_1)^{B+1}] \\ & + \frac{C}{m_2(g+1)} [(E_C - m_1 W_1)^{B+1} \\ & - (E_C - m_1 W_1 - m_2 W_2)^{B+1}] = 1 \end{aligned} \quad (4.5)$$

m1 and m2 is the sloped of the electric field and are related to doping concentration. Noted that ND1 is fixed at  $2e14\text{cm}^{-3}$ . The slope of the electric field in zone 2 can then be expressed as:

$$m_2 = \frac{V_{PT} - \frac{1}{2}m_1 W_1^2}{\frac{1}{2}W_2^2 + W_1 W_2} \quad (4.6)$$

However, after imposing these three conditions with the corresponding equation Eq. (4.1), Eq. (4.3) and Eq. (4.5), there are still infinite combinations of ( $W_1, W_2, N_{D2}$ ). Table 1 lists the 5 possible combination of parameters in zone 1 and zone 2, all of which have the same breakdown voltage and punch through exactly at 10kV. Figure 4-5 plots the distribution of the electric field at 1500kV. Figure 4-6 shows that the devicse with higher doping in zone 2 has larger dv/dt at higher collector voltage and smaller turn-off loss.

Table 4.1 Combinations of the parameters in the two-zone drift region.

|                      | $W_1(\mu\text{m})$ | $N_{D1}(\text{cm}^{-3})$ | $W_2(\mu\text{m})$ | $N_{D2}(\text{cm}^{-3})$ |
|----------------------|--------------------|--------------------------|--------------------|--------------------------|
| Device A             | 171                | 3.6E14                   | N/A                | N/A                      |
| Device B             | 80                 | 2e14                     | 79                 | 4.95e14                  |
| Device C             | 100                | 2e14                     | 57                 | 5.9e14                   |
| Device D             | 120                | 2e14                     | 33                 | 8.6e14                   |
| Device E             | 130                | 2e14                     | 21                 | 1.23e15                  |
| Device F             | 140.5              | 2e14                     | 9                  | 2.58e15                  |
| Cree's 15kV n - IGBT | 140                | 2e14                     | 5                  | 2e16                     |

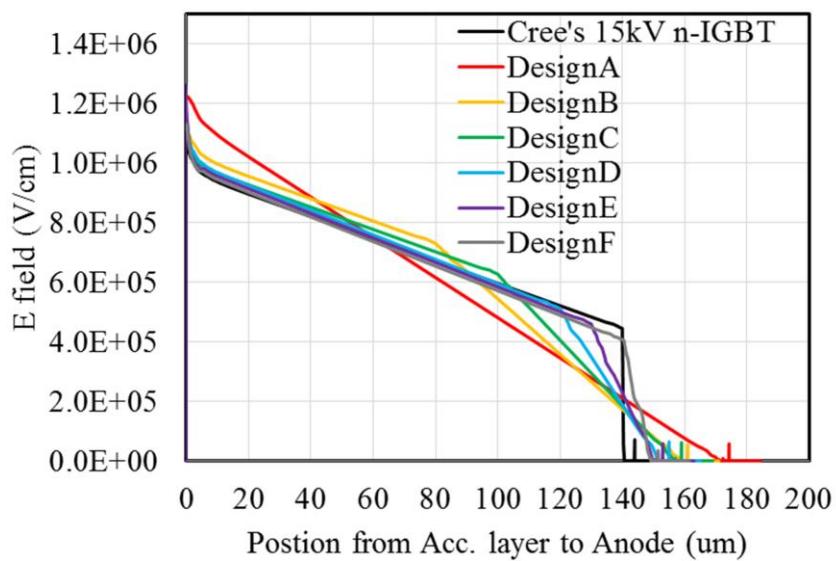


Figure 4-5 Different electric fields of five combination of drift region parameters at 8kV.

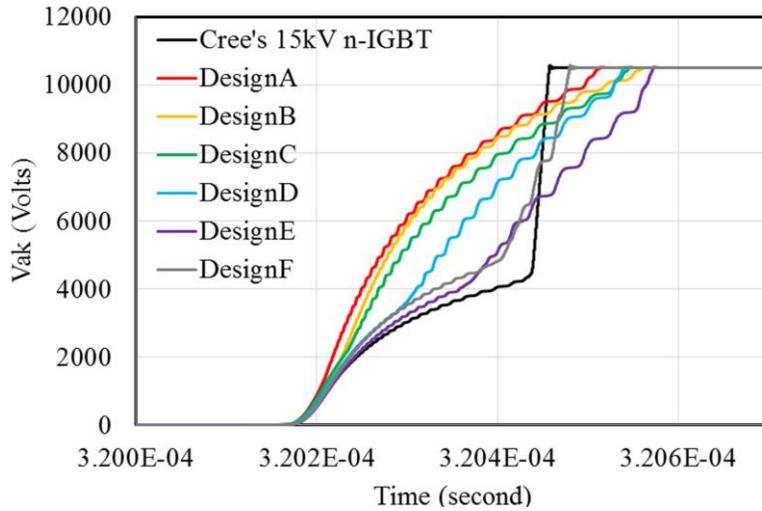


Figure 4-6 Turn-off waveforms of different drift region designs.

In fact, there is another restriction to be imposed in order to have an exact combination of the drift region parameter – the maximum allowable  $dv/dt$  in different applications. The  $dv/dt$  right before the punch through is given by:

$$\frac{dV}{dt}_{V \rightarrow V_{pt}} \approx \frac{J_T}{[(C_{gd}(V_{pt}) + C_{ds}(V_{pt})] \frac{b}{1+b} \frac{\lambda_W}{1+\lambda_W}} \quad (4.7)$$

, where  $\lambda_W = N_{D2}/p_W$ . If  $\lambda_W \ll 1$ ,  $dv/dt$  will be small. If  $\lambda_W \approx 1$ ,  $dv/dt$  will be much larger. For example, if the maximum allowable  $dv/dt$  for a system is  $100\text{kV}/\mu\text{s}$ , then  $N_{D2}/p_W$  has to be no bigger than 0.1. A reasonable  $p_w$  at the current density of  $30\sim50\text{A}/\text{cm}^2$  should be between  $5\text{E}15\sim1\text{E}16 \text{ cm}^{-3}$ , which gives the range of  $N_{D2}$  in the range between  $1\text{E}15 \sim 2\text{E}15$ .

Figure 4-7 plots the  $E_{off}$ - $V_{ce,sat}$  trade-off curve for all the designs discussed above. Cree's Design has the best trade-off with the highest  $dv/dt$ . The design F, with the exactly the same structure except for the additional 9  $\mu m$  zone 2, has a  $dv/dt$  only 1/3 of Cree's design, while still maintaining good  $E_{off}$ - $V_{ce,sat}$  trade-off. Single zone design, although the  $dv/dt$  is very small, has largest  $E_{off}$  with reasonable  $V_{ce}$ .

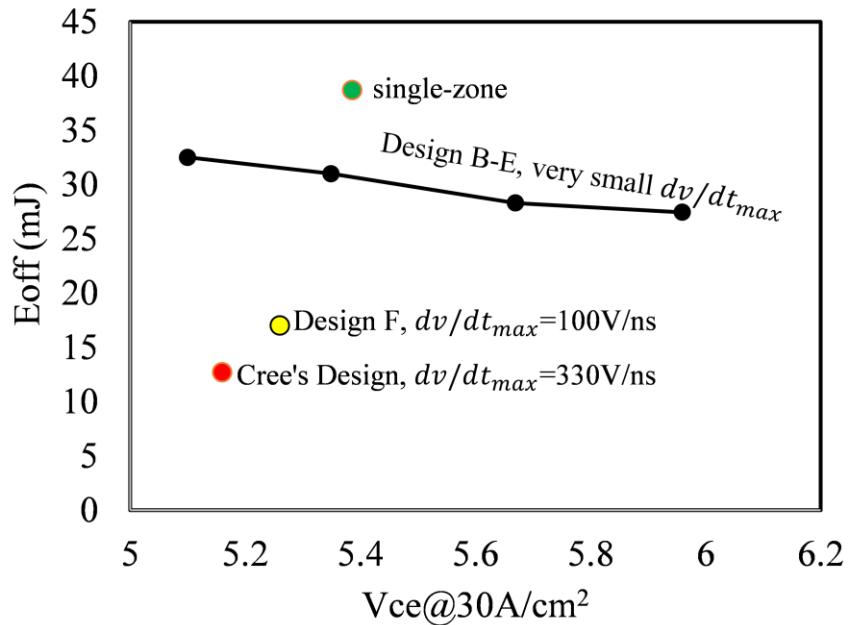


Figure 4-7  $E_{off} - V_{ce,sat}$  trade-off curve for different designs of drift region.

# Chapter 5

## 4H-SiC p-GTO

### 5.1 Introduction of 4H-SiC p-GTO

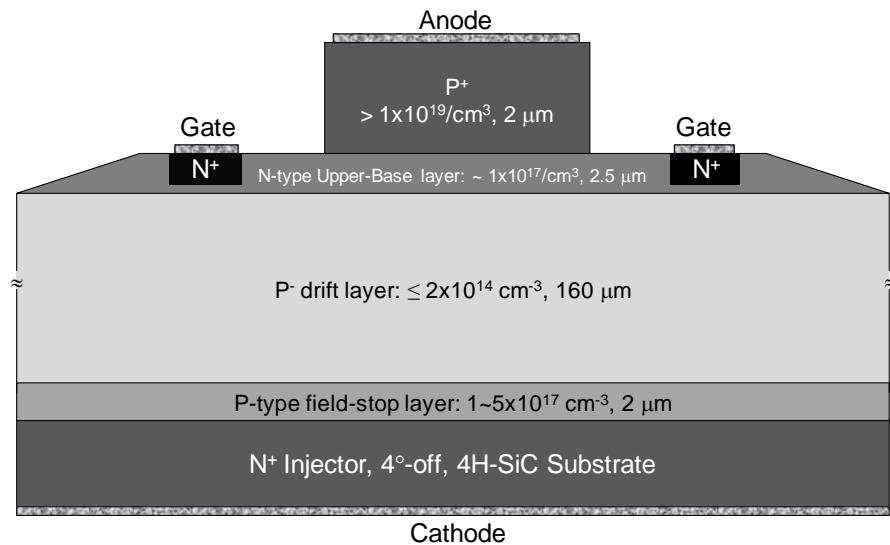


Figure 5-1 Cross section of a 22kV 4H-SiC p-GTO.

Gate turn-off thyristor is a gate-controlled four-layered switches that is suitable for high power and medium to low frequency applications. It can be turned on by applying a gate signal to turn on the p-n junction closer to the Anode, triggering the regeneration action so that the device can stay on by just providing a small amount of holding current from the gate. It can be turn-off by diverting a portion of total current through the gate, disturbing the regeneration

action and finally turn-off the device. GTO can also be configured into an Emitter Turn-off Thyristor (ETO) [42], which has a faster switching speed because of the unity gain turn-off.

The advantages of GTO, compared to IGBT, is that there is no inverted channel within the structure, in which the mobility has been an issue for 4H-SiC materials. In addition, due to the latch-up phenomenon and the absence of JFET region, the injection is stronger from the gate side than that in IGBT. This leads to a much lower voltage drop during on-state compared to IGBT, making GTO a more attractive candidate in high power applications. Due to the superior material properties, 4H-SiC GTO have been developed over the decade [43, 44]. Figure 5-1 shows the cross section of the latest 22kV 4H-SiC p-GTO developed by CREE.

Although its great potential in the application such as HVDC and FACTS, very few SiC thyristor device models for circuit simulation developed so far [45, 46] especially for the voltage range that SiC thyristors are predicted to be dominated in. In silicon world, lumped charge modeling techniques have been employed to build GTO models [47]. However, as discussed earlier, using only three nodes to describe the carrier dynamic in a long drift region is insufficient. The proposed p-GTO model for circuit simulation will have the following features:

- (I ) Include the effect of carrier density profile.
- (II) Accurate predictions of waveforms for both turn-on and turn-off.
- (III) Easy and systematic parameter extraction.
- (III) Fast computational speed.

## 5.2 N-type and p-type ambipolar transistors

Before delved into the discussion and the development of p-ETO model, it is of interest to discuss the fundamental difference between n- and p-type ambipolar transistors. Due to the quality of the 4H-SiC n-type substrate [4], p-type devices have been the focus for the GTO device technology. Regardless of the substrate issue, it has been discussed in [3] that n-channel IGBTs are superior to the p-channel ones in terms of both conducting and switching speed. The difference between n-type and p-type ambipolar transistors will be discussed in this section in terms of stored charge and turn-off speed.

### 5.2.1 *Injection capability between n-type and p-type devices*

In [3], it is pointed out that the injection efficiency alone is insufficient to estimate the charge stored in the drift region. For example, 4H-SiC n-IGBTs typically has an injection efficiency of around 0.12 compared to the p-IGBT of 0.91. However, n-IGBT stores more charge at given current density than that in p-IGBT.

Eq. (5.1) and (5.2) [3, 11] are the boundary minority carrier density at drift/buffer junction in the drift region for n-IGBT and p-IGBT, respectively.

$$p_W = \frac{r_{En}' L \tanh(W/L)}{2qD_p} J_T \quad (5.1)$$

$$n_W = \frac{r_{Ep}' L \tanh(W/L)}{2qD_n} J_T \quad (5.2)$$

, with  $\gamma_{En} = r_{En}(1 + 1/b) - 1/b$  and  $r_{Ep}' = \gamma_{Ep}(1 + b) - b$

By integrating Eq. (5.1) and (5.2) along the drift region, the charge stored in the drift region at given current density for n-IGBT and p-IGBT are given by:

$$\begin{aligned} Q_h &= \frac{b}{1+b} J_T \tau_{HL} r_{En}' \tanh\left(\frac{W_B}{L}\right) \tanh\left(\frac{W_B}{2L}\right) \\ &= (\gamma_{En} - \gamma_{En_{min}}) J_T \tau_{HL} \left(1 - \frac{1}{\cosh\left(\frac{W_B}{L}\right)}\right) \end{aligned} \quad (5.3)$$

$$\begin{aligned} Q_e &= \frac{1}{1+b} J_T \tau_{HL} r_{Ep}' \tanh\left(\frac{W_B}{L}\right) \tanh\left(\frac{W_B}{2L}\right) \\ &= (\gamma_{Ep} - \gamma_{Ep_{min}}) J_T \tau_{HL} \left(1 - \frac{1}{\cosh\left(\frac{W_B}{L}\right)}\right) \end{aligned} \quad (5.4)$$

, where  $\gamma_{En,min}$  and  $\gamma_{Ep,min}$  are the theoretical minimum value of the injection efficiency for n- nad p-type ambipolar devices and are given by  $1/(1+b)$  and  $b/(1+b)$ , respectively. The constant b is the ratio between electron and hole mobility and is around the value of 7.7 for 4H-SiC. The injection capability is defined as the difference between the injection efficiency and its minimum value ( $\gamma_E - \gamma_{Emin}$ ). It is worth pointing out that the minimum injection

efficiency of p-IGBT, for example, is 0.885. This means that, even if a 4H-SiC p-IGBT has an injection efficiency of 0.9, which is close to unity, the injection capability of this device is little since the difference to its minimum value is only 0.005. On the other hand, for n-IGBT, the injection efficiency of 0.2 will have an injection capability of about 0.085, which is much larger than that of p-IGBT.

A 15kV p-IGBT model in Simulink was built to directly compare with n-IGBT. The injection efficiency of the p-IGBT model is tuned such that the storage charge is the same at given current density as it is in n-IGBT, as shown in Figure 5-2. It can be seen that, in order to achieve the same stored charge, or the same injection capability, the injection efficiency of p-IGBT has to be a lot of higher than that of n-IGBT.

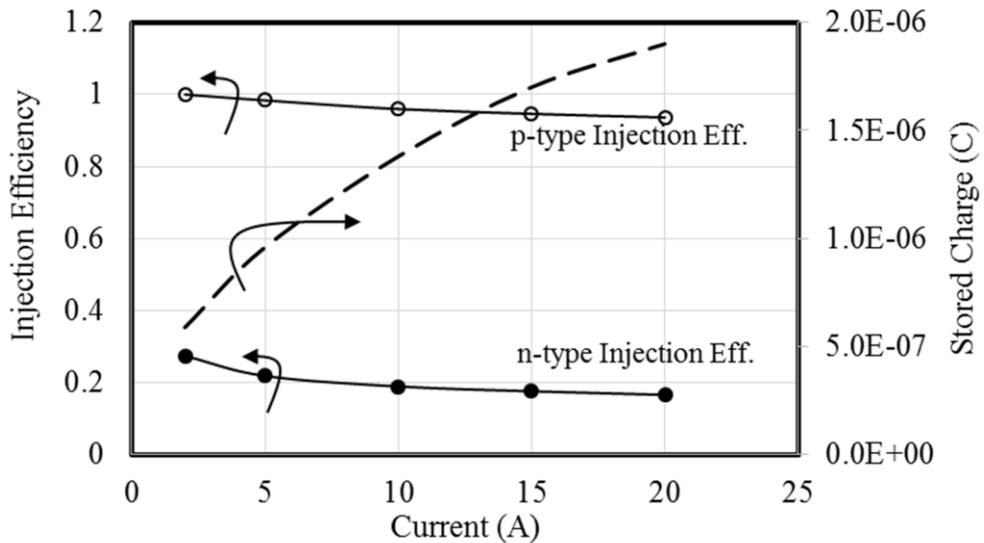


Figure 5-2 Injection efficiency function of n- and p-IGBT that will result in the same stored charge at given current.

### 5.2.2 Turn-off speed between n-type and p-type devices

The physics that determines turn-off speed involves a lot of factors and can be less straightforward than ambipolar ones. In [3], an analytical manner is provided by using the injection efficiency and the charge continuity equation. The changing rate of the minority carriers during the turn-off is given by:

$$\frac{dQ_m}{dt} = -\frac{Q_m}{\tau_D} + I_{min} - I_{mout} \quad (5.5)$$

Eq. (5.5) can be rewritten by ignoring the displacement current and the minority current that goes into the drift region is approximately the total terminal current:

$$\frac{dQ_m}{dt} = -\frac{Q_m}{\tau_D} - I_T(1 - \gamma_E)$$

Since for n-type devices, the injection efficiency is much smaller than that for p-type ones, the charge removal rate is expected to be larger for n-type than for p-type devices during inductive turn-off.

A more direct way of determining the switching speed is to run the simulation in Simulink/Matlab. Figure 5-3 is the simulated turn-off voltage waveform for 15kV 4H-SiC n-IGBT with same amount of initial stored charge. In order to have the same conductivity modulation for p-IGBT, the speed of the p-IGBT is 8 times slower than that of n-IGBT. From Figure 5-2 and Figure 5-3, it can be concluded that n-type transistors are better than p-type ones in terms of conductivity modulation and the switching speed.

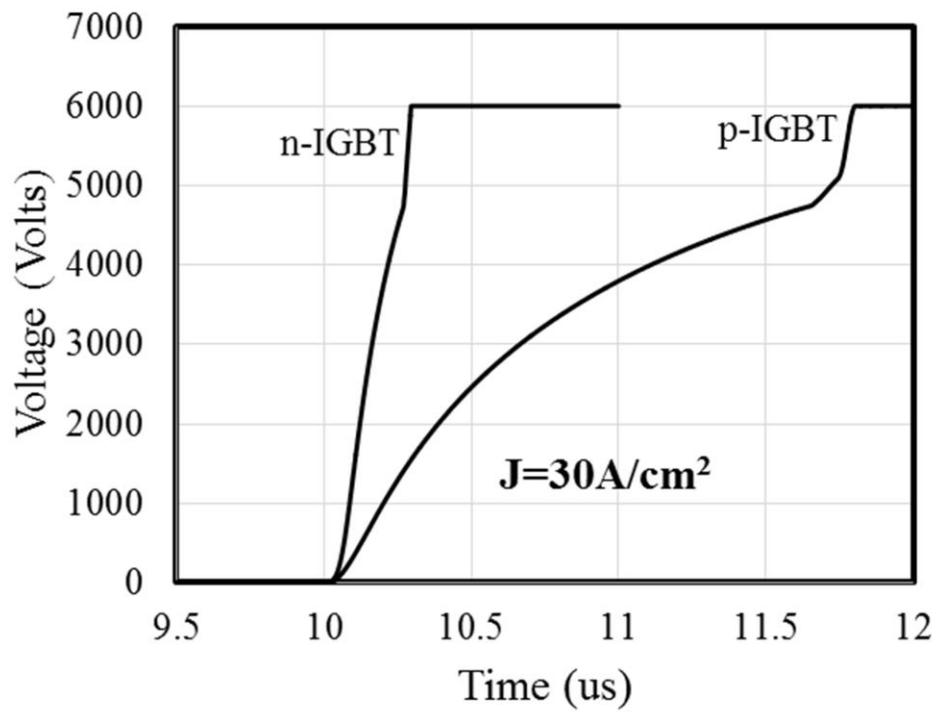


Figure 5-3 The inductive turn-off for n- and p-IGBT with the same amount of stored charge.

### 5.3 Developing sub-circuit p-GTO model

The sub-circuit model of the proposed GTO model will be modified from the proposed IGBT model. From the equivalent circuit shown in Figure 5-3Figure 5-4, one can see that GTO consists of two complementary BJTs with long drift region; while for IGBT, the internal MOSFET provide base current to drive the BJT with long drift region.

Figure 5-5 shows the proposed SiC p-GTO model in Simulink. Two internal BJT structures in p-GTO are providing each other the base current, and this is known as the regenerate event. The total amount of current of  $I_{pp}$  and  $i_{dsj}$  determines the amount of charge stored in the drift region calculated in  $Q_{nb}$ . The total amount of the current of  $I_C$ ,  $i_q$  and  $i_{dsj}$  determine the charge amount stored in the base region of the PNP transistor calculated in  $Q_{pb}$ .

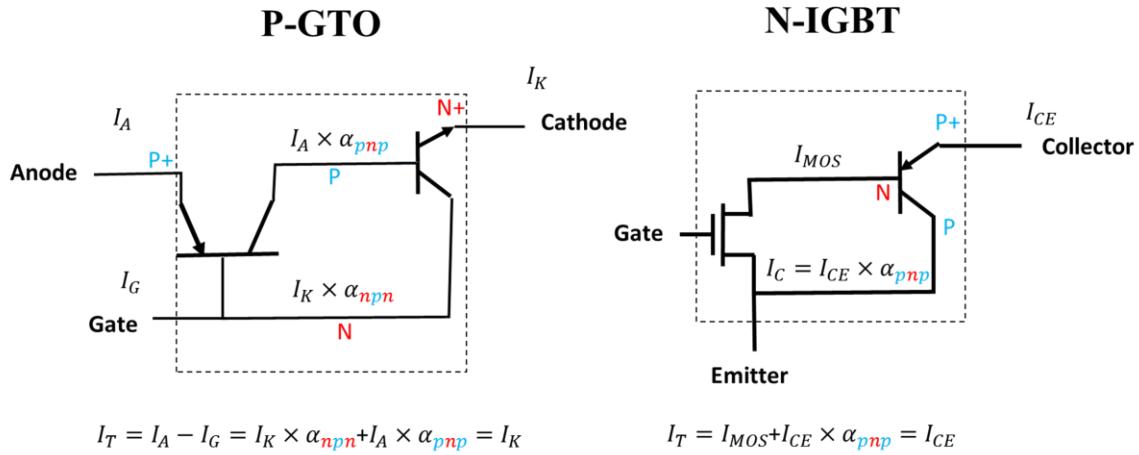


Figure 5-4 Equivalent circuit for p-GTO and n-IGBT.

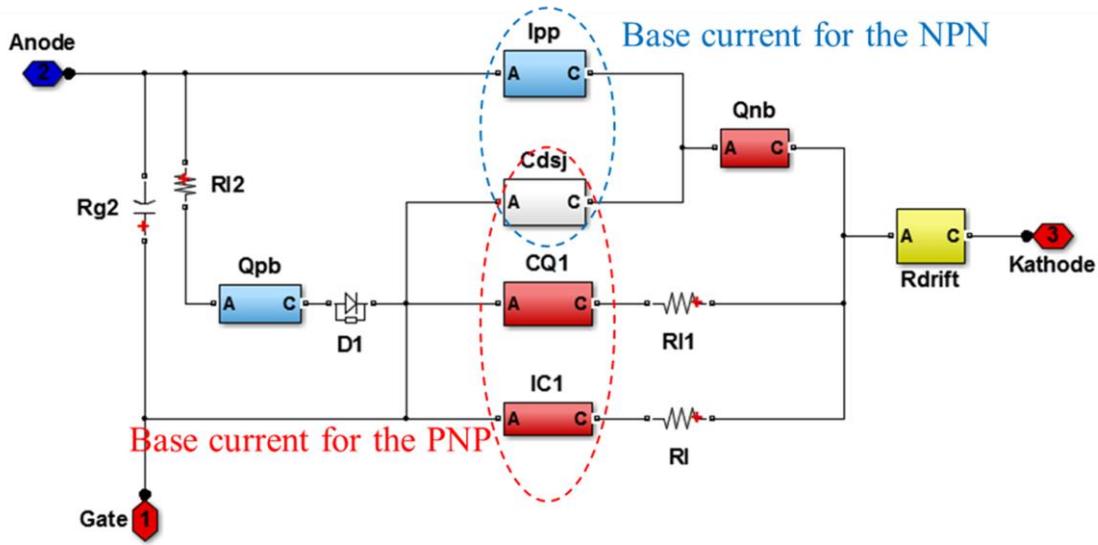


Figure 5-5 4H-SiC p-GTO model implemented in Simulink/Matlab.

The steady state base current  $I_{pp}$  is determined by the charge of  $Q_{pb}$  and is approximated by:

$$I_{pp} = D_{pb} \frac{2Q_{pb}}{AW_{NB}} \quad (5.6)$$

, where  $W_{NB}$  is the thickness of the n-type base layer. The stored charge denoted as  $Q_{nb}$  and  $Q_{pb}$  are calculated by detecting the current (a.k.a base current) flowing through the blocks. The charge  $Q_{nb}$  consists of the charge  $Q_D$  in the drift region and  $Q_B$  in the p-buffer layer. They can be calculated in the same manner as discussed in Chapter 3. The charge  $Q_{pb}$  is given by:

$$\frac{dQ_{pb}}{dt} = -\frac{Q_{pb}}{\tau_{pb}} - q \times h_n \times P_b \times \frac{Q_{pb}}{q \times W_{NB} \times A} + I_C \quad (5.7)$$

The first term in Eq. (5.7) accounts for the recombination and the second term accounts for the back injection into the P+ anode. The current  $I_C$  consists of the current from the steady-state  $I_C$  and the charge removal current  $I_Q$ , as shown in Figure 5-5. This equation can be further reduced to Eq. (5.8) for the sake of simpler parameter extraction procedure.

$$\frac{dQ_{pb}}{dt} = -\frac{Q_{pb}}{\tau_{pb}'} + I_C \quad (5.8)$$

, where  $\tau_{pb}'$  consists of the recombination in the buffer layer and the back injection into the P+ anode.

The turn-on procedure in this model is described as the following: (i) small amount of the gate current is provided to charge  $Q_{pb}$  (at this moment the NPN BJT is still off) (ii)  $I_{pp}$  will be activated by the presence of  $Q_{pb}$  given by Eq. (5.6). (iii) the current  $I_{pp}$  will serve as the based current to charge the PNP BJT and  $Q_{nb}$  start to increase (iv) the current  $I_C$  will be activated by the presence of  $Q_{nb}$  (v) the current  $I_C$  will start to serve as the base current of NPN BJT to charge  $Q_{pb}$ , and the gate current can be kept small due to the regeneration action.

## 5.4 Parameter Extractions and model validation

Figure 5-6 is the flow chart of the parameter extraction procedure. The procedure is similar to the one for IGBT model except for the last step – effective lifetime in the upper base region.

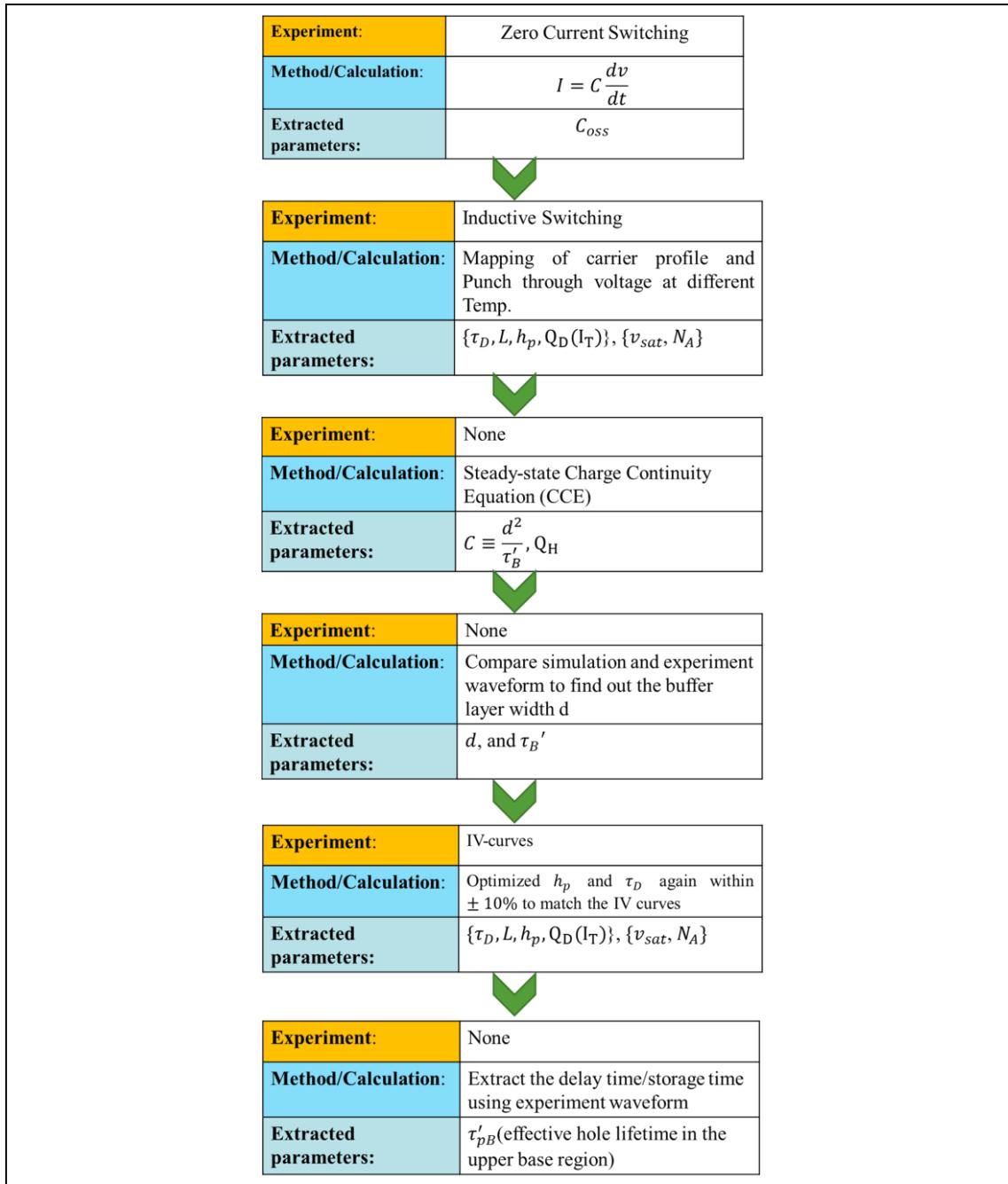


Figure 5-6 Proposed parameter extraction procedure for 4H-SiC GTO. There are six steps and only requires two experiments.

However, for GTO, there is no JFET region and the carrier density is more 1-D than that in IGBT. The carrier density will be higher near the anode of the p-GTO, which leads to longer delay time than that compared to IGBT. The charge storage time, the time delay after the gate is turned off and before the voltage starts to rise, will be used to extract the parameters in the upper base region shown in Figure 5-1.

#### *5.4.1 Evaluate the accuracy of the ECDM near the upper base region*

In GTO, carrier injection near the upper base region can be as strong as it is near the emitter. This part of excess carrier will determine largely the charge storage time as well as the  $V_{ce,sat}$ . Therefore, it is important to investigate whether the proposed ECDM (Excess Carrier Distribution Mapping) technique is capable of making good prediction for the carrier profile at the region near the upper base.

TCAD simulation is used in order to directly verify the calculated and simulated carrier profile. Two SiC p-GTO with different injection capability are simulated in the TCAD and were switched at the current density of  $30A/cm^2$ . Figure 5-7 shows the voltage ramping for two p-GTOs before punch-through. Figure 5-8 are the results of the ECDM and the simulated profile. It can be seen that the carrier concentration is slightly overestimated near the emitter (cathode) and underestimated toward the anode. The discrepancies between the simulation and the calculation may result from the fact that the ECDM technique ignores the diffusion current as discussed earlier in Chapter 3.

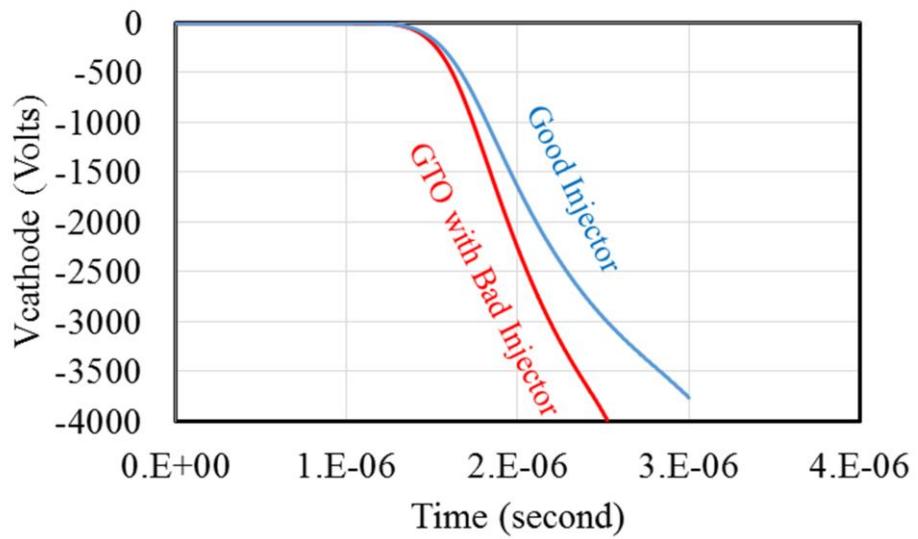


Figure 5-7 The inductive turn-off of two p-GTO with different injection efficiency are simulated in TCAD. Current density is  $30\text{A}/\text{cm}^2$ .

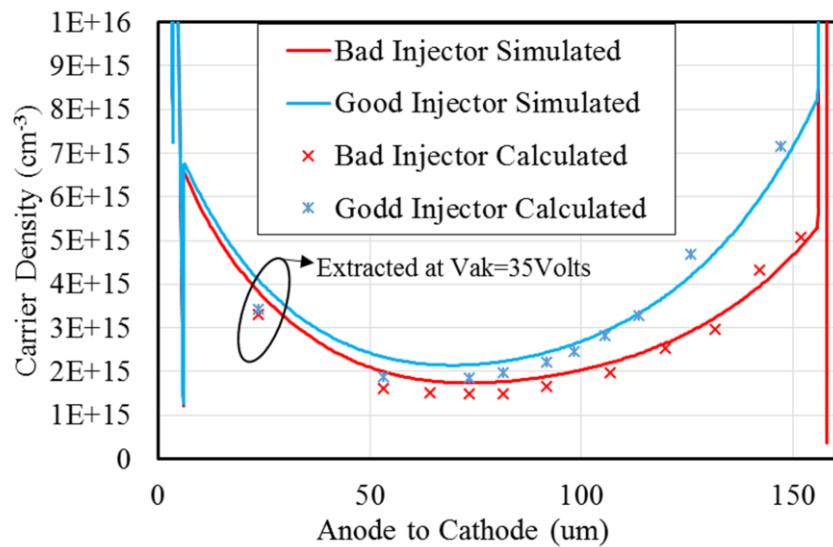


Figure 5-8 Extracted carrier density profile using the proposed ECDM technique.

There are two limitation of the proposed technique. Firstly, the leftmost data points are extracted at the voltage of 35 Volts. In reality, it is very difficult to extract the slope at this low voltage, as the measured waveform shown in Figure 5-9.

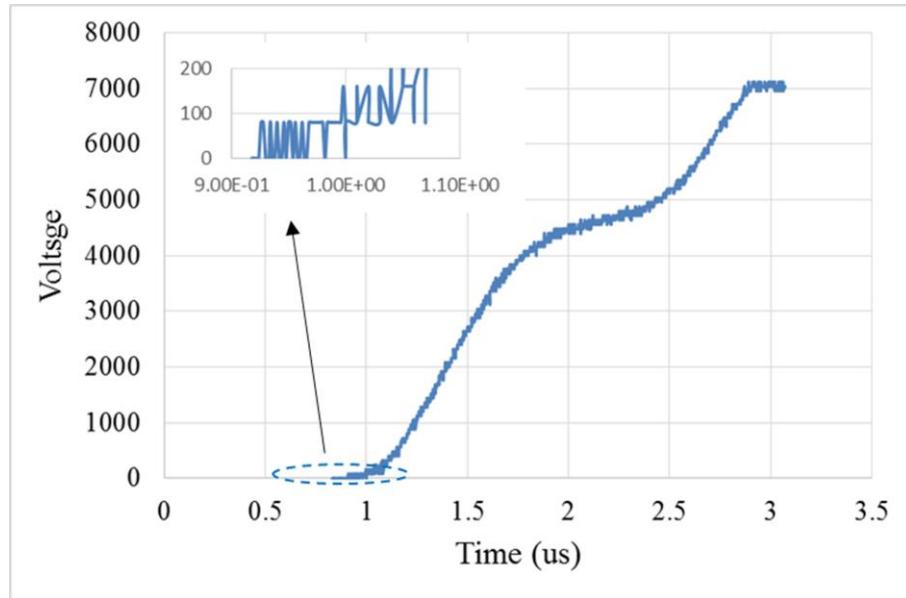


Figure 5-9 Switching waveform zoom-in at low voltage range.

Another limitation for the resolution of the ECDM is set by the model itself when describing the retreating of the excess carrier as the depletion region is expanding. Figure 5-10 illustrates the carrier dynamics during the GTO turn-off. Not until the moment of  $t_2$  will the voltage start to rise. Figure 5-11 depicts how the dynamic of excess carrier is being calculated in the proposed model as well as the ECDM procedure. During the removal of the excess near  $x=0 \mu\text{m}$ , the  $\frac{dv}{dt}$  remain nearly zero since there is no formation of the depletion region. Therefore, the leftmost carrier concentration that can be extracted start after  $t_2$ .

Therefore, The proposed ECDM technique cannot directly obtain the carrier density at  $x=0$ ,  $n_0$ , since  $dv/dt$  is zero. It is, however, possible to extrapolate the profile back to  $x=0$  to estimate  $n_0$  if assuming (1) lifetime is uniform and (2) no 2-D effect regarding the current flow. It is worth to mention that the proposed model somehow include the charge stored time by the “if statement” shown in Figure 5-11. Before  $X' < 0 \mu\text{m}$ , or before  $t_2$  (also known as delay time), the if statement makes sure the voltage due to the charging of output capacitance is zero.

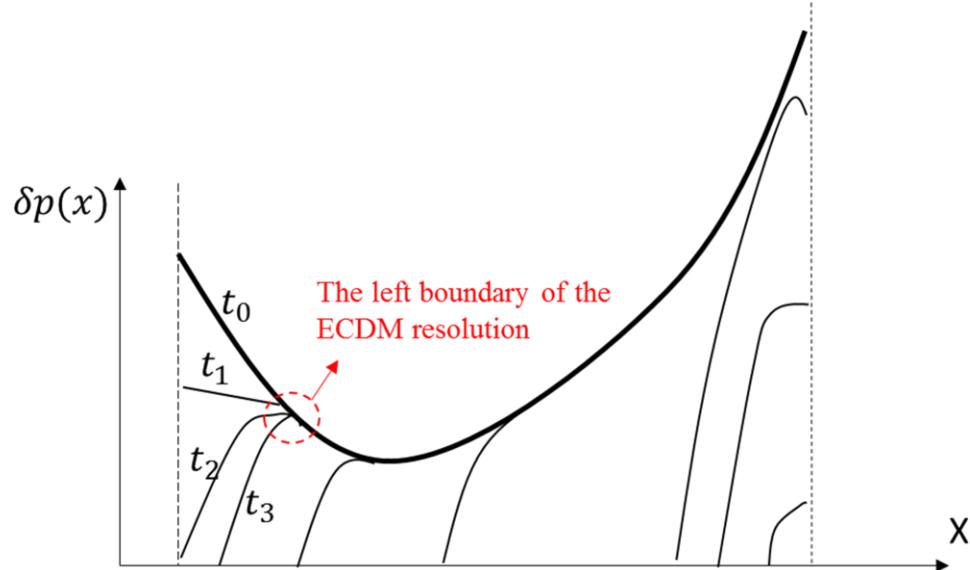
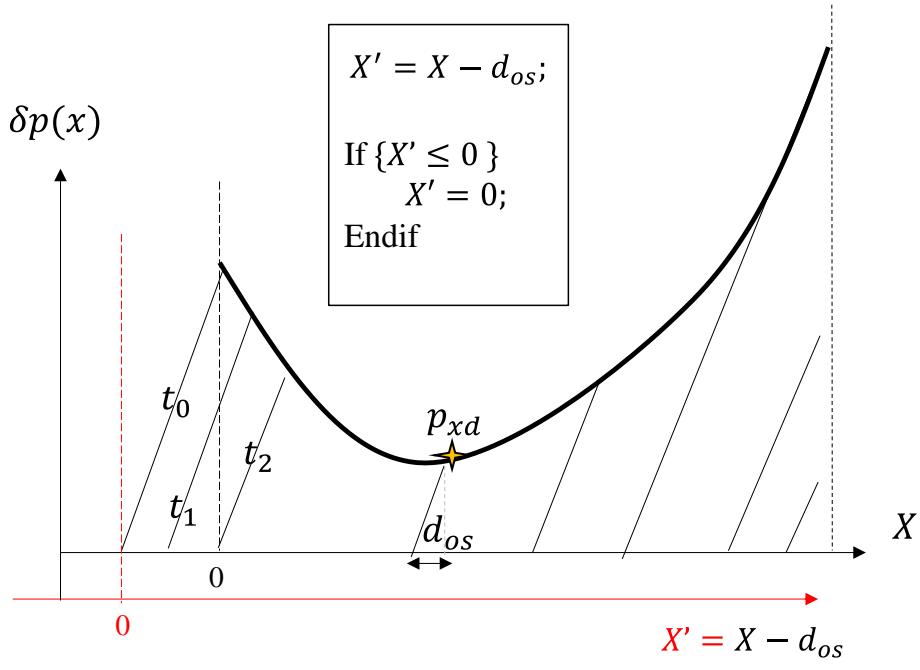


Figure 5-10 The depiction of the dynamic of excess carrier during turn-off.



\*  $X$ : Location of the tip of the carrier concentration

\*  $X'$ : Location of the depletion boundary

\*  $d_{os}$ : Offset length

Figure 5-11 A model describing the carrier dynamic during switching. A slice of local excess charge with a tilted rectangular shape is being removed at each time step.

#### 5.4.2 Effective high level lifetime $\tau_{D,eff}$ and $h_p$

After extracting the output capacitance of the p-GTO (not discussed), the second step is to obtain the high level lifetime in the drift region by using the proposed direct carrier profile mapping technique. After mapping the carrier density at several position, it is found that for this 4H-SiC pGTO, the carrier density profile cannot be matched using single lifetime. The reason might be the 5 hour lifetime enhancement process [44] is not effective throughout the long drift region. According to the original research [48] of the lifetime enhancement using high temperature oxidation, five hour treatment would only reach 50 $\mu\text{m}$  from the surface. To

deal with the non-uniformity of the lifetime and the corresponding carrier density profile, the proposed model uses an effective lifetime, such that the corresponding uniform carrier density results in the same amount of charge, as shown in Figure 5-12.

The ECDM result can also be used to have an initial estimation of the excess carrier concentration at  $x=0$  um,  $n_0$ . The parameter  $h_p$  that describe the relationship between the current density and the injected carrier concentration from the upper base can be used to extract  $h_p$ :

$$n_0 \approx \sqrt{\frac{I_T \times \frac{1}{1+b}}{q \times h_p}} \quad (5.9)$$

The extracted  $h_p$  here will be optimized again while conducting the IV curve fitting.

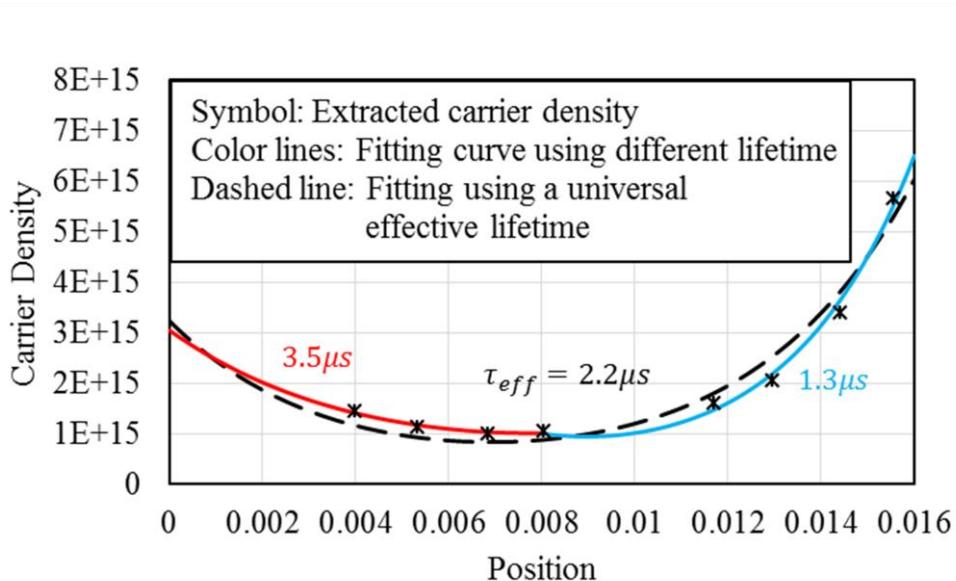


Figure 5-12 The extracted carrier profile using ECDM technique and the fitted curve using different lifetime.

### 5.4.3 $d^2/\tau_B'$ , $Q_H$ and $d$

The extraction procedure is similar to the one discussed in the proposed IGBT model and its parameter extraction procedure. The only difference is that the polarity of the device. The lumped parameter  $C \equiv \frac{d^2}{\tau_B'}$  and  $Q_H$  can be obtained by solving two steady-state CCE at different current. The steady-state CCE states that:

$$\frac{dQ_T}{dt} \equiv 0 = -\frac{Q_D}{\tau_D} - \frac{Q_B}{\tau_B'} + I_{bss} \quad (5.10)$$

The buffer layer excess charge  $Q_B$  can be expressed in terms of  $Q_D$  and total current  $I_T$  by using Boltzmann junction law and is given by:

$$Q_B = \frac{Q_D^2}{Q_H} \left( \frac{d}{L\alpha} \right)^2 + \frac{d^2}{2D_{nb}} \frac{I_T \times b}{1+b} \quad (5.11)$$

, where

$$\alpha = \frac{\cosh\left(\frac{W}{L}\right) - \cosh\left(\frac{W-x_d}{L}\right)}{\sinh(W/L)} \quad (5.12)$$

The steady-state base current in Eq. (5.10),  $I_{bss}$  is approximated to be  $1/(1+b) \times I_T$  for the parameter extraction purpose.

Eq. (5.10) can now be rewritten as:

$$\frac{1}{1+b} \times I_T = \frac{QD}{\tau H} + C \left[ \frac{QD^2}{\tau H} \left( \frac{1}{L\alpha} \right)^2 + \frac{IT \times b}{2Dnb(1+b)} \right] \quad (5.13)$$

, where  $C$  is a lumped parameter and is defined as  $d^2/\tau_{B'}$ . The only two unknowns –  $Q_H$  and  $C$  – can be obtained by solving Eq. (5.13) at different current.  $Q_D$  at different current level can be obtained by using the proposed ECDM technique.

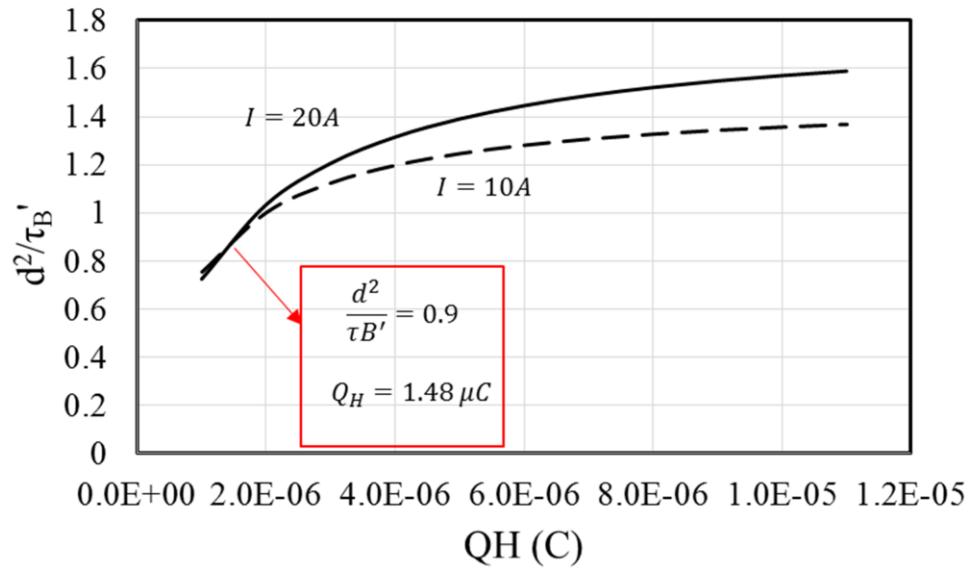


Figure 5-13 Extract  $C$  and  $Q_H$  using the curve generated at two different current. The cross point is point that satisfies Eq. (5.13) at different current level.

#### 5.4.4 Effective N-base lifetime

The n-base lifetime can be extracted by using the delay time – the duration after the gate is turned off and before voltage starts to rise. Noted that  $h_p$  in Eq. (5.9) and the n-base lifetime  $\tau_{Bn}$  together determines the delay time. Since  $h_p$  is extracted in the previous step, the n-base lifetime can be obtained by finding the value that matches the measured delay time.

#### 5.4.4 Extracted parameters

Table 5.1 Extracted parameter inputs of the proposed model at different temperatures.

|   |                    |             |
|---|--------------------|-------------|
| Chip size   | $A_{chip}(cm^2)$   | 2           |
| Active Area   | $A_{active}(cm^2)$ | 0.53        |
| Drift region width                                    | $W_D(\mu m)$       | 160         |
| Buffer layer width                                    | $d(\mu m)$         | 3           |
| Drift region doping                                   | $N_D(cm^{-3})$     | $1.84E14$   |
| Buffer layer dose                                     | $Q_B(cm^{-2})$     | $1.7E13$    |
| Ambipolar lifetime in the drift region                | $\tau_D(\mu s)$    | 1.3/3.5     |
| Effective minority lifetime in the buffer             | $\tau_B'(\mu s)$   | 0.129       |
| Minority lifetime in the upper base region            | $\tau_{Bn}(\mu s)$ | 0.07        |
| Effective electron saturation velocity at 25°C        | $v_{sat,n}(v/cm)$  | $1.33E7$    |
| Recombination constant at upper base junction at 25°C | $h_p(cm^4/s)$      | $1.5E - 12$ |

## 5.5 Model Validation

### 5.5.1 Steady-state IV curve

Figure 5-14 shows the simulated results match well with the measurement even at high current range. This is due partially to the model taking into account the injection from the anode of the p-GTO. In addition, the proposed ECDM technique allows more direct insight of the excess carrier level near the anode.

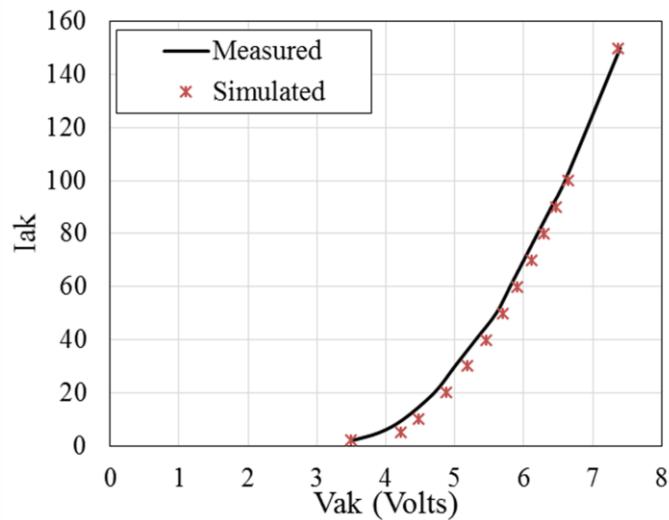


Figure 5-14 Simulated and measured IV curve for 15kV p-GTO at 25°C.

### 5.5.2 Switching Transient validation

It has been shown in Figure 5-12 that the lifetime is higher close to the surface and lower from the middle to the cathode. Even the steady-state IV curve can be matched using a constant effective lifetime throughout the drift region, it is found that this simplification will cause some disagreement between the simulated and measured waveforms despite with the same total turn-off time, as show in Figure 5-15. The switching is simulated using the proposed GTO model in the ETO configuration. The simulated dv/dt is slower and then faster compared to the measurement.

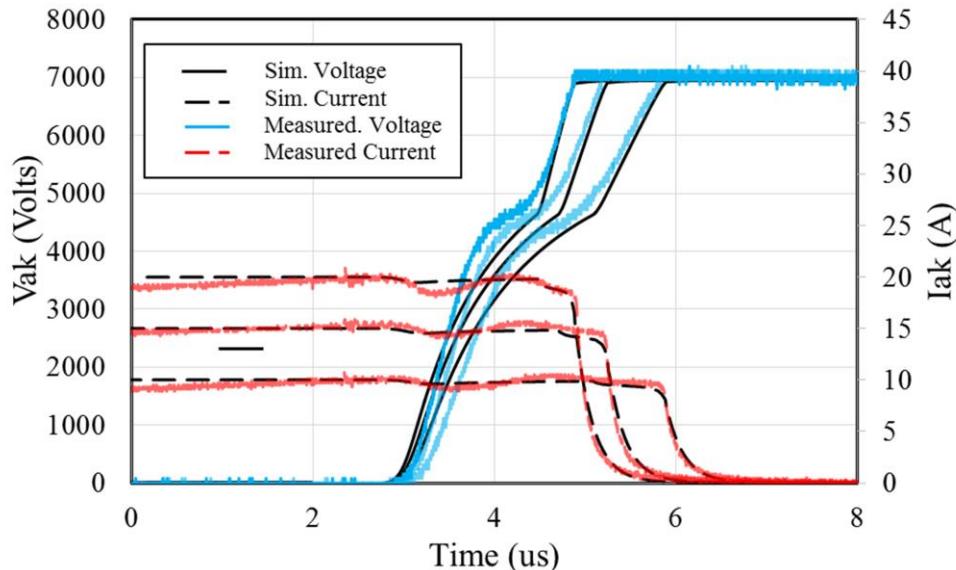


Figure 5-15 Measured versus simulated turn-off waveforms at different current level. The ambipolar lifetime of  $2.2 \mu\text{s}$  is used throughout the drift region.

A solution to this discrepancy is to have an if-else statement in the simulator, so that the lifetime will change once the depletion region expands beyond certain point. Figure 5-16 shows again the simulated waveforms after adding the so called – two zone correction. The proposed model not only takes into account the injection from both sides of the device, but also the non-homogeneous lifetime distribution, if any.

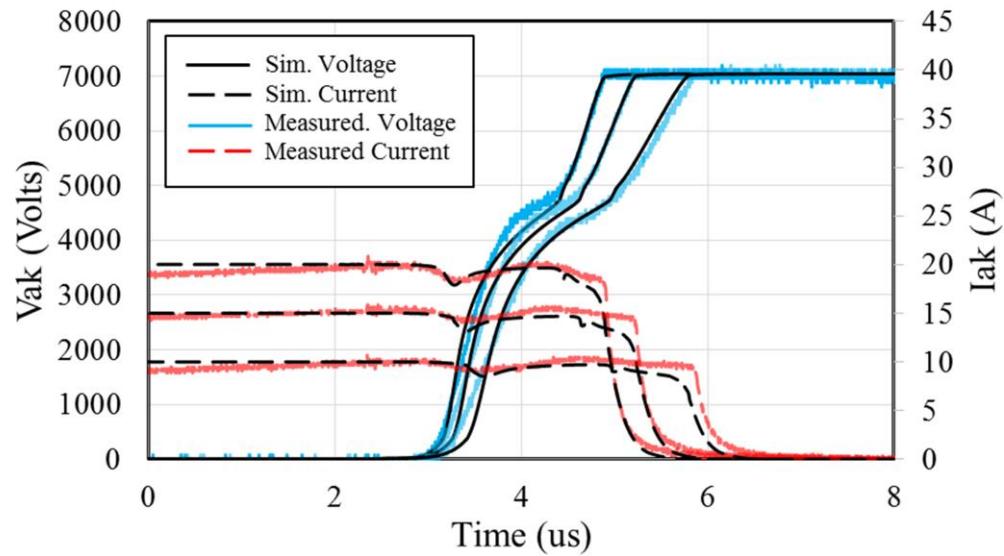


Figure 5-16 Measured versus simulated turn-off waveforms at different current level. The ambipolar lifetime of  $3.5 \mu\text{s}$  is used near the surface and  $1.5 \mu\text{s}$  is used closed to the cathode.

The  $E_{\text{off}}$  as a function of current is plotted in Figure 5-18, showing that the model predicts the loss better if including the two-zone correction. Figure 5-17 compares the switching loss as a function of current between n-IGBT and p-GTO.

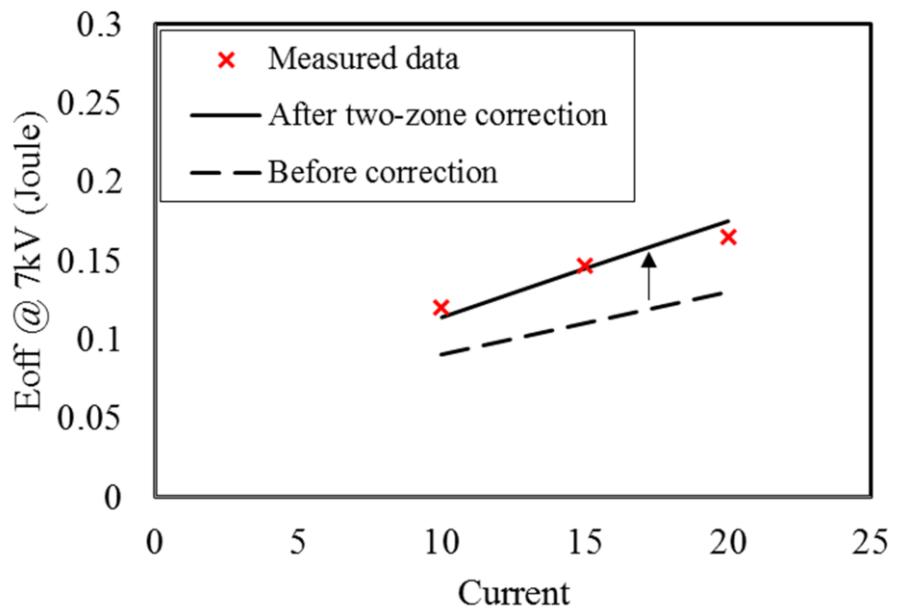


Figure 5-18 Improvement of the accuracy of the proposed model by incorporating two-zone correction.

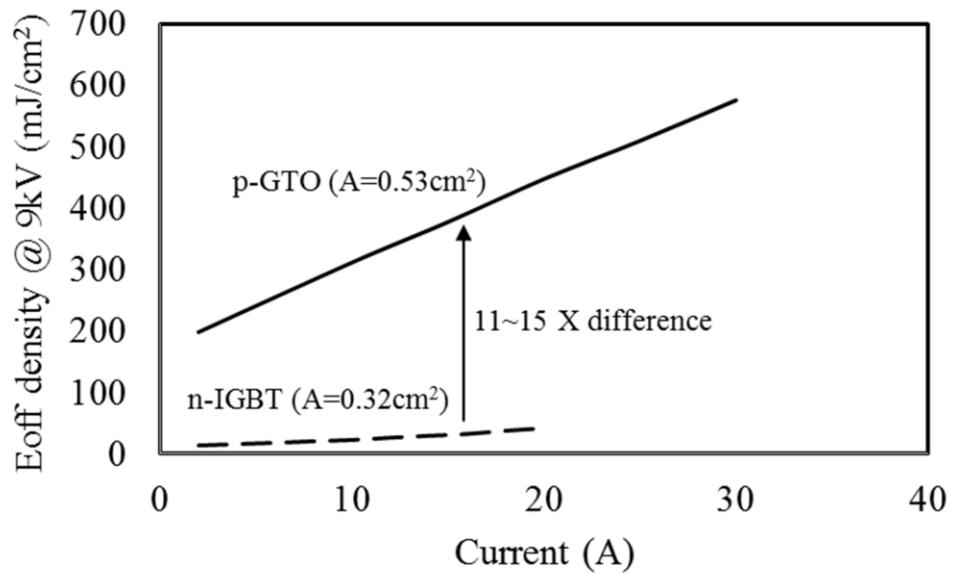


Figure 5-17 The switching speed of 15kV n-IGBT is more than 10 times faster than p-GTO.

# Chapter 6

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## Summary

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### Major contribution

Modeling 4H-SiC MOSFET:

- (a) Simulate IV curves at high current density in the saturation region.
- (b) Wide range of IV curves are simulated with region-wise manner in order to minimize the number of parameters compared to previous works.
- (c) Simulate the loss associate with the output capacitance that cannot be measured using terminal current/voltage values.

Modeling 4H-SiC n-IGBT:

- (a) Propose a novel characterization technique – Excess carrier density mapping – that can profiling the carrier and extract the lifetime even if it is not constant throughout the drift region.
- (b) Take into account the injection from the channel when calculating on-state voltage drop and switching.
- (c) Unravel the analytical relationship between dv/dt and the local excess carriers and implement it into a sub-circuit model.

Propose two-zone 4H-SiC IGBT with moderate dv/dt

- (a) Successfully reduce the dv/dt by 3 times while maintaining low turn-off energy.
- (b) Provide design rules for how to select the length and the doping of the two zones in the drift region

Modeling 4H-SiC pGTO

- (a) Compare analytically 4H-SiC n- and p-type ambipolar switches in terms of injection capability and switching speed.
- (b) Developed a Sub-circuit p-GTO model based on the proposed IGBT model.

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