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Analysis and Control of Direct Voltage Regulated Active DC Link Capacitance Reduction Circuit

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Abstract— The paper focuses on control analysis and operational issues of a recently proposed direct voltage regulated active capacitance reduction circuit, consisting of a small auxiliary capacitance interfaced to DC link by bidirectional DC-DC converter. The aim of such a system is replacing the bulk DC bus capacitor without escalating the ripple. While the hardware of the system under study is similar to some of the proposed active capacitance reduction solutions, the control structure is quite different. The primary goal of the controller is direct regulation of DC link voltage rather than DC link current, performed by most of existing solutions, thus avoiding the use of invasive DC link current measurement/s. It is revealed that such an active capacitance reduction circuitry may be perceived as output-voltage regulated wide-input-range converter feeding a bidirectional power load. Such an arrangement was neither mentioned nor analyzed in the literature by far, requiring non-trivial and challenging control design. A dual-loop voltage-current arrangement widely used in typical power supplies is proposed to control the active capacitance reduction circuitry. It is shown that the control structure is sufficient to yield satisfactory performance even though the system possesses a slow unstable mode when absorbing power from the DC link. The revealed findings are fully supported by simulations and experimental results.

Keywords— Grid-interfacing converters, DC link ripple, voltage regulation, stability.

I. INTRODUCTION

It is well-known that instantaneous power of practical power converters, connected to single-phase or unbalanced three-phase grids contains both DC and pulsating components. While the DC part of grid power is transferred to the load, pulsating component must be absorbed by an instantaneous power-matching element, typically realized by bulk DC link capacitor [1]. In case AC load is connected to the DC bus via power electronics interface, it also might contribute pulsating power, which needs to be captured as well by the same power-matching element. Pulsating energy absorbed/supplied by the bulk capacitance creates DC-link voltage ripple, which must reside within predetermined limits, set by both grid-connected converter topology and DC link capacitor voltage rating. These constraints lead to necessity of utilizing electrolytic capacitors in applications rated 50W and higher [2]. Consequently, reliability and physical size issues related to electrolytic capacitors constitute an important drawback of modern power electronics based energy conversion systems [3] – [7].

In order to tackle the mentioned shortcomings, two main groups of solutions were suggested in the literature, namely passive and active. The former is based on adding inductors to the DC link in order to realize a resonant filter, tuned to the pulsating power fundamental frequency [8]. Since more than single fundamental component may be present at relatively low frequencies, bulky DC link resonant filter banks are required. Active solutions require addition of much smaller passive components and has therefore attracted much more attention, focusing on three main research directions as follows:

- It was shown in [9] – [11] that some DC link capacitance reduction is possible by distorting the input current of the grid-interfacing converter at the expense of power factor;

- H-bridge related circuit topologies, allowing reducing the total DC link capacitor required by differential operation, were developed in [12] – [17].
- Replacing the bulk DC link capacitor by additional power converter terminated by a much smaller capacitance [18] – [30].

The latter is probably the most popular research direction. Principle of operation of such active capacitance reduction circuits (ACRC) is based on the fact that the amount of useable bulk DC link capacitor energy comprises only small fraction of the energy stored, i.e. much lower capacitance is sufficient to cope with pulsating power component once capacitor voltage ripple constraints are released. Consequently, decoupling the power matching capacitor from DC link by a bidirectional power converter allows significant decrease of utilized capacitance value. It should be emphasized that both parallel and series ACRCs were proposed in the literature. An interested reader is further referred to [31] for detailed comparison of active power decoupling topologies in single-phase systems.

The paper further focuses on a solution, belonging to the latter subgroup, namely parallel-connected ACRCs. Most of related solutions operate similarly to active power filters, resembling current controlled current sinks (from the DC bus point of view), drawing the pulsating component of the total DC link current thus allowing DC link capacitance reduction. In order to accomplish this, pulsating current component is extracted from the total DC link current and used as ACRC current reference. Necessity of multiple currents sensors as well as access to measurement points are probably the major drawbacks of the method (refer to the next Section for details). Recently, direct voltage regulation based ACRCs were proposed in [32] – [38]. There, pulsating current component is displaced into the ACRC without measuring DC link currents, thus requiring DC link voltage sensing only. In [32], [33] and [36], ripple component is

extracted from the sensed DC link voltage and regulated to zero; in [34] and [34] DC link reference voltage is directly fed into PWM generator in a certain way while in [37] – [39], DC link voltage is directly controlled. The authors of [37] proposed combined control structure of ACRC and grid-interfacing converter. Unfortunately, the algorithm required MHz switching frequency to stabilize the system and was thus verified by simulations only. On the other hand, the approach presented in [38] and further elaborated in [39] has demonstrated the following advantages. First, is has the potential of operating with typical voltage controllers of grid interfacing converters with minor external adjustments only. Second, switching frequency of several tens of kHz was sufficient to stabilize the ACRC stabilization by a dual-loop control structure, common to typical power converters. It was also shown that the proposed system allows "breaking" the tradeoff between power factor and DC link voltage loop bandwidth. Consequently, DC link voltage quality becomes a function of ACRC regulation capabilities.

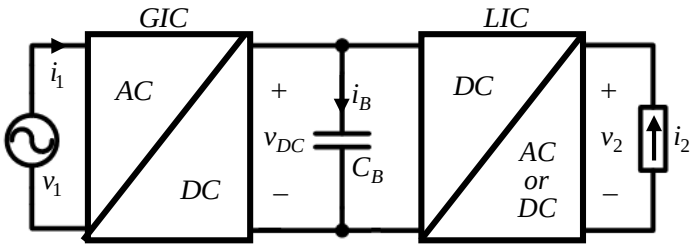
However, neither analytical insight into small-signal behavior of the system nor control design details were given in [38] and [39]. Therefore, this paper reveals modeling and control design of direct voltage regulated ACRC in detail. It is demonstrated that the ACRC under study may be perceived as an output-voltage regulated wide-input-range boost converter feeding a bi-directional power load. Even though regulation of boost converters with non-varying input voltage feeding unidirectional constant power loads has been recently treated in the literature (mainly by nonlinear or advanced linear control techniques [40] – [43]), the case arising here is non-trivial and was neither mentioned nor analyzed in the literature by far. Moreover, modifying the feedback signal to an existing grid interfacing converter voltage controller is challenging too since auxiliary voltage ripple magnitude as well as value

of ACRC capacitor are different from the ones used to design compensation network of grid interfacing controller.

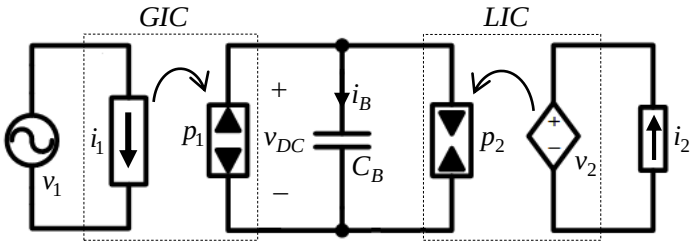
The rest of the paper is organized as follows. Principle of investigated ACRC operation is briefly reviewed and compared to classical solutions in Section II. Example of applying the proposed solution to a DC power supply with PFC front end is discussed in Section III, followed by detailed simulations-accompanied modeling and control design in Section V. Experimental validation is carried out in Section VI and the paper is concluded in Section VII.

II. ACTIVE CAPACITANCE REDUCTION ESSENTIALS

Typical generalized grid-connected power conversion system is shown in Fig. 1(a), comprising grid-interfacing converter (GIC), bulk DC link capacitance C_B and (optional) load interfacing converter (LIC). Fig. 1(b) depicts corresponding functional diagram, of the system.



(a) Generalized topology.



(b) Functional diagram.

Fig. 1. Typical grid-connected power conversion system.

Considering sinusoidal grid voltage

$$v_1(t) = V_1 \sin\left(\omega_1 t + \theta_1\right), \tag{1}$$

and generalized periodic grid current

$$i_1(t) = I_{10} + \sum_{n=1}^{\infty} I_{1n} \sin\left(n\omega_1 t + \varphi_{1n}\right), \tag{2}$$

instantaneous GIC input power is given by

$$p_1(t) = v_1(t) i_1(t) = P_1 + \Delta p_1(t) \tag{3}$$

with

$$P_1 = 0.5 V_1 I_1 \cos\left(\theta_1 - \varphi_1\right) \tag{4}$$

denoting active power term and $\Delta p_1(t)$ symbolizing zero-average pulsating power component. Similarly, instantaneous load power may be expressed by

$$p_2(t) = v_2(t) i_2(t) = P_2 + \Delta p_2(t). \tag{5}$$

Bulk capacitor instantaneous power (cf. Fig. 1) is then given by

$$p_3(t) = v_{DC}(t) i_B(t) = p_1(t) + p_2(t) = P_3 + \Delta p_3(t) \tag{6}$$

with

$$P_3 = P_1 + P_2, \quad \Delta p_3(t) = \Delta p_1(t) + \Delta p_2(t). \tag{7}$$

In case GIC operates with unity power factor, the input current is

$$i_1(t) = I_1 \sin\left(\omega_1 t + \theta_1\right), \tag{8}$$

leading to

$$P_1 = 0.5 V_1 I_1, \quad \Delta p_1(t) = -P_1 \cos 2\left(\omega_1 t + \theta_1\right). \tag{9}$$

Moreover, in case of a DC load, there is

$$p_2(t) = P_2, \quad \Delta p_2(t) = 0. \tag{10}$$

Pulsating power component of the bulk capacitor is then given by

$$\Delta p_3(t) = -P_1 \cos 2\left(\omega_1 t + \theta_1\right). \tag{11}$$

Instantaneous bulk capacitance energy and voltage are given by

$$E_B(t) = E_B(0) + \int_0^t p_3(\tau) d\tau = E_B(0) + P_3 t - \frac{P_1}{2\omega_1} \sin 2\left(\omega_1 t + \theta_1\right) \tag{12}$$

and

$$v_{DC}(t) = v_{DC}(0) \sqrt{1 + \frac{2P_3}{v_{DC}^2(0) C_B} t - \frac{P_1}{\omega_1 v_{DC}^2(0) C_B} \sin 2\left(\omega_1 t + \theta_1\right)}, \tag{13}$$

respectively. In steady state, $P_1 = -P_2$, i.e. $P_3 = 0$ and (13) reduces to

$$v_{DC}^{ss}(t) = V_{DC}^* \sqrt{1 - \frac{P_1}{\omega_1 \left(V_{DC}^*\right)^2 C_B} \sin 2\left(\omega_1 t + \theta_1\right)} \tag{14}$$

with V_{DC}^{*} denoting average DC link voltage reference. In case steady state instantaneous DC link voltage is restricted by

$$v_{DC}^{MIN} < v_{DC}^{ss}(t) < v_{DC}^{MAX}, \tag{15}$$

the minimum value of the bulk capacitance is determined as

$$C_B = \frac{P_1}{\omega_1} \max\left\{ \frac{1}{\left(V_{DC}^{*}\right)^2 - \left(v_{DC}^{MIN}\right)^2}, \frac{1}{\left(v_{DC}^{MAX}\right)^2 - \left(V_{DC}^{*}\right)^2} \right\}. \tag{16}$$

Adding safety margins, 1mF/kW of DC link capacitance is typically required. Consequently, applications above several tens of watts usually require capacitance values realizable only by electrolytic capacitors due to physical size and price constraints. As a remedy, active capacitor reduction concept was proposed, as shown in Fig. 2(a). Bulk DC link capacitor is replaced by an ACRC, comprising a bidirectional DC-DC converter and auxiliary capacitance $C_A << C_B$. The main idea is decoupling the power matching capacitance from the DC link thus releasing the constraints (15). In in case of a DC load, steady state instantaneous auxiliary capacitor voltage would then be given by

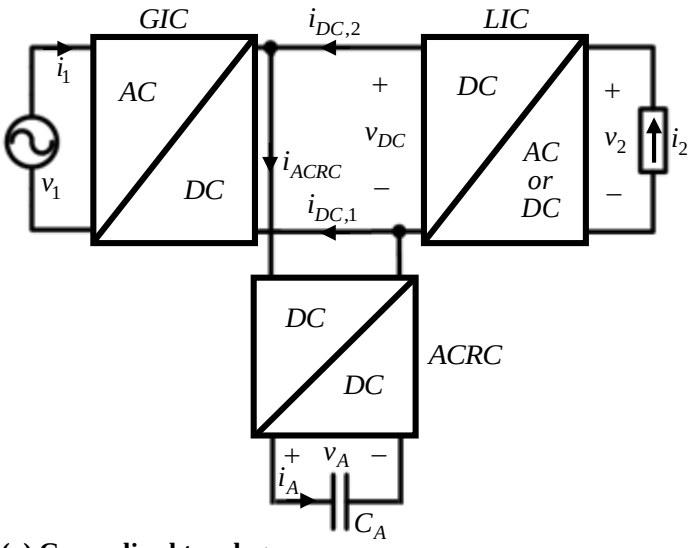
$$v_A^{ss}(t) = V_A^{*} \sqrt{1 - \frac{P_1}{\omega_1 \left(V_A^{*}\right)^2 C_A} \sin 2\left(\omega_1 t + \theta_1\right)} \tag{17}$$

with V_A^{*} denoting the reference for average auxiliary capacitance voltage. Limits of v_A, given by

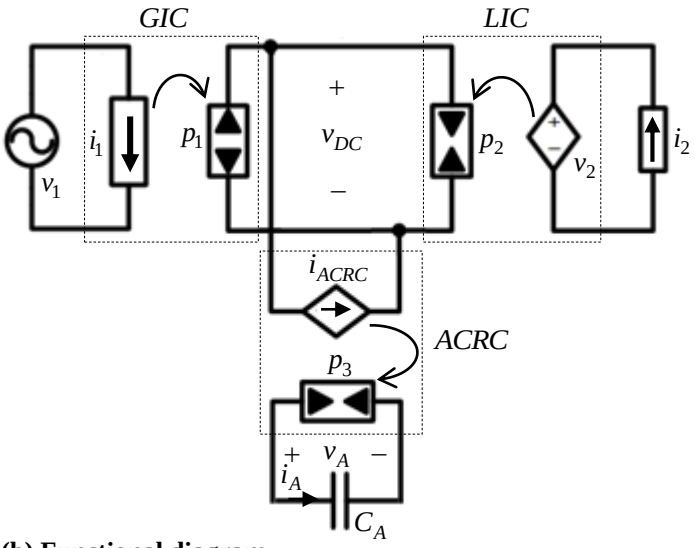
$$v_A^{MIN} \le v_A^{ss}(t) \le v_A^{MAX}, \tag{18}$$

depend on the auxiliary converter topology and related practical constraints. The minimum auxiliary capacitance value is then determined as

$$C_A = \frac{P_1}{\omega_1} \max\left\{ \frac{1}{\left(V_A^{*}\right)^2 - \left(v_A^{MIN}\right)^2}, \frac{1}{\left(v_A^{MAX}\right)^2 - \left(V_A^{*}\right)^2} \right\}. \tag{19}$$



(a) Generalized topology.



(b) Functional diagram.

Fig. 2. Grid-connected power conversion system with active capacitance reduction circuit.

According to (19), C_A is minimized for

$$V_A^* = \sqrt{\frac{1}{2}\left(\left(v_A^{MAX}\right)^2 + \left(v_A^{MIN}\right)^2\right)}, \tag{20}$$

as

$$C_{A,MIN} = \frac{2P_1}{\omega_1\left(\left(v_A^{MAX}\right)^2 - \left(v_A^{MIN}\right)^2\right)}. \tag{21}$$

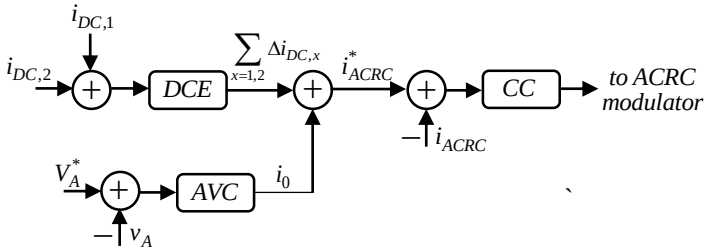
From the DC link side point of view, ACRC appears as a controlled current source i_{ACRC} (cf. Fig. 2(b)). In most of the cases, ACRC was realized as a current controlled current source (CCCS), resembling operation of an active power filter. Typical control structure is shown in Fig. 3(a) and operates as follows. GIC and LIC DC link side currents (cf. Fig. 2(a))

$$i_{DC,1}(t) = I_{DC,1} + \Delta i_{DC,1}(t),\ i_{DC,2}(t) = I_{DC,2} + \Delta i_{DC,2}(t) \tag{22}$$

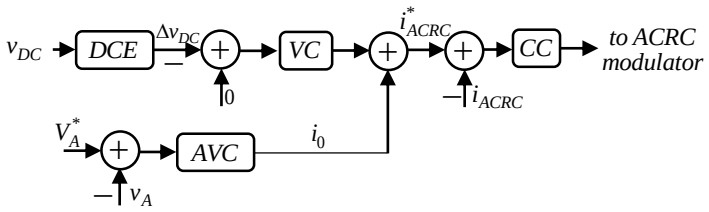
are sensed and summed, DC component $I_{DC,1} + I_{DC,2}$ is removed by DC eliminator (DCE) block and the remaining pulsating current component is set as the ideal ACRC DC link side reference current. Since ACRC is not 100%-efficient, the losses are displaced by adding compensating current $i_0(t)$, generated by auxiliary voltage controller (AVC), to the ideal ACRC current reference, i.e.

$$i^*_{ACRC}(t) = \Delta i_{DC,1}(t) + \Delta i_{DC,2}(t) + i_0(t). \tag{23}$$

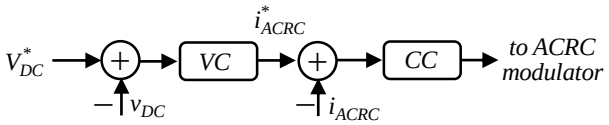
ACRC converter duty cycle is then obtained via an inner current loop based on dedicated current controller (CC). Consequently, DC link voltage is indirectly regulated by diverting the pulsating current components into the ACRC. This requires up to N current sensors in case of N DC link connected converters and access to corresponding measurement points. Moreover, DCE circuitry constitutes additional delay to the system. Different control structure was proposed in [32] – [38]. Instead of measuring N DC link currents, only DC link voltage $v_{DC}(t) = V_{DC} + \Delta v_{DC}$ is sensed. Then, DC component V_{DC} is eliminated by means of a suitable DCE and resonant voltage controller VC attempts minimizing pulsating component Δv_{DC}, as shown in Fig. 3(b). The authors of [39] – [41] alternatively proposed direct regulation of DC link voltage to a constant value V^*_{DC}, as shown in Fig. 3(c), avoiding implications related to post-processing of measured DC link voltage.



(a) Active filter based.



(b) Direct ripple eliminating.



(c) Direct voltage regulating.

Fig. 3. Different ACRC control structures.

Once the DC link voltage (or its ripple) is appropriately regulated, pulsating current components are indirectly diverted to ACRC without sensing any DC link current, thus taking away the need for current sensors and proximity to corresponding measurement points, requiring DC link voltage sensing only.

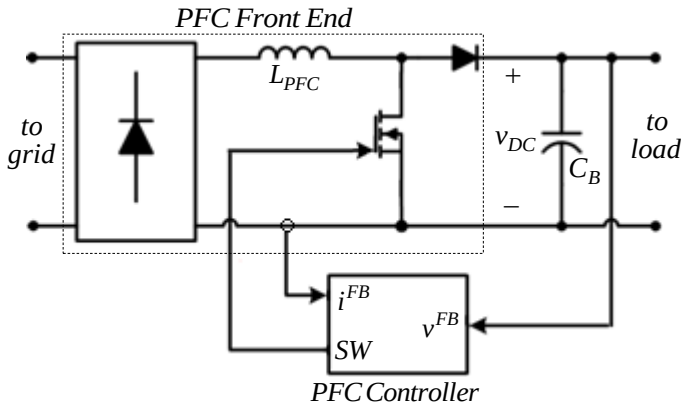
However, the method of Fig. 3(c) was shown to possess the following implication: once DC link voltage is tightly regulated, it no longer reflects the power balance of the system. Since the mismatch between LIC and GIC power is diverted to the ACRC, auxiliary capacitance voltage v_A rather than v_{DC} should be used as power balance indicator. This means that existing slow GIC voltage control loop must be closed around v_A instead of v_{DC}. On the other hand, no additional voltage loop is required to generate i_0 as in Figs. 3(a) and 3(b). In addition, since DC link voltage is regulated by ACRC rather than by GIC, corresponding control loop bandwidth is no longer coupled

with grid input current quality. Hence, it should be selected as high as possible to enhance DC link voltage dynamics and quality.

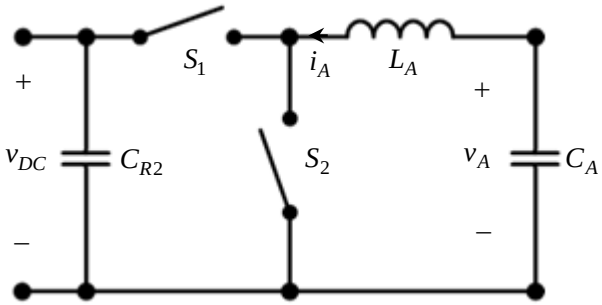
Since the power flow through the ACRC is bidirectional, small-signal dynamics gain polarity changes every half cycle. Hence, ACRC duty cycle is typically calculated separately for each power flow direction (i.e. current controllers in Fig. 3 usually contain two subsystems, each activated during corresponding half cycle). Nevertheless, in [40], [41] single-entity current controller was adopted for ACRC duty cycle calculation in case of direct voltage regulation control structure shown in Fig. 3(c). The underlying basis for utilizing such a control structure is developed in the subsequent sections.

III. DUAL-LOOP CONTROLLER DESIGN FOR DIRECT VOLTAGE REGULATED ACRC

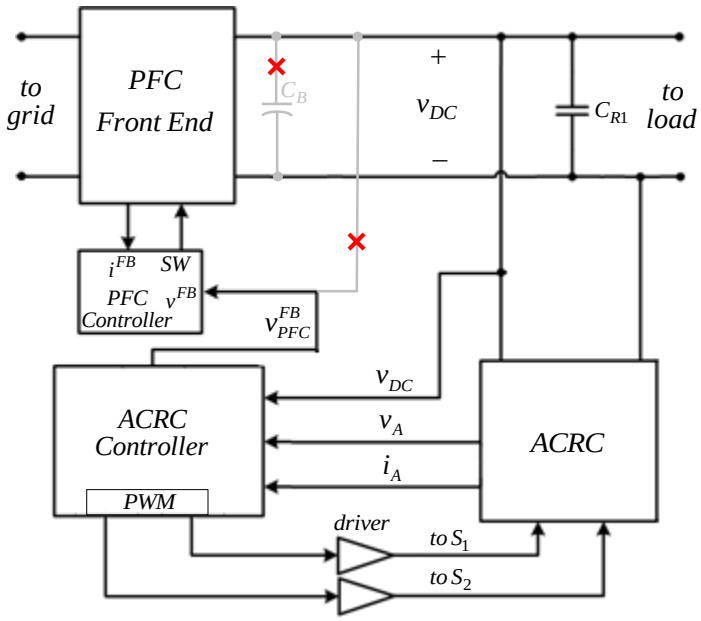
Consider an off-the shelf feedback controlled PFC front end, shown in Fig. 4(a). The aim of using an off-the-shelf hardware is demonstrating that the proposed ACRC system may be combined with existing GIC in a nearly plug-and-play fashion. Nevertheless, in case a from-scratch design is carried out, it would be a particular case of the approach revealed next. Typical PFC front end comprises power stage and feedback controller, operating in dual-loop arrangement while sensing DC link voltage and inductor (or switch) current, as shown. Bulk DC link capacitance C_B, present to absorb pulsating power component, is intended to be replaced by ACRC shown in Fig. 4(b). Small ceramic capacitor C_{R2} is connected across the DC link side terminals of ACRC to absorb switching ripple. The combined PFC–ACRC system is depicted in Fig. 4(c). Bulk DC link capacitance is eliminated and original DC link voltage feedback is disconnected from the PFC controller. Small ceramic capacitor C_{R1} remains connected across DC link-side terminals of the PFC to absorb switching ripple. DC link voltage v_{DC}, auxiliary capacitance voltage v_A and current i_A are measured and fed to ACRC controller, which in turn both drives ACRC converter switches and creates a feedback signal to the PFC controller instead of the disconnected one. Consequently, the proposed control structure allows changing only the voltage feedback to the PFC controller in order to implement the voltage loop variable modification mentioned in the preceding Section (i.e. PFC voltage control loop is now closed around v_A instead of v_{DC}). The rest of PFC-related circuitry (voltage loop compensation network, inner current loop, protection and soft-start sequences and the power stage) remains unaltered. To conclude, bulk capacitor disconnection and voltage feedback branch modification are the only required GIC variations. This is referred as "nearly plug-and-play" operation.



(a) Off-the-shelf controlled PFC front end.



(b) ACRC hardware.



(c) Combined PFC-ACRC system.

Fig. 4. Component of the proposed system.

The structure of the proposed ACRC controller (cf. Fig. 4(c)) is shown in Fig. 5. Dual-loop voltage-current controller with (optional) feedback linearization by voltage loop gain scheduling (GS) and current loop feed-forwarding (FF) is used to regulate the DC link voltage v_{DC} to a constant reference V_{DC}^{*}. Reasons for selecting the particular control arrangement are revealed next. On the other hand, sensed auxiliary capacitor voltage v_A is notch-filtered to remove the double-grid-frequency pulsating component (the motive is explained further on) and then shifted and scaled to create voltage feedback to the PFC controller v_{PFC}^{FB}.

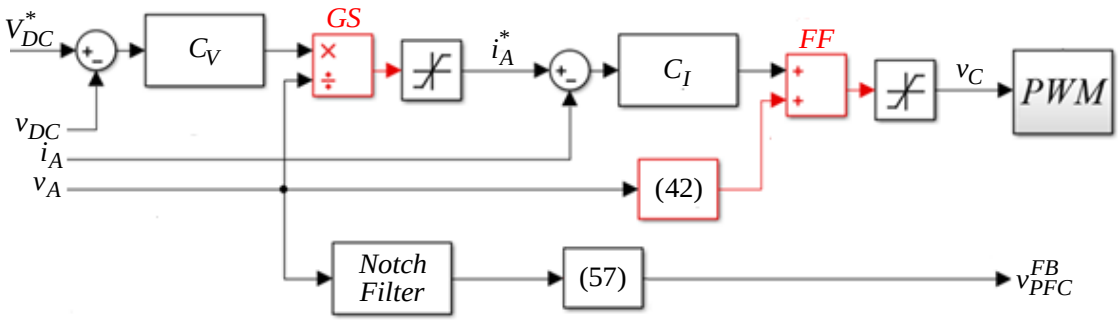


Fig. 5. ACRC controller structure.

A. ACRC modeling

Consider the output of the current controller C_I satisfying

$$-1 < v_C(t) < 1, \tag{24}$$

relating to the auxiliary converter duty cycle and its complimentary as

$$d = \frac{v_C + 1}{2},\ 1 - d = \frac{1 - v_C}{2}. \tag{25}$$

Corresponding ACRC switching-cycle-averaged model is then shown in Fig. 6. It may be concluded that the DC-DC converter drives a bidirectional power load p_3 while driven by a widely varying input voltage v_A. Such a configuration has not been analyzed in the literature by far.

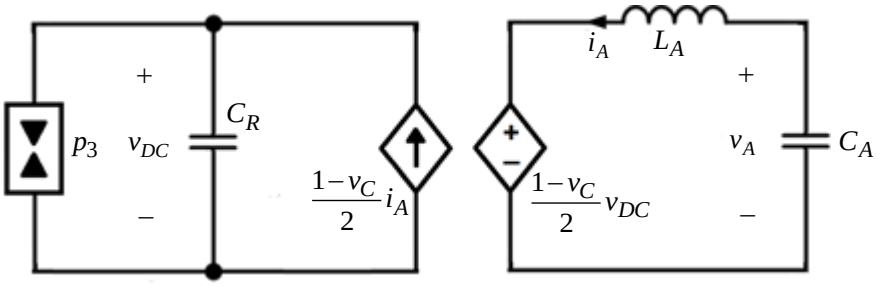


Fig. 6. Switching-cycle-averaged model of the ACRC.

ACRC large-signal dynamics is governed by

$$\begin{aligned} C_A \frac{dv_A}{dt} &= -i_A \\ L_A \frac{di_A}{dt} &= v_A - \frac{1-v_C}{2} v_{DC} \\ C_R \frac{dv_{DC}}{dt} &= \frac{1-v_C}{2} i_A - \frac{p_3}{v_{DC}} \end{aligned} \tag{26}$$

with $C_R = C_{R1} + C_{R2}$. Perturbing the time-varying quantities as

$$v_A = V_A + \tilde{v}_A, v_{DC} = V_{DC} + \tilde{v}_{DC}, i_A = I_A + \tilde{i}_A, v_C = V_C + \tilde{v}_C, p_3 = P + \tilde{p}, \tag{27}$$

and substituting in (26), control-to-output transfer function is obtained as

$$\frac{\tilde{v}_{DC}}{\tilde{v}_C}(s) = \frac{V_{DC}^2}{2V_A} \frac{L_A C_A s^2 - \frac{C_A V_A^2}{P} s + 1}{-\frac{V_{DC}^2 C_R L_A C_A}{P} s^3 + L_A C_A s^2 - \frac{C_R V_{DC}^2 + C_A V_A^2}{P} s + 1}, \tag{28}$$

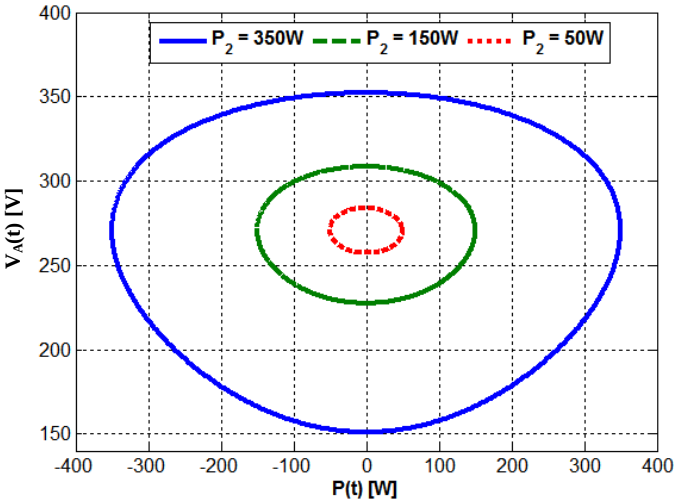
linearized around the operating trajectory, given by

$$\begin{aligned} P(t) &= -P_1 \cos 2\left(\omega_1 t + \theta_1\right) \\ V_A(t) &= V_A^* \sqrt{1 - \frac{P_1}{\omega_1 \left(V_A^*\right)^2 C_A} \sin 2\left(\omega_1 t + \theta_1\right)} \\ I_A(t) &= \frac{P(t)}{V_A(t)} \end{aligned} \tag{29}$$

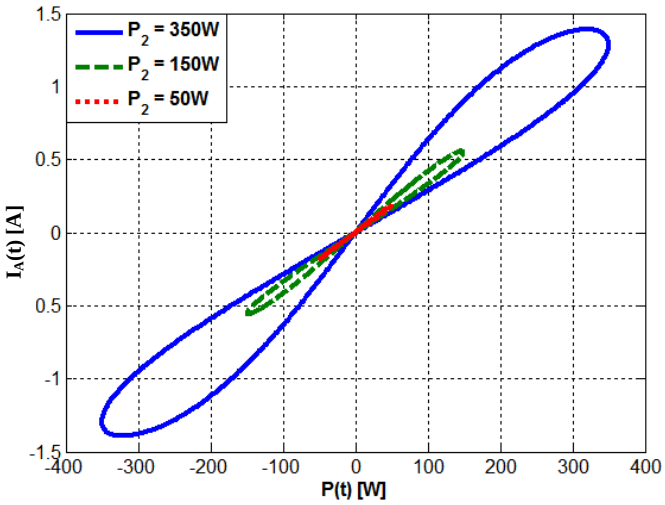
in steady-state and shown in state plane in Fig. 7 for different load power levels (graphical results here and thereafter are obtained for data given in Table I, which corresponds to the values used in experimental setup).

TABLE I
SYSTEM PARAMETER VALUES

Parameter	Value	Units
Switching frequency, T_S^{-1}	50	*kHz*
ACRC inductance, L_A	320	μH
ACRC capacitance, C_A	22	μF
Total DC link capacitance, C_R	9.4	μF
Grid frequency, ω_1	100π	*rad/s*
Reference voltage, V_A^*	271	*V*
Reference voltage, V_{DC}^*	400	*V*
Rated load power, $P_{2,MAX}$	360	*W*



(a) Auxiliary capacitor voltage.



(b) Auxiliary capacitor current.

Fig. 7. Operation trajectory versus pulsating power component instantaneous magnitude.

According to (29), the polarity of $P(t)$ alternates periodically. As long as P is negative (i.e. the ACRC supplies power to the DC link), the control-to-output transfer function (28) is stable, containing two stable zeros, and may hence be stabilized by any

classical method. However, when the ACRC absorbs power from the DC link (i.e. P is positive), the plant becomes unstable and contains two unstable zeros. In this case, stabilization is nontrivial and challenging. Moreover, it is not easy to design a unified controller, suitable for both cases. In [43], unidirectional power load feeding boost converter with constant input voltage was analyzed. There, somewhat similar instability was successfully treated by a dual-loop controller configuration. Therefore, dual-loop configuration is adopted here as the starting design point. Nevertheless, system analysis and controller shaping in present case are quite different from [43]. It is revealed, that utilization of current-mode-control cannot globally stabilize the plant in case of bidirectional power load. Nevertheless, as shown further on, it may significantly reduce the unstable mode magnitude, preventing the system from divergence during corresponding half cycle.

B. Current controller design

First, consider the classical approach of current loop shaping where v_A and v_{DC} are treated as independent, slow-varying disturbances. Then, small-signal version of current-loop-related part of (26) is given by

$$\tilde{i}_A = \frac{V_{DC}}{2L_A s}\left(\tilde{v}_C + \tilde{v}_D\right) \tag{30}$$

with

$$\tilde{v}_D = \frac{2}{V_{DC}}\left(\tilde{v}_A - \frac{V_A}{V_{DC}}\tilde{v}_{DC}\right) \tag{31}$$

denoting total disturbance entering the current loop. Simplified transfer functions from control and disturbance inputs to ACRC current are

$$P_{CI}(s) = \frac{\tilde{i}_A(s)}{\tilde{v}_C(s)} = \frac{V_{DC}}{2L_A s}, \quad P_{DI}(s) = \frac{\tilde{i}_A(s)}{\tilde{v}_D(s)} = \frac{V_{DC}}{2L_A s}, \tag{32}$$

respectively. Selecting a PI controller

$$C_I(s) = \frac{K_{PI}s + K_{II}}{s} \tag{33}$$

as current loop regulator yields

$$\tilde{i}_A(s) = T_I(s)i_A^*(s) + D_I(s)\tilde{v}_D(s) \tag{34}$$

with

$$T_I(s) = \frac{\frac{V_{DC}}{2L_A}K_{PI}s + \frac{V_{DC}}{2L_A}K_{II}}{s^2 + \frac{V_{DC}K_{PI}}{2L_A}s + \frac{V_{DC}K_{II}}{2L_A}}, \quad D_I(s) = -\frac{\frac{V_{DC}}{2}s}{s^2 + \frac{V_{DC}K_{PI}}{2L_A}s + \frac{V_{DC}K_{II}}{2L_A}}, \tag{35}$$

in closed loop, i.e. unity tracking DC gain and zero disturbance rejection DC gain are secured. Nevertheless, v_A cannot be considered as slow varying. Moreover, note that auxiliary voltage and current are actually coupled,

$$\tilde{v}_A = -\frac{1}{C_A s}\tilde{i}_A. \tag{36}$$

Hence, (30) turns into

$$\tilde{i}_A = \frac{C_A s}{L_A C_A s^2 + 1}\frac{V_{DC}}{2}\left(\tilde{v}_C + \tilde{v}_D\right) \tag{37}$$

with

$$\tilde{v}_D = -\frac{2V_A}{V_{DC}^2}\tilde{v}_{DC}. \tag{38}$$

and (32) becomes

$$P_{CI}(s) = \frac{\frac{V_{DC}}{2}C_A s}{L_A C_A s^2 + 1}, \quad P_{DI}(s) = \frac{\frac{V_A}{V_{DC}}C_A s}{L_A C_A s^2 + 1}, \tag{39}$$

characterized by two undamped poles (in reality, these are lightly damped poles due to parasitic resistances). In [44], closed-loop damping of such system was carried out by proportional controller only, leading to band-pass-filter-like behavior of the closed loop. Nevertheless, since in this case ACRC current i_A must contain DC component to

compensate parasitic losses, low DC gain may lead to poor performance. Consequently, utilizing (33) as loop controller yields (34) with

$$T_I(s)=\frac{\frac{V_{DC}K_{PI}}{2L_A}s+\frac{V_{DC}K_{II}}{2L_A}}{s^2+\frac{V_{DC}K_{PI}}{2L_A}s+\frac{1}{L_AC_A}+\frac{V_{DC}K_{II}}{2L_A}},\quad D_I(s)=-\frac{\frac{V_A}{V_{DC}}C_As}{s^2+\frac{V_{DC}K_{PI}}{2L_A}s+\frac{1}{L_AC_A}+\frac{V_{DC}K_{II}}{2L_A}},\quad (40)$$

i.e. zero disturbance rejection DC gain is assured. On the other hand, tracking low-frequency gain is less than unity, given by

$$T_I(s\to 0)=\frac{1}{1+\frac{2}{C_AV_{DC}K_{II}}},\quad (41)$$

i.e. some steady-state current tracking error is expected, which can be minimized (but not eliminated) by increasing C_A, V_{DC} and/or K_{II}.

It is possible to eliminate the steady-state current tracking error completely by adding a feed-forward term (cf. Fig. 5)

$$v_{FF}=1-\frac{2v_A}{v_{DC}}\quad (42)$$

to the control signal v_C, turning the second equation of (26) into

$$L_A\frac{di_A}{dt}=\frac{1}{2}v_Cv_{DC}\quad (43)$$

thus "breaking" the current loop dependence on v_A. Linearizing, there is

$$\tilde{i}_A=\frac{V_{DC}}{2L_As}\left(\tilde{v}_C+\tilde{v}_D\right)\quad (44)$$

with

$$\tilde{v}_D=\frac{V_{DC}-2V_A}{V_{DC}^2}\tilde{v}_{DC}.\quad (45)$$

Utilizing (33) retains (35), bringing back both unity tracking DC gain and zero disturbance rejection DC gain. Moreover, once DC link voltage is tightly regulated, its constant reference value V_{DC}^* may be used in (42) instead of measured v_{DC}.

PI controller design should maximize current loop bandwidth for the desired phase margin φ_M while taking into account switching delay T_d [45]. Here, φ_M = 45^o was selected and $T_d = T_S$ was assumed, leading to crossover frequency of ~4kHz. Simulation results shown in Fig. 8 demonstrate current loop performance without and with feedforward action for rated load operation (ACRC inductor current is filtered to remove the switching ripple harmonic for clarity). Nonzero steady state error is noticeable in the former case and eliminated in the latter, as expected.

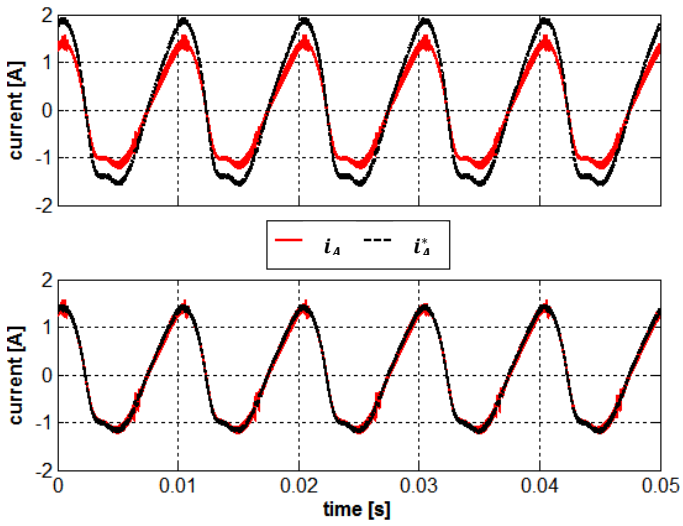


Fig. 8. Simulation results, rated load operation. Reference and actual ACRC inductor currents without (top) and with (bottom) feedforward action.

C. Voltage controller design

Once current and voltage loops are decoupled in frequency domain and the former is well-designed, $i_A = T_I(s \to 0) i_A^*$ may be assumed. Assuming $T_I(s \to 0) = 1$, DC link voltage small-signal dynamics is obtained as

$$\tilde{v}_{DC} = P_{CV}(s)\tilde{i}_A^* + P_{DV}(s)\tilde{p} \tag{46}$$

with

$$P_{CV}(s)=\frac{-P}{C_R V_{DC} C_A V_A}\frac{L_A C_A s^2-\frac{V_A^2 C_A}{P}s+1}{s^2},\quad P_{DV}(s)=-\frac{1}{C_R V_{DC} s}. \tag{47}$$

Inductor-related zero typically resides significantly outside the desired control bandwidth for all possible operation points, control-to-output transfer function may be simplified as

$$P_{CV}(s)\approx G\frac{1+\omega_Z^{-1}s}{s^2} \tag{48}$$

with

$$G=\frac{-P}{C_R V_{DC} V_A C_A},\quad \omega_Z^{-1}=-\frac{V_A^2}{P}C_A. \tag{49}$$

Corresponding gain and zero dependences on pulsating power component value are graphically shown in Fig. 9. Apparently, once pulsating power reverses its direction, both gain and zero of (48) reverse polarities as well. It should be emphasized that in general, if control-to-output transfer function reverses polarity, the controller sign should be inverted as well to preserve stability.

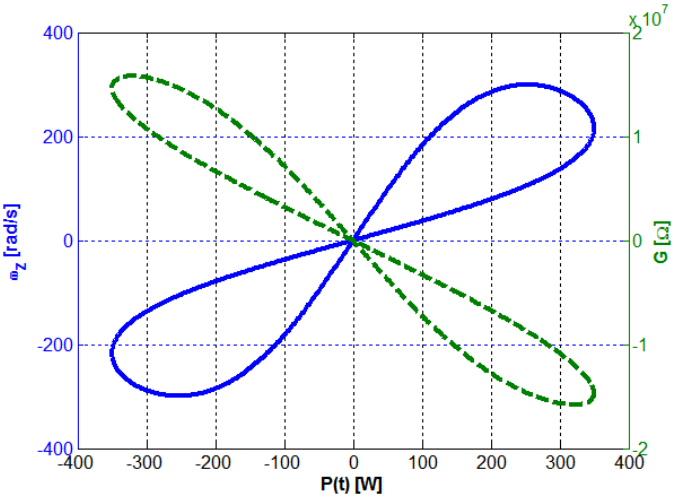


Fig. 9. Gain and zero values of the voltage loop control-to-output transfer function versus pulsating power.

Moreover, different controllers should be designed for each pulsating power polarity to obtain similar closed loop dynamics for both cases. Here, non-traditional yet simple approach allowing utilizing the same controller for both cases is proposed as follows. First, consider the operating point in which $P = 0$. Then,

$$P_{CV}(s) = \frac{V_A}{C_R V_{DC} s} \tag{50}$$

and PI controller

$$C_V = \frac{K_{PV} s + K_{IV}}{s} \tag{51}$$

brings the closed-loop system dynamics to

$$\tilde{v}_{DC}(s) = T_V(s) i_A^*(s) + D_V(s) \tilde{p}(s) \tag{52}$$

with

$$T_V(s) = \frac{\frac{V_A K_{PV}}{C_R V_{DC}} s + \frac{V_A K_{IV}}{C_R V_{DC}}}{s^2 + \frac{V_A K_{PV}}{C_R V_{DC}} s + \frac{V_A K_{IV}}{C_R V_{DC}}}, \quad D_V(s) = -\frac{s}{s^2 + \frac{V_A K_{PV}}{C_R V_{DC}} s + \frac{V_A K_{IV}}{C_R V_{DC}}}, \tag{53}$$

i.e. unity tracking DC gain and zero disturbance rejection DC gain are assured. The crossover frequency of the voltage loop was selected as 800Hz (one-fifth of the current loop bandwidth) to allow decent loops decoupling. Using (51) with the general control-to-output transfer function (48) yields

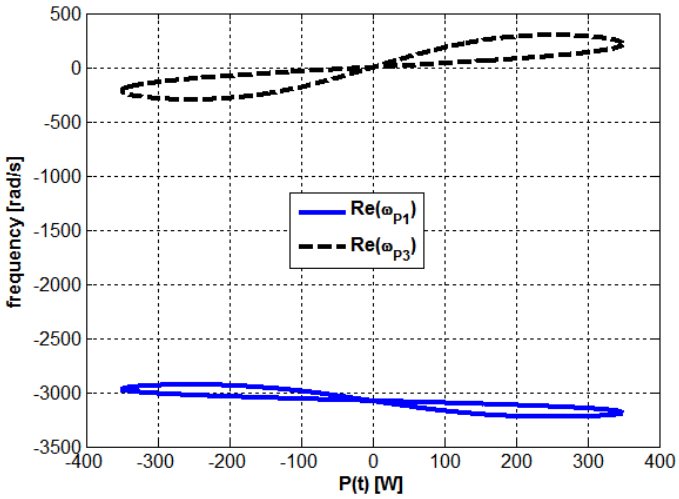
$$T_V(s) = \frac{G K_{PV} \omega_Z^{-1} s^2 + G\left(K_{PV} + K_{IV} \omega_Z^{-1}\right) s + G K_{IV}}{s^3 + G K_{PV} \omega_Z^{-1} s^2 + G\left(K_{PV} + K_{IV} \omega_Z^{-1}\right) s + G K_{IV}}. \tag{54}$$

At the first glance, (54) appears to possess unity DC gain, as desired. Nevertheless, G and ω_Z^{-1} are negative when $P > 0$. Since the coefficients of PI controller (51) are positive, (54) contains an unstable pole and hence its step response diverges. On the other hand, when $P < 0$, no instability occurs and step response of (54) is expected to converge.

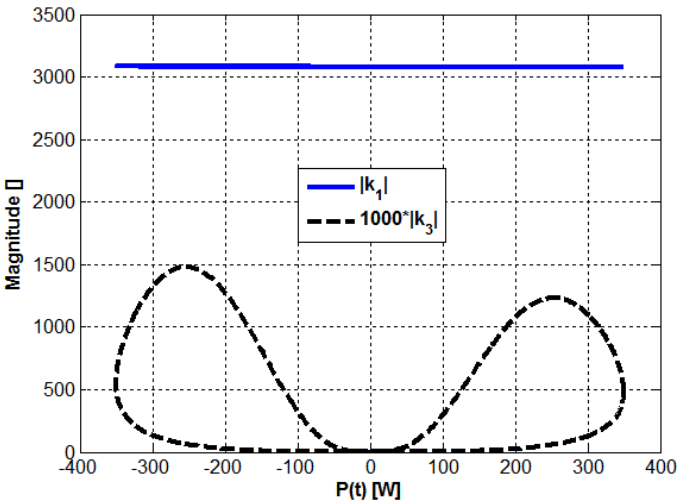
Decomposing (54) into partial fractions as

$$T_V(s) = \frac{k_1}{s+\omega_{P1}} + \frac{k_1^*}{s+\omega_{P1}^*} + \frac{k_3}{s+\omega_{P3}}, \tag{55}$$

location of poles real parts and partial fractions gains absolute values versus pulsating power are depicted in Figs. 10(a) and (b), respectively, for rated load operation.



(a) Poles (real parts).

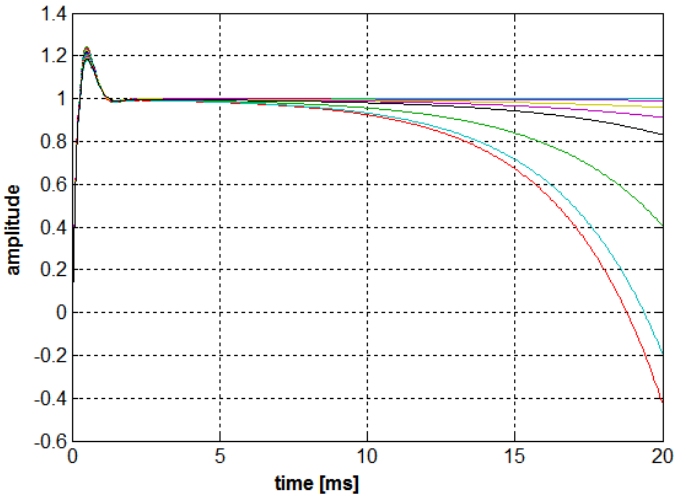


(b) Gains.

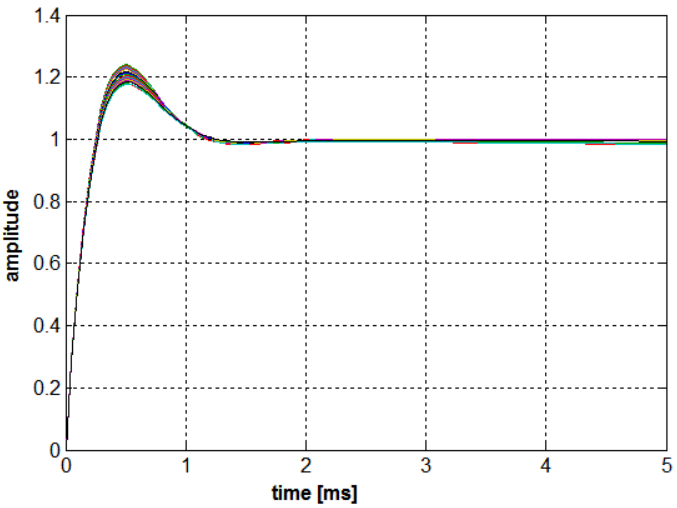
Fig. 10. State plane loci of partial fractions versus pulsating power instantaneous magnitude.

Apparently, the real part of ω_{P3} is positive for $P > 0$, as expected, with $max(|\omega_{P3}|)|_{P>0}$ = 298. In spite of this, partial fraction gain of the unstable mode is significantly lower (three orders of magnitude) that that of stable modes with $max(|k_3|)|_{P>0}$ = 1.233. Step

response of the unstable mode is given by $\frac{k_3}{\omega_{P3}}(1 - e^{\omega_{P3}t})$; thus in 50Hz grid (where P > 0 for 5ms) it will only contribute -0.014 (1.4%) to the overall step response after 5ms. The unstable pole is thus expected to be insufficient to influence the stability in such short interval. To demonstrate this, step responses of (54) for different points along operating trajectory are shown in Fig. 11(a) for rated load operation.



(a) Full.



(b) Zoomed within 5ms.

Fig. 11. Step responses of closed voltage loop throughout the operating region for rated load operation.

As expected, step responses corresponding to positive pulsating power component values diverge while the ones related to negative pulsating power component values

converge. Nevertheless, zooming the results to a 5ms period, as shown in Fig. 11(b), reveals convergence throughout the whole operation range with near-similar dynamics, i.e. the system may be assumed stable within 5ms period and it is possible to utilize a single controller (51) for both polarities of P.

It is possible to further improve the dynamics of the voltage loop by gain scheduling as follows. According to (50), the control-to-output voltage transfer function gain is proportional to v_A, which is time-varying. Since the voltage across auxiliary capacitance is measured, it may be used in a gain-scheduling (GS) fashion to eliminate the dependence on v_A, as shown in Fig .5. Simulation results shown in the top subplot of Fig. 12 compare voltage loop performance (rated load operation) of the four following cases: with 270µF electrolytic capacitor (the curve labeled "EC"); with dual-loop controlled ACRC without feedforward and gain scheduling actions (the curve labeled "ACRC"), with dual-loop controlled ACRC with feedforward action but without gain scheduling (the curve labeled "ACRC-FF") and with dual-loop controlled ACRC with both feedforward and gain scheduling actions (the curve labeled "ACRC-FF-GS").

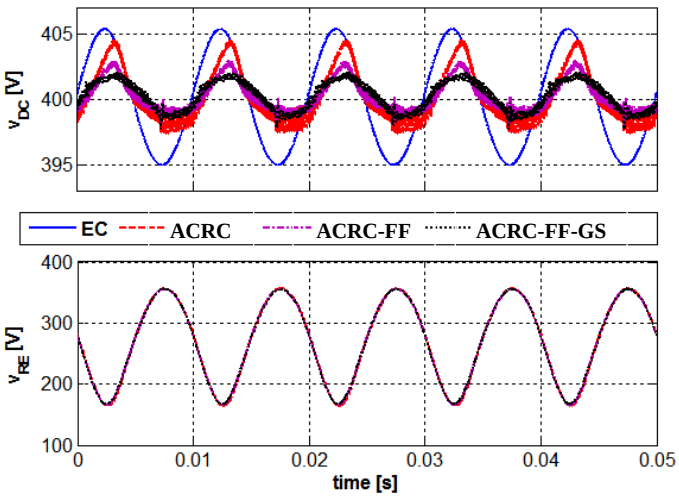


Fig. 12. Simulation results, rated load operation. DC link (top) and auxiliary capacitance (bottom) voltages. EC stands for electrolytic capacitor based operation; ACRC denotes dual loop controlled ACRC based operation without FF and GS actions; ACRC-FF relates to dual loop controlled ACRC based operation with FF action; ACRC-FF-GS refers to dual loop controlled ACRC based operation with both FF and GS enhancements.

Apparently, ACRC-based system outperforms electrolytic capacitor based system in terms of pear-to-peak ripple magnitude (yet possessing higher harmonic content). Moreover, feedforward and gain scheduling actions addition (often referred to as "feedback linearization") further improves the DC link voltage quality without significantly affecting auxiliary capacitance voltage, as shown in the bottom subplot of Fig. 12. In addition, it may be concluded that marginal improvement of current loop feed-forward action addition is much more noticeable than that of voltage loop gain scheduling based enhancement.

D. PFC controller feedback manipulation

As stated in the preceding Section, when utilizing the proposed ACRC, system power balance is reflected by auxiliary capacitance rather than DC link voltage. Since PFC voltage controller task is maintaining the system power balance, it should now rely on v_A rather than v_{DC}. However, two problems arise. First, voltage loop compensator design of the off-the-shelf PFC controller is based on the value of bulk DC link capacitance C_B rather than on C_A (in case of a from-scratch design, this issue doesn't come up). Utilizing the controller gain designed according to C_B for operation with $C_A << C_B$ would increase the bandwidth of PFC voltage loop, and as a result PFC input current would be distorted.

The following may be performed to solve the issue. As shown in [1], PFC voltage loop bandwidth is proportional to the DC value of the loop gain $L_V(0)$ and inversely proportional to the bulk capacitance value,

$$\omega_{V,PFC} \sim \frac{L_V(0)}{C_B}. \tag{56}$$

Moreover, the original loop bandwidth (typically set to around one-fifth of the fundamental grid frequency) should not be altered to maintain input current quality and original PFC dynamics. Consequently, the loop gain must be modified accordingly to preserve $\omega_{V,PFC}$. This may be accomplished by altering either compensation network gain or feedback path slope. The latter is preferable since it allows keeping the original PFC controller as is and the feedback path can easily be modified by the ACRC controller.

The second issue is as follows. Auxiliary capacitance voltage ripple is much higher than the original DC link ripple (~200V versus ~12V, see Figs. 12 and 13). Internal reference voltage of a typical off-the-shelf PFC controller is 5V, i.e. 1/80 voltage divider is employed to scale the 400V DC link voltage reference. The 12V DC link ripple is then scaled to 0.15V feedback signal ripple. Consequently, under/overvoltage detection limits are typically set to 4.75V and 5.25V, respectively [46]. In case v_A is scaled down from 271V down to 5V, 200V ripple turns into 3.7V feedback signal ripple, as shown in the top subplot of Fig. 13. This would trip the under/overvoltage protection circuitry of the PFC controller, preventing normal operation.

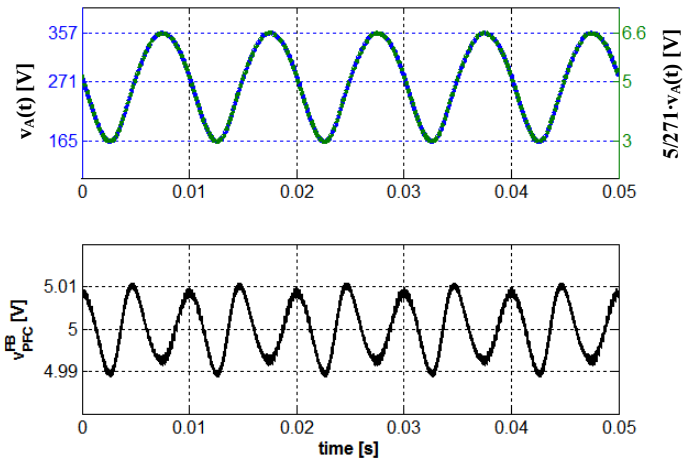


Fig. 13. Simulation results, rated load operation. Top - actual and scaled auxiliary capacitance voltage; Bottom –PFC controller feedback voltage synthesized by ACRC controller.

In order to eliminate the excessive feedback ripple problem, auxiliary capacitance voltage may e.g. be notch-filtered (cf. Fig 5) at double-grid-frequency to eliminate the dominant harmonic (in general, additional harmonics elimination may be required as well since that v_A is periodic, thus containing higher harmonics as well). In case of a DC power supply with PFC pre-converter, elimination of double-grid-frequency harmonic only would be sufficient.

Therefore, the PFC feedback signal is synthesized by ACRC controller according to

$$v_{PFC}^{FB} = 5 + \frac{1}{80\dfrac{C_B}{C_A}}\left(NF\{v_A\} - V_A^*\right). \tag{57}$$

Hence, in case filtered value of v_A equals 271V, 5V signal is fed back to the PFC controller, as required. Otherwise, the difference is scaled down by $80\frac{C_B}{C_A}$ to account for both 400V-to-5V conversion gain expected by the PFC controller and loop gain manipulation. Bottom subplot of Fig. 13 demonstrates the PFC controller feedback voltage synthesized by ACRC controller. Note that the ripple is well within permitted range. Moreover, it is well evident that after passing through a 100Hz notch filter, the ripple is dominated by 200Hz harmonic of insignificant magnitude, as stated in the preceding paragraph discussion.

IV. EXPERIMENTAL VALIDATION

In order to validate the proposed ACRC control system, Texas Instruments UCC28180EVM-573 360[W] active PFC front-end evaluation board [47] was utilized as GIC. The PFC (cf. Fig. 4(a)) is terminated by a bulk DC link electrolytic capacitor C_B = 270[μF] and operated by UCC28180 controller. In order to realize ACRC-based operation, bulk electrolytic capacitor C_B was replaced by ceramic capacitor C_{R1} = 4.7[μF] and original voltage feedback was disconnected from UCC28180 controller without any further evaluation board modifications. Auxiliary DC-DC converter shown in Fig. 4(b) was designed according to Table I with C_{R2} = 4.7[μF]. Switches S_1 and S_2 were implemented by Infineon 20N60C3 MOSFETs and auxiliary inductor current was sensed via a LEM Ltsr-15 Hall sensor. TMS320F28332 digital signal processor (DSP) was utilized as ACRC controller (cf. Fig. 4(c)).

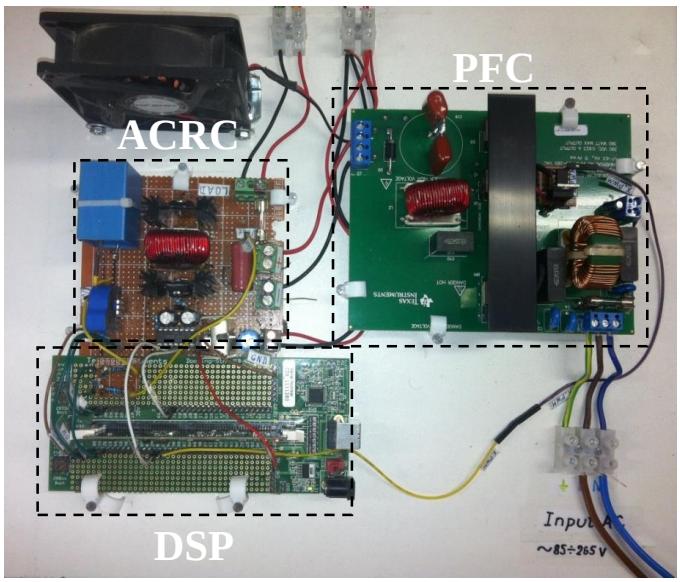


Fig. 14. Experimental setup.

The switches were driven by two of DSP PWM output ports via International Rectifier IR 2113 driver. The three measured signals (v_{DC}, v_A, i_A) were sampled by DSP A/D ports at switching frequency while the synthesized voltage feedback signal v_{PFC}^{FB} fed to

UCC28180 controller was output via DSP PWM output (realizing 1-bit D/A). Experimental setup is pictured in Fig. 14.

A. Soft start

It should be emphasized that the UCC28180EVM-573 evaluation board circuitry employs an embedded soft start sequence. Hence, v_{DC} rather than modified v_A is fed back to the PFC controller feedback during soft start as v_{PFC}^{FB} (i.e. original evaluation board functionality is restored) to enable normal execution of the embedded soft start sequence. At the same time, ACRC converter switches are driven with constant duty cycle PWM signals calculated so that when DC link voltage reaches V_{DC}^*, auxiliary capacitance voltage reaches V_A^*. Once DC link voltage is equal to its rated value, soft start sequence is completed and the system begins executing the proposed algorithm by providing modified v_A (cf. (57)) to PFC controller and v_{DC} to ACRC voltage controller as corresponding feedback signals.

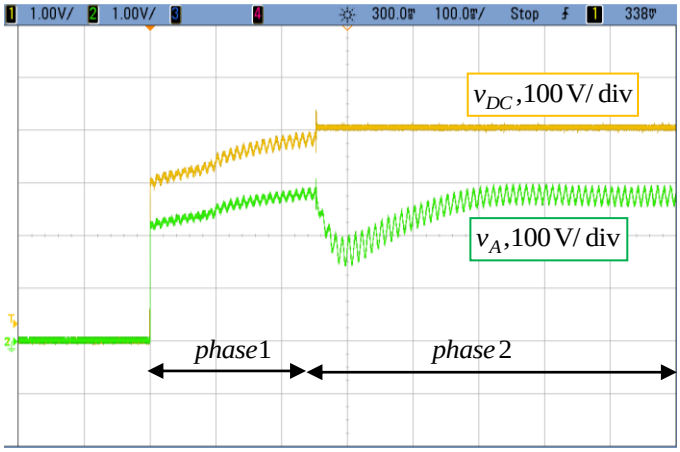


Fig. 15. Experimental result. Soft start under 50W load.

Experimental result of the soft start sequence under 50W load is shown in Fig. 15. During phase 1, DC link voltage possesses significant ripple, as expected from PFC pre-converter terminated by small ceramic capacitor C_R under slow voltage loop of

~10Hz. Once phase 2 begins, DC link voltage becomes tightly regulated to 400V by 800Hz bandwidth ACRC voltage loop. At the same time, auxiliary capacitor C_A begins absorbing the pulsating power component while its voltage average becomes regulated to 271V after a noticeable transient, reflecting the slow voltage loop of the PFC.

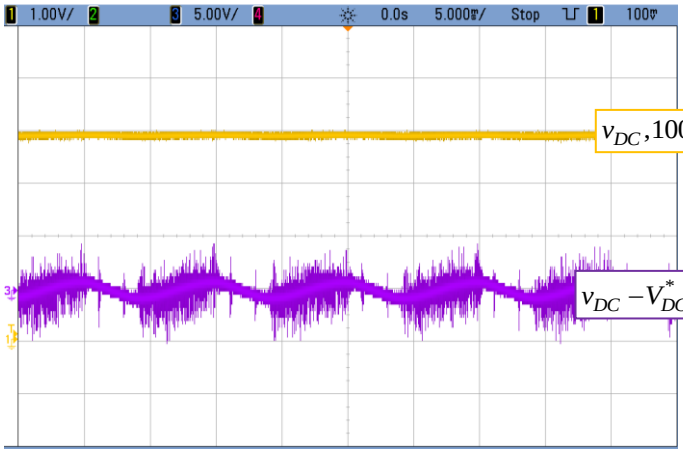
B. Steady state operation

Steady-state operation results (DC link voltage and corresponding ripple) of the original bulk-capacitor-terminated PFC under different load levels are shown in Figs. 16(a)-(c) for subsequent comparison with the proposed system performance. The DC link ripple values are slightly higher than predicted by (15) and Fig. 12 due to non-unity efficiency (97% efficiency is attained by the off-the-shelf PFC front end under rated load operation). Measured peak-to-peak value of DC link ripple under rated load appears to be circa 14V.

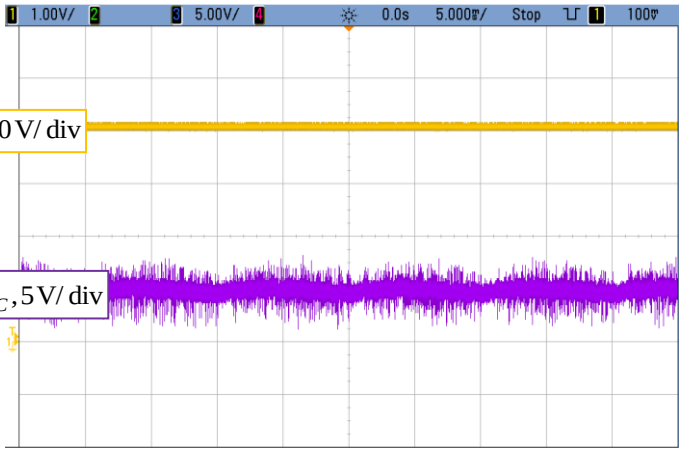
Steady-state operation results of the proposed system (with both GS and FF actions) under different load levels are shown in Figs. 16(d)-(f). It may be concluded that DC link ripple of the proposed system is noticeably lower than of the original electrolytic capacitor based system. Measured peak-to-peak value of the proposed system DC link ripple under rated load is circa 6V, which again is slightly higher than predicted by simulation (Fig. 12) due to non-unity efficiency (92.5% efficiency was attained by the combined system under rated load operation, corresponding to ~95% efficiency of the ACRC). Nevertheless, peak-to-peak ripple improvement ratio matches that of the simulation. It must be emphasized that the ACRC prototype was not optimized for efficiency, i.e. the losses may be further decreased.

Fig. 17 demonstrates the contribution of FF and GS actions to the proposed system performance. As predicted by simulation results in Fig. 12, marginal performance improvement caused by the addition of FF term to the basic dual loop operation is more

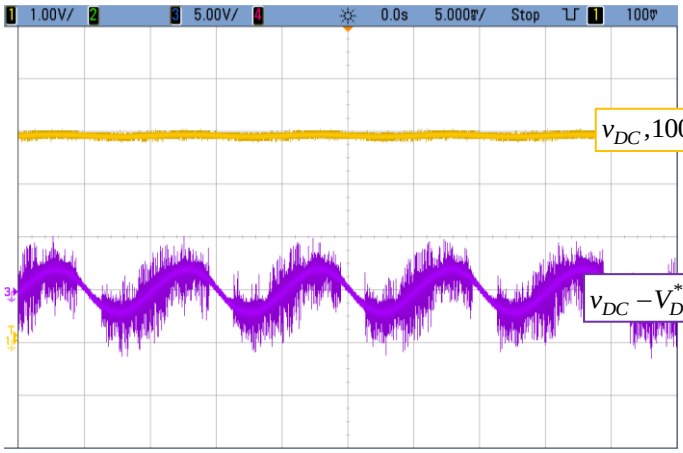
significant than subsequent introduction of GS action. Moreover, the behavior of auxiliary capacitance voltage is similar in all the three cases, as predicted.



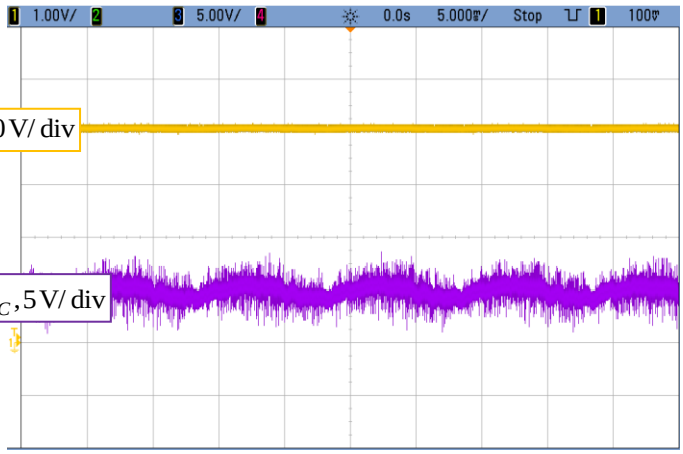
(a) with C_B, 50W load



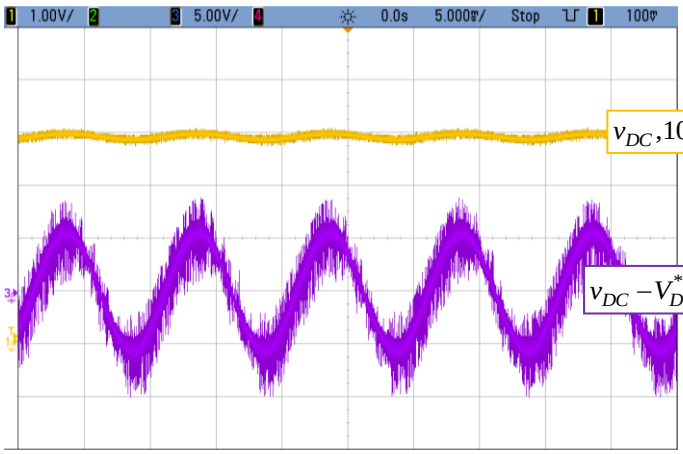
(d) with C_A, 50W load



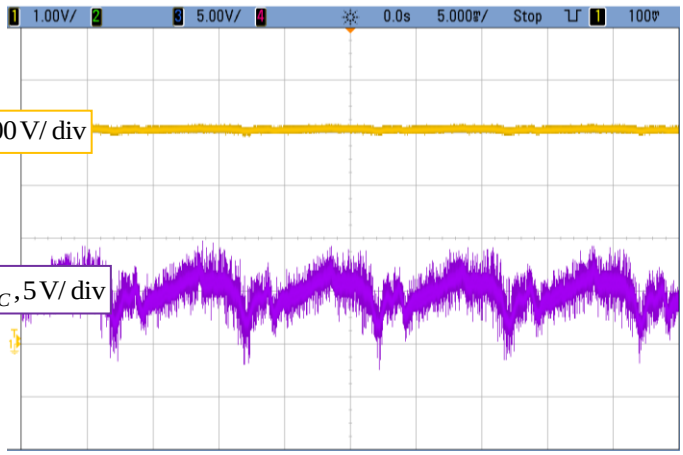
(b) with C_B, 150W load



(e) with C_A, 150W load

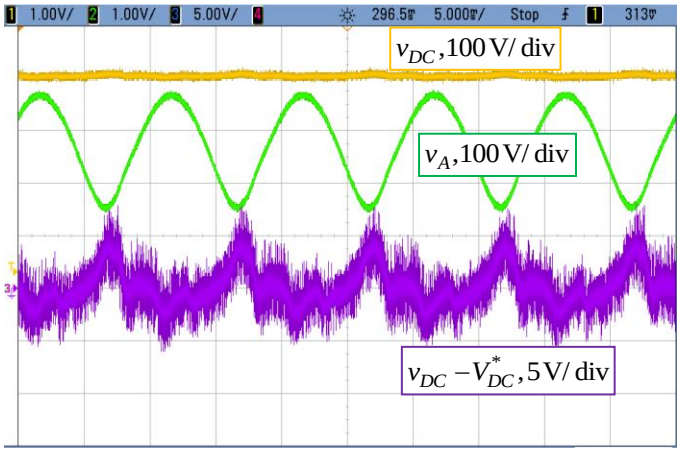


(c) with C_B, 350W load

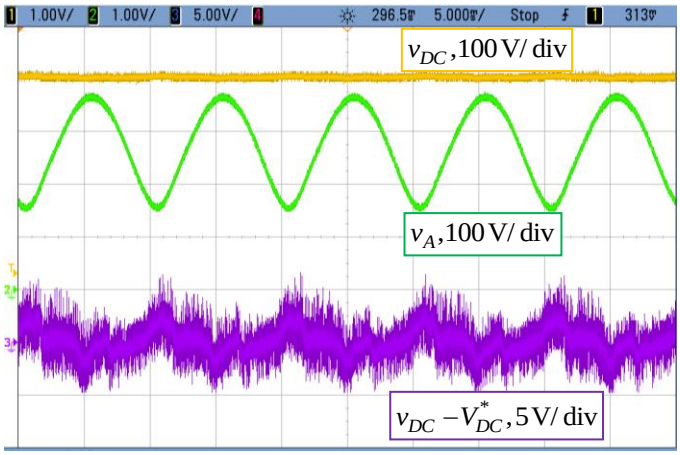


(e) with C_A, 350W load

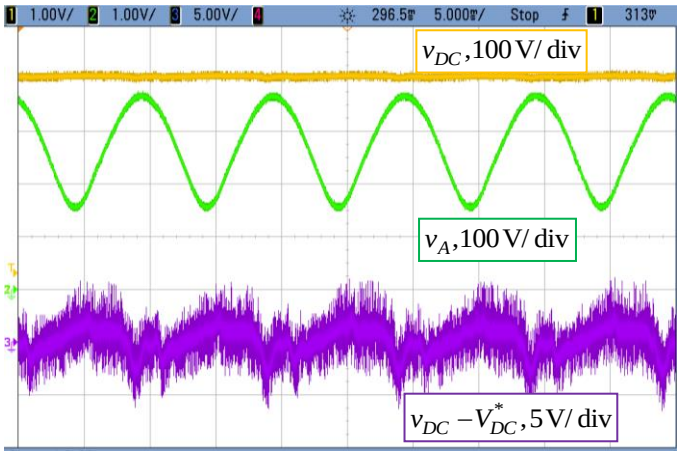
Fig. 16. Experimental results. Steady state DC link voltage comparison of original and proposed systems for different load levels.



(a) ACRC.



(b) ACRC-FF.



(c) ACRC-FF-GS.

Fig. 17. Experimental results. Steady state performance comparison of three ACRC control schemes under rated load operation.

C. Transients handling

It is well-known that one of the main ACRC drawbacks is abridged hold-up ability, translated into poor handling of abrupt transient events. In classical systems, transient energy upon sudden load change is supplied/absorbed by the bulk DC link capacitor until the slow voltage loop of the GIC takes over. In ACRC-based systems, energy content of the auxiliary capacitor is much lower than that of the classical DC link bulk capacitor. Moreover, while DC link capacitor voltage remains around 400V in steady state, auxiliary capacitance voltage pulsates between two distant extremes (cf. Eqs. 17 and 18). This poses the following trade-off: increasing v_A^{MAX} and/or decreasing v_A^{MIN} decreases the value of auxiliary capacitance while increasing the possibility of poor transient response.

Transients handling (response to step-like variations of load power) of the proposed system is demonstrated in Fig. 18. As expected, upon sudden load increase, energy stored in the auxiliary capacitance is insufficient to compensate the load demand. As a result, auxiliary voltage collapses to zero while DC link voltage drops significantly since only the small DC link capacitor C_R supplies the load power when C_A is empty. Once PFC voltage loop reacts, DC link voltage is quickly restored (due to the fast ACRC voltage loop) while the auxiliary capacitance is refilled relatively slow (at PFC voltage loop rate). The opposite happens upon sudden load decrease. Auxiliary capacitance absorbs the excessive energy supplied by PFC and its voltage rises. Once it reaches the DC link voltage value, C_A and C_R become shortened through the anti-parallel diodes of the auxiliary converter switches and rise together. At this point, overvoltage protection embedded into the PFC controller is tripped and PFC output is forced to reduce. Once power balance is restored, the system returns to normal operation. DC link voltage transient performance of the original and the proposed

systems are depicted in Fig. 19. As expected, while operating with lower steady-state ripple, the proposed system possesses higher transient peaks than the original bulk DC link capacitance-terminated PFC front end. Apparently, abrupt transient handling is problematic and needs to be further investigated for possible improvement.

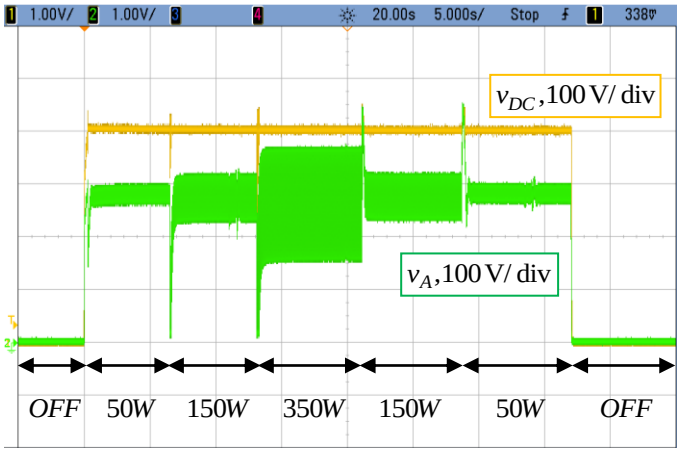
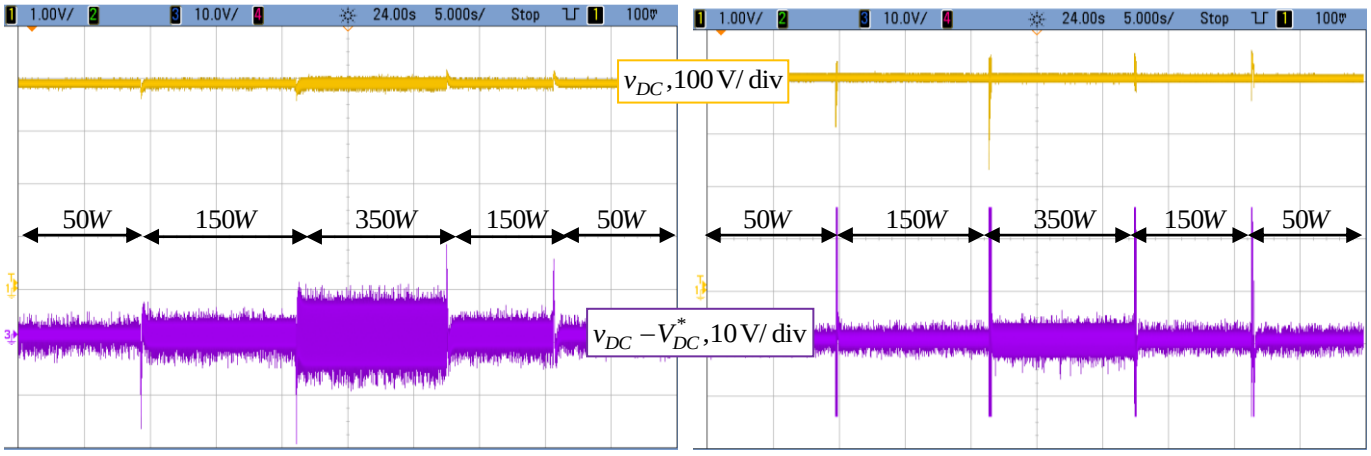


Fig. 18. Experimental result. Performance of the proposed system under load transients.



(a) with C_B **(b) with C_A**

Fig. 19. Experimental results. Performance comparison of the original and the proposed system under load transients.

D. PFC voltage feedback manipulation

As mentioned in the preceding Section, in order to feed the auxiliary capacitance voltage back to PFC controller, it must be manipulated according to (57) to suppress the ripple and preserve the original loop gain. Fig. 20 demonstrates auxiliary

capacitance voltage v_A along with its manipulated version v_{PFC}^{FB} during load power variation induced transient. Apparently, while the former possesses significant ripple and regulated to 271V in steady state, the latter is nearly ripple-free with 5V average in steady state, as required.

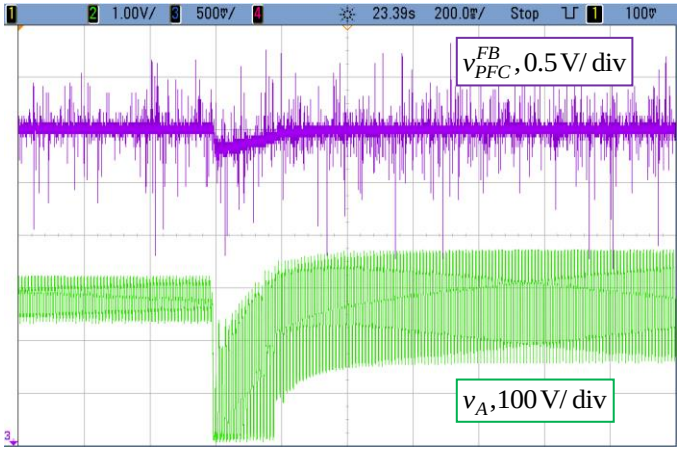


Fig. 20. Experimental result. Auxiliary capacitance voltage v_A and its modified version v_{PFC}^{FB}.

V. CONCLUSION

Modeling of a direct voltage regulated active DC link capacitance reduction circuit for grid interfacing converters and subsequent controller design were revealed in the paper. Unlike common solutions, aimed to reduce the pulsating component of DC link current, the main task of the proposed system is directly regulating the DC link voltage. Under such an operation, the system was shown to resemble an output-voltage regulated wide-input-range boost converter feeding a bi-directional power load. Control design appeared to be non-trivial since the resulting transfer function of the plant undergoes significant changes throughout the operational region and is unstable during power absorbing phase. Dual-loop control structure with current feedforward and voltage gain scheduling was formed to cope with the control challenge. Experimental results of applying the proposed system to DC link regulation of an off-the-shelf PFC front end support the suggested control structure. Future work on the subject will focus on transient events handling improvement.

REFERENCES

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Kluwer Academic, 2001.

[2] H. Wen et al., "Analysis and evaluation of DC-link capacitors for high power density electric vehicle drive systems," *IEEE Trans. Veh. Technol*., vol. 61, no. 7, pp. 2950 – 2964, Sep. 2012.

[3] W. Huai and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569-3578, Sep.-Oct. 2014.

[4] J. L. Stevens *et al*., "The service life of large aluminum electrolytic capacitors: effects of construction and application," *IEEE Trans. Ind. Appl.*, vol. 38, no. 5, pp.1441-1446, Sep.-Oct. 2002.

[5] M. A. Vogelsberger *et al*., "Life-cycle monitoring and voltage-managing unit for DC-link electrolytic capacitors in PWM converters," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 493-503, Feb. 2011.

[6] H. Lei and N. Narendran, "An accelerated test method for predicting the useful life of an LED driver," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2249-2257, Aug. 2011.

[7] R. Wang et al., "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron*., vol. 26, no. 5, pp. 1430-1443, May 2011.

[8] M. Vasiladiotis and A. Rufer, "Dynamic analysis and state feedback voltage control of single-phase active rectifiers with DC-link resonant filters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5620-5633, Oct. 2014.

[9] G. Linlin *et al*., "Means of eliminating electrolytic capacitor in AC/DC power supplies for LED lightings," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1399-1408, May 2009.

[10] Y. Kai et al., "Reducing storage capacitor of a DCM boost PFC converter," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 151-160, Jan. 2012.

[11] W. Beibei et al., "A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less AC–DC drivers," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 592-601, Mar. 2010.

[12] W. Yao, X. Wang, P. C. Loh, X. Zhang and F. Blaabjerg, "Improved power decoupling scheme for single-phase grid-connected differential inverter with realistic mismatch in storage capacitances," *IEEE Trans. Power Electron*., vol. 32, no. 1, pp. 186 – 199, Jan. 2017.

[13] I. Serban, "Power decoupling method for single-phase H-bridge inverters with no additional power electronics," *IEEE Trans. Ind. Electron*., vol. 62, no. 8, pp. 4805 – 4813, Aug. 2015.

[14] D. B. W. Abeywardana, B. Hredzak and V. G. Agelidis, "An input current feedback method to mitigate the DC-side low frequency ripple current in a single-phase boost inverter," *IEEE Trans. Power Electron*., vol. 31, no. 6, pp. 4594 – 4603, Jun. 2016.

[15] G.-R. Zhu, S.-C. Tan, Y. Chen and C. K. Tse, "Mitigation of low-frequency current ripple in fuel-cell inverter systems through waveform control," *IEEE Trans. Power Electron*., vol. 28, no. 2, pp. 779 – 792, Feb. 2013.

[16] W. Cai, L. Jiang, B. Liu, S. Duan and C. Zou, "A power decoupling method based on four-switch three-port DC/DC/AC converter in DC microgrid," *IEEE Trans. Ind. Appl*., vol. 51, no. 1, pp. 336 – 343, Jan. 2015.

[17] Q. C. Zhong and W. L. Ming, "A theta-converter that reducs common mode currents, output voltage ripples and total capacitance required," *IEEE Trans. Power Electron*., vol. 31, no. 12, pp. 8435 – 8447, Dec. 2016.

[18] X. Du et al., "DC link active power filter for three-phase diode rectifier," *IEEE Trans. Ind. Electron*., vol. 59, no. 3, pp. 1430-1442, Mar. 2012.

[19] W. Cai et al., "An active low-frequency ripple control method based on the virtual capacitor concept for BIPV systems," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1733-1745, Apr. 2014.

[20] W. Rong-Jong and L. Chun-Yu, "Active low-frequency ripple control for clean-energy power-conditioning mechanism," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3780-3792, Nov. 2010.

[21] J.-I. Itoh, and F. Hayashi, "Ripple current reduction of a fuel cell for a single-phase isolated converter using a DC active filter with a center tap," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 550-556, Mar. 2010.

[22] W. Chen and S. Hui, "Elimination of an electrolytic capacitor in AC/DC light-emitting diode (LED) driver with high input power factor and constant output current," *IEEE Trans. Power Electron*., vol. 27, no. 3, pp. 1598 – 1607, Mar. 2012.

[23] C. Xin et al., "Ripple eliminator to smooth DC-bus voltage and reduce the total capacitance required," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2224-2235, Apr. 2015.

[24] M. Su, P. Pan, X. Long, Y. Sun and J. Yang, "An active power decoupling method for single-phase AC-DC converters," *IEEE Trans. Ind. Inform*., vol. 10, no. 1, pp. 461 – 468, Feb. 2014.

[25] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin and P. Wang, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," *IEEE Trans. Power Electron*., vol. 30, no. 4, pp. 1855 – 1865, Apr. 2015.

[26] Y. Ohnuma, K. Orikawa and J. Itoh, "A single-phase current source PV inverter with power decoupling capability using and active buffer," *IEEE Trans. Ind. Appl*., vol. 51, no. 1, pp. 531 – 538, Jan. 2015.

[27] G.-R. Zhu, H. Wang, B. Liang, S.-C. Tan and J. Jiang, "Enhanced single-phase full-bridge inverter with minimal low-frequency current ripple," *IEEE Trans. Ind. Electron*., vol. 63, no. 2, pp. 937 – 943, Feb. 2016.

[28] W. Huai et al., "Use of a series voltage compensator for reduction of the DC-link capacitance in a capacitor-supported system," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1163-1175, Mar. 2014.

[29] W. Liu et al., "Modeling and design of series voltage compensator for reduction of DC-link capacitance in grid-tie solar inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2534-2548, May 2015.

[30] P. T. Krein et al., "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690-4698, Nov. 2012.

[31] Y. Sun, Y. Liu, M. Su, W. Xiong and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron*., vol. 31, no. 7, pp. 4778 – 4794, Jul. 2016.

[32] S. Li, A. Lee, S.-C. Tan and S. Y. Hui, "A plug-and-play ripple mitigation approach for DC-links in hybrid systems," in Proc. *Applied Power Electroics Conf. (APEC)*, Long Beach, USA, 20 – 24 Mar., 2016.

[33] S. Li, W. Qi, S. C. Tan and S. Y. R. Hui, "Integration of an active filter and a single-phase AC/DC converter with reduced capacitance requirement and component count," *IEEE Trans. Power Electron*., vol. 31, no. 6, pp. 4121–4137, Jun. 2016.

[34] Y. Tang, Z. Qin, F. Blaabjerg and P. C. Loh, "A dual voltage control strategy for single-phase PWM converters with power decoupling function," *IEEE Trans. Power Electron*., vol. 30, no. 12, pp. 7060–7071, Dec. 2015.

[35] W. Qi, H. Wang, X. Tan, G. Wang and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in Proc. *Applied Power Electroics Conf. (APEC)*, Fort Worth, USA, 16 – 20 Mar., 2014.

[36] E. Mickus, T. T. Vu and T. O'donnel, "A low-profile, high power density inverter with minimal energy storage requirement for ripple cancellation," in Proc. *7th IEEE Int. Symp. Power Electron Dist. Gen. Syst. (PEDG)*, Vancouver, Canada, 27-30 Jun., 2016.

[37] G. Yona and G. Weiss, "The virtual infinite capacitor," *Int. J. Contr.*, vol. 90, no. 1, pp. 78 – 89, 2017.

[38] M. Mellincovsky, V. Yuhimenko, M. M. Peretz and A. Kuperman, "A novel approach to active DC link capacitance reduction for single phase power factor correction circuits," in Proc. *Power Electronics Machines and Drives Conf. (PEMD)*, Glasgow, Scotland, 19 – 21 Apr., 2016. Available for dowloading at: http://www.filedropper.com/pemd2016fullpapermartin.

[39] M. Mellincovsky, V. Yuhimenko, M. M. Peretz and A. Kuperman, "Infinite virtual capacitor realization for grid-connected power converters," in Proc. *IEEE Int. Conf. Sci. Electr. Eng. (ISCEE)*, Nov. 16 – 18, Eilat, Israel, 2016

[40] J. Zeng, Z. Zhang and W. Qiao, "An interconnection and damping assignment passivity-based controller for a DC-DC boost converter with a constant power load," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2314 – 2322, Jul. 2014.

[41] J. A. Solsona, S. G. Jorge and C. A. Busada, "Nonlinear control of a buck converter which feeds a constant power load," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7193 – 7201, Dec. 2015.

[42] S. Singh, D. Fulwani and V. Kumar, "Robust sliding-mode control of dc/dc boost converter feeding a constant power load," *IET Power Electron.*, vol. 8, no. 7, pp. 1230 – 1273, 2015.

[43] Y. Li, K. R. Vannorsdel, A. J. Zirger, M. Norris and D. Maksimovic, "Current mode control for boost converters with constant power loads," *IEEE Trans. Circ. Syst. – I: Reg. Papers*, vol. 59, no. 1, pp. 198 – 206, Jan. 2012.

[44] D. De and V. Ramanarayanan, "A proportional+multiresonant controller for three-phase four-wire high-frequency link inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 899 – 906, Apr. 2010.

[45] D. G. Holmes, T. A. Lipo, B. P. McGrath and W. Y. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417 – 2426, Nov. 2009.

[46] http://www.ti.com/lit/ds/symlink/ucc28180.pdf.

[47] http://www.ti.com/tool/ucc28180evm-573.