High-Efficiency, High Step-Up DC–DC Converters

Qun Zhao, *Student Member, IEEE,* and Fred C. Lee, *Fellow, IEEE*

***Abstract*—Many applications call for high step-up dc–dc converters that do not require isolation. Some dc–dc converters can provide high step-up voltage gain, but with the penalty of either an extreme duty ratio or a large amount of circulating energy. DC–DC converters with coupled inductors can provide high voltage gain, but their efficiency is degraded by the losses associated with leakage inductors. Converters with active clamps recycle the leakage energy at the price of increasing topology complexity. A family of high-efficiency, high step-up dc–dc converters with simple topologies is proposed in this paper. The proposed converters, which use diodes and coupled windings instead of active switches to realize functions similar to those of active clamps, perform better than their active-clamp counterparts. High efficiency is achieved because the leakage energy is recycled and the output rectifier reverse-recovery problem is alleviated.**

***Index Terms*—Coupling inductor, dc–dc conversion, reverse recovery, voltage gain.**

I. Introduction

MANY applications powered by batteries call for high-performance, high step-up dc–dc converters. As an example, for a high intensity discharge (HID) lamp ballast used in automotive headlamps in which the start-up voltage is up to 400 V [1], [2], the dc–dc converter needs to boost the 12 V of the battery voltage up to 100 V during steady-state operation. Fig. 1(a) shows the diagram of a HID ballast. Another example of a high step-up application is the front-end converter with dual inputs, as shown in Fig. 1(b). The convergence of computer and telecommunications industries makes the well-defined −48 V battery plant a good choice for offering hours of reserve time during outages of the ac mains [3]–[5]. Although both powered by the −48 V dc power plant, the dc-input converter is more efficient and less complex than the uninterruptible power supply (UPS) [3], [5], [6]. The dc-input converter must boost the 48 V of the dc bus voltage to about 380–400 V. Generally speaking, the high step-up dc–dc converters for these applications have the following common features.

1) High step-up voltage gain. Generally, about a tenfold step-up gain is required.
2) High efficiency.
3) No isolation is required.

There are two major concerns related to the efficiency of a high step-up dc–dc converter: large input current and high output voltage. The large input current results from low input voltage; therefore, low-voltage-rated devices with low $R_{DS\text{-}on}$ are necessary in order to reduce the conduction loss. Another concern is the severe reverse-recovery problem that occurs in the output rectifier due to the high output voltage. The boost and buck–boost converters are the simplest nonisolation topologies. Unfortunately, the switch sustaining the high output voltage has a high $R_{DS\text{-}on}$. Furthermore, the short pulse current with high amplitude that flows through the output rectifier due to extreme duty ratio induces a severe rectifier reverse-recovery problem. The high $R_{DS\text{-}on}$ of the switch and the severe rectifier reverse-recovery problem limit the output power [5]. The nonisolation converters [7] can provide high step-up voltage gain without incurring extreme duty ratios. For the third-order two-switch converter, the voltage gain is infinite when the duty is equal to 0.5. The basic idea behind this group of circuits is to store sufficient energy in the inductors by assembling the input and output voltage sources so that they are in series during switch-on time. However, having the output voltage source charge the inductor introduces high levels of circulating current. The voltage stress of the switch is $2V_o + V_i$. The high $R_{DS\text{-}on}$ of the switch and the huge circulating current make it extremely difficult to achieve decent efficiency. One attractive solution is the two-cascade boost converter. Although there are two energy-processing steps, the efficiency of the two-cascade continuous-current-mode (CCM) boost converters can still be very high [5]. The major drawback to this solution is the complexity resulting from the two sets of active switches, the magnetic components and the controllers. The controllers must be synchronized to avoid the beat frequency, and the stability of the converter is also a concern [8]. Due to the high levels of both output power and output voltage, the output rectifier of the second boost stage has a severe reverse-recovery problem, which not only degrades efficiency but also causes EMI noise.

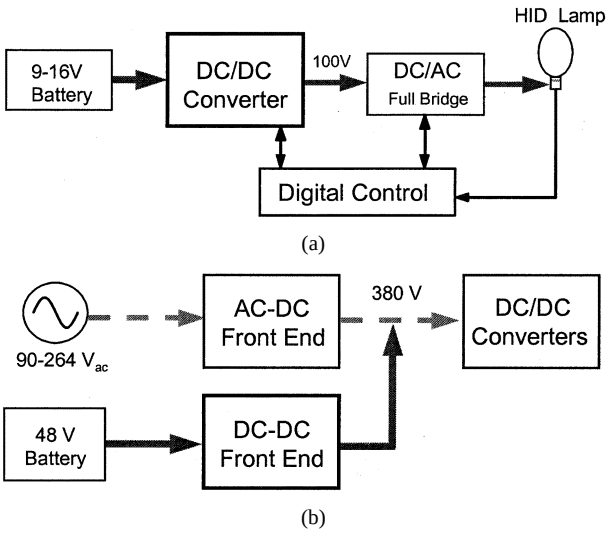

Fig. 1. Applications of high step-up dc–dc converters: (a) HID lamp ballast and (b) dual-input front-end converters.

Manuscript received March 18, 2001; revised August 28, 2002. This work was supported by Philips Research and the ERC Program of the National Science Foundation under Award EEC-9731677. Recommended by Associate Editor K. Smedley.

The authors are with the Center for Power Electronics Systems, The Bradley Department of Electrical Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061-0111 USA.

Digital Object Identifier 10.1109/TPEL.2002.807188

Instead of nonisolation converters or cascade dc–dc converters, those with coupled inductors, such as flyback or isolation Sepic converters, could be used [1], [9], [10]. Converters with coupled inductors can easily achieve high step-up voltage gain, utilizing low $R_{DS\text{-}on}$ switches at low power levels. However, the leakage energy induces high voltage stress, large switching losses and severe EMI problems. An active-clamp circuit can recycle the leakage energy with minimal voltage stress to the main switch, but at the cost of topology complexity and some losses related to the clamp circuit [11], [12]. Adding the active-clamp switch and the floating gate driver increases both the circuit complexity and the cost. Any accidental overlap between the main and active-clamp switch gate-drive signals could lead to a fatal failure of the circuit. The efficiency improvement is limited because the high current through the active-clamp switch can induce high conduction loss.

This paper presents a family of high-efficiency, high step-up clamp-mode converters without extreme duty ratios. By only adding one additional diode and a small capacitor, the proposed converters' operation is similar to that of their active-clamp counterparts, but with better performance. In the proposed converters, the additional diode serves as the body diode of the active-clamp switch. The coupled winding and output rectifier together act as a switch similar to a magnetic switch [13], [14], serving the same function as the active-clamp switch. Topologies with one active switch have significantly reduced cost and circuit complexity compared to those using the active-clamp scheme. Therefore, the reliability of the converter could be dramatically increased. The proposed clamp-mode coupled-inductor converters can use a low-voltage-rated switch to minimize the conduction loss. The clamp circuit recovers the leakage energy and has a lower circulating current. The leakage inductor can be used to control the current decrease rate di/dt of the output rectifier. Therefore, the output rectifier reverse-recovery problem is significantly alleviated. High efficiency is achieved because of the low $R_{DS\text{-}on}$ of the switch, the efficient recycling of leakage energy, and the controlled di/dt of the output rectifier.

II. Topology Derivation and Operation Analysis

Coupled-inductor converters, such as the Flyback and the isolation Sepic converter, are good candidates for high step-up applications. Although it is easy to achieve high voltage gain by employing a coupled inductor, the leakage inductance of the coupled inductor not only induces high voltage stress but also dramatically degrades efficiency. A resistor-capacitor-diode (RCD) clamp circuit can reduce the voltage stress, but the loss is high. The coupled-inductor converter with RCD clamp cannot achieve good efficiency as compared to the scheme involving lossless leakage energy recovery.

The active-clamp flyback converter can recover the leakage energy and minimize the voltage stress. Fig. 2 shows the circuit diagram and key waveforms. The drawbacks of the active-clamp solution are the topology complexity and the loss related to the clamp circuit. The active-clamp solution requires two switches and two isolated gate drivers. The current through the active-clamp switch is the high primary current, which can induce high conduction losses in the active-clamp circuit.

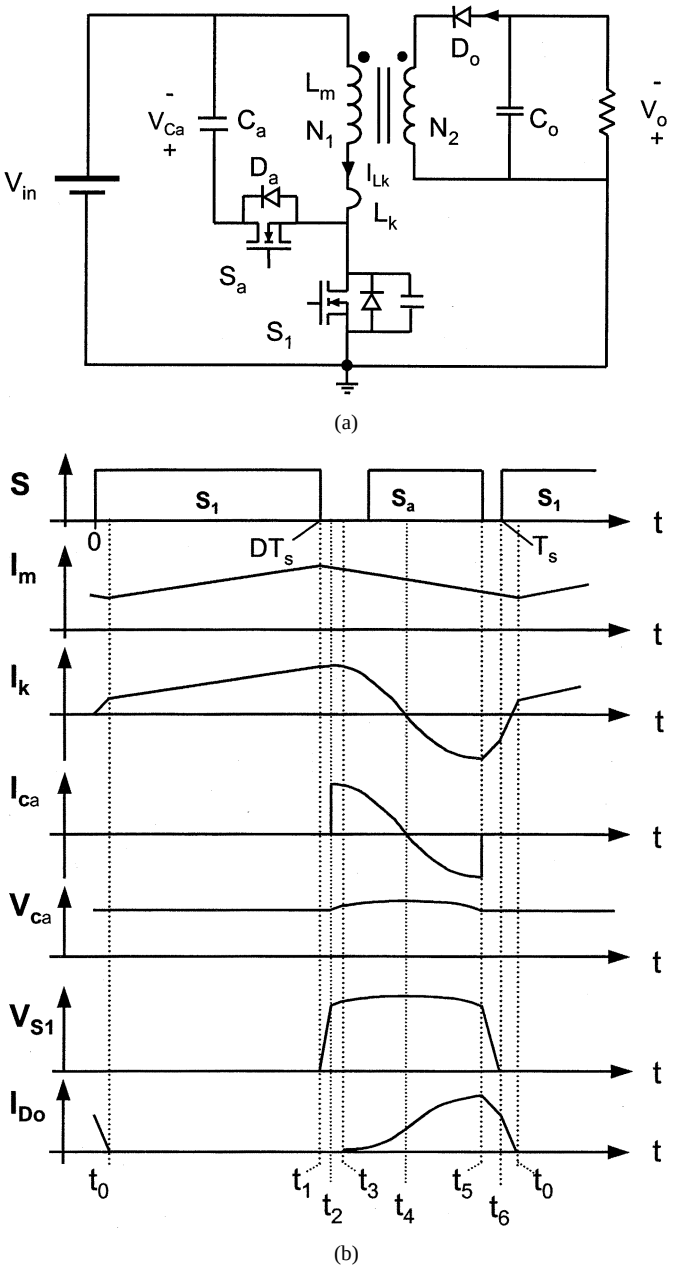

Fig. 2. Active-clamp flyback converter: (a) circuit diagram and (b) key waveforms.

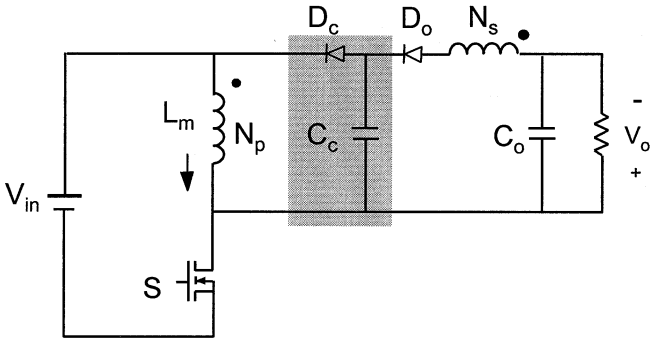

Fig. 3. Proposed clamp-mode coupled-inductor buck–boost converter.

Taking advantage of the nonisolation requirement, the proposed solution shown in Fig. 3 requires only one addi-

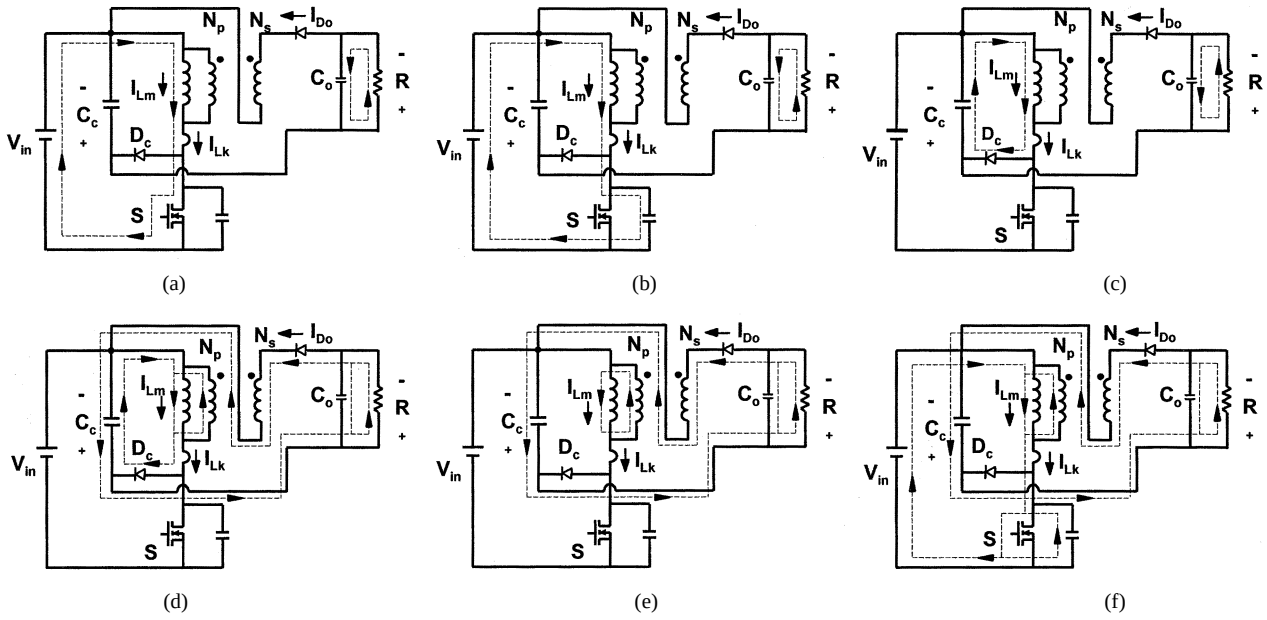

Fig. 4. Operation modes of the clamp-mode coupled-inductor buck–boost converter: (a) $[t_0,\ t_1]$, (b) $[t_1,\ t_2]$, (c) $[t_2,\ t_3]$, (d) $[t_3,\ t_4]$, (e) $[t_4,\ t_5]$ and (f) $[t_5,\ t_0]$.

tional clamp capacitor C_c and one diode D_c. The converter can achieve a level of operation comparable to that of the active-clamp scheme. The clamp capacitor C_c and the added diode D_c function as the active-clamp charging path, while the induced current in the secondary winding N_s of the coupled inductor is used to discharge the clamp capacitor C_c. Therefore, the secondary winding of the coupled inductor serves the same function as the active-clamp switch, and is referred to here as a magnetic switch.

Fig. 4 illustrates the six topological stages in one switching cycle for the proposed clamp-mode coupled-inductor buck–boost converter. The coupled inductor is modeled as a magnetizing inductor L_m, an ideal transformer with a turns ratio of $N = N_s : N_p$, and a leakage inductor L_k. The converter is redrawn to facilitate comparison with the active-clamp flyback converter. Fig. 5 shows the key waveforms. The six operation modes are briefly described as follows.

$[t_0,\ t_1]$: Switch S is on, and the output rectifier D_o is reverse-biased. Both the magnetizing inductor and the leakage inductor are linearly charged by the input voltage source V_{in}.

$[t_1,\ t_2]$: Switch S turns off at t_1. The parasitic capacitor of the switch is charged by the magnetizing current in an approximately linear way.

$[t_2,\ t_3]$: At t_2, the parasitic capacitor of switch S is charged to the voltage of $V_{in} + V_{Cc}$. Clamp diode D_c conducts. Almost all of the magnetizing current begins to charge clamp capacitor C_c.

$[t_3,\ t_4]$: At t_3, V_{Cc} is charged to the point that output diode D_o is forward-biased. The reflected voltage from the secondary winding N_s of the coupled inductor clamps the primary winding N_p. Leakage inductor L_k and clamp capacitor C_c begin to resonate.

$[t_4,\ t_5]$: At t_4, the resonant current reaches zero. All of the magnetizing current is reflected to the secondary winding N_s from the primary winding N_p. The clamp capacitor is then discharged by the output rectifier current $I_{Do}(I_{Lm}/N)$.

$[t_5,\ t_0]$: Switch S turns on at t_5. The leakage inductor L_k is quickly charged by the sum of input voltage V_{in} and the reflected voltage $(V_o - V_c)/N$ until the leakage inductor current I_{Lk} is equal to the magnetizing cur-

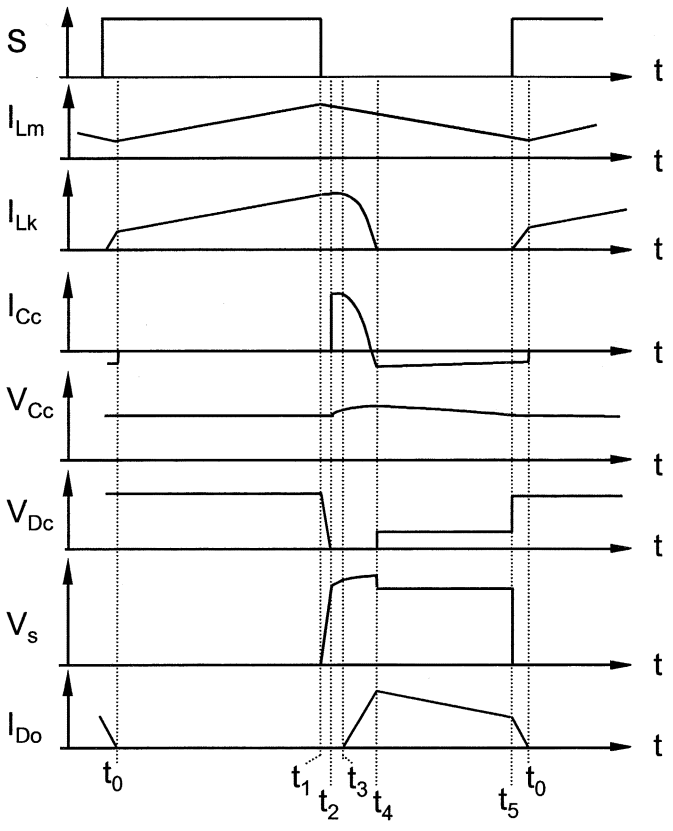

Fig. 5. Key waveforms of the clamp-mode coupled-inductor buck–boost converter.

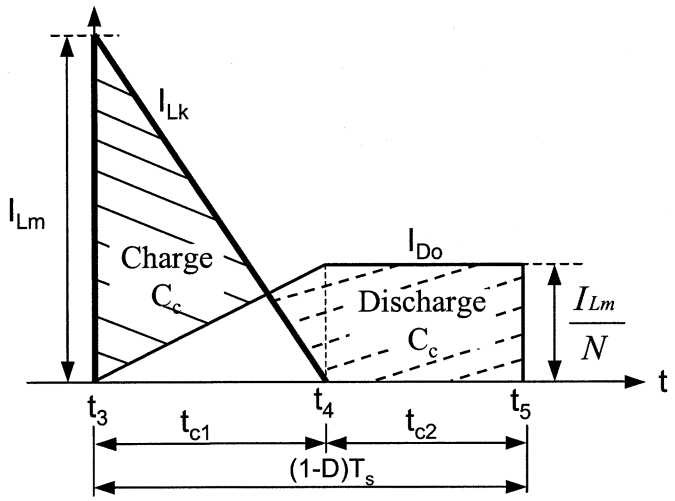

Fig. 6. Relationship of clamp capacitor charge and discharge current.

rent I_{Lm}. The output rectifier D_o is reverse-biased. Then, the next switching cycle begins.

As can be seen from the analysis, the leakage energy stored in L_k is recovered by the clamp capacitor such that the voltage of the switch is clamped. The clamp capacitor is discharged by the output rectifier current I_{Do}, which is equal to the reflected secondary current from the primary transformer winding. The primary transformer current equals the difference between the magnetizing current and the leakage inductor current. Fig. 6 shows the relationship between the clamp capacitor charge and discharge currents by assuming that the magnetizing current is ripple-free. The clamp capacitor needs to maintain a balance between charge and discharge. By making the charge area equal to the discharge area, the following relationship is found:

$$t_{c1} = \frac{2}{N+1} \cdot (1-D) \cdot T_s. \tag{1}$$

To make the following derivation simple, define K as:

$$K = \frac{L_m}{L_m + L_k}. \tag{2}$$

By applying the volt-second balance of both the magnetizing inductor and the leakage inductor, the voltage gain and the clamp capacitor voltage of the converter are given by (3) and (4), respectively. The reset time of the leakage inductor is represented by t_{c1} in (1).

$$\frac{V_o}{V_i} = \frac{d}{1-d} \cdot (N+1) \cdot \frac{(1+K)}{2} \tag{3}$$

$$V_c = \frac{d}{1-d} \cdot V_i \cdot \frac{(1+K)+(1-K) \cdot N}{2}. \tag{4}$$

The proposed converter is able to provide high step-up voltage gain without requiring an extreme duty ratio.

III. Advantages of the Proposed Converter

A. Advantages Over its Active-Clamp Counterpart

On one hand, the active-clamp scheme utilizes the entire off-time of the main switch to reset the leakage inductor. Therefore, the average voltage of the clamp capacitor is minimized.

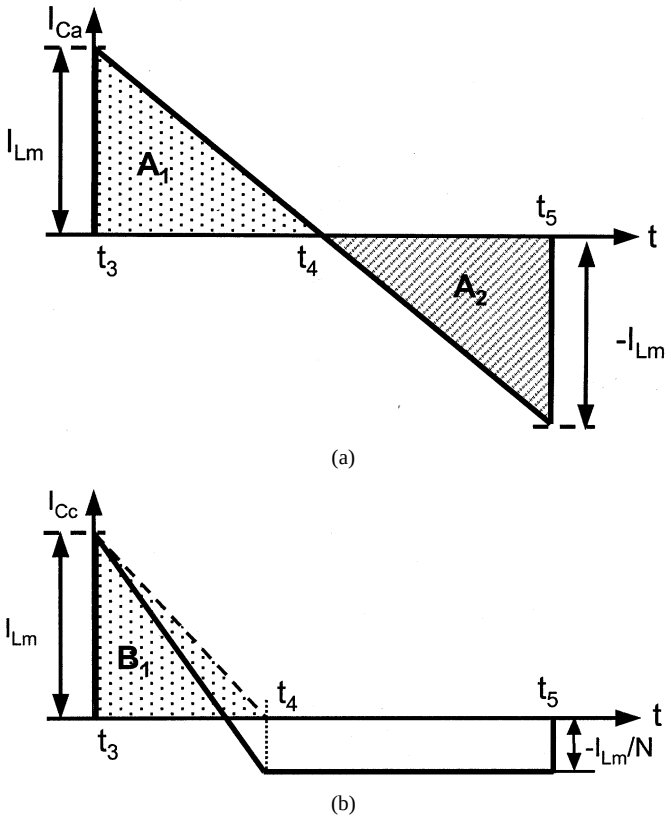

Fig. 7. Comparison of circulating energy: (a) active-clamp counterpart and (b) clamp-mode coupled-inductor buck–boost converter.

The average voltage V_{Ca} of the clamp capacitor C_a is given by (5):

$$V_{Ca} = \frac{d}{1-d} \cdot V_i. \tag{5}$$

On the other hand, a large circulating current goes through either the active-clamp switch body diode or the active-clamp switch, as shown in Fig. 2, because N_1 acts as a voltage source reflected from N_2 after D_o conducts. The leakage inductor L_k resonates with the clamp capacitor C_a. The difference between the proposed converter and its active-clamp counterpart is that the clamp capacitor is linearly discharged by the secondary reflected magnetizing current (I_{Lm}/N)during $[t_4,\ t_5]$, as shown in Fig. 5. The secondary reflected magnetizing current is much smaller than the primary magnetizing current because $N \gg 1$. The discharge period $[t_4,\ t_5]$ in the proposed converter is longer than half of the $[t_3,\ t_5]$ period in the active-clamp converter. A longer $[t_4,\ t_5]$ period makes the charge period $[t_3,\ t_4]$ shorter in the proposed converter than it is in the active-clamp scheme. Therefore, the proposed converter has less circulating energy in the additional clamp circuit.

Fig. 7 compares the proposed clamp-mode coupled-inductor buck–boost converter shown in Fig. 3 with the corresponding active-clamp scheme shown in Fig. 2 after the main switch turns off. The leakage inductor current begins to charge the clamp capacitor in both converters, with the initial current acting as the magnetizing current. For the active-clamp converter, the charge current, represented by the dotted area A_1 in Fig. 7(a), goes through the clamp switch D_a. This current is independent of

TABLE I
LOSS COMPARISON

	Reason for Loss in D_a or D_c	Reason for Loss in S_a
Active-Clamp Converter	Average of A_1	RMS of A_2
Proposed Converter	Average of B_1	N/A (=0)
Comparison	$A_1 > B_1$	$A_2 >> 0$

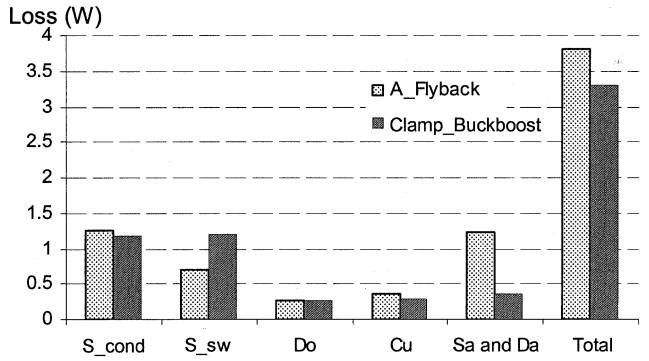

Fig. 8. Loss breakdown.

the turns ratio. But for the proposed circuit, the current going through the clamp diode D_c, represented by the dotted area B_1 in Fig. 7(b), is much smaller than it is in the active-clamp converter. Unlike the active-clamp circuit, the current going through the clamp capacitor in the proposed circuit depends on the turns ratio: The larger the turns ratio, the smaller the current. Another advantage of the proposed circuit can be observed after the charge current decreases to zero. In the active-clamp converter, the reversed discharge current goes through the active-clamp switch S_a, which is a high primary-side current when the input voltage is low, as shown by the area of A_2 in Fig. 7(a). This part of the circulating energy results in a high conduction loss in the active-clamp switch. In the proposed circuit, the current goes directly to the output filter through the output rectifier D_o. The loss related to the clamp switch is zero. Table I summarizes these comparisons.

Fig. 8 illustrates the loss breakdown comparison of the proposed converter and the active-clamp converter. The operation conditions are: $V_{in} = 12$ V, $V_o = 90$ V, $P_o = 36$ W, and $F_s = 100$ KHz. As can be seen, the active-clamp flyback converter has less switching loss due to its zero-voltage-switching (ZVS) turn-on, but the high primary current can result in large conduction losses. Although the proposed clamp-mode coupled-inductor converters have higher switching losses, the loss in the clamp switch is much less. Therefore, the efficiency is higher in the clamp-mode coupled-inductor converters than in the active-clamp flyback converters.

The proposed converter has much less clamp circuit-related loss, because the clamp capacitor voltage is higher than it is in the active-clamp solution. Fig. 9 shows the clamp capacitor voltage of the proposed converter, normalized to the clamp capacitor voltage of its active-clamp counterpart. The difference between the clamp capacitor voltage and the primary winding voltage resets the leakage inductor. Fortunately, the leakage inductance is small, so the extra reset voltage does not need to be high. In fact, the small extra voltage stress in the proposed

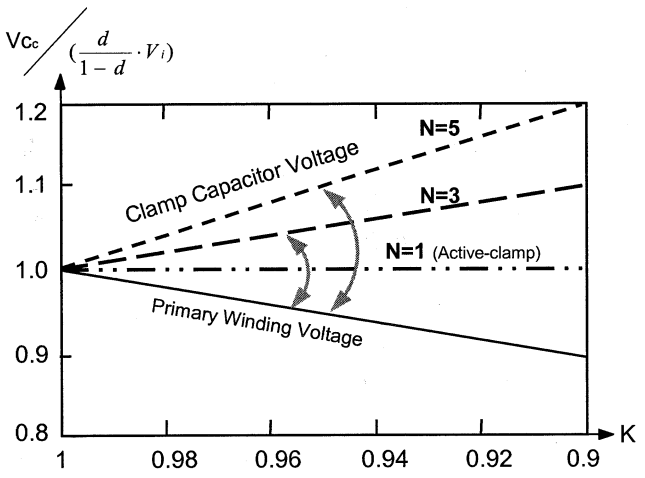

Fig. 9. Normalized clamp capacitor voltage.

converter does not have to change the device voltage rating as it does in the active-clamp converter.

B. Advantages Over the Non-Isolation DC–DC Converters

During the time period $[t_3, t_4]$, the maximum voltage applied to the switch is $V_{in} + V_c$. This voltage is given by

$$V_{DS} = V_i + \frac{d}{1-d} \cdot V_i \cdot \frac{(1+K) + (1-K) \cdot N}{2}. \quad (6)$$

Because of the high step-up features of the application requirements, the conduction loss resulting from high input current is a major obstacle to improving the efficiency of basic dc–dc converters, in which the minimum switch stress is the output voltage. The transformer function of coupled inductors makes the voltage stress of the switch in the proposed converter less than the output voltage. Therefore, low-voltage-rating devices with less $\mathrm{R_{DS\text{-}on}}$ could be used to reduce the conduction loss.

Another advantage of the proposed converter is that the output rectifier reverse-recovery problem can be significantly lessened. Before switch S turns on, there is no current through clamp diode D_c. Therefore, diode D_c has no reverse-recovery problem. When switch S turns on, the current decrease rate through diode D_o is controlled by the leakage inductor L_k. The rate is given by

$$\frac{dI_{Do}}{dt} = \frac{V_i}{L_k} \cdot \left(1 + \frac{d}{1-d} \cdot K\right). \quad (7)$$

Because the input voltage is generally low, this controlled rate could be very low. Although the output rectifier has high forward current and high reverse voltage, the output rectifier reverse-recovery problem can be dramatically alleviated due to the slow current decrease rate.

IV. TOPOLOGY VARIATIONS

The proposed concept can be applied to other step-up converters. Fig. 10 shows how to apply the same concept to other coupled-inductor converters, such as boost and Sepic

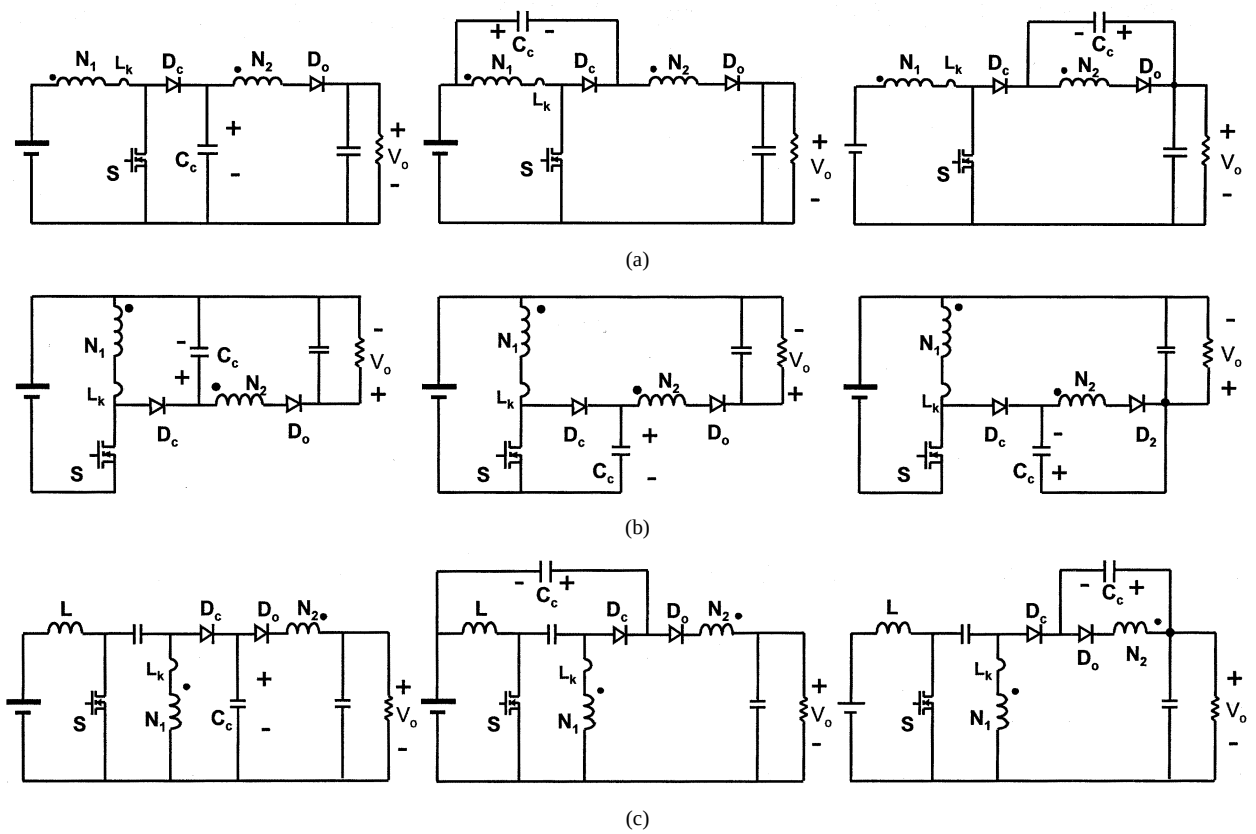

Fig. 10. Topology variations: (a) clamp-mode coupled-inductor boost converters, (b) clamp-mode coupled-inductor buck–boost converters, and (c) clamp-mode coupled-inductor Sepic converters.

converters. Each version has different variations by applying the capacitor-shifting rule. All of these converters can easily achieve high step-up voltage gains without incurring extreme duty ratios. The leakage energy is efficiently recycled by the added diode and capacitor, and is then discharged directly to the output by the secondary coupled winding. Compared to the active-clamp schemes, the proposed solutions use only one active switch to achieve the same clamp function, while dramatically reducing losses related to the clamp circuit.

V. Design Guidelines

The key design step is to determine the turns ratio that allows both a low-voltage-rated device and a sufficient safety margin. The key design equation to calculate the turns ratio is given by

$$N = \frac{V_{o\_\max}}{V_{DS} - V_{i\_\min}} - 1. \tag{8}$$

Fig. 11 is the design graph targeted at dc–dc front-end converters for HID ballasts with 9–16 V input voltage and 60–100 V output voltage (start-up voltage 400 V). The horizontal axis and the left vertical axis of Fig. 11 show the relationship between switch voltage stress and input voltage using different turns ratios. In the same graph, the relationship between duty ratio and input voltage under different turns ratios is shown on the horizontal axis and the right vertical axis. After the turns ratio is defined, the corresponding duty ratio can be determined from Fig. 11. The voltage rating of the output rectifier and the clamp capacitor can be easily calculated. The design must make

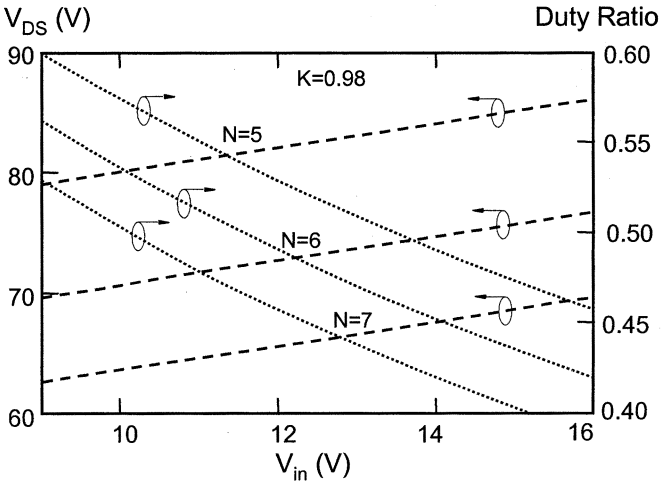

Fig. 11. Design graph to determine the turns ratio and duty ratio.

a tradeoff between the switch and rectifier voltage stress. The optimized design can be achieved by carrying out the process shown in Fig. 12. The loss-analysis mechanism is based on the switching-cycle performance [15].

VI. Experimental Verifications

As shown in Fig. 3, a converter targeted at the HID lamp ballast application is built. Because the converter must generate 400 V open-circuit voltage to ignite the HID lamp, the voltage rating of the selected active switch is 100 V. The maximum

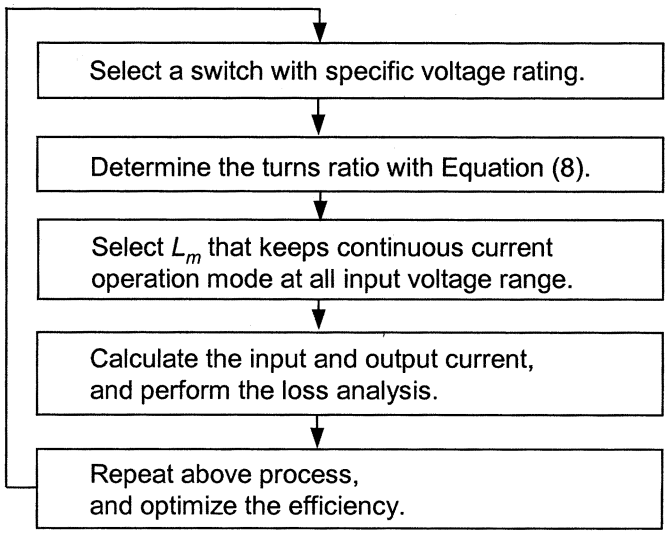

Fig. 12. Optimization procedure.

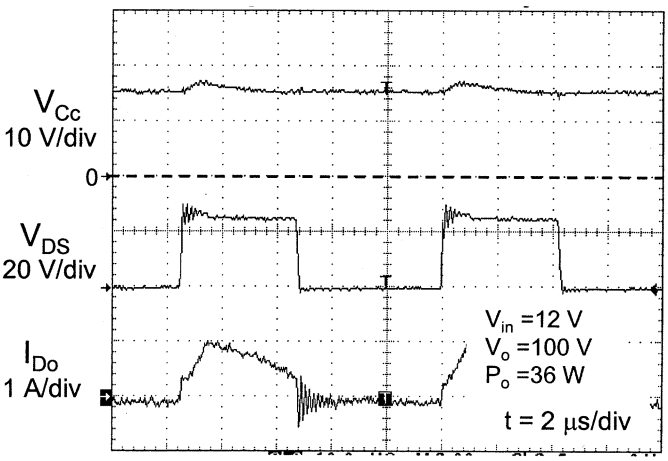

Fig. 13. Experimental waveforms of the dc–dc converter for use in HID ballasts.

voltage stress is designed to be 70 V when the 400 V open-circuit voltage is generated. The prototype has the following parameters:

$$N_1 = 14T,\ N_2 = 82T, \text{ and } C_c = 1.36\ \mu F$$

S is IRF1310, D_o is MUR860, and D_c is 3 A, 100 V Schottky diode.

Fig. 13 shows the experimental waveforms of the proposed circuit. The waveforms agree with the analysis, and the voltage of the switch is effectively clamped.

Fig. 14 shows that the voltage stress is about 70 V when the 400 V start-up output voltage is generated. The 100V MOSFET has sufficient safety margins. A 100 V-voltage-rating MOSFET has much less $\mathrm{R_{DS\text{-}on}}$ than does a 500 V MOSFET.

By adopting the analysis approach based on the detailed dynamic switching performance [15], the loss analysis is conducted for three different step-up converters; these results are given in Fig. 15. For the 36 W dc–dc front-end converter of the HID ballast, the proposed clamp-mode coupled-inductor buck–boost converter has higher efficiency than does the active-clamp flyback converter. Furthermore, the proposed

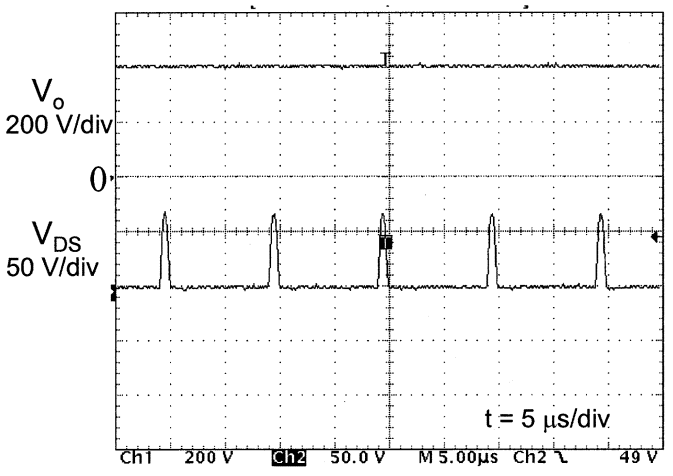

Fig. 14. Experimental waveforms when generating 400 V open-circuit output voltage.

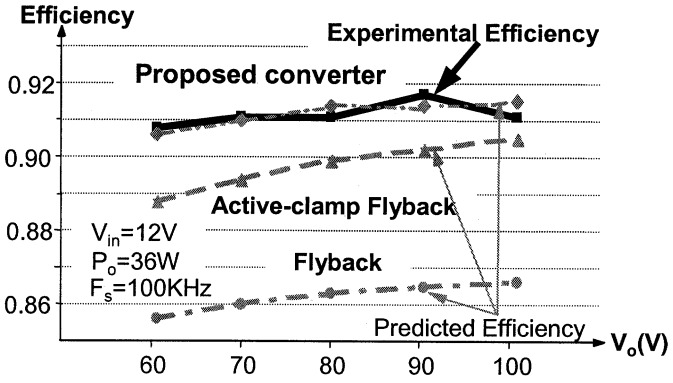

Fig. 15. Predicted and measured efficiency.

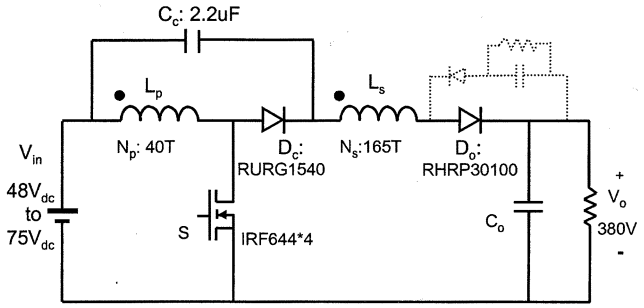

Fig. 16. Boost version for use of the dc-input front-end converter.

converter is more cost-effective and more reliable than the active-clamp flyback converter for those applications that do not require isolation. The experimental results are also shown by the solid line in Fig. 15. The theoretical and measured efficiency are closely matched.

A 1 kW dc-input front-end converter targeting 750 W power supplies for high-end server systems [16] was also built. The circuit topology is a clamp-mode coupled-inductor boost converter. Fig. 16 shows the topology and circuit parameters. Because the leakage inductor of the coupled inductor and the parasitic capacitor of the output diode resonate after boost switch S turns on, a proper snubber circuit is necessary in order to reduce the output rectifier peak voltage. The input voltage is 48–75 V

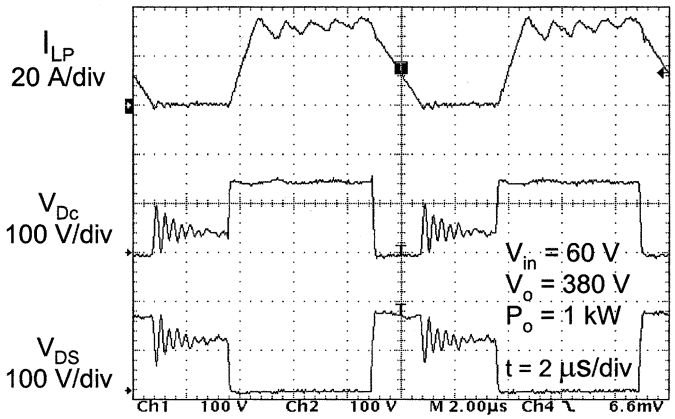

Fig. 17. Experimental waveforms of input inductor current and switch voltage.

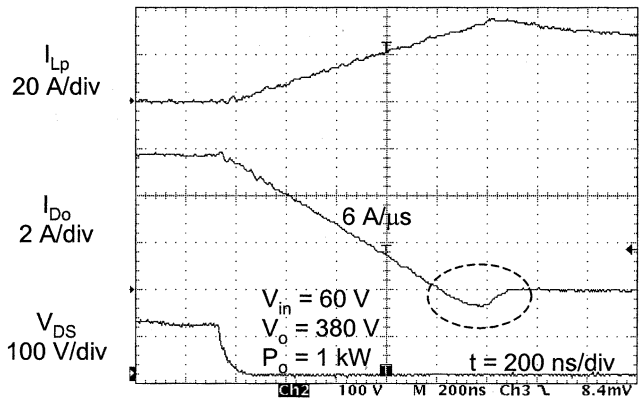

Fig. 18. Experimental waveforms of input inductor current, output diode current and switch voltage.

TABLE II
MEASURED EFFICIENCY OF THE 1 KW DC-INPUT FRONT-END CONVERTER

V_{in}	48 V	60 V	75 V
Duty Ratio	0.60	0.52	0.45
Efficiency	90.5%	91.8%	92.3%

and the output voltage is 380 V. Switch S is implemented with four paralleled IRF644s (250 V, 14 A, 0.28 Ω, To-220AB) from IR. The coupled inductor is implemented with one Kool Mμ toroidal core 77 110-A7 from Magnetics. The primary winding is 40 turns with four strands of 175/40 litz wire in parallel. The secondary winding is 165 turns with 100/40 litz wire.

Fig. 17 shows the current waveform through the primary side of the coupled inductor I_{Lp}, the voltage waveform of clamp diode V_{Dc}, and the voltage waveform of active switch V_S. Because the output rectifier is in series with the secondary winding of the coupled inductor, the leakage inductor limits the diode current decrease rate di/dt. The reverse-recovery problem of the output rectifier is significantly lessened although the converter has high output power and high output voltage. As can be seen in Fig. 18, not only is the reverse-recovery current reduced, it is also delayed. There is no overlap between the switch voltage and the reverse-recovery current.

Table II shows the measured efficiency of the prototype converter. As can be seen, the converter achieves more than 90% conversion efficiency under nominal operation conditions.

VII. CONCLUSION

This paper presents the topology derivation, theoretical analysis, practical design and experimental results for a family of high-efficiency, high step-up, clamp-mode coupled-inductor converters. The operation of the proposed converters is similar to that of their active-clamp counterparts, but the new converters utilize one additional diode and one coupled winding instead of an active switch in order to realize the clamp function. By adding a small clamp capacitor, the leakage energy is recovered in such a way as to generate only a low level of circulating current, and the switch voltage stress is significantly reduced. Utilizing the leakage inductor to control the output current decrease rate di/dt dramatically alleviates the reverse-recovery problem of the output rectifier. The experimental results closely match both the theoretical analysis and the efficiency prediction.

REFERENCES

[1] R. Fiorello, "Powering a 35W dc metal halide high intensity discharge (HID) lamp using the UCC3305 HID lamp controller," in *Unitrode Application Handbook U-161*.
[2] J. Melis. Ballast design overview. Tech. Rep. [Online]. Available: http://www.ballastdesign.com/.
[3] J. Åkerlund, "−48 V dc computer equipment topology—An emerging technology," in *Proc. IEEE-INTELEC'98 Conf.*, 1998, pp. 15–21.
[4] T. M. Fruzs and J. Hall, "AC, dc or hybrid power solutions for today's telecommunications facilities," in *Proc. IEEE-INTELEC'00 Conf.*, 2000, pp. 361–368.
[5] L. Huber and M. M. Jovanovic, "A design approach for server power supplies for networking," in *Proc. IEEE-APEC'00 Conf.*, 2000, pp. 1163–1169.
[6] J. Perkinson, "UPS systems—A review," in *Proc. IEEE-APEC'88 Conf.*, 1988, pp. 151–154.
[7] R. Tymerski and V. Vorperian, "Generation, classification and analysis of switched-mode dc-to-dc converters by the use of converter cells," in *Proc. IEEE-INTELEC'86 Conf.*, 1986, pp. 181–195.
[8] X. G. Feng, J. J. Liu, and F. C. Lee, "Impedance specifications for stable dc distributed power systems," *IEEE Trans. Power Electron.*, vol. 17, pp. 157–162, Mar. 2002.
[9] E. Rodriguez, D. Abud, and J. Arua, "A novel single-stage single-phase dc uninterruptible power supply with power-factor correction," *IEEE Trans. Industry Electron.*, vol. 46, pp. 1137–1147, Dec. 1999.
[10] K. W. Ma and Y. S. Lee, "An integrated flyback converter for dc uninterruptible power supply," *IEEE Trans. Power Electron.*, vol. 11, pp. 318–327, Mar. 1996.
[11] R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," in *Proc. IEEE-PESC Annu. Meeting*, 1994, pp. 909–916.
[12] C. T. Choi, C. K. Li, and S. K. Kok, "Modeling of an active clamp discontinuous conduction mode flyback converter under variation of operating condition," in *Proc. IEEE-PEDS'99 Conf.*, 1999, pp. 730–733.
[13] H. Watanabe, Y. Kobayashi, and Y. Sekine, "The suppressing harmonic currents, MS (magnetic-switch) power supply," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 1995, pp. 783–790.
[14] M. Daniele, P. Jain, and G. Joos, "A single-stage power-factor-corrected AC-dc converter," *IEEE Trans. Power Electron.*, vol. 14, pp. 1046–1055, Nov. 1999.
[15] L. Spaziani, "A study of MOSFET performance in processor targeted buck and synchronous rectifier buck converters," in *Proc. HFPC Power Conv. Conf.*, 1996, pp. 123–137.
[16] B. R. Mower, "SSI: Building compliant power elements for servers," in *Proc. IEEE-APEC'99 Conf.*, 1999, pp. 23–27.

Qun Zhao (S'96) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1990 and 1996, respectively, and is currently pursuing the Ph.D. degree at Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg.

He joined the Center for Power Electronics Systems (CPES), Virginia Tech, as a Research Assistant in 1996. He has been involved in several projects funded by Artesyn Technology and Philips Research as their fellowship student from 1997 to 2001. His research interests include high-frequency power conversion, distributed power systems, and power factor correction techniques.

Mr. Zhao chaired the 2002 CPES Power Electronics Annual Seminar and NSF Site Visit, which involved over 170 participants from the five universities of CPES and more than 100 participants worldwide.

Fred C. Lee (S'72–M'74–SM'87–F'90) received the B.S. degree in electrical engineering from the National Cheng Kung University, Taiwan, R.O.C., in 1968 and the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, in 1971 and 1974, respectively.

He is a University Distinguished Professor with Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, and prior to that he was the Lewis A. Hester Chair of Engineering at Virginia Tech. He directs the Center for Power Electronics Systems (CPES), a National Science Foundation engineering research center whose participants include five universities and over 100 corporations. In addition to Virginia Tech, participating CPES universities are the University of Wisconsin-Madison, Rensselaer Polytechnic Institute, North Carolina A&T State University, and the University of Puerto Rico-Mayaguez. He is also the Founder and Director of the Virginia Power Electronics Center (VPEC), one of the largest university-based power electronics research centers in the country. VPEC's Industry-University Partnership Program provides an effective mechanism for technology transfer, and an opportunity for industries to profit from VPEC's research results. VPEC's programs have been able to attract world-renowned faculty and visiting professors to Virginia Tech who, in turn, attract an excellent cadre of undergraduate and graduate students. Total sponsored research funding secured by him over the last 20 years exceeds $35 million. His research interests include high-frequency power conversion, distributed power systems, space power systems, power factor correction techniques, electronics packaging, high-frequency magnetics, device characterization, and modeling and control of converters. He holds 19 U.S. patents, and has published over 120 journal articles in refereed journals and more than 300 technical papers in conference proceedings.

Dr. Lee received the Society of Automotive Engineering's Ralph R. Teeter Education Award (1985), Virginia Tech's Alumni Award for Research Excellence (1990), and its College of Engineering Dean's Award for Excellence in Research (1997), in 1989, the William E. Newell Power Electronics Award, the highest award presented by the IEEE Power Electronics Society for outstanding achievement in the power electronics discipline, the Power Conversion and Intelligent Motion Award for Leadership in Power Electronics Education (1990), the Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronic Systems Technology (1998), the IEEE Millennium Medal, and honorary professorships from Shanghai University of Technology, Shanghai Railroad and Technology Institute, Nanjing Aeronautical Institute, Zhejiang University, and Tsinghua University. He is an active member in the professional community of power electronics engineers. He chaired the 1995 International Conference on Power Electronics and Drives Systems, which took place in Singapore, and co-chaired the 1994 International Power Electronics and Motion Control Conference, held in Beijing. During 1993-1994, he served as President of the IEEE Power Electronics Society and, before that, as Program Chair and then Conference Chair of IEEE-sponsored power electronics specialist conferences.