A Datasheet Driven Power MOSFET Model and Parameter Extraction Procedure for 1200V, 20A SiC MOSFETs

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Keywords

Device modeling, device simulation, device characterisation, MOSFET, silicon carbide (SiC).

Abstract

A compact model for SiC Power MOSFETs has been presented. The model has been validated with measurements from commercially available 1200V, 20A SiC power MOSFETs. The model features temperature scaling from 25°C to 225°C, which is the operating temperature for the new devices. In order to improve the user's experience with the model, a new datasheet driven parameter extraction strategy has been proposed. The parameter extraction strategy requires only the data normally given in device datasheets, so off-the-shelf devices can characterized quickly. The model includes charge conserving expressions for all non-linear capacitances of the power MOSFET. The SiC power MOSFET shows excellent performance over elevated temperatures, with small variation in on-state resistance over temperature.

Introduction

Unipolar devices like MOSFETs inherently have several advantages over their bipolar counterparts including faster switching, lower switching losses and simplified gate drive requirements [1]. Despite the various advantages, Si power MOSFETs are limited to power applications requiring blocking voltages lower than 200V due to their high on-state resistance at increased blocking voltages. The relationship between on-state resistance and breakdown voltage is given by [2] as

$$R_{ON} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^2} \tag{1}$$

SiC has a much larger breakdown voltage (BV) as compared to Si due its large band-gap. As a result, SiC on-state resistance is lower by a factor of approximately 100 than Si for the same blocking voltage [3]. This lower on-state resistance allows SiC power MOSFETs to be a favorable choice in medium power applications.

In order to fully utilize the performance of the new 1200V, 20A SiC power MOSFETs, accurate device models are needed in circuit simulators, which incorporate the various physical effects occurring inside the device, while at the same time being simple enough to keep simulation times reasonable. SiC devices show good performance over wide temperatures. As a result, the model must also be able to scale well over temperature. A key factor in the adoption of device models is the relative ease of extracting parameters for a given device. The proposed model incorporates a datasheet-driven parameter extraction, which only requires device data which is readily available in datasheets. The parameter extraction strategy also provides the user with a guideline on extracting relevant parameters from the various device characteristics.

The model has been validated by comparing simulation results of the extracted model with measured device characteristics. The DC characteristics have been measured over temperature from 25°C to 225°C. The CV characteristics of the MOSFET, including input capacitance (CISS), output capacitance (COSS) and reverse capacitance (CRSS), have been measured and compared with model simulation. Finally, the switching characteristics have also been compared between the model and the measured device characteristics.

Table I: Important terms in the model

Term	Description	Term	Description
A	Active device area	I_{MOSL}	Low channel current
A_{GD}	Gate-drain overlap area	I_{MOSH}	High channel current
A_{GS}	Gate-source overlap area	P_{VF}	Pinch-off voltage
CDS	Drain-source overlap capacitance	ND	Base doping concentration
CGD	Gate-drain zero bias capacitance	$THETA$	Transverse field reduction factor
CGS	Gate-source overlap capacitance	$THETA_T$	THETA temperature coefficient
C_{OXD}	Gate-oxide capacitance	V_{CGDT}	Gate-drain overlap threshold
KFL	Current gain for low current in saturation region	WB	Base width
KPL	Current gain for low current in linear region	V_A	Early Voltage
KFH	Current gain for high current in saturation region	VGS_{THETA}	High transverse field current reduction parameter
KPH	Current gain for high current in linear region	V_{TH}	Threshold voltage for high current
I_{MOS}	Main channel current	V_{TL}	Threshold voltage for low current

Table II: Important equations in the model

On state equations	
$I_{MOS} = I_{MOSL} + I_{MOSH}$	$yx = \frac{KFX_T}{KFX_T - P_{VF}/2}$
$Linear\ V_{DS} < \frac{V_{GS}-V_{TX}}{P_{VF}}, V_{GS} < VGS_{THETA}$	

$$I_{MOSX} = KFX_T * KPX_T * \frac{\left\{(V_{GS}-V_{TXT})V_{DS} - P_{VF}{}^{(yx-1)}(V_{GS}-V_{TXT})^{\left(\frac{2-yx}{yx}\right)}\right\}}{\{1+\theta_T(V_{GS}-V_{TXT})\}}\left(1+\frac{V_{DS}}{V_{AT}}\right)$$

For $V_{GS} \geq VGS_{THETA}$,

$$I_{MOSX} = KFX_T * KPX_T * \frac{\left\{(V_{GS}-V_{TXT})V_{DS} - P_{VF}{}^{(yx-1)}(V_{GS}-V_{TXT})^{\left(\frac{2-yx}{yx}\right)}\right\}}{\{1+\theta_T(V_{GS}-V_{TXT})\}\{1+XTHETA_T(V_{GS}-VGS_{THETA})\}}\left(1+\frac{V_{DS}}{V_AT}\right)$$

Saturation $V_{DS} \geq \frac{V_{GS}-V_{TX}}{P_{VF}}$, $V_{GS} < VGS_{THETA}$

$$I_{MOSX} = KPX_T * \frac{(V_{GS}-V_{TXT})^2}{2\{1+\theta_T(V_{GS}-V_{TXT})\}}\left(1+\frac{V_{DS}}{V_{AT}}\right)$$

For $V_{GS} \geq VGS_{THETA}$,

$$I_{MOSX} = KPX_T * \frac{(V_{GS}-V_{TXT})^2}{2\{1+\theta_T(V_{GS}-V_{TXT})\}\{1+XTHETA_T(V_{GS}-VGS_{THETA})\}}\left(1+\frac{V_{DS}}{V_{AT}}\right)$$

Transient equations

$$C_{DSJ} = CDS * \left(\frac{V_{bi}}{V_{bi}+V_{DS}}\right)^m \qquad Q_{DSJ} = CDS * V_{bi}^m * \{(V_{bi}+V_{DS})^{(1-m)} - V_{bi}^m\}/(1-m)$$

$$W_{GDJ} = \sqrt{\frac{2\varepsilon_{SiC}(V_{DG}+V_{CGDT})}{qN_D}} \qquad C_{GD} = \begin{cases} C_{OXD}, & V_{DG}+V_{CGDT} \leq 0 \\ \dfrac{C_{OXD} * C_{GDJ}}{C_{OXD}+C_{GDJ}}, & V_{DG}+V_{CGDT} > 0 \end{cases}$$

$$C_{GDJ} = \frac{A_{GD}\varepsilon_{SiC}}{W_{GDJ}} \qquad Q_{DG} = 2\varepsilon_{SiC}A_{GD}\sqrt{\frac{qN_D}{2\varepsilon_{SiC}}\left(\sqrt{V_{DG}+V_{CGDT}} - \sqrt{V_{CGDT}}\right)}$$

$$CISS = CGD + CGS \qquad COSS = CGD + CDS \qquad CRSS = CGD$$

Temperature Scaling

$$\mu_n(T) = \frac{947}{1+\left(\frac{N_D}{1.94\times10^{17}}\right)^{0.61}}\left(\frac{T}{T_0}\right)^{-2.15} \qquad n_i(T) = 3.87\times10^{16}T^{3/2}e^{-(2.02\times10^3)/T}$$

$$KPX_T = KPX\left(\frac{T}{T_0}\right)^{KPXTEXP}$$

$$V_{TXT} = V_{TX} + V_{TXTEXP}(T-T_0) \qquad KFX_T = KFX\left(\frac{T}{T_0}\right)^{KPXTEXP}$$

$$THETA_T = THETA\left(\frac{T}{T_0}\right)^{THETATEXP} \qquad XTHETA_T = XTHETA + (T-T_{-0})XTHETATEXP$$

Final Current Expressions

$$I_D = I_{MOS} + \frac{dQ_{DSJ}}{dt} \qquad I_G = \frac{dQ_{DG}}{dt} + \frac{dQ_{GS}}{dt}$$

Model Description

The McNutt power MOSFET model [4] has shown good performance for SiC MOSFETs from room temperature to 100°C. The source code for the McNutt model is not available, and its parameter extraction procedure has been presented using a proprietary NIST tool which is not available as freeware. Hence, a new power MOSFET model based on McNutt's power MOSFET model has been developed in MAST modeling language for Saber simulator. The model has been enhanced by including new temperature scaling equations to scale the model from 25°C to 225°C. The model also includes a high gate-voltage mobility reduction formulation. The capacitance equations in the model have been modified to be charge conserving and expressions to directly compute CISS, COSS and CRSS have been added.

Model On-State Description

Table I gives a brief nomenclature for the various terms used in the model. All the parameters with subscript T are temperature scaled values for the parameters. The main channel current I_{MOS} is split into two components: I_{MOSL} and I_{MOSH}, which represent the low and high currents respectively. Low current is the current due to the turn-on of outer cells in the power MOSFET structure and is appreciable at lower gate voltages, where only the outer cells of the power MOSFET turn on. High current results from the turn-on of the remaining bulk of cells in the power MOSFET, at higher gate voltages. This parallel channel description enables the modeling of a soft transconductance of the MOSFET, as is observed in [5]. I_{MOSL} and I_{MOSH} have independent threshold voltage parameters V_{TL} and V_{TH} as well as transconductance parameters KFL, KPL and KFH, KPH respectively to give much better control of the main channel current inside the model.

Due to the non-uniform dopant density in the channel region, carrier diffusion is observed [4], which results in different current values in the linear and saturation region. In order to accurately model this difference, each current gain has two parameters KPL, KPH and KFL, KFH. By having two separate parameters, the difference in saturation and linear current values can be modeled easily, with easy parameter extraction. The voltage pinch-off parameter P_{VF} allows a smooth transition from the linear to saturation region. The reduction in channel mobility due to transverse field caused by high gate voltages is modeled by $THETA$. Another set of parameters, $XTHETA$ and VGS_{THETA}, have be introduced to account for additional reduction in channel mobility due to very high electric fields encountered in the channel of the MOSFET at close to maximum rated gate voltage.

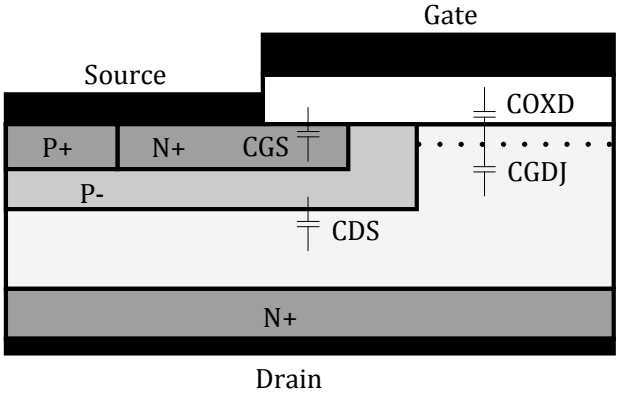


Fig. 1: Power MOSFET structure with internal capacitances

The proposed model has been scaled to work between operating temperatures of 25°C and 225°C, which is the intended range of the power MOSFETs application. In order to develop the temperature scaling equations for the model, all the model parameters were first extracted at room temperature. Using this initial parameter set as a starting point, parameter sets were extracted at each temperature,

while keeping the model's temperature the same as the simulator temperature. This disables all temperature scaling equations in the model, and corresponding values for the parameters at each temperature is obtained as a function of temperature. Using this function, temperature scaling equations are described for the relevant parameters. The intrinsic carrier concentration, electron channel mobility [6] and built-in voltage variation with temperature are also included.

Model Transient Description

The structure of a power MOSFET with the internal capacitances is shown in Figure 1. The gate-source capacitance includes gate metallization capacitance and gate-source overlap capacitance, and is given by the constant parameter CGS. The drain-source capacitance depends on the area of the drain-body junction A_{DS} and the depletion width. The depletion width is calculated using the base doping parameter N_D and built-in potential V_{bi}. The gate to drain capacitance is a two phase capacitance. When the drain-gate voltage is lower than the threshold parameter V_{CGDT}, the gate-drain capacitance is equal to the gate-oxide capacitance C_{OXD}. For drain-gate voltages greater than V_{CGDT}, the gate-drain capacitance becomes a series of C_{OXD} and C_{GDJ} where C_{GDJ} is the junction capacitance between the gate-oxide and the drain. In order to ease the parameter extraction procedure, the various capacitances have been combined to yield the input, output and reverse transfer capacitances as shown along-with other important equations in Table II.

Table III: Parameter Extraction Strategy

Parameter	**Description**	**Extraction Characteristics**
A	Device area	Die Information
V_{TL}, KPL, V_{TH}, KPH	Low and high current threshold voltage and transconductance gain	ID-VGS in saturation
$THETA$, VGS_{THETA}, $XTHETA$	Transverse field reduction factors	ID-VDS in saturation
P_{VF}, KFL, KFH, VA	Output characteristics parameters	ID-VDS
V_{CGDT}, C_{OXD}, N_D	Gate-drain capacitance parameters	CRSS-VDS
CGS	Gate-source capacitance	CISS-VDS
CDS, M	Drain-source capacitance parameters	COSS-VDS
RS	Series Resistance	On-state voltage vs. VGS
V_{TLTEXP}, V_{THTEXP}, KPL_{TEXP}, KPH_{TEXP}	Transconductance parameter temperature scaling	ID-VGS in saturation over T
$THETA_{TEXP}$, VA_{TEXP}, $XTHETA_{TEXP}$	Transverse field temperature scaling parameters	ID-VDS

Parameter Extraction

Table III describes the steps involved in the parameter extraction. Parameter extraction starts with the extraction of low current threshold voltage V_{TL} and transconductance gain parameter KPL from the region I of the ID-VGS characteristics where the device has barely turned on, as shown in Fig. 2. The high current threshold voltage V_{TH} and transconductance gain parameter KPH are then extracted from the linear slope in region II of the ID-VGS characteristics. The current reduction factor due to high transverse electric field $THETA$ can be extracted from region III.

After extracting the transconductance parameters, the saturation current gain parameters KFL and KFH are extracted. Along-with these parameters, P_{VF} which affects the transition from linear to saturation region, should be extracted. Transverse field current reduction parameters $THETA$ and $XTHETA$ can then be refined as shown in Fig. 3.

Since the proposed parameter extraction strategy is datasheet driven, the capacitance parameters are extracted from the transfer capacitances available in all device datasheets. The gate-oxide capacitance C_{OXD} can be extracted from the CRSS-VDS characteristics at zero drain bias. The curvature of the CRSS-VDS characteristics depends on the variation of the depletion width under the gate-oxide, which also depends on the doping density in the base N_D. The gate-source and drain-source parameters can be extracted next from the CISS-VDS and COSS-VDS characteristics as shown in Fig. 7b.

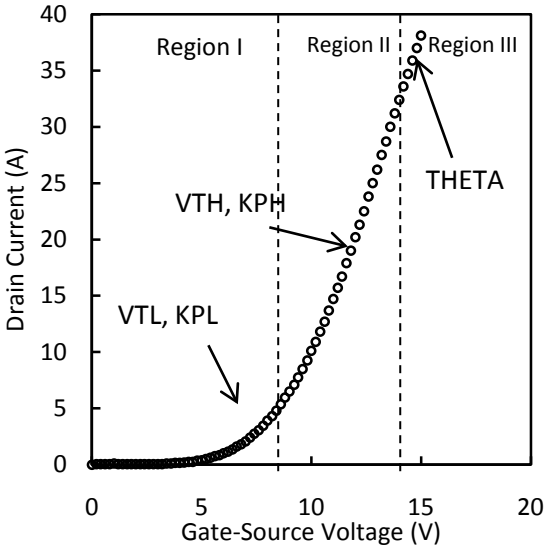


Fig. 2: Transconductance characteristics of a SiC power MOSFET with different regions for identified parameter extraction.

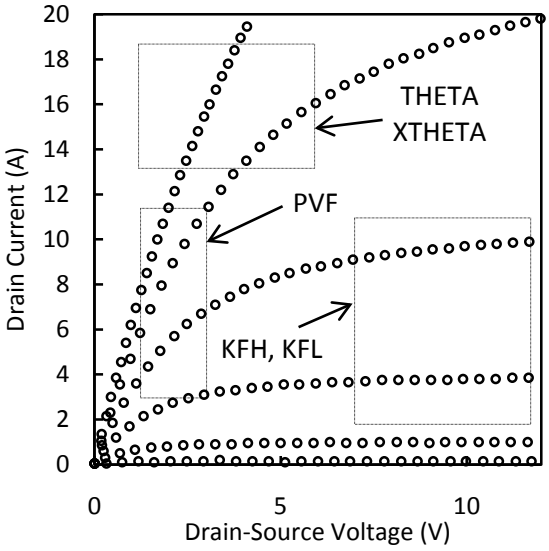


Fig. 3: Output characteristics of a SiC power MOSFET with different regions identified for parameter extraction.

Measured and Simulated Results

In this section, parameters for the model described in previous sections have been extracted over temperature for a 1200V, 20A SiC power MOSFET. The extracted parameters at room temperature are shown in Table IV. All the model parameters are extracted at room temperature. After obtaining a complete parameter set, temperature scaling parameters are extracted using the data at elevated temperatures.

Fig. 4 shows the simulated and measured transconductance characteristics of the 1200V 20A SiC power MOSFET at 25°C, 125°C and 225°C. The model can be seen to simulate the transconductance

behavior well over the entire temperature range. Fig. 5 shows the variation of threshold voltage over temperature calculated by extrapolating the linear region of the ID-VGS curve. As expected, the threshold voltage decreases with an increase in temperature due to the variation of surface potential with temperature [7].

Fig. 6 shows the simulated and measured output characteristics of the power MOSFET at 25°C, 125°C and 225°C. The on-state resistance at gate-source voltage of 20V in the linear region is calculated and shown in Fig. 7a. The channel mobility in SiC increases with increased temperature due to the release of trapped electrons in the interface states [8]. The drift region resistance on the other hand decreases with increased temperature, and these opposing temperature coefficients cause the on-state resistance to only increase slightly over temperature, when compared with Si. The transition of the output curves from linear to saturation is gradual, due to the fact that in SiC devices, the resistance of the drift region, which is the major contributor in Si devices, is very low. The surface mobility of electrons in SiC is low, which makes the channel resistance the major contributor in SiC devices. Thus the linear region in SiC devices follows the shape of channel resistance, which changes gradually from linear to saturation.

The transient parameters have been extracted using the transfer capacitance data. The measured and simulated transfer capacitances CISS, COSS and CRSS have been shown in Fig. 7b. In order to verify the extracted transient parameters, the switching performance of the 1200V, 20A power MOSFET was measured using the circuit shown in Fig. 7c. The gate was pulsed from 0V to 15V and the turn-on characteristics were measured. Fig. 8 shows the turn-on characteristics at room temperature. A good agreement is seen between the measured and simulated switching waveforms. The Miller effect can also be seen during turn-on, which highlights the two-phase gate-drain capacitance inside the model.

Conclusion

A SiC power MOSFET model has been presented. The model has been used to characterize a 1200V, 20A SiC power MOSFET available commercially over temperature from 25°C to 225°C. The model has been shown to perform well over temperature in both static and dynamic tests. A parameter extraction strategy has also been provided with the model which uses data available in device datasheets.

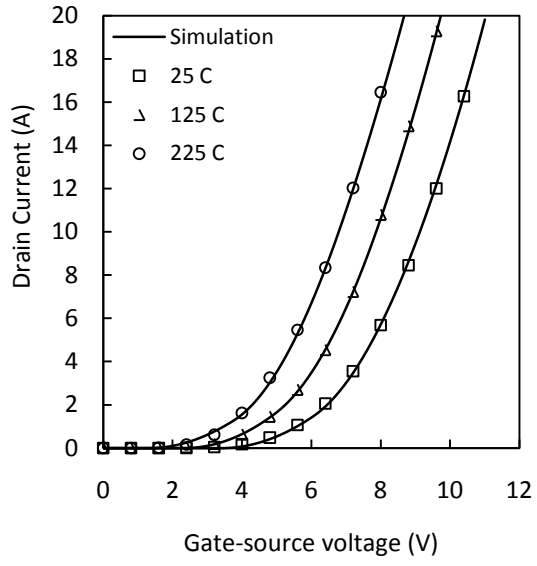


Fig. 4: Measured (markers) and simulated (solid) transconductance at 25°C, 125° and 225°C.

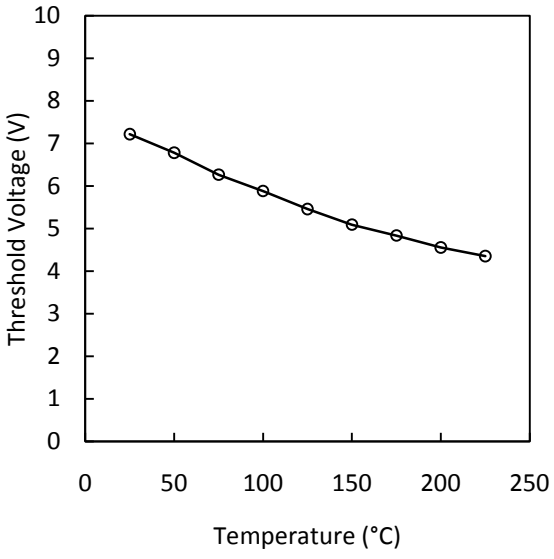
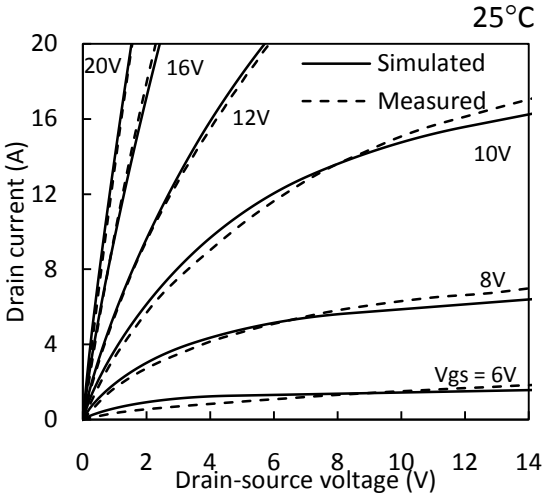
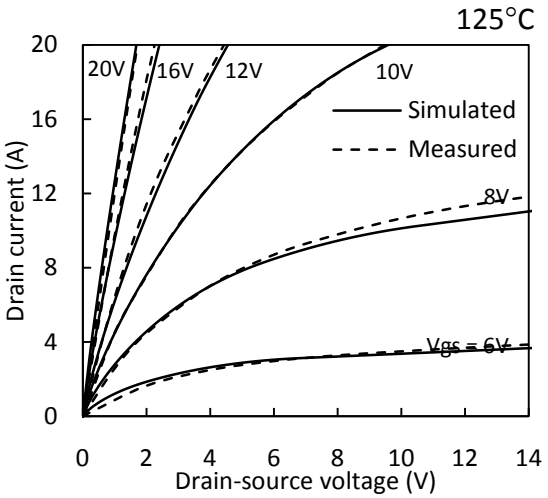


Fig. 5: Calculated threshold voltage over temperature.





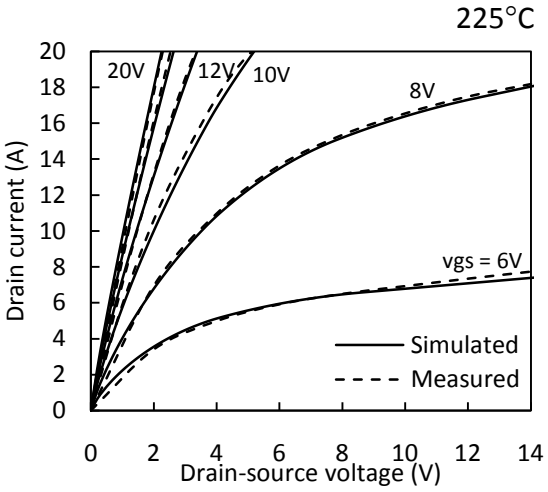
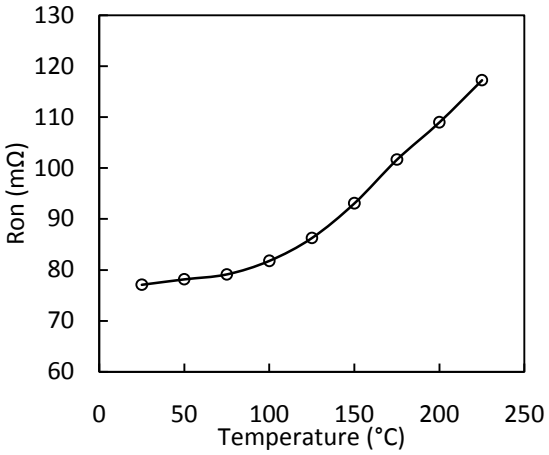
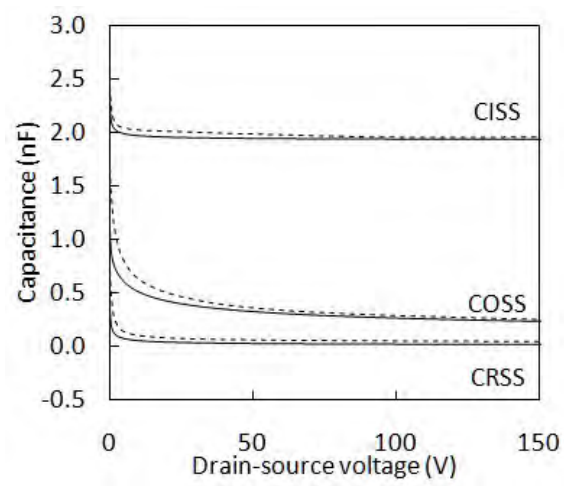


Fig. 6: Measured (markers) and simulated (solid) output characteristics at 25°C (top), 125° (middle) and 225°C (bottom).





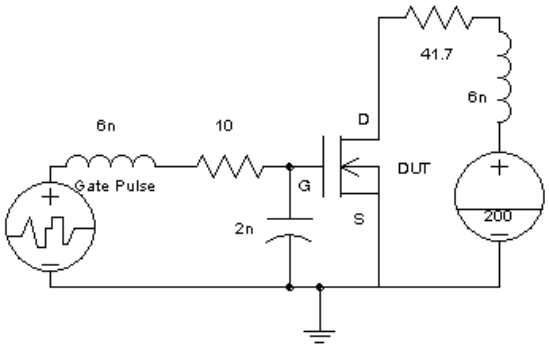


Fig. 7a (top): Calculated on-state resistance Ron vs. temperature. 7b (Middle): Measured (hashed) and simulated (solid) transfer capacitances. 7c (Bottom): Schematic for switching test.

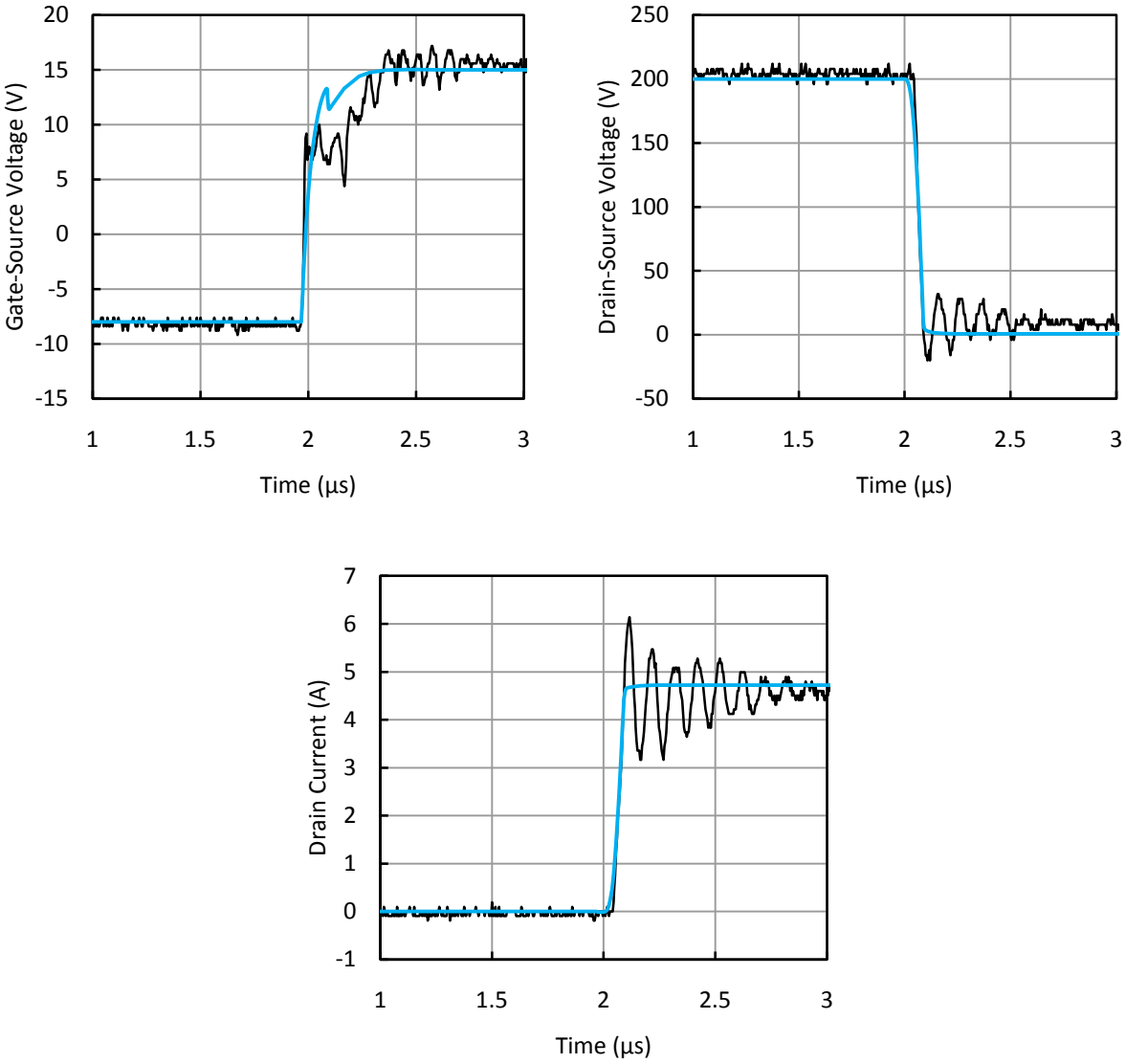


Fig. 7: Measured (black) and simulated (blue) gate-source voltage (top-left), drain-source voltage (top-right) and drain current (bottom) waveforms during turn-on.

Table IV: Extracted Model Parameters

Parameter	**Value**	**Parameter**	**Value**
V_{TH}	6.15	V_{TL}	3.5
V_{THTEXP}	-12m	V_{TLTEXP}	-11m
KPH	0.54	KPL	0.36
KPH_{TEXP}	-0.7	KPL_{TEXP}	-0.02

KFH	5	KFL	3
KFH_{TEXP}	-0.02	KFL_{TEXP}	-0.03
P_{VF}	0.54	V_A	35
$THETA$	1.2m	$THETA_{TEXP}$	4.8
$XTHETA$	0.1	VGS_{THETA}	14
$XTHETA_{TEXP}$	1.6m	N_D	3.1 x 10^{15}
$COXD$	2.56n	CDS	550p
CGS	1.62n	A	0.02

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