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Buck-Boost and Ĉuk Topology Based Single Phase Cycloconverters with Low THD and High Power Factor

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***Abstract* -- Two topologies of single phase cycloconverters based on Buck-Boost and Ĉuk topologies are presented. Instead of simple switching scheme of P and N controlled rectifier-converters, high frequency switching of uncontrolled rectifiers outputs have been used with the help of Buck-boost and Ĉuk converters. The input supply is an AC source followed by a full bridge rectifier circuit, the output of which is fed to the SMPS converters. The output voltages of the proposed cycloconverters are controllable step-up and step down in nature with duty cycle control of switching regulators. Total Harmonic Distortion (THD) of the input current of the proposed circuits is minimized by input filters before the rectifier. Input power factor and efficiency of the circuits are high. The circuits exhibit such performances at variable switching frequencies and duty cycles.**

***Index Terms*--Cycloconverter, Buck-Boost, Cuk, Switching frequency, Harmonic distortion, SMPS, Rectifying circuit, AC-AC conversion, Input filter.**

I. INTRODUCTION

The traditional cycloconverter requires a large number of thyristors, at least 36 and usually more for good motor performance, together with a complex control circuit, and it has some performance limitations, for satisfactory operation of the converter the realistic upper limit of the output frequency is about one third of the input frequency [1]. Cycloconverters deliver averaged sinusoidal output waveform which results low pulsating torque in rotary loads. Their input current is distorted and its Fourier series involves harmonics which include, a) higher order harmonics [2], b) sub-harmonics [3], and c) nonstandard harmonics [4], [5]. Cycloconverter output voltages also involve harmonics and sub-harmonics. As a result, the control strategy must be chosen in a way to limit these harmonics and minimize their effect on output voltage. Generally, harmonic behavior of cycloconverters is dependent on their pulse number, structure and switching strategy. The higher the pulses number the better the cycloconverter performance [6].

The conventional methods of filter [7] cannot be used to reduce harmonics in cycloconverters. Different control strategies widely influence cycloconverter harmonic behavior. The change of a control strategy may result in the change of the input currents, and further, the electric power quality in the supply feeder. The basic idea proposed for this paper is shown in Fig1.

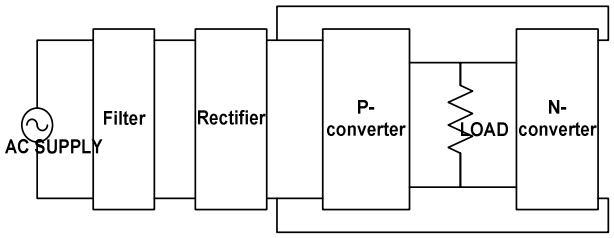


Fig. 1. Basic Topology for proposed circuits

In this paper, switch mode power supply (SMPS) converters are employed to control the output voltages. In each cycle of the input AC signal the voltage is made unidirectional by employing full bridge rectifier. Then, depending on the required frequency at the load, this unidirectional voltage either appears on the same side or on the opposite side of the load. To provide output voltages at opposite polarities two SMPS topology based converters (one p and one n converter) are connected across the load [8]. The proposed topology differs from the available circuits in two ways. Firstly, for single phase AC-AC conversion[9], SMPS topology based converters is employed instead of conventional eight SCR cycloconverter scheme, thereby, output voltage both higher and lower than the supply voltage is achievable by controlling the duty cycle of the SMPS converter. Secondly, in case of single phase AC supply, the p and n type converters have reduced number of switches. The reduction of switches has four advantages compared to conventional cycloconverter topologies. Firstly, it reduces the switching losses and thereby increases the efficiency. Secondly, the proposed circuits have to deal with less number of isolation schemes. Thirdly, the number of drives is reduced and finally, the proposed topology has higher reliability as the number of switches is reduced. The performance of the proposed topology is evaluated in terms of THD, input power factor, output voltage, output frequency and efficiency along the range of the duty cycle of the control signal.

II. PROPOSED CIRCUIT CONFIGURATION

A. Scheme I

The proposed scheme for Buck-Boost topology based cycloconverter is shown in Fig2.

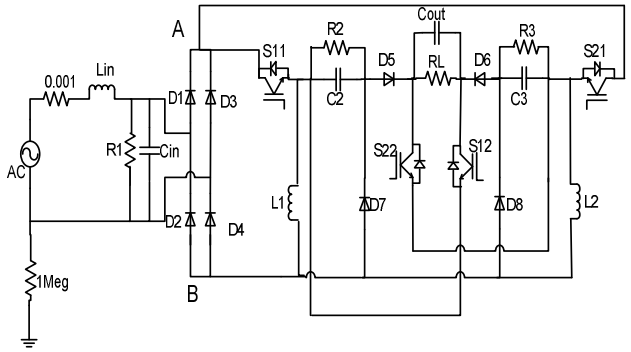


Fig. 2. Proposed Buck-Boost Topology Based Cycloconverter

The resistive load RL is differentially connected between the P-converter and N-converter. The output capacitor, Cout stabilizes the output voltage across the load. Switch S11 and S12 are used to chop the P-converter input. Switch S21 and S22 are used to chop the N-converter input.C2 and C3 are the functioning capacitors for P and N-converter respectively. L1 and L2 are the functioning inductors for P and N-converter respectively. The diodes D1, D2, D3, D4 forms a full-bridge rectifier which allows the AC input from AC source to always maintain a certain direction in the converter circuit. Thus point A is always at (+)ve and point B is always (-)ve voltage, which ensures DC input for basic cycloconverter circuit topology. Diodes D5 and D6 are used to restrict current flow in backward direction from the load for P and N-converter respectively. Diodes D7 and D8 provide the discharging path for the capacitors C2 and C3 respectively when the corresponding switches are in OFF position.

B. Scheme II

The proposed scheme for Cuk topology based cycloconverter is shown in Fig3.

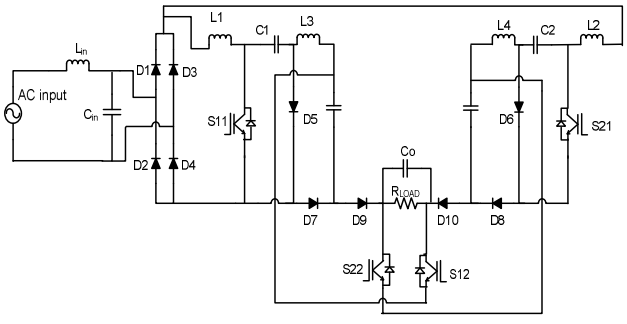


Fig. 3. Proposed Cuk Topology Based Cycloconverter

Like the proposed buck-boost converter, the load (R_{LOAD}) is also differentially connected between the P- and N-converter. An output capacitor (C_o) provides increased output voltage stability. The P-converter is made up of the switches S_{11} and S_{12}, while to N-converter comprises of switches S_{21} and S_{22}. The capacitors C_1 and C_2 are the main energy-storage components of the P-converter and the N-converter respectively. The P-converters also includes the inductors L1, L3 and diode D5. Inductors L2, L4 and diode D6 are similar components in the N-converter. The converters are connected to the full-bridge rectifier comprising of diodes D1, D2, D3 and D4. An LC-filter is made up of inductor Lin and capacitor Cin to reduce harmonics from the primary voltage source AC input.

III. OPERATION

A. Scheme I

The proposed topology comprises of two basic topologies, Cycloconverter and Buck-Boost converter. For basic cycloconverter, operation can be defined in two steps: P-conversion and N-conversion. For basic Buck-Boost converter, operation can be defined by charging and discharging of a capacitor, maintaining the current through the inductor always flowing in a single direction. Alternatively operation when the switch is in ON and OFF position.

Combining these two topologies, proposed Buck-Boost based cycloconverter operates in four different states: a)Switch ON in P-converter, b)Switch OFF in P-converter, c)Switch ON in N-converter, d)Switch OFF in N-converter

Fig. 4 shows the P-conversion process. The N-conversion cycle is same as the P-conversion.

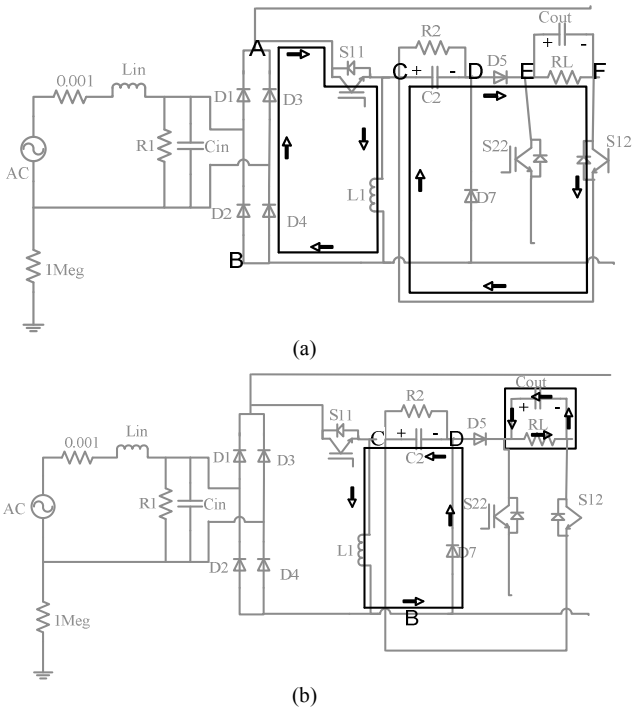


Fig. 4. The P-converter operation in Buck-Boost topology (a) Switch ON, (b) Switch OFF

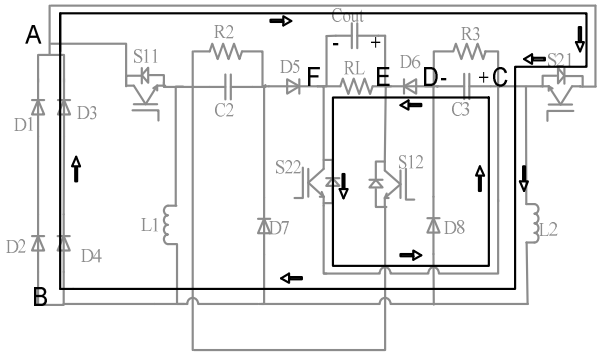
Switch ON P-converter: S11 and S12 work as a short circuit connection ideally. Current flows from A to B through the inductor L1 (downward). The capacitor C2 is charged having +ve terminal at C and -ve terminal at D. Cout is charged with +ve at E and –ve at F.

Switch OFF P-converter: The output capacitor, Cout across the load, also discharges through RL. The current flow through the load is in the same direction as before. Thus we always get a positive current in P-conversion cycle but varying in magnitude

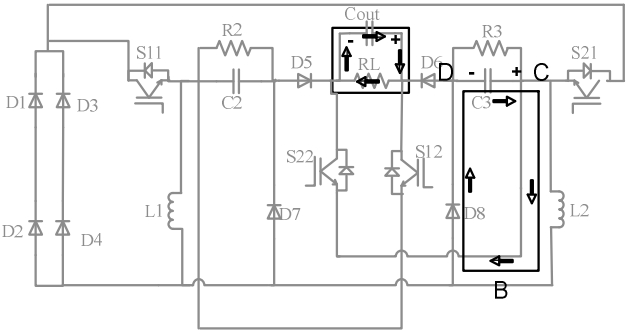
N-conversion process is shown at Fig 5. For clarity only the relevant converter is shown. As in P-conversion process, N-convertor can be considered absent or cut off from the circuit.

The only difference between the P-conversion and N-conversion is that, the output capacitor Cout is charged in opposite direction. For P-conversion the capacitor charged with positive on the left. While at N-converter, the capacitor is charged with positive at the right. This alternate charging explains the P and N cycles.

The output waveforms for the Buck-Boost converter for both the cycles are shown at Fig6. As can be noticed from the output curve, the output frequency is one third of the input. It can be altered by the switching scheme.

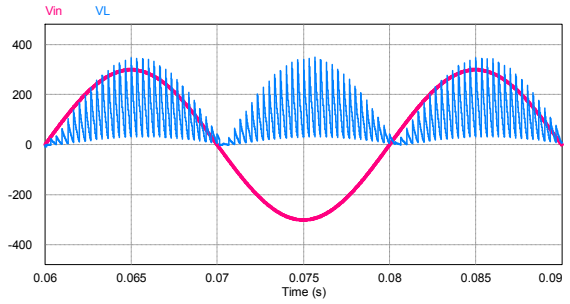


(a)

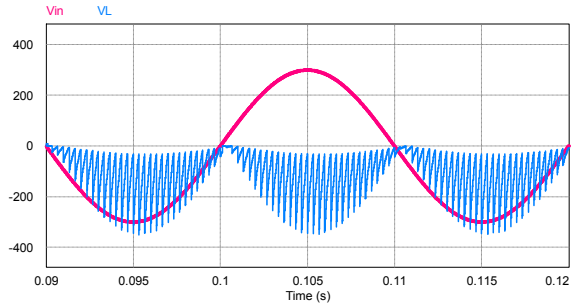


(b)

Fig. 5. N-converter operation of the Buck-Boost topology (a) Switch ON, (b) Switch OFF



(a)



(b)

Fig. 6. Input and Output waveforms for proposed Buck-Boost circuit (a) P-conversion, (b) N-conversion

The high frequency component at the output can be further eliminated by using a low pass filter. Higher the switching frequency, better is the output filter performance.

IV. PERFORMANCE OF THE CIRCUITS

The simulation of the proposed circuits is performed with PSIM software.

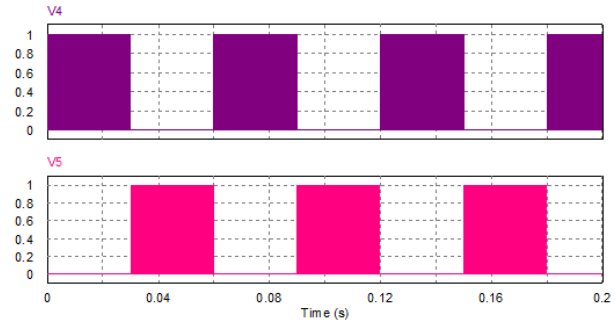
A. Circuit Parameters

The initial power supply for both the circuits has been chosen to be a 50Hz 300V (RMS 212V) supply. An IGBT is used as the switching device and the switching frequency is varied from 1~10 KHz with duty 0.2~0.9. Increasing the switching frequency requires lower duty cycle for desired power quality. This is the basic sweeping scheme suggested in this paper.

For the Buck-Boost topology the input filter is designed with Lin 5~30mH and Cin 5uF. For the Cuk topology it is designed with Lin 5mH and Cin 5~10uF. Cout is fixed at 1uF for both. The inductance increases with decreasing duty cycle to prevent the harmonic components.

The switching scheme is so designed when P-converter is in operation; N-converter is totally cut off from the circuit. Same argument is applicable for the N-converter. This is achieved via an AND gate between high frequency source and a low frequency source with desired output wavelength.

The switching is shown at Fig. 7.



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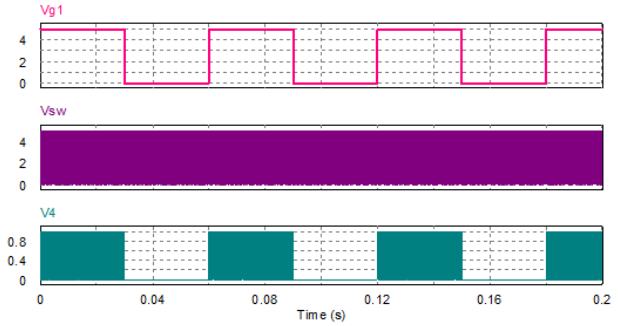


(b)

Fig. 7. (a) Alternate switching of the P and N converter (b) AND gate scheme for one converter

B. Results from Simulation

Simulation was performed by varying duty cycle and frequency to achieve the desired sweeping characteristics.

The desirable power quality is described by three parameters (a) THD<12%, (b) input power factor>0.85 (c) efficiency>80%. We put more emphasis on THD and input power factor.

TABLE I. INPUT CURRENT THD(%), pf and OUTPUT EFFICIENCY FOR BUCK-BOOST CONVERTER SCHEME

D	f	Vo.rms	Iin.max	THD	Pf(in)	η
0.2	10	26	0.95	**1.21**	**0.238**	**61**
0.3	8	38	1.12	**4.04**	**0.422**	**74**
0.4	6	67	1.21	**3.99**	**0.78**	**82**
0.5	4	118	1.49	**2.89**	**0.93**	**81**
0.6	3	127	2.36	**3.18**	**0.985**	**90**
0.7	2	173	4.59	**6.05**	**0.998**	**90**
0.8	1.5	279	12.82	**9.22**	**0.961**	**93**
0.9	1	318	25.25	**19.21**	**0.667**	**94**

It can be observed from the Table I that performance is quite satisfactory at duty cycles between 0.4~0.7. The THD ranges between 2.98~9.62, input power factor is 0.831~0.971 and efficiency between 87~96%.

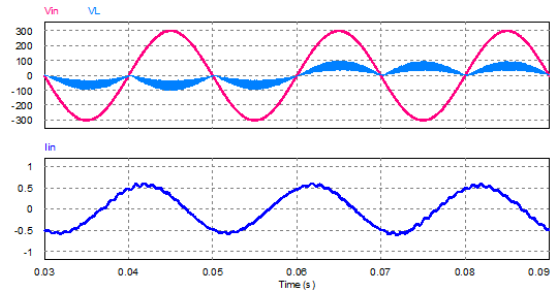
TABLE II. INPUT CURRENT THD(%), pf and OUTPUT EFFICIENCY FOR CUK CONVERTER SCHEME

D	f	Vo.rms	Iin.max	THD	Pf(in)	η
0.3	10	127	1.12	**18.72**	**0.892**	**76**
0.4	8	220	1.21	**7.54**	**0.933**	**78**
0.5	6	402	1.49	**6.33**	**0.955**	**80**
0.6	4	591	2.36	**4.75**	**0.945**	**80**
0.7	3.5	787	4.59	**4.29**	**0.953**	**82**
0.8	3	851	12.82	**9.26**	**0.865**	**79**
0.9	2	889	25.25	**14.47**	**0.792**	**73**

It can be observed from the Table II that performance is quite satisfactory at duty cycles between 0.4~0.7. The THD ranges between 4.29~7.54, input power factor is 0.933~0.953 and efficiency between 78~82%.

Similar to the basic performance of SMPS Buck-Boost and Cuk topology, for duty<0.5 a buck and for duty>0.5 a boost operation is observed at the output waveform. At duty=0.5 the output RMS value is almost equal to the input as it should be. Fig. 8 shows the output for varying duty cycle at Buck-Boost cycloconverter.

The output is not exactly equal to the input at D=0.5, due to other circuit components involved it the cycloconverter. The input filter and the series components cause a little amount of voltage loss and the output is slightly less than input at D=0.5.



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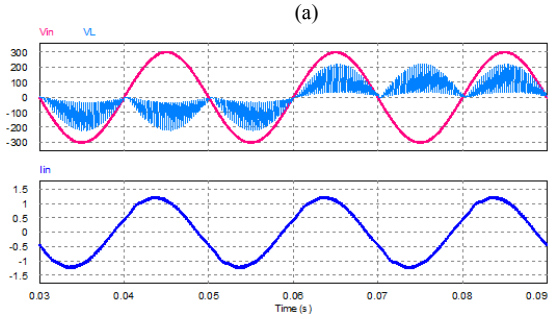

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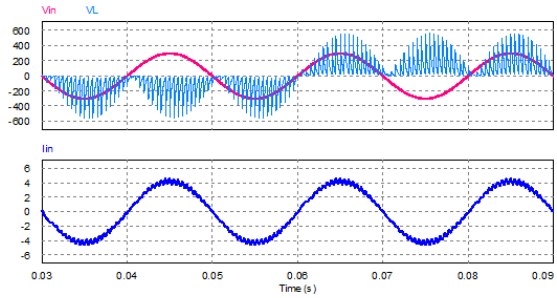


(c)

Fig. 8. Output voltage and Input current and voltage for Buck-Boost topology (a) D<0.5, (b) D=0.5 (c) D>0.5

The high frequency at output is due to the high frequency switching. The output frequency is chosen to be one third of the input as it can be noticed from the output voltage waveforms.

TABLE III. INPUT CURRENT THD(%), pf and OUTPUT EFFICIENCY FOR VARIOUS CONVERTER SCHEME

Buck-Boost			Cuk			8-SCR		
THD	pf	η	THD	pf	η	THD	pf	η
4	.422	74	19	.892	76	100	.112	73
4	.78	82	8	.933	78	71	.235	76
3	.93	81	6	.955	80	51	.379	78
3	.985	90	5	.945	80	36	.525	78
6	.998	90	4	.953	82	23	.837	79
9	.961	93	9	.865	79	12	.763	79
19	.667	94	14	.792	73	3	.675	79

From the tables I and II, it can be noticed that the total harmonic distortion of input current remains in an allowable limit. This phenomenon is reflected in the power spectrum having a high magnitude at center frequency 50Hz and very small component around the switching frequency. Thus the undesired distortion can be easily removed by a filter. The spectrum of input current for the Cuk topology at switching frequency of 2 KHz is shown at Fig.9. Fig. 10 shows the spectrum of input current for the Buck-Boos topology at switching frequency of 2 KHz.

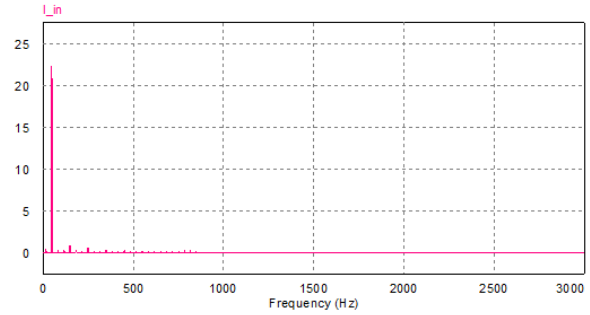


Fig. 9. Spectrum of the input current for the Cuk converter

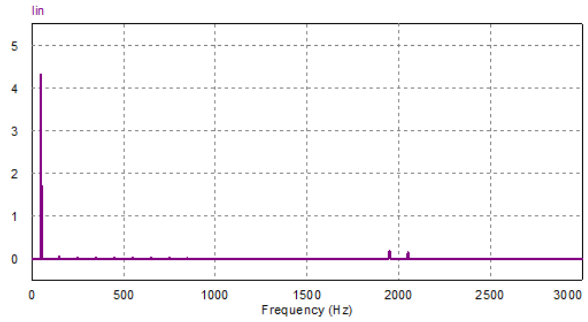


Fig. 10. Spectrum of the input current for Buck-Boost topology

C. Quantitative Comparison

From Table III, the power quality for the proposed Cuk and Buck-Boost topology is compared with the conventional 8-SCR scheme. Proposed cycloconverter topologies are advantageous than conventional ones for two reasons. Firstly, the input current THD will be much lower in the proposed topologies due to high frequency switching of the switch mode topologies. Another advantage of this input current switching is the requirement of much smaller input filters. The input current THD of the conventional converters will be possible to reduce if large intergroup reactors (IGRs) are added. The power quality can be discussed based on three parameters a) Input current THD, b) input power factor, c) efficiency.

The input current spectrum for the conventional 8-SCR topology is shown at Fig.11. It is evident from the figure that current contain a large harmonic component distributed throughout the spectrum, filtration is almost impossible in this case.

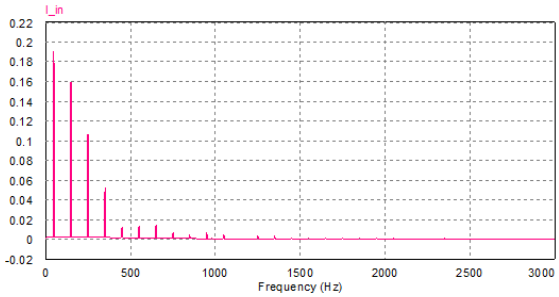
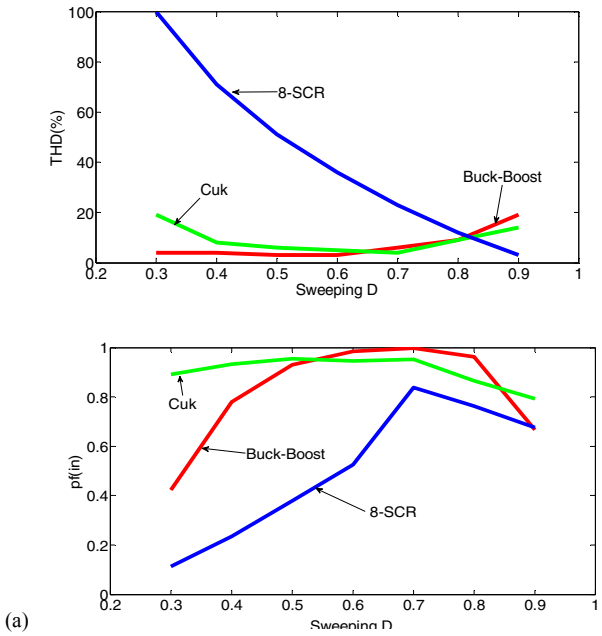


Fig. 11. Fourier representation of input current of 8-SCR cycloconverter

The comparison of the output parameters of the 8-SCR cycloconverter with the proposed Buck-Boost and Cuk topology is shown at Fig. 12.



(a)

(b)

Fig. 12. Comparison of (a) THD, (b) input power factor of the proposed topologies with conventional 8-SCR topology

As evident from the graphs presented in Fig.12, the THD of conventional 8-SCR cycloconverter is good only at very high duty cycle, very poor for most of the duty cycles. But Cuk and Buck-boost topology based cycloconverter shows reasonable amount of distortion throughout graph. Again the input power factor for 8-SCR are not acceptable throughout the operation. But the performance for proposed topologies show power factor above 80% for a wide range of operation. These two graphs are sufficient to compare the power quality of the proposed topologies with the conventional one.

V. CONCLUSION

The results presented in this paper showed that the proposed cycloconverters are able to provide AC-AC conversion at higher efficiencies maintaining better power quality than the conventional 8 SCR cycloconverters. Another advantage worth mentioning here is that, the proposed topologies are able to provide output voltages with controllable amplitude and frequencies both smaller and greater than the input ones. In summary, the proposed switch mode cycloconverter topologies render wider range of AC-AC conversion ensuring higher power quality.

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