EE214 Digital Circuits Laboratory
Wadhwani Electronics Laboratory
Electrical Engineering IIT Bombay

Problem set: 6 Date: September 25, 2025

Asynchronous Down Counter

Instructions:

1. Use **Behavioral** modeling for writing VHDL description
2. Perform RTL simulation using the provided testbench and tracefile.
3. Perform hardware implementation by using pin planning.
4. Demonstrate the simulations to your RA

Problem Statement

- Write VHDL description in **Behavioral** modeling to implement an **asynchronous set reset D flip flop** and use it to generate **asynchronous down counter** using port mapping.
- Create two seperate vhdl files for D flip flop and Counter.
- The D flip flop must contain inputs and outputs (< Clock Set Reset D >< Q Q_bar >)
- Set and reset are both active high.
- Reset is asynchronous in nature i.e. reset affects the output sequence irrespective of the input clock arrival.
- On Reset, counter should start from "111".

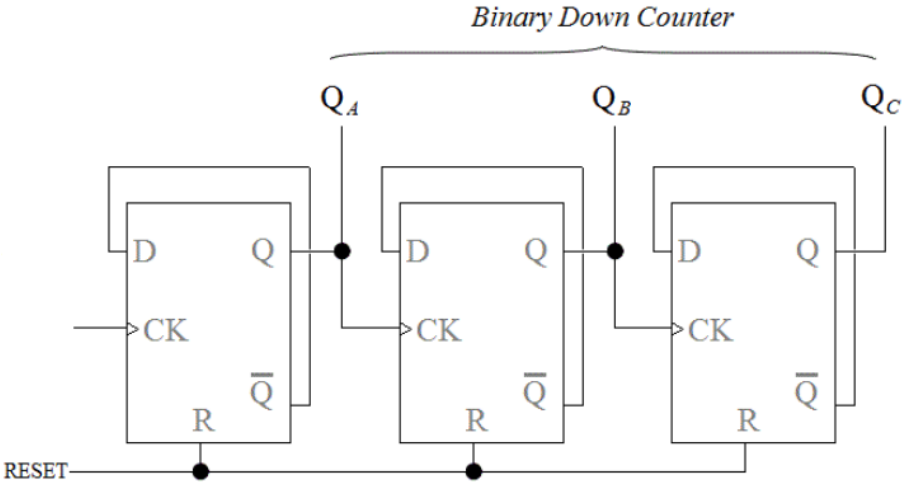

Figure 1: 3-bit Down Counter

- Tracefile format: ($< clock\ reset >$ $< Qc\ Qb\ Qa >$ $< Maskbit >$)
  Tracefile
- For pin planning, use onboard 1Hz clock, switch as reset and LEDs as output.