Experiment No.: 01

Experiment Name: Study of logic gates and verification of their truth tables

OBJECTIVES:

1. To study the basic logic functions AND, OR, INVERTER (NOT), NAND and NOR.
2. To study the representation of these functions by truth tables, logic diagrams and Boolean algebra.

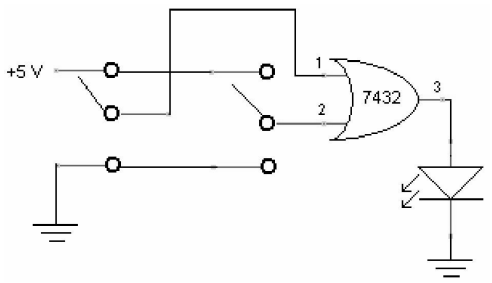
REQUIRED ICs:

1. 2 input AND gate (7408)
2. 2 input OR gate (7432)
3. NOT gate (7404)
4. 2 input NAND gate (7400)
5. 3 input NAND gate (7410)
6. 2 input NOR gate (7402)

EXPERIMENTAL PROCEDURE:

Make all circuit arrangements as given below and complete the truth tables. For each part of the experiment apply the indicated voltage. Use LED to see the output change for different input combinations.

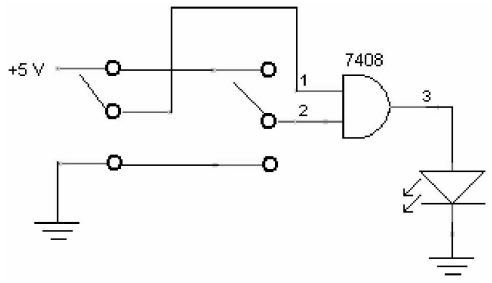
OR Gate:



Truth table: OR gate

Pin 1	Pin 2	Pin 3
0	0	
0	+5	
+5	0	
+5	+5	

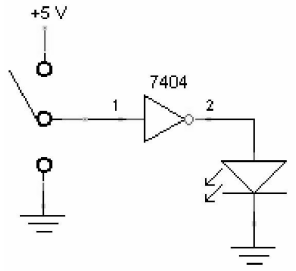
AND Gate:



Truth table: AND gate

Pin 1	Pin 2	Pin 3
0	0	
0	+5	
+5	0	
+5	+5	

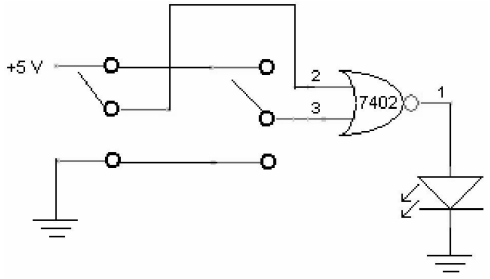
NOT Gate:



Truth table: NOT gate

Pin 1	Pin 2
0	
0	
+5	
+5	

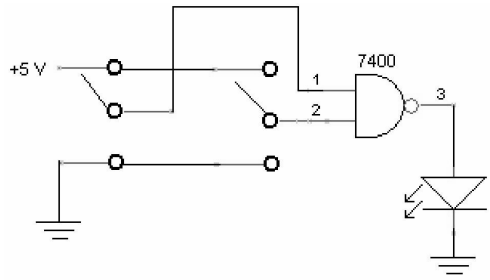
NOR Gate:



Truth table: NOR gate

Pin 2	Pin 3	Pin 1
0	0	
0	+5	
+5	0	
+5	+5	

NAND Gate:



Truth table: NAND gate

Pin 1	Pin 2	Pin 3
0	0	
0	+5	
+5	0	
+5	+5	

TASK:

1. Write the truth table for 3 input NAND gate.
2. Complete the truth table for the diagram of Fig. 1.

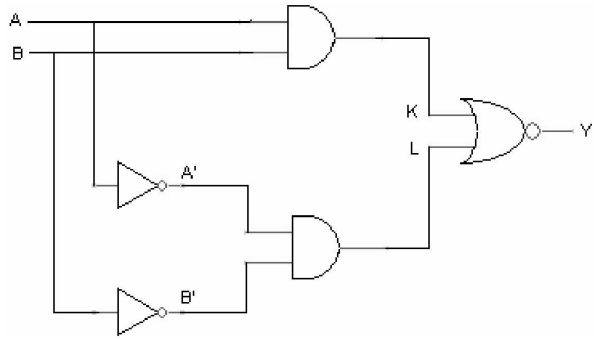


Fig. 1

A	B	A'	B'	K	L	Y
0	0					
0	1					
1	0					
1	1					

REPORT:

1. For each of the logic gate experimented above, draw the circuit diagram and show the measured truth table of your circuit. In the case of truth tables, use 1 and 0, defining logic 1 as a voltage greater than 2.5 V and logic 0 as a voltage less than 1.0 V.
2. Express the Boolean equations between inputs and outputs for each logic gate. Use letter inputs and outputs where they are used.
3. Answer all the questions given in the sheet.
4. Discussion.

Experiment No.: 02

Experiment Name: Study the methods of representation and simplification of logic equations by Boolean algebra

OBJECTIVES:

To study the methods of representation and simplification of logic equations by Boolean algebra.

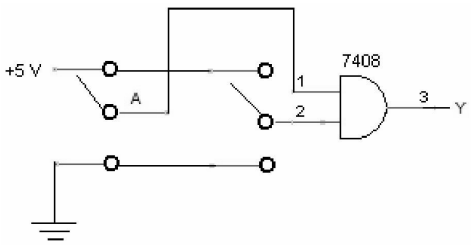
REQUIRED ICs:

1. 2 input OR gate (7432)
2. NOT gate (7404)
3. 2 input AND gate (7408)
4. 2 input NAND gate (7400)

EXPERIMENTAL PROCEDURE:

For all ICs in this experiment; V_{cc} = +5 V to pin 14, 0 (ground) to pin 7.
Make all circuit arrangements as given below and complete the truth tables. For each part of the experiment apply the indicated voltage. Use LED to see the output change for different input combinations.

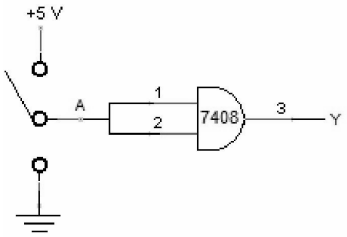
A.1 = A, A.0 = 0:



Truth table

A	Y (A.1)	Y (A.0)
0		
1		

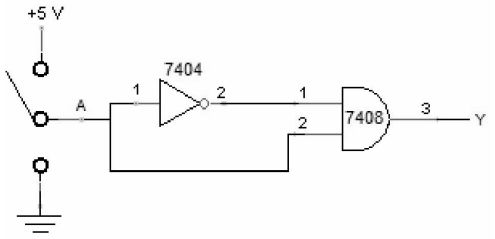
A.A = A:



Truth table

A	Y (A.A)
0	
1	

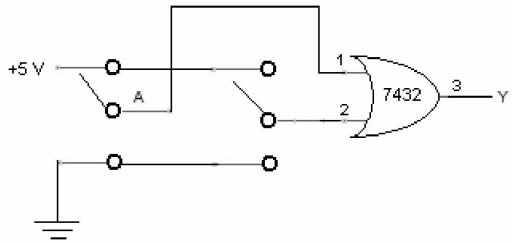
A.A′ = 0:



Truth table

A	A′	Y
0		
1		

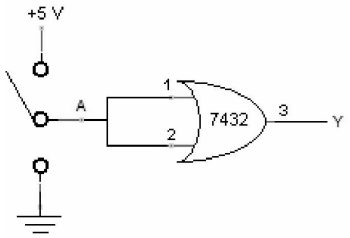
A + 1 = 1, A + 0 = 0:



Truth table

A	Y (A+1)	Y (A +0)
0		
1		

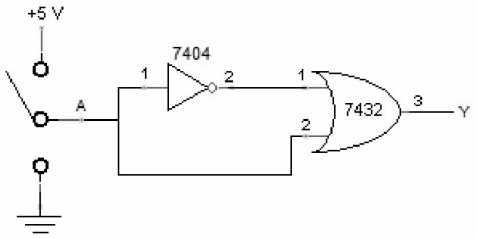
A + A = A:



Truth table: NAND gate

A	Y
0	
1	

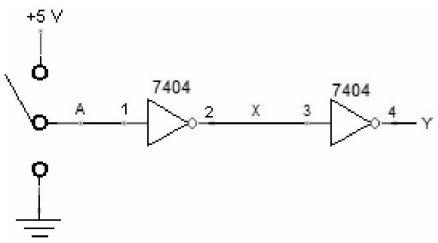
A + A′ = 1:



Truth table

A	A′	Y
0		
1		

A″ = A:



Truth table

A	X	Y
0		
1		

TASK:

1. Complete the truth table and write the Boolean equation of X and Y in terms A and B using Fig. 1.

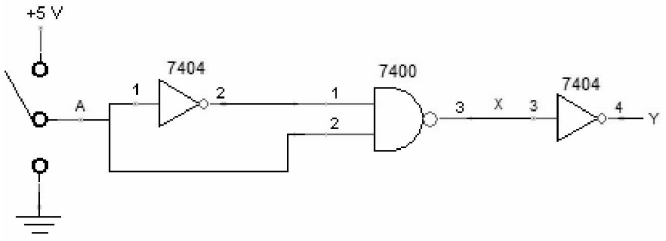


Fig. 1

Truth table for Task-1

A	X	Y
0		
1		

2. Complete the truth table and write the Boolean equation of X and Y using Fig. 2.

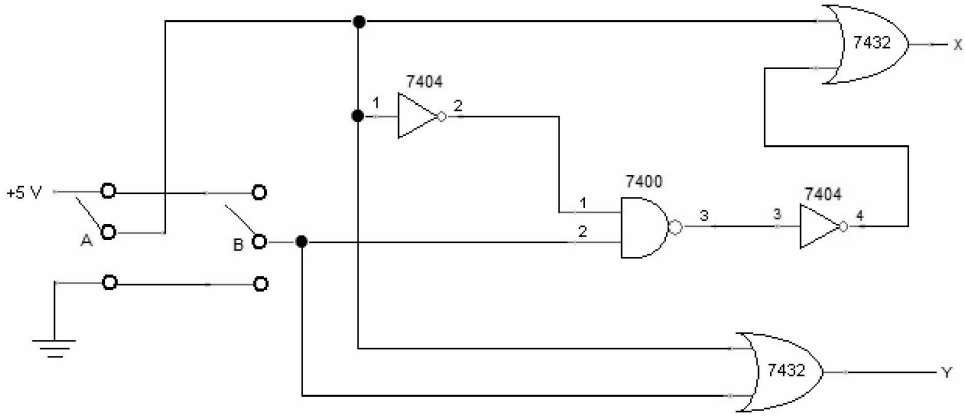


Fig. 2

Truth table for Task-2

A	B	X	Y
0	0		
0	1		
1	0		
1	1		

REPORT:

1. For each of the Boolean algebra experimented above, draw the circuit diagram and show the measured truth table of your circuit.
2. Answer all the questions given in the sheet.
3. Discussion.

Experiment No.: 03

Experiment Name: Study the technique of representing all logic gates by using NAND gate

OBJECTIVES:

To study the technique of representing all logic gates by using NAND gate.

REQUIRED ICs:

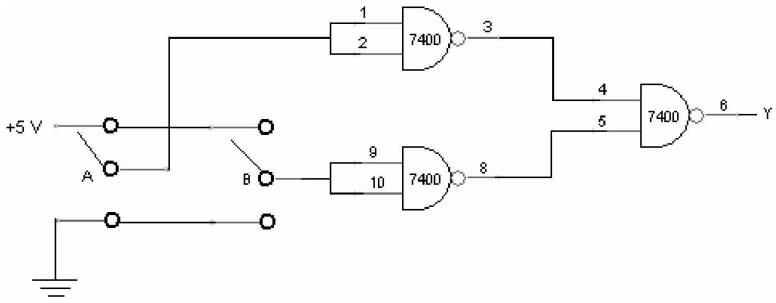
1. 2 input NAND gate (7400)

UNIVERSAL GATE: The NAND gate is said to be a universal gate because any digital system can be implemented with it. To show that any Boolean function can be implemented with NAND gates, we need only show that the logic operations AND, OR and NOT can be implemented with NAND gates. A convenient way to implement a combinational circuit with NAND gates is to obtain the simplified Boolean functions in terms of AND, OR and NOT and convert the functions to NAND logic.

EXPERIMENTAL PROCEDURE:

For all ICs in this experiment; V_{cc} = +5 V to pin 14, 0 (ground) to pin 7.
Make all circuit arrangements as given below and complete the truth tables. For each part of the experiment apply the indicated voltage. Use LED to see the output change for different input combinations.

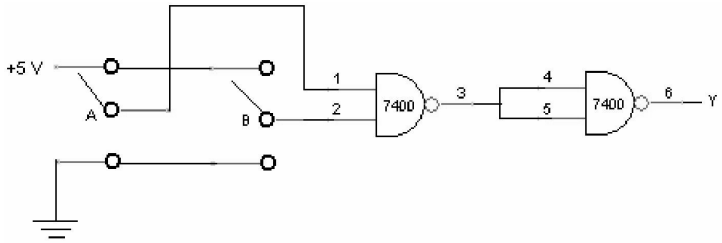
OR Gate:



Truth table: OR gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

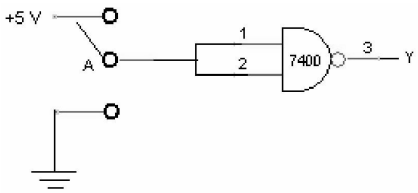
AND Gate:



Truth table: AND gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

NOT Gate:



Truth table: NOT gate

A	Y
0	
1	

TASK:

1. Write the function of F and implement this function using only NAND gate. Verify the correctness of implemented NAND logic diagram by comparing truth table of both diagrams.

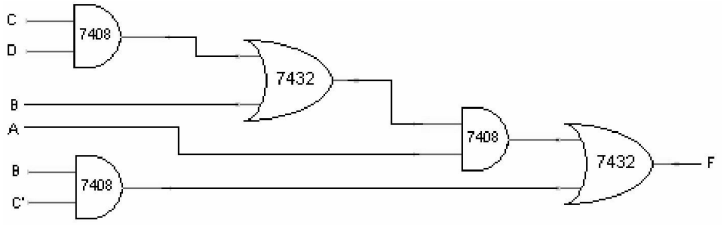


Fig.1

2. Implement OR, AND and NOT logic using only NOR gate. Draw the NOR logic diagram of Fig. 1.

REPORT:

1. For each part experimented above, draw the circuit diagram and show the measured truth table of your circuit.
2. Answer all the questions given in the sheet.
3. Discussion.

Experiment No.: 04

Experiment Name: Design and construction of half adder and full adder circuits

OBJECTIVE:

To realize half and full adder using X-OR and basic gates and verify its truth table.

REQUIRED ICs:

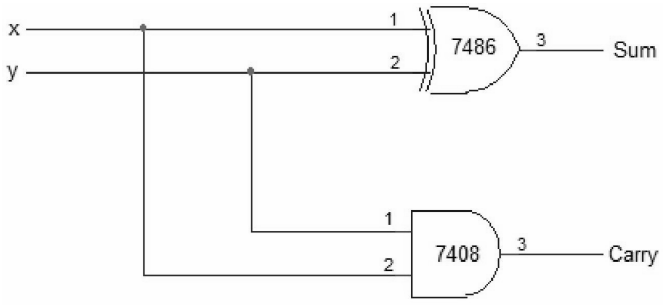
1. AND gate (7408)
2. OR gate (7432)
3. X-OR gate (7486)
4. 4-bit full-adder (7483)

EXPERIMENTAL PROCEDURE:

For all ICs in this experiment; V_{cc} = +5 V to pin 14, 0 (ground) to pin 7.

1. Make the connections as per the circuit diagram.
2. Switch on VCC and apply various combinations of input according to truth table.
3. Note down the output readings for half/full adder sum and the carry bit for different combinations of inputs.

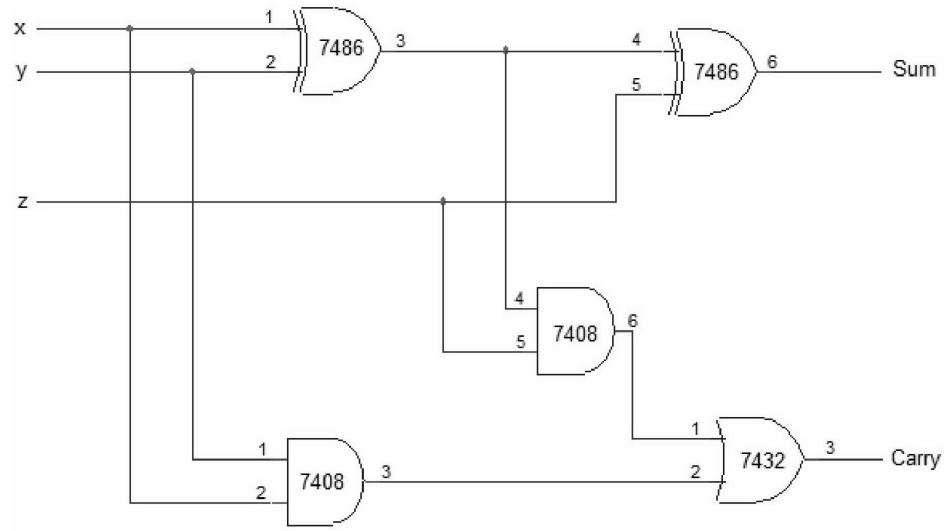
Half-Adder:



Truth table for Half-Adder

Input		Output	
X	Y	S	C
0	0		
0	1		
1	0		
1	1		

Full-Adder:



Truth table for Full-Adder

Input			Output	
X	Y	Z	S	C
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

TASK:

1. Implement the NAND logic diagram of Half-adder and Full-adder.
2. Design and Implement 4-bit binary adder.
3. Implement the BCD adder using 7483.

REPORT:

1. For each part experimented above, draw the circuit diagram and show the measured truth table of your circuit. Compare your measured truth table with actual one.
2. Write the Boolean logic equation for each circuit output.
3. Complete all the tasks given in the sheet.
4. Discussion.

Experiment No.: 05

Experiment Name: Design and implementation of one bit and two bit Magnitude Comparator using logic gates

OBJECTIVE:

To design and implement one bit and two bit Magnitude Comparator using logic gates.

REQUIRED ICs:

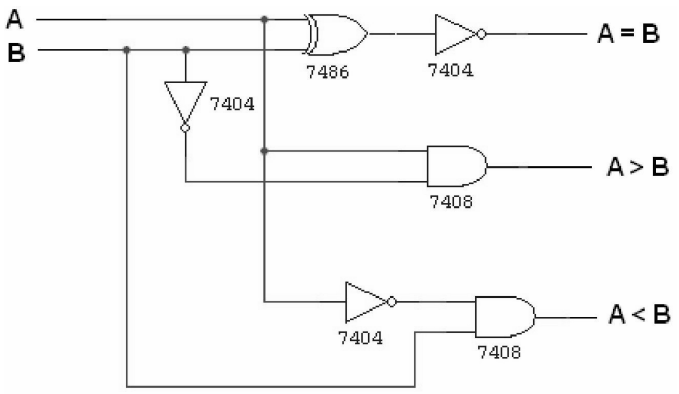
1. NOT gate (7404)
2. AND gate (7408)
3. OR gate (7432)
4. X-OR GATE (7486)

EXPERIMENTAL PROCEDURE:

For all ICs in this experiment; V_{cc} = +5 V to pin 14, 0 (ground) to pin 7.

1. Make the connections as per the circuit diagram.
2. Switch on V_{CC} and apply various combinations of input according to truth table.
3. Note down the output readings of 1-bit and 2bit magnitude comparator for different combinations of inputs.

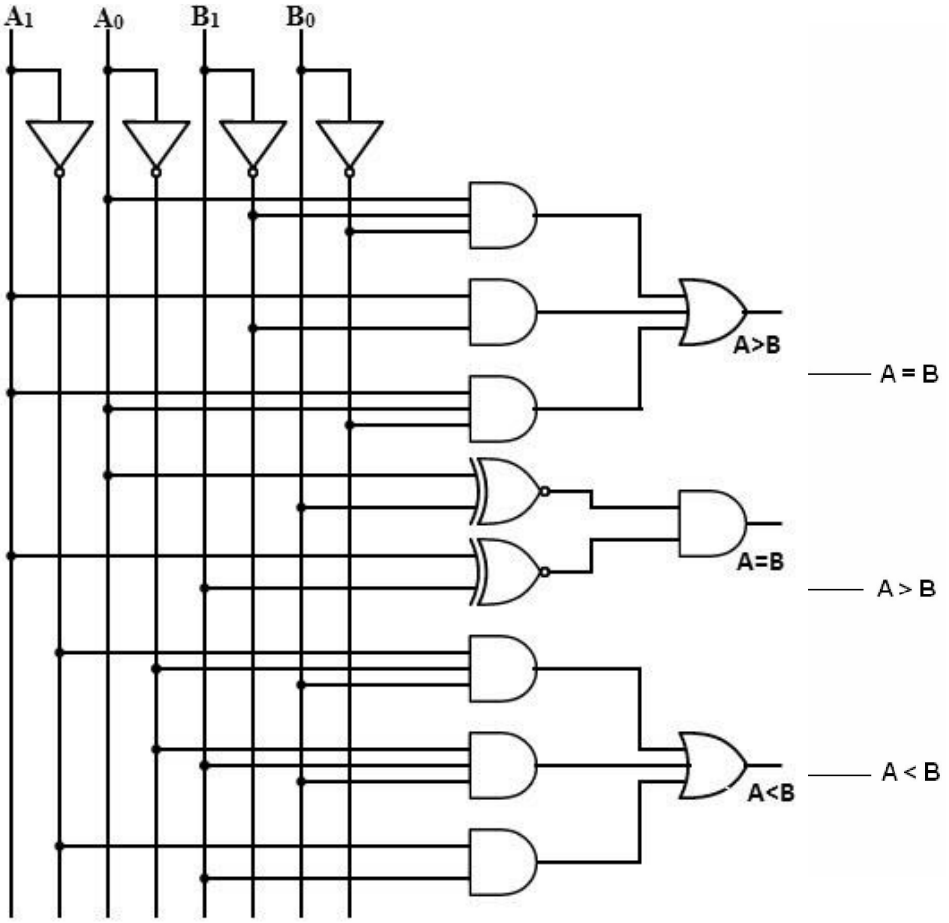
1-bit Magnitude Comparator:



Truth table of 1 bit magnitude comparator

Input		Output		
A	B	A>B	A=B	A<B
0	0			
0	1			
1	0			
1	1			

2-bit Magnitude Comparator:



Truth table of 2 bit magnitude comparator

Input				Output		
A_0	A_1	B_0	B_1	A>B	A=B	A<B
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			

1	1	0	1			
1	1	1	0			
1	1	1	1			

TASK:

1. Design and implement a 4-bit magnitude comparator.
2. Write the truth table of 4-bit magnitude comparator and verify it with your implemented comparator.

REPORT:

1. For each part experimented above, draw the circuit diagram and show the measured truth table of your circuit.
2. Write Boolean logic equation for each circuit.
3. Answer all the questions given in the sheet.
4. Discussion.

Experiment No.: 06

Experiment Name: Design and implementation of multiplexer and demultiplexer

OBJECTIVE:

To design and implement multiplexer and demultiplexer using logic gates.

REQUIRED ICs:

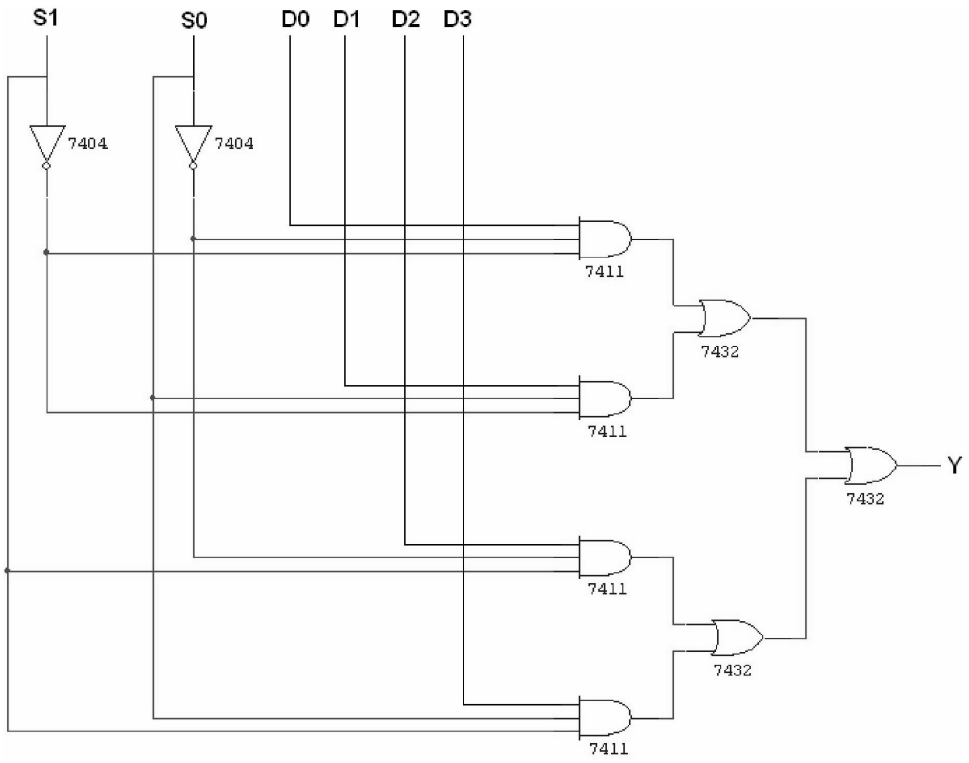
1. NOT gate (7404)
2. 3 input AND gate (7411)
3. OR gate (7432)

EXPERIMENTAL PROCEDURE:

For all ICs in this experiment; V_{cc} = +5 V to pin 14, 0 (ground) to pin 7.

1. Make the connections as per the circuit diagram.
2. Switch on V_{CC} and apply various combinations of input according to truth table.
3. Note down the output readings for each logic circuit for different combinations of inputs.

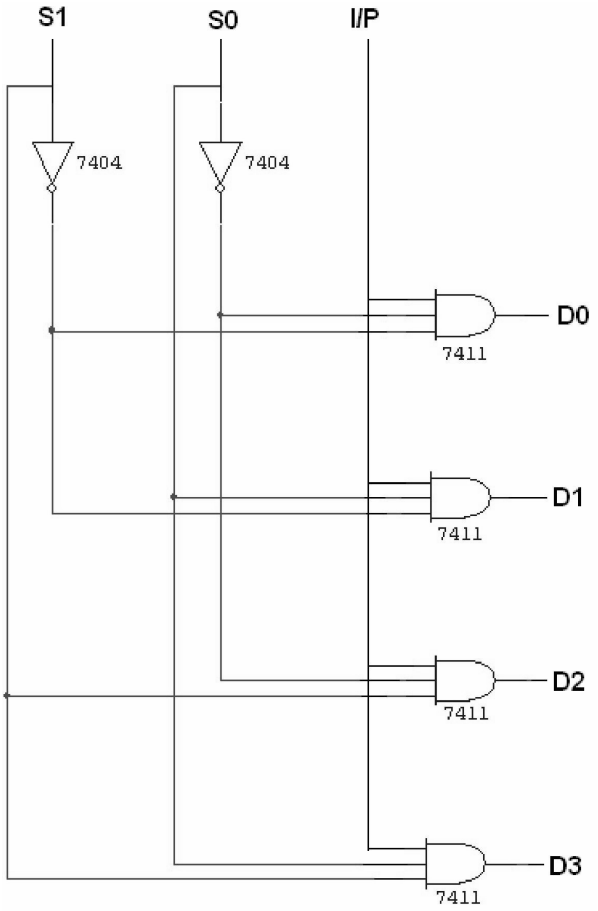
Multiplexer:



Truth table of Multiplexer

Input		Output	
S0	S1	Y	Actual
0	0		D_0
0	1		D_1
1	0		D_2
1	1		D_3

Demultiplexer:



Truth table of Demultiplexer

Input			Output			
i/p	S_0	S_1	D_0	D_1	D_2	D_3
0	X	X				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

TASK:

1. Design and construct a demultiplexer with NAND gate and write its truth table.
2. Obtain an 8 X 1 multiplexer with a dual 4-line to 1-line multiplexer having separate enable inputs but common selection lines. Use a block diagram construction.

REPORT:

1. For each part experimented above, draw the circuit diagram and show the measured truth table of your circuit.
2. Complete all the tasks given in the sheet.
3. Discussion.

Experiment No.: 07

Experiment Name: Design and implementation of encoder and decoder

OBJECTIVES:

To design and implement encoder and decoder using logic gates.

REQUIRED ICs:

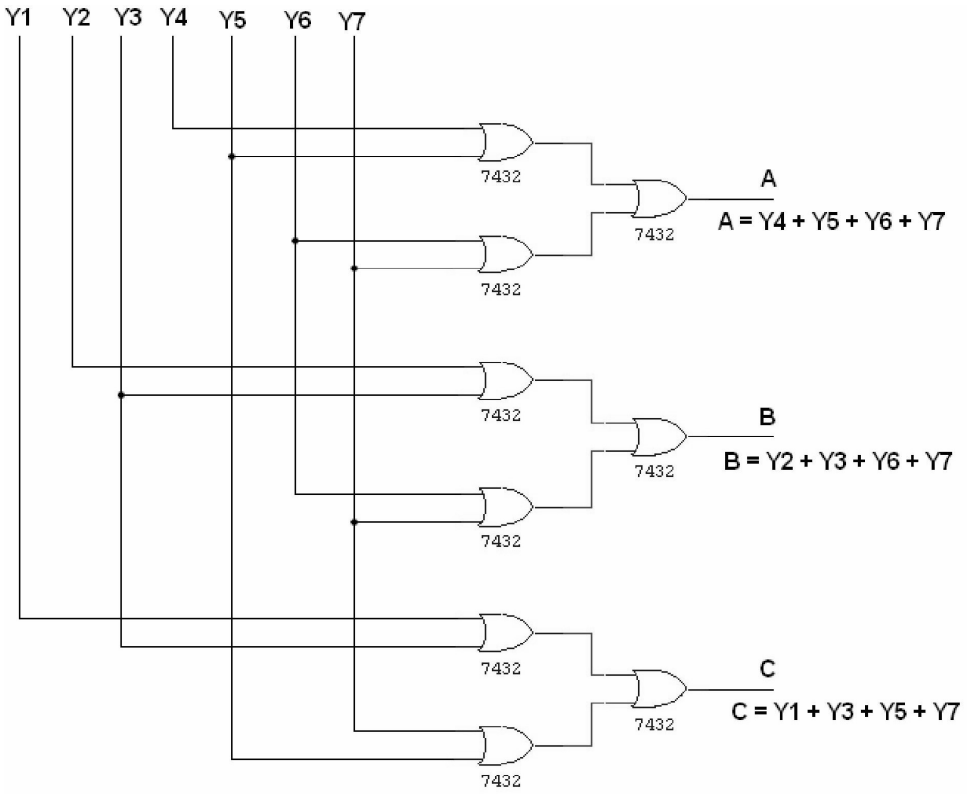
1. NOT gate (7404)
2. 3 input NAND gate (7410)
3. OR gate (7432)

EXPERIMENTAL PROCEDURE:

For all ICs in this experiment; V_{cc} = +5 V to pin 14, 0 (ground) to pin 7.

1. Make the connections as per the circuit diagram.
2. Switch on V_{CC} and apply various combinations of input according to truth table.
3. Note down the output readings of encoder and decoder circuit for different combinations of inputs.

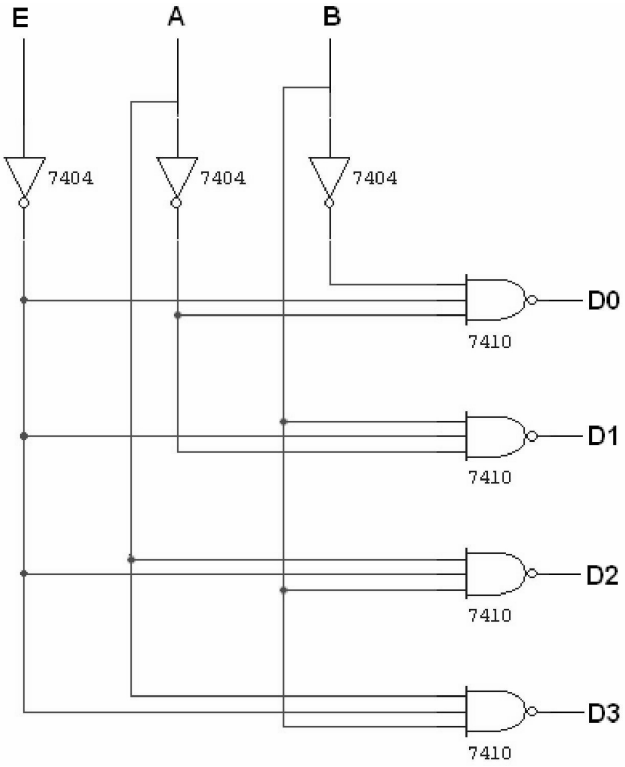
Encoder:



Truth table of Encoder

Input								Output		
Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	A	B	C
1	0	0	0	0	0	0	0			
0	1	0	0	0	0	0	0			
0	0	1	0	0	0	0	0			
0	0	0	1	0	0	0	0			
0	0	0	0	1	0	0	0			
0	0	0	0	0	1	0	0			
0	0	0	0	0	0	1	0			
0	0	0	0	0	0	0	1			

Decoder:



Truth table of Decoder

Input			Output			
E	A	B	D0	D1	D2	D3
1	0	0				
0	0	0				
0	0	1				
0	1	0				
0	1	1				

TASK:

1. Design and implement a 3-to-8 line decoder. Write the Boolean logic function for all its output. Verify its truth table.
2. Design a encoder using NOR gate and write the truth table for it.

REPORT:

1. For each part experimented above, draw the circuit diagram and show the truth table of that circuit. Verify the measured truth table with the actual one.
2. Complete all the tasks given in the sheet.
3. Discussion.

Experiment No.: 08

Experiment Name: Study of different types of Flip Flop

OBJECTIVE:

To Study the different types of Flip Flop.

REQUIRED ICs:

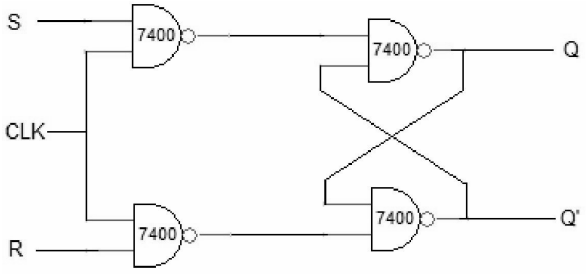
1. NANDgate (7400)
2. NOT gate (7404)

EXPERIMENTAL PROCEDURE:

For all ICs in this experiment; V_{cc} = +5 V to pin 14, 0 (ground) to pin 7.

1. Make the connections as per the circuit diagram.
2. Switch on V_{CC} and apply various combinations of input according to truth table.
3. Note down the output readings of different flip flop circuits for different combinations of inputs.

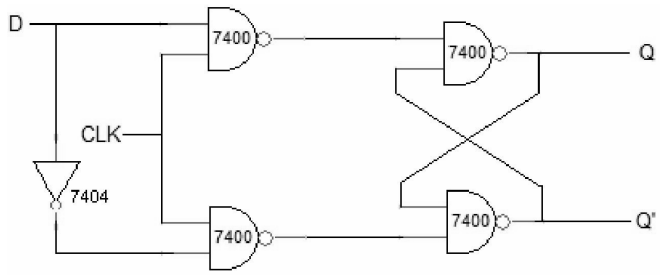
RS Flip-Flop:



Characteristic table of RS Flip-Flop

Q	S	R	Q (t+1)	Q′ (t+1)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

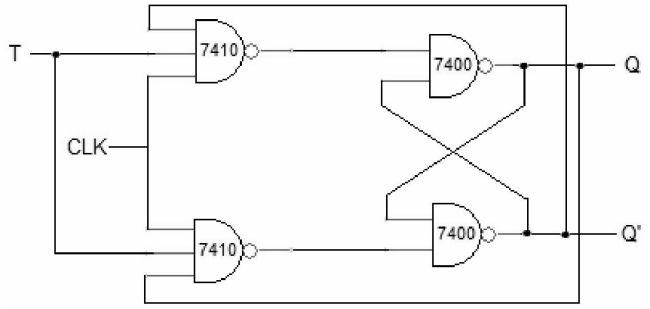
D Flip-Flop:



Characteristic table of D Flip-Flop

Q	D	Q (t+1)	Q′
0	0		
0	1		
1	0		
1	1		

T Flip-Flop:



Characteristic table of T Flip-Flop

Q	T	Q (t+1)	Q′
0	0		
0	1		
1	0		
1	1		

TASK:

1. Design and implement JK Flip-Flop and verify its characteristic table. Write also its characteristic equation.
2. Design RS, D and T flip-flop with AND and NOR gate and write characteristic equation and table for them.

REPORT:

1. For each Flip-flop experimented above, draw the circuit diagram and show the measured characteristic table of your circuit.
2. Complete all the tasks given in the sheet.
3. Discussion.

Experiment No.: 09

Experiment Name: Construction and verification of 4-bit ripple counter

OBJECTIVES:

To construct and verify the 4-bit ripple counter.

REQUIRED ICs:

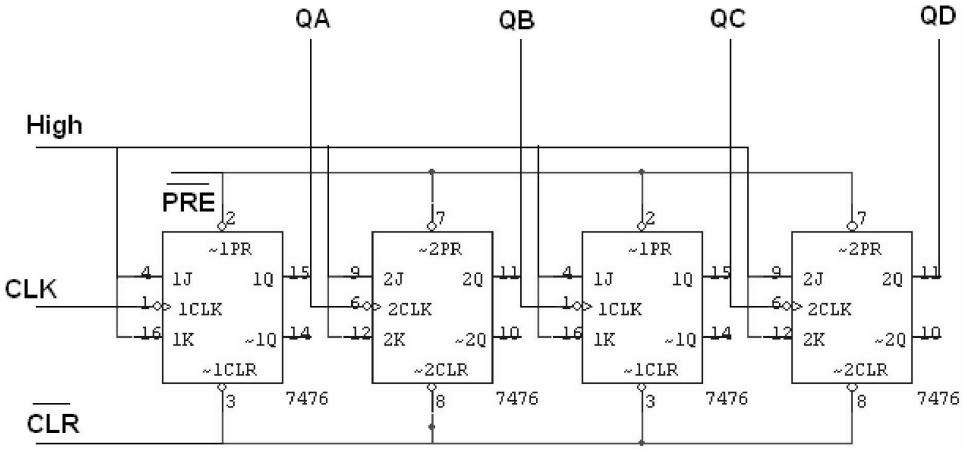
1. JK Flip flop (7476)
2. NAND gate (7400)

EXPERIMENTAL PROCEDURE:

For all ICs in this experiment; V_{cc} = +5 V to pin 14, 0 (ground) to pin 7.

1. Make the connections as per the circuit diagram.
2. Switch on V_{CC} and apply various combinations of input according to truth table.
3. Note down the output readings of 4-bit ripple counter for different combinations of inputs.

4-bit Ripple Counter:



Count sequence for a binary Ripple Counter				
CLK	Q_A	Q_B	Q_C	Q_D
0				
1				
2				
3				
4				
5				
6				
7				

8				
9				
10				
11				
12				
13				
14				
15				

TASK:

1. Design and implement a BCD ripple counter. Show its count sequence for different clock pulse.
2. Design and implement a 4-bit synchronous binary counter.

REPORT:

1. For 4-bit binary ripple counter experimented above, draw the circuit diagram and show the measured count sequence of your circuit.
2. Answer all the questions given in the sheet.
3. Discussion.

Experiment No.: 10

Experiment Name: Study of shift register in all its modes

OBJECTIVES:

To design and implement

(i) Serial in serial out
(ii) Serial in parallel out
(iii) Parallel in serial out
(iv) Parallel in parallel out

REQUIRED ICs:

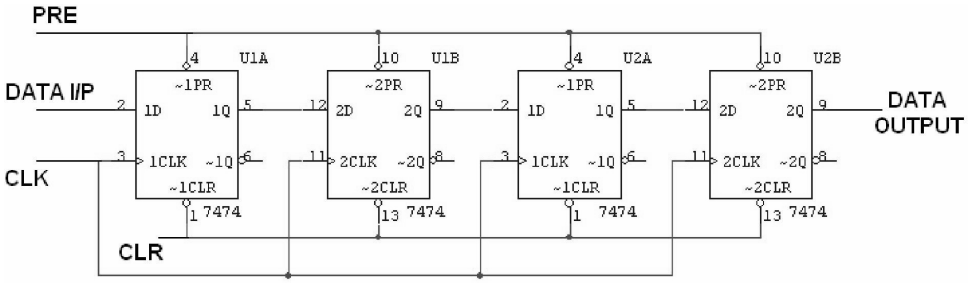
1. D Flip flop (7474)
2. OR Gate (7432)
3. Shift register (7495)

EXPERIMENTAL PROCEDURE:

For all ICs in this experiment; V_{cc} = +5 V to pin 14, 0 (ground) to pin 7.

1. Make the connections as per the circuit diagram.
2. Switch on V_{CC} and apply various combinations of input according to truth table.
3. Note down the output readings for different modes of shift register for different combinations of inputs.

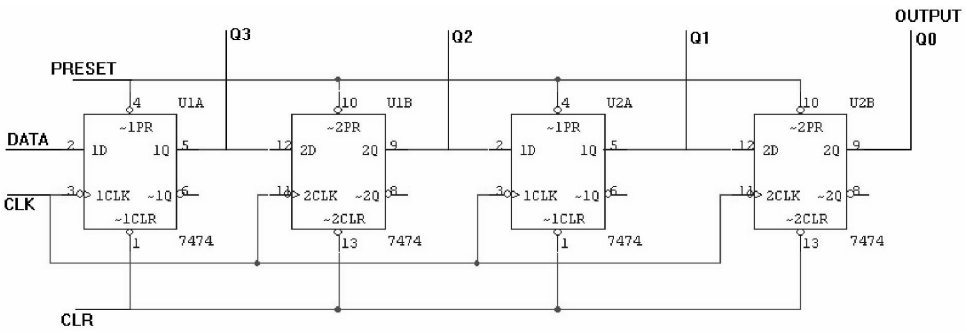
Serial In Serial Out:



Truth table of SISO

CLK	Serial in	Serial out
1	1	
2	0	
3	0	
4	1	
5	X	
6	X	
7	X	

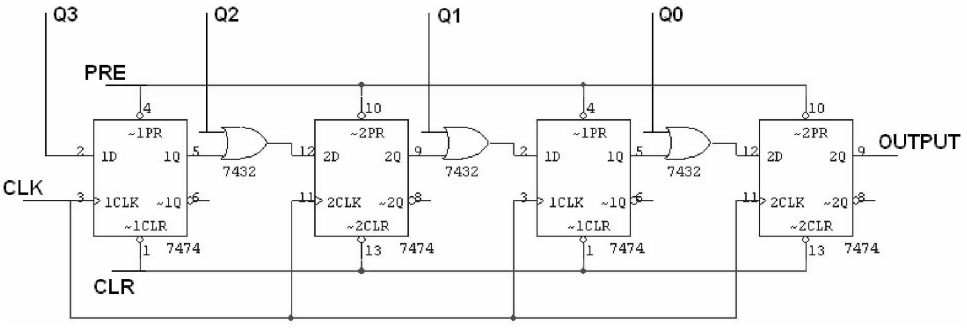
Serial In Parallel Out:



Truth table of SIPO

CLK	Data	Output			
		Q_1	Q_2	Q_3	Q_4
1	1				
2	0				
3	0				
4	1				

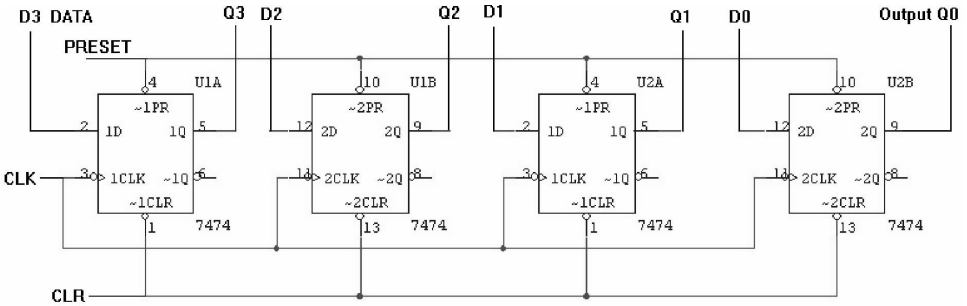
Parallel In Serial Out:



Truth table of PISO

CLK	Q_3	Q_2	Q_1	Q_0	O/P
0	1	0	0	1	
1	0	0	0	0	
2	0	0	0	0	
3	0	0	0	0	

Parallel In Parallel Out:



Truth table of PIPO

CLK	Data input				Output			
	D_A	D_B	D_C	D_D	Q_A	Q_B	Q_C	Q_D
1	1	0	0	1				
2	1	0	1	0				

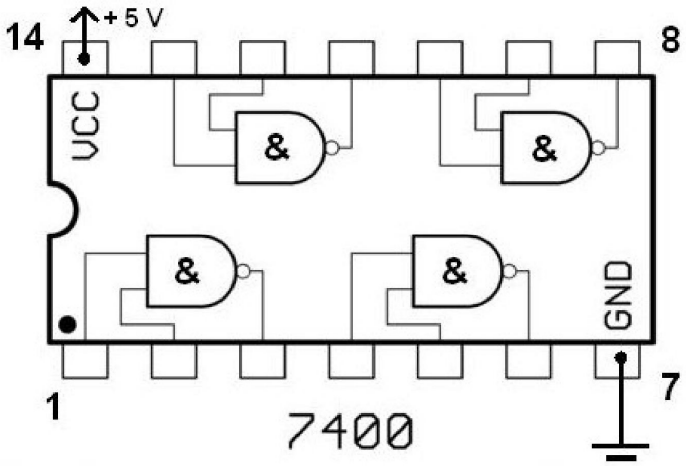
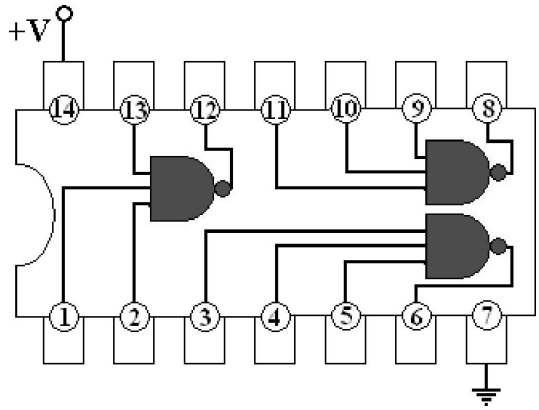
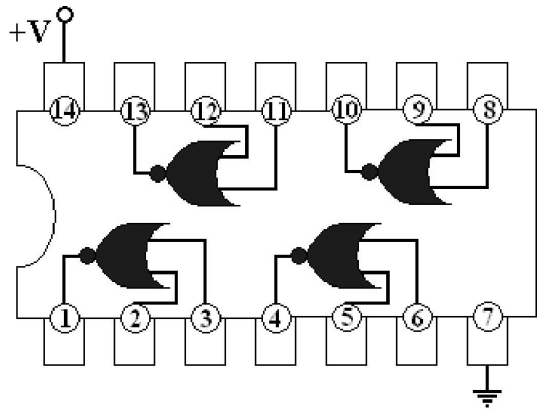
TASK:

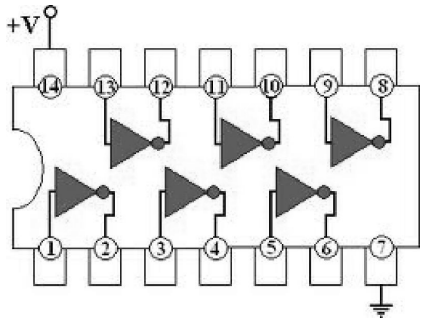
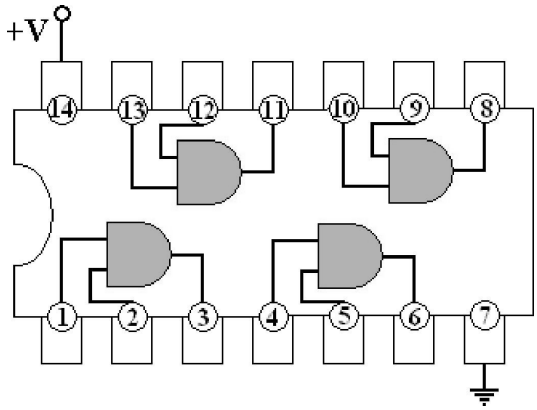
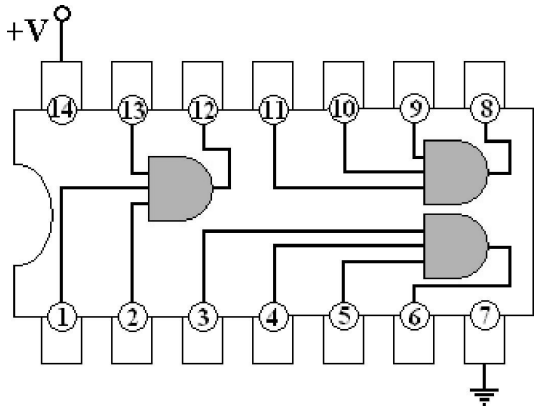
1. Implement all the modes using shift register 7495.
2. Give data 1010 as input in Parallel in serial out register and use the obtained output as input to Serial in parallel out register. Write truth table in terms of input and final output.

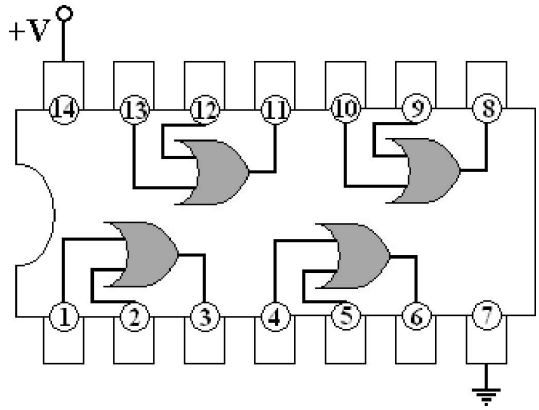
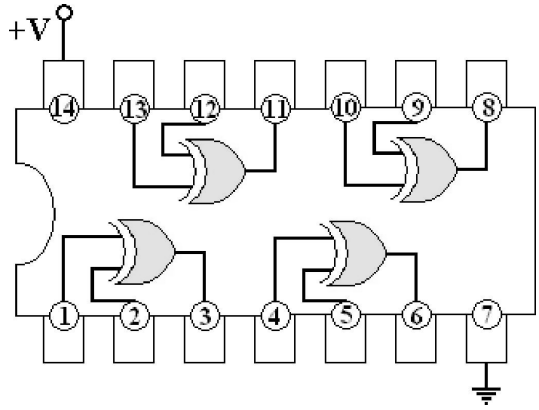
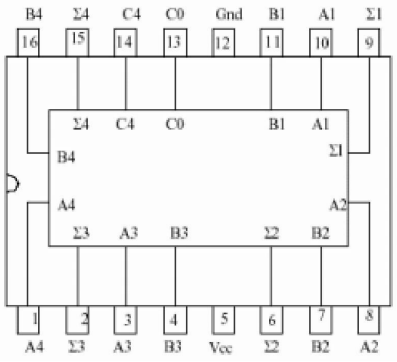
REPORT:

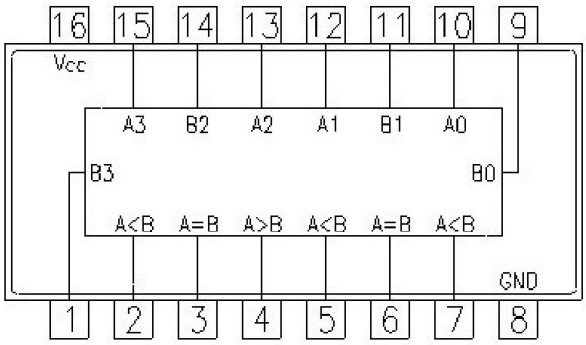
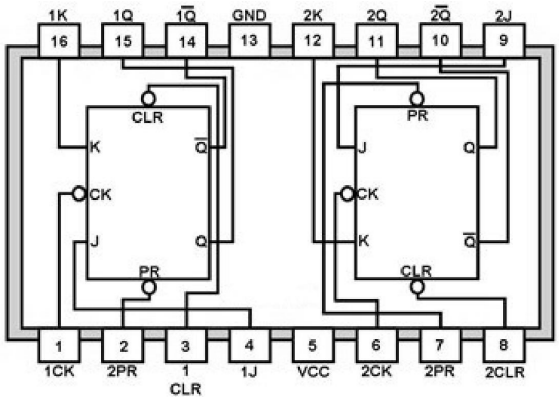
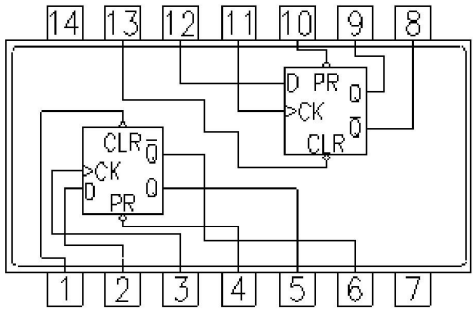
1. For each mode of shift register experimented above, draw the circuit diagram and show the measured truth table of your circuit. Verify this truth table.
2. Answer all the questions given in the sheet.
3. Discussion.

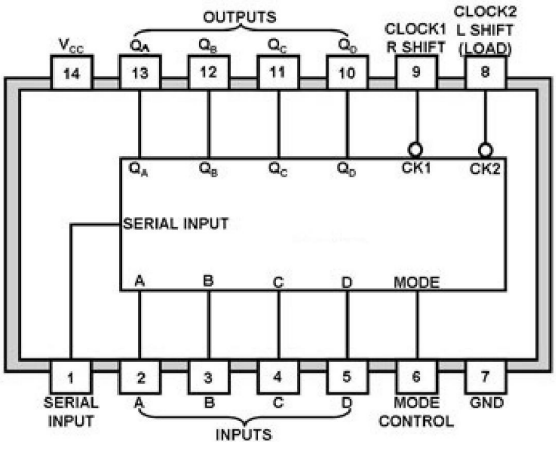
IC Pin Diagram

2 input NAND gate **7400**	
3 input NAND gate **7410**	
NOR gate **7402**	

NOT gate **7404**	
2 input AND gate **7408**	
3 input AND gate **7411**	

OR gate **7432**	
X-OR gate **7486**	
4-bit Adder **7483**	

4-bit Magnitude Comparator **7485**	 7485 4–Bit Magnitude Comparator
JK Flip-flop **7476**	
D Flip-flop **7474**	 7474 Dual D Flip–Flop with Preset and Clear

Shift Register **7495**	
SRAM **7489**