GUJARAT TECHNOLOGICAL UNIVERSITY (GTU)

Competency-focused Outcome-based Green Curriculum-2021 (COGC-2021)
Semester- III

Course Title: Digital Techniques
(Course Code: 4331701)

Diploma program in which this course is offered	Semester in which offered
Instrumentation and Control Engineering	Third

1. RATIONALE

Digital electronics and techniques are almost part and parcel of any modern industrial equipment. Integrating industrial process signals for logical and mathematical operations, using combinational and sequential logic for process control components are some of the skills required in this area by IC engineers. This requires every diploma engineer to possess the basic skills of digital techniques to maintain various digitally controlled industrial process systems effectively and efficiently. Hence, this course has been designed to fulfill this purpose.

2. COMPETENCY ('Program Outcome' according to NBA Terminology)

The course content should be taught and implemented with the aim to develop different types of skills so that students are able to acquire following competency:

- **Implement various sequential and combinational logic circuits using Logic gates.**

3. COURSE OUTCOMES (COs)

The practical exercises, the underpinning knowledge and the relevant soft skills associated with this competency are to be developed in the student to display the following COs:

a) Convert the given number from one number system to another number system.
b) Realize Boolean expressions using logic gates.
c) Simplify Boolean expression using Boolean algebra & Karnaugh map.
d) Implement various combinational logic circuits.
e) Implement various sequential logic circuits.

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P/2)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	CA	ESE	CA	ESE	
3	0	2	4	30	70	25	25	150

***Legends: L**-Lecture; **T** – Tutorial/Teacher Guided Theory Practice; **P** - Practical; **C** – Credit, **CA** - Continuous Assessment; **ESE** - End Semester Examination.*

5. SUGGESTED PRACTICAL EXERCISES

The following practical outcomes (PrOs) are the sub-components of the COs. Some of the PrOs marked '*' are compulsory, as they are crucial for that particular CO at the 'Precision Level' of Dave's Taxonomy related to 'Psychomotor Domain'.

S. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. required
1	Test the functionality of basic logic gates.	2	2*
2	Build/ test the functionality of exclusive-OR gate.	2	2*
3	Build/ test the functionality of NAND gate as a universal gate.	2	2*
4	Build/ test the functionality of NOR gate as a universal gate.	2	2*
5	Verify De Morgan's theorem.	2	2*
6	Test simplified circuit using minimum logic gates employing Karnaugh map method for given Boolean expression.	3	2
7	Test simplified circuit using minimum logic gates employing Boolean algebra theorems for given Boolean expression.	3	2
8	Build/test the 1 bit HALF ADDER circuit.	4	2
9	Build/test the 4 bit FULL ADDER circuit.	4	2
10	Build/test 1 bit HALF SUBTRACTOR circuit.	4	2
11	Verify 3 to 8 Decoder	4	2
12	Verify 4 to 2 encoder	4	2
13	Build/test odd parity bit generator	5	2
14	Build/test even parity bit checker	5	2
15	Build/test S-R flip flop.	5	2*
16	Build/test JK, T & D flip flop.	5	2*
17	Build/test 4 bit asynchronous counter.	5	2
18	Build/test 4 bit synchronous counter.	5	2
19	Build/test shift register	5	2
	Total (any 14)		**28**

Note

*i. More **Practical Exercises** can be designed and offered by the respective course teacher to develop the industry relevant skills/outcomes to match the COs. The above table is only a suggestive list.*

*ii. The following are some **sample** 'Process' and 'Product' related skills (more may be added/deleted depending on the course) that occur in the above listed **Practical Exercises** of this course required which are embedded in the COs and ultimately the competency..*

S. No.	Sample Performance Indicators for the PrOs	Weightage in %
1	Prepare of experimental setup	20
2	Operate the equipment setup or circuit	20
3	Follow safe practices measures	10
4	Record observations correctly	20
5	Interpret the result and conclude	30
Total		**100**

6. MAJOR EQUIPMENT/ INSTRUMENTS REQUIRED

This major equipment with broad specifications for the PrOs is a guide to procure them by the administrators to usher in uniformity of practicals in all institutions across the state.

i. Bread boards
ii. DC Regulated power supply 0-30 volt DC (10 Nos.)
iii. Digital IC Tester (40 pins)

iv. Digital Logic trainer kit (10 Nos.)
v. Hardwired relay logic trainer (5 Nos.)

7. AFFECTIVE DOMAIN OUTCOMES

The following sample Affective Domain Outcomes (ADOs) are embedded in many of the above mentioned COs and PrOs. More could be added to fulfil the development of this competency.

a) Work as a leader/a team member.
b) Follow safety practices while using electrical appliances.
c) Practice environmental friendly methods and processes. (Environment related)

The ADOs are best developed through the laboratory/field based exercises. Moreover, the level of achievement of the ADOs according to Krathwohl's 'Affective Domain Taxonomy' should gradually increase as planned below:

i. 'Valuing Level' in 1st year
ii. 'Organization Level' in 2nd year.
iii. 'Characterization Level' in 3rd year.

8. UNDERPINNING THEORY

Only the major Underpinning Theory is formulated as higher level UOs of Revised Bloom's taxonomy in order development of the COs and competency is not missed out by the students and teachers. If required, more such higher level UOs could be included by the course teacher to focus on attainment of COs and competency.

Unit	Major Learning Outcomes ('Course Outcomes' in Cognitive Domain according to NBA terminology)		Topics and Sub-topics	
Unit – I Number Systems	1a	List types of numbers systems.	1.1	Number systems: Binary, Octal, Decimal and Hexadecimal
	1b	Represent numbers (with integer and fractional part) from the given number systems.		
	1c	Convert the given number from one number system to another number system.	1.2	Conversion of numbers
			1.2.1	Binary, octal & hexadecimal numbers to Decimal number.
			1.2.2	Decimal number to binary number.
			1.2.3	Octal & Hexadecimal number to binary number.
	1d	Perform arithmetic operations on binary numbers.	1.3	Binary arithmetic Operation: addition, subtraction, multiplication and division
Unit – II Logic Gates and Boolean Algebra	2a	Represent signals in logic 0 and logic 1 in positive logic system.	2.1	Two state logical operation:
	2b	Represent signals in logic 0 and logic 1 in positive logic system.		
	2c	State tri-state operation.	2.2	Tristate logic operation
	2d	Draw the symbol and equivalent electrical circuits of given gates.	2.3	Logic Gates: : AND,OR, NOT,NAND, NOR,EX-OR & EX-NOR Gates: Symbols, Boolean expression, Equivalent electrical circuits and truth table of each gates
	2e	Explain functionality of any gate with the help of its truth table.		
	2f	Implement all the other gates with the help of universal gate.		

Unit	Major Learning Outcomes ('Course Outcomes' in Cognitive Domain according to NBA terminology)		Topics and Sub-topics	
	2g	State and verify De Morgan's First and Second theorem.	2.4	De Morgan's theorems
	2h	List Boolean expressions for Properties of Boolean Algebra.	2.5	Laws, theorems and postulates of Boolean algebra
	2i	Obtain dual expressions of the above listed Boolean expressions.		
	2j	Realize above listed Boolean expressions using logic gates.		
Unit – III Design of Combinational Circuits	3a	Define combinational Logic circuits	3.1	Combinational circuits: definition
	3b	Simplify given expression using Boolean algebra and represent SOP using logic gates	3.2	Boolean expressions types: Sum of Products(SOP), Product of Sums(POS)
	3c	Simplify given expression using Boolean algebra and represent POS using logic gates		
	3d	Simplify given expression using Karnaugh map and represent SOP or POS using logic gates	3.3	Karnaugh map method(up to 4 variables) for simplification of Boolean expression including don't care cases
Unit – IV Digital Arithmetic	4a	Obtain 1's and 2's complement of given binary number.	4.1	1's and 2's complements of binary number.
	4b	Perform binary subtraction using 1's & 2's complement.	4.2	Binary subtraction using 1's and 2's complement method
	4c	Explain given circuits using Logic gates and truth table.	4.3	Arithmetic Circuits: 1 bit Half adder, 1 bit full adder, 1 bit half and full subtractor, 4 bit parallel adder, 4 bit subtractor using 2's complement circuit,
	4d	Explain given circuits using Logic gates and truth table.	4.4	Decoder: 2 to 4 & 3 to 8
			4.5	Encoder: 4 to 2 & 8 to 3
			4.6	Multiplexer: 4 to 1
			4.7	Demultiplexer: 1 to 4
	4e	List types of codes	4.8	Types of codes: Weighted binary code: Normal, BCD(8421), 2421 non weighted: Excess-3, Gray code
	4f	Convert binary code to non-weighted code		
	4g	Convert non weighted code to binary code		
	4h	Explain given circuits using Logic gates and truth table.	4.9	Code Converters: 4 bit Binary to gray and gray to binary code converters
	4i	Explain given circuits using Logic gates and truth table.	4.10	Parity bit Generators and Checker circuits.
Unit – V Sequential	5a	Define terms related to sequential logic circuits.	5.1	Digital clock signal, duty cycle, synchronous and asynchronous circuit operation, Edge and Level

Unit	Major Learning Outcomes ('Course Outcomes' in Cognitive Domain according to NBA terminology)		Topics and Sub-topics	
Circuits				triggered operation.
	5b	Draw block diagram of sequential circuit	5.2	Sequential Circuits: introduction
	5c	Compare combinational & sequential circuits		
	5d	Explain given flip-flop using logic gate & truth table	5.3	Flip-Flops: S-R, J-K, T and D
	5e	Explain given counter using timing & circuit diagram.	5.4	Counters: 4 bit asynchronous, 4 bit synchronous
	5f	Explain given shift register using timing & circuit diagram.	5.5	Shift Registers: 4 bit serial in-serial out, serial in-parallel out & parallel in –serial out

***Note**: The UOs need to be formulated at the 'Application Level' and above of Revised Bloom's Taxonomy' to accelerate the attainment of the COs and the competency.*

9. SUGGESTED SPECIFICATION TABLE FOR QUESTION PAPER DESIGN

Unit	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Number Systems	8	04	06	04	14
II	Logic Gates and Boolean Algebra	8	06	04	04	14
III	Design of Combinational Circuits	8	02	06	06	14
IV	Digital Arithmetic	10	04	04	06	14
V	Sequential Logic Circuits	8	02	06	06	14
	Total	**42**	**18**	**26**	**26**	**70**

Legends: R = Remember; U = Understand; A = Apply and above levels (Bloom's revised taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers.

The actual distribution of marks in the question paper may vary slightly from above table.

10. SUGGESTED LIST OF STUDENT ACTIVITIES

Following is the list of proposed student activities such as:

i. Students may be asked to collect photographs using internet which is relevant to field application of various topics and have to prepare learning materials using it.
ii. Teachers guided self learning activities, Course/library/internet/lab based mini projects, industrial visit etc.
iii. Students activities like: course/ topic based seminars, Internet based assignments.

iv. Students should deliver a seminar in groups on materials used in various Digital Techniques and advances/latest trends in Digital Techniques.

11. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES (if any)

i. Take small instrumentation components to the class when teaching
ii. Give simple numerical to students on Boolean Algebra
iii. Internet based home assignments
iv. Mini project

12. SUGGESTED MICRO-PROJECTS

Only one micro-project is planned to be undertaken by a student that needs to be assigned to him/her at the beginning of the semester. In the first four semesters, the micro-project are group-based. However, in the fifth and sixth semesters, it should be preferably be individually undertaken to build up the skill and confidence in every student to become problem solver so that he/she contributes to the projects of the industry. In special situations where groups have to be formed for micro-projects, the number of students in the group should not exceed three.

The micro-project could be industry application based, internet-based, workshop- based, laboratory-based or field-based. Each micro-project should encompass two or more COs which are in fact an integration of PrOs, UOs and ADOs. Each student will have to maintain a dated work diary consisting of individual contributions in the project work and give a seminar presentation of it before submission. The total duration of the micro-project should not be less than 16 (sixteen) student engagement hours during the course. The student ought to submit a micro-project by the end of the semester to develop the industry oriented COs.

A suggestive list of micro-projects is given here. This has to match the competency and the COs. Similar micro-projects could be added by the concerned course teacher:

a. Build a IC tester.
b. Analog to Digital Converter.
c. Digital to Analog converter.
d. Light Detector.
e. Laboratory Kits for digital technique.

13. SUGGESTED LEARNING RESOURCES

Sr. No.	Title of Books	Author	Publication
1	Digital circuit	Kumar, Ananad	PHI Learning, New Delhi , Latest edition
2	Digital Electronics	Subrata Ghoshal	Cengage Learning
3	Digital Electronics	Kharate, G.K.	Oxford University Press, Latest edition
4	Principles of digital electronics	Malvino and Leach	TMH, New Delhi , Latest edition
5	Digital Design	Mano ,M. Morris	Pearson, New Delhi , Latest edition

6	Digital electronics :Principles, devices and applications	Maini ,A .K.	John Willy and Sons, Latest edition
7	Digital Techniques	Godse ,A.P.	Technical publications, Latest edition

14. List of Software/Learning Websites

i. www.nptel.com
ii. http://en.wikipedia.org/wiki/Digital_electronics
iii. http://my.safaribooksonline.com/book/electrical-engineering/computer-engineering/9780750645829/chapter-10dot-instrumentation-and-interfacing/
iv. http://www.hss.energy.gov/deprep/ftcp/directives /QSR-InstrumentationControl.pdf

15. PO-COMPETENCY-CO MAPPING

Semester I	**Digital Techniques(Course Code: 4331701)**						
	POs						
Competency & Course Outcomes	**PO 1 Basic & Discipline specific knowledge**	**PO 2 Problem Analysis**	**PO 3 Design/ develop-ment of solutions**	**PO 4 Engineering Tools, Experimen-tation & Testing**	**PO 5 Engineering practices for society, sustainability & environment**	**PO 6 Project Manage-ment**	**PO 7 Life-long learning**
Competency	**"Implement various sequential and combinational logic circuits using Logic gates"**						
CO1: Convert the given number from one number system to another number system	2						3
CO2: Realize Boolean expressions using logic gates.	2					1	3
CO3: Simplify Boolean expression using Boolean algebra & Karnaugh map	2	2	1	2		1	3
CO4: Implement various combinational logic circuits	2	2	1	2	1		3
CO:5 Implement various sequential logic circuits	2	1	1	1			2

Legend: '**3'** for high, '**2**' for medium, **'1'** for low or **'-'** for the relevant correlation of each competency, CO, with PO/ PSO

16. COURSE CURRICULUM DEVELOPMENT COMMITTEE

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