

Recent progresses of NMOS and CMOS logic functions based on two-dimensional semiconductors

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ABSTRACT

Metal-oxide-semiconductor field effect transistors (MOSFET) based on two-dimensional (2D) semiconductors have attracted extensive attention owing to their excellent transport properties, atomically thin geometry, and tunable bandgaps. Besides improving the transistor performance of individual device, lots of efforts have been devoted to achieving 2D logic functions or integrated circuit towards practical application. In this review, we discussed the recent progresses of 2D-based logic circuit. We will first start with the different methods for realization of n-type metal-oxide-semiconductor (NMOS)-only (or p-type metal-oxide-semiconductor (PMOS)-only) logic circuit. Next, various device polarity control and complementary-metal-oxide-semiconductor (CMOS) approaches are summarized, including utilizing different 2D semiconductors with intrinsic complementary doping, charge transfer doping, contact engineering, and electrostatics doping. We will discuss the merits and drawbacks of each approach, and lastly conclude with a short perspective on the challenges and future developments of 2D logic circuit.

KEYWORDS

field effect transistors, two-dimensional semiconductors, logic circuit, complementary-metal-oxide-semiconductor (CMOS), polarity control

1 Introduction

With intrinsic layered structure, two-dimensional (2D) semiconductors have emerged as promising channel materials for field effect transistors (FET) [1–6]. Within atomic thin body thickness below 1 nm, 2D transistors represent the ultimate body thickness scaling limit to minimize the short-channel-effect, power consumption and heat generation, which are essential for further extending Moore's Law. With nearly a decade of intensive study, the performance figure-of-merits of 2D transistors has been aggressively pushed and is approaching that of state-of-the-art silicon devices. For example, high performance MoS₂ transistors have been demonstrated with on-off ratio over 10⁸ [1], contact resistance below 0.2 kΩ·μm [7], on-state current of 0.83 mA/μm [8], gate electrode length ~ 1 nm [9], and intrinsic power gain and cut-off frequency up to 50 and 42 GHz [10], respectively. Similarly, highest current densities of 0.9 and 1.2 mA/μm have been demonstrated for WSe₂ and black phosphorus (BP) transistors [11, 12], respectively, which are comparable or higher than the low-power (LP) target of silicon counterparts [13]. More importantly, with atomic flat and dangling-bond-free surface, the carrier mobility of 2D transistors varies little with body thickness [4, 5, 14], in great contrast to the exponentially reduced Si mobility with decreasing body thickness [15] and is of great importance for further extending Moore's law to sub-5 nm or 3 nm technology nodes.

With desired electrical properties, various efforts have been devoted to constructing logic circuit based on 2D metal oxide semiconductor field effect transistor (MOSFET). Early attempts

utilized n-type metal-oxide-semiconductor (NMOS)-only or p-type metal-oxide-semiconductor (PMOS)-only technology, where 2D transistors are used as the switching devices and the resistive loads at the same time. This technology feathers simple fabrication processes since it only involves one type of the devices (either PMOS or NMOS), and various logic functions based on this approach have been demonstrated, such as NAND, NOR, XOR. Particularly, with recent advances in large-scale or wafer-scale synthesis of 2D monolayer or thin film [16, 17], more complex logic functions such static random-access memory (SRAM), resistance random-access memory (RRAM), multi-stage ring oscillator and fully functional microprocessor have been demonstrated [18–20].

On the other hand, complementary-metal-oxide-semiconductor (CMOS) technique is the backbone for state-of-the-art integrated circuit, composing of p-type transistor and n-type transistor pairs at the same time. Since one transistor of the pairs is always at off-state, the CMOS device does not have obvious static current flow, demonstrating low power consumption and thus high integration density. This is in great contrast to the transistor-transistor logic (TTL) or NMOS-only technology, which normally has a pull-down resistor and standing current flow even without changing states. Although CMOS technology has demonstrated advantages in terms of heat generation and has dominated silicon industry for decades, the successfully transferring this technique to 2D transistors remains a key challenge. In silicon microelectronics, the complementary logic functions are typically achieved through high-energy ion-implantation followed by high temperature dopant activation

to achieve complementary wells within a single Si wafer. Similar strategies are used in III-V semiconductor technologies. However, applying state-of-the-art processes for creating 2D CMOS is not straightforward because their atomically thin and delicate lattice structure, which is not compatible with the aggressive implantation process. For example, implantation of Ar^+ ions has been demonstrated to degrade the monolayer MoS_2 performance [21] with suppressed photoluminescence (PL) intensity or even being totally etched away, and similar behavior is also observed for other 2D semiconductors [22, 23] such as MoSe_2 , WSe_2 or using other ions (e.g., He^+). Using small electrons (compared to ions) for implantation/radiation may help alleviate this problem [24], but sever defects, damages or phase transformation are still observed [25–27], especially for 2D monolayers. Moreover, the following dopant activation also requires high temperature through rapid thermal annealing (RTA) processes, which is incompatible with various 2D semiconductors.

To overcome this processing incompatibility and to realize high performance 2D complementary logic devices, various efforts have been devoted to developing more mild doping techniques and complementary devices recent years, without damaging the delicate 2D lattice. In this review article, we focus on the recent research progresses for realization of logic functions of 2D transistors. We will first start with the various reported approaches for NMOS-only or PMOS-only integrated circuit. Next, different approaches to control the device polarity and to create complementary MOSFETs are summarized, including utilizing different 2D semiconductors with intrinsic complementary doping, charge transfer doping (e.g., molecular absorption, oxide deposition), contact engineering (e.g., different metal work function, different metallization techniques), electrostatics doping (e.g., statistic electrical field, ferroelectric dielectric). We will discuss the merits and drawbacks of each approaches, and finally conclude with a short perspective on the challenges and future developments of 2D CMOS functions. Overall, we aim to summarize current approaches of 2D

semiconductors for realizing logic functions and integrated circuit, and similar methods could also benefit other emerging semiconductors such as organic semiconductor, hybrid perovskite, and van der Waals (vdW) heterostructures.

2 Logic inverter and integrated circuit based on NMOS-only technology

2.1 NMOS logic inverter

The inverter is fundamental building blocks for integrated circuit design. An inverter can be simply realized through NMOS-only technology by connecting one n-type transistor with a pull-up load, where load can be either a resistor (resistor-load) or another NMOS transistor (NMOS-load by connecting gate and source), as shown in Figs. 1(a) and 1(b). With applying gate voltage, the resistance of the transistor can be switched to a higher (or lower) value compared to the load, leading to the change of divided output voltage. The main advantage of NMOS-load is the smaller occupied space, easier and compatible fabrication process as well as better device performance, and hence it is widely used in 2D NMOS studies. Similarly, PMOS inverter can also be realized using two p-type transistors with one acting as the switching transistor, and the other utilizing as the pull-down PMOS-load.

Based on this only NMOS technique, inverter functions have been realized in various 2D transistors. For example, by simply connecting two top-gated MoS_2 transistors fabricated on an exfoliated monolayer (Fig. 1(c)), logic inverter is realized [28] with a voltage gain of higher than 4. One of the transistors is used as the pull-up NMOS load by connecting the gate and output, and the other functions as a typical n-type transistor for the switching of output voltage, as shown in Fig. 1(d). Moreover, the connecting of output and gate electrode is not always necessary to realize MOS-load, where an inverter function can also be achieved using two identical ambipolar transistors

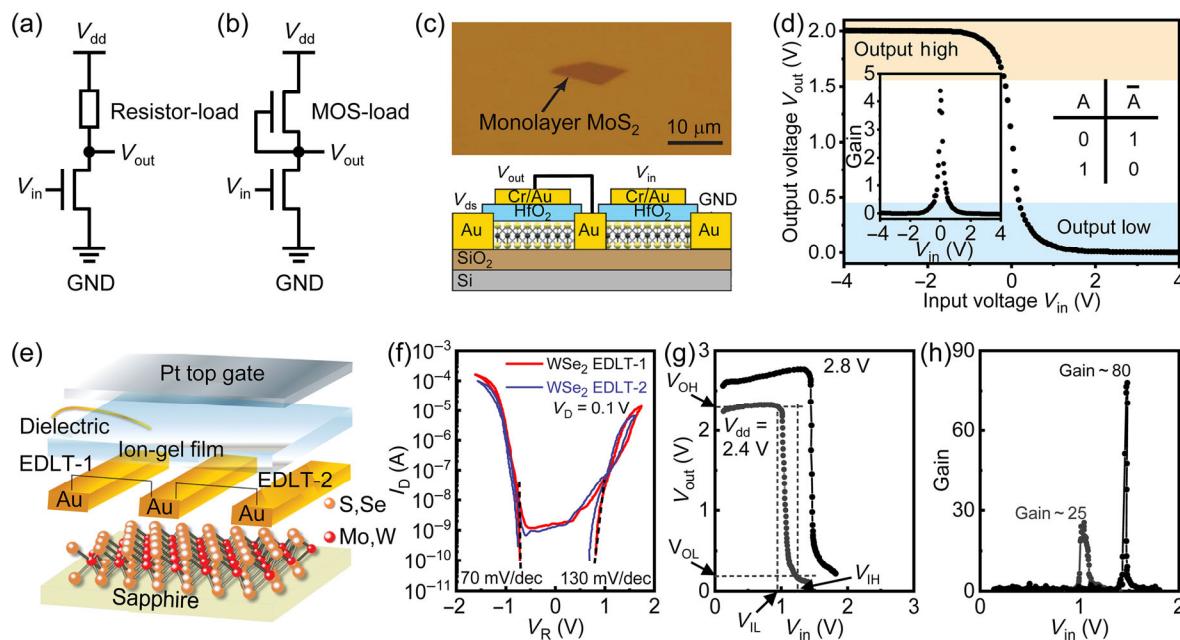


Figure 1 (a) and (b) Circuit diagrams of a resistor-load inverter and NMOS-load inverter. (c) Mechanically exfoliated monolayer MoS_2 flake (upper) and the schematic illustration of monolayer MoS_2 NMOS inverter (bottom). (d) The voltage transfer characteristics (VTC) of monolayer MoS_2 logic inverter with corresponding voltage gain and the truth table (inset). (e) The structure of ambipolar electric double layer transistors (EDLTs) with ion-gel thin-film coupling based on CVD growth of monolayer TMDC onto a sapphire substrate. (f) I_{ds} - V_{gs} transfer characteristics of two different ambipolar WSe_2 EDLTs, demonstrating similar electrical properties. (g) and (h) VTC of monolayer WSe_2 logic inverter with different applied bias voltages (g) and corresponding high voltage gain (h). (e)–(h) are reproduced with permission from Ref. [29], © Wiley-VCH Verlag GmbH & Co. KGaA 2016.

based on transition metal dichalcogenide semiconductors (TMDCs) [29]. As shown in Fig. 1(e), two ambipolar WSe₂ transistors (with similar drain current–gate voltage curves: I_{ds} – V_{gs} transfer characteristic, Fig. 1(f)) are connected in series and ion-gel film is used as gate dielectric. As displayed in the input and output relationship in Fig. 1(g), when input voltage (V_{in}) is low and less than supply voltage (V_{dd}), the top transistor is at on-state, leading to a high output voltage (V_{out}) close to V_{dd} , and similarly, when input voltage is high, the bottom transistor is at on-state ($V_{in} > 0$), resulting in a large voltage gain of 80 (Fig. 1(h)). However, one drawback of this technology is the relatively high off-state voltage and small noise margin.

Furthermore, benefited from the recent advancement in large scale synthesis of monolayer 2D semiconductors using chemical vapor deposition (CVD) or molecular beam epitaxial (MBE) approaches [17, 30, 31], scalable 2D inverters based on NMOS-only technology have been demonstrated. For example, inverter based on CVD grown MoS₂ triangle has been reported [32] using HfO₂ as the gate dielectric and Ti/Au as the contact metals (Fig. 2(a)), yielding a voltage gain close to 20 (at bias voltage of 5 V, Fig. 2(b)). However, one typical challenge for the monolayer transistor is the poor metal–semiconductor contact, where the delicate monolayer lattice could be easily damaged during the aggressive fabrication process such as the solution-based lithography process or high-energy metal deposition/sputtering process [33, 34]. To improve the metal–2D interface and to reduce the contact resistances, 2-inch wafer-scale monolayer MoS₂ film has been synthesized [30] with localized multi-layer MoS₂ islands as contact region (Fig. 2(c)), minimizing the fabrication induced damage and mimicking the structure of ultra-thin body (UTB) silicon transistor with

a raised S/D poly-silicon contact [35]. In the meantime, the multilayer MoS₂ within contact regions typically has smaller bandgap compared to monolayer counterparts, hence could result in smaller contact barrier and contact resistance. Together, these devices demonstrate high carrier mobility of $70 \text{ cm}^2/(\text{V}\cdot\text{s})$, low subthreshold swing of $\sim 150 \text{ mV/dec}$, as well as an inverter gain of 23 (at the bias voltage of 3 V, Fig. 2(d)) [36]. Alternatively, the metal–2D interface can be optimized using graphene as a vdW contact to 2D semiconductors [37–39]. As shown in Fig. 2(e), large scale CVD MoS₂ is used as the transistor channel and pre-patterned graphene (CVD grown) is transferred on top, serving as contact electrodes, gate electrodes as well as circuit interconnects at the same time [40]. The atomically clean and sharp interface between graphene and MoS₂ reduces the Fermi level pinning effect in conventional metal–2D interfaces, and at the same time, the tunable graphene work function (through gate field) enables perfect band alignment between graphene work function and the conduction band of MoS₂, leading to the demonstration of high performance NMOS inverter arrays (Fig. 2(f)). Similarly, CVD grown graphene is utilized as the contact for large scale p-type ReSe₂, as shown in Figs. 2(g) and 2(h). Within this report [41], ion gate is applied as gate dielectric with larger gate capacitance ($5\text{--}8 \mu\text{F}\cdot\text{cm}^{-2}$, corresponding to an equivalent oxide thickness $< 1 \text{ nm}$), therefore, the device can work under low gate voltage $< 2 \text{ V}$, leading to the realization of low power PMOS-only logic inverters.

2.2 One-step growth of NMOS logic inverter

Besides synthesizing the 2D semiconductor channel, logic inverter can also be realized through one-step CVD growth of

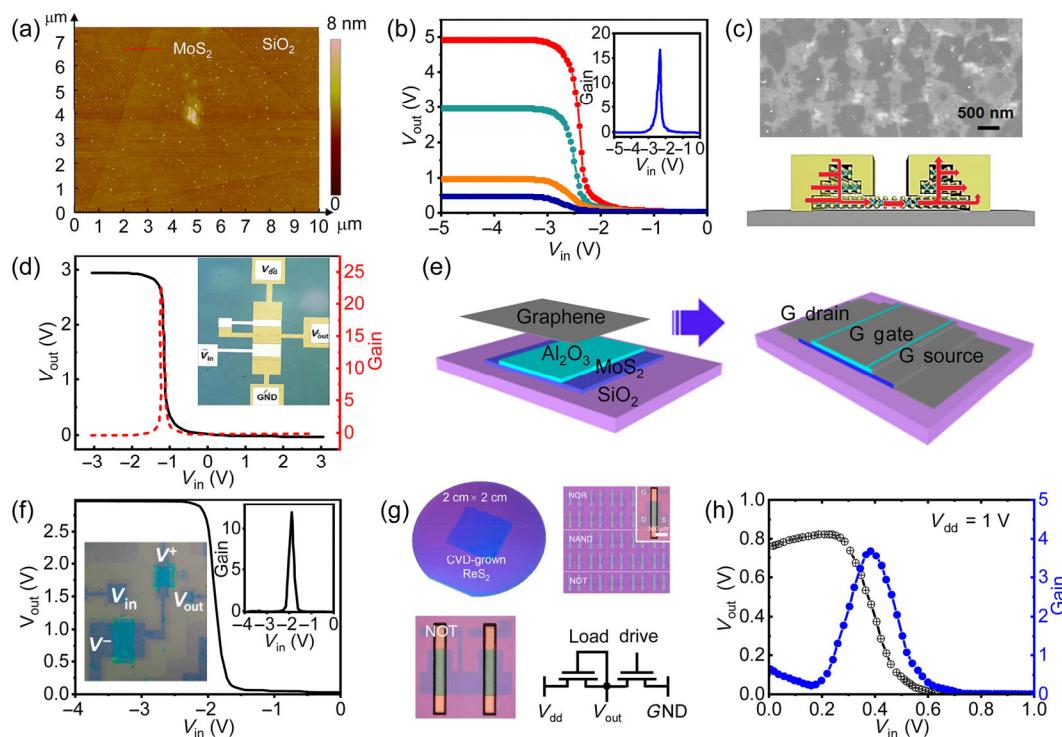


Figure 2 (a) Atomic force microscopy (AFM) image of CVD-grown monolayer MoS₂ flake. (b) VTC and voltage gain under applied voltages of the resulting monolayer MoS₂ NMOS logic inverter. (a) and (b) are reproduced with permission from Ref. [32], © IEEE 2012. (c) Scanning electron microscopy (SEM) image of CVD grown multilayer MoS₂ film (upper) and corresponding device schematic using multilayer region as the contact to improve the metal–semiconductor junction. (d) VTC and voltage gain of the MoS₂ logic inverter and the corresponding optical image. (c) and (d) are reproduced with permission from Ref. [36], © Wiley-VCH Verlag GmbH & Co. KGaA 2018. (e) CVD growth of large-scale MoS₂ transistors using semi-metal graphene as the contacts, gate electrodes as well as the interconnects. (f) VTC and voltage gain of the graphene contacted MoS₂ logic inverter and corresponding optical image. (e) and (f) are reproduced with permission from Ref. [40], © American Chemical Society 2014. (g) Photos and images of CVD grown large-area ReS₂, as well as the fabricated logic circuits after patterning process. (h) VTC and voltage gain of monolayer ReS₂ logic inverter using PMOS-only technology. (g) and (h) are reproduced with permission from Ref. [41], © American Chemical Society 2017.

the channel and the contact metal at the same time. For example, chemical growth of lateral graphene/MoS₂/graphene heterostructures has been reported [42, 43] with MoS₂ used as the channel and graphene used as the contact metal, as shown in Fig. 3(a). This one-step growth and construction strategy can significantly reduce contact barriers compared with traditional approaches based on contact metal deposition. Moreover, different from previous reports that rely on vdW assembling (transfer graphene as the contact) with limit transfer resolution, the metal and channel can be precisely aligned without any potential polymer contaminations, leading to one-step realization of scalable logic inverter, as shown Fig. 3(b). With a lower contact resistance, higher voltage gain of 70 at V_{dd} of 4 V can be achieved, compared with other methods using NMOS-only technology. This one-step growth (of channel and contact) strategy is not only limited to MoS₂ and graphene, but could be well extended to other combinations between different 2D semiconductors and 2D metals [11, 44], such as CVD growth of metallic VSe₂ or NiTe₂ on top of semiconducting WSe₂. Importantly, the one-step “stitching” growth method has also been realized between insulating BN and semiconducting MoS₂ (Fig. 3(c)) [43], paving the road of device isolation for large scale integration. Furthermore, the channel and contact materials within inverter arrays are also realized using a single 2D material, but different phases [45, 46]. As shown in Fig. 3(d), MoTe₂ is used as the active material as it can provide both semiconducting phase (2H) and metallic phase (1T'). By tellurizing the pre-deposited different precursor (MoO_{2.0-2.5} for 2H and MoO₃ for 1T') at high temperature of ~ 650 °C, channels, contacts and interconnects could be simultaneously produced and connected into well-organized logic inverters, where all these components are connected through covalent bonds instead of vdW interfaces [46], as shown in Figs. 3(e) and 3(f). Furthermore, benefited from the atomically thin channel and flexible integration strategy, monolithic three-dimensional (3D) integration has been demonstrated, where multiple MoTe₂ arrays are stacked on the same wafer, separated by HfO₂ insulating layers and partially connected through etched via holes. As shown in Figs. 3(g) and 3(h), the obtained FETs in the two different tiers

showed p-type device characteristic with similar on/off ratios (~ 10⁵) and mobility (~ 30 cm²/(V·s)), suggesting that synthesis of the top layers does not impact the performance of the bottom layers, which is essential for integrating more device layers for 3D integration.

2.3 Complex NMOS logic functions and integrated circuit

Beyond inverter, more complex logic functions have been realized through NMOS-only technology, and are largely based on MoS₂ channel owing to its high stability (compared to other 2D semiconductors). Early study focused on using a mechanical exfoliated bilayer MoS₂ as the channel material [47]. Top gate electrodes with different work functions (Al or Pd) are used to effectively shift the threshold voltages (Fig. 4(a)), where high work function Pd gate electrode ($W_M \sim 5.2\text{--}5.6$ eV) p-dopes the channel and low work function Al gate electrode ($W_M \sim 4.1$ eV) n-dopes the channel, resulting in enhancement-mode and depletion-mode transistors, respectively. The realization of enhancement-mode MoS₂ transistor here is essential for the realization of multistage cascaded circuits, leading to demonstration of a NAND gate, a SRAM cell, and a five-stage ring oscillator, as shown in Fig. 4(b). Furthermore, scalable logic circuits are realized using gate-first technology for CVD monolayer MoS₂ with the assistance of custom computer-aided design (CAD) flow [20]. Using gate-first technique, all the critical components are fabricated before the MoS₂ transfer step and the high-energy atomic layer deposition (ALD) process (of top gate dielectric) is avoided, leading to high device uniformity with 100% yield (of over 200 transistors). In the meantime, the use of CAD tool enables the modeling of device parameter and fast designs the layout process, which is important in complex circuit design. Together, high-performance enhancement-mode MoS₂ FETs are demonstrated with various logic functions, including AND, OR, NAND, NOR, XNOR, latch and edge-trigger register, as shown in the design layout and measurement results in Fig. 4(c). Besides CVD grown monolayers, recent reports also demonstrated high performance solution-processable MoS₂ transistors with mobility > 10 cm²/(V·s),

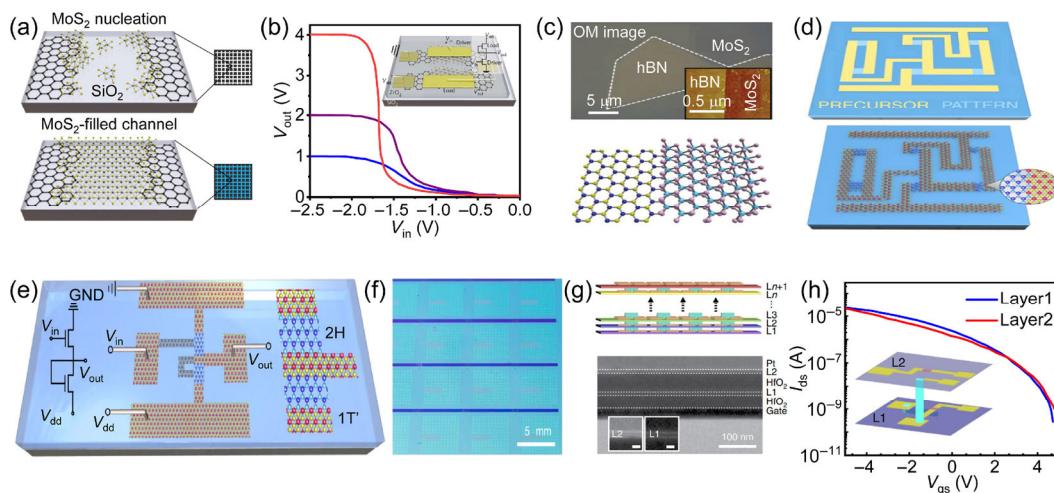


Figure 3 (a) Schematic diagram of the direct CVD growth of MoS₂-graphene heterostructures. (b) VTC of MoS₂-graphene logic inverter with schematic illustration of an inverter circuit and circuit diagram (inset). (a) and (b) are reproduced with permission from Ref. [42], © Macmillan Publishers Limited, part of Springer Nature 2016. (c) Optical image, AFM image and schematic illustration of the parallel stitched MoS₂-hBN heterostructures (reproduced with permission from Ref. [43], © Wiley-VCH Verlag GmbH & Co. KGaA 2016). (d) Scalable MoTe₂ channels, contacts and interconnects can be synthesized through one-step tellurizing process of pre-deposited precursors, leading to ultrathin MoTe₂ based circuit. (e) and (f) Schematic view of a chemically synthesized inverter and optical image of ~ 1,500 synthesized devices on a small scale. (g) Schematic illustration of vertical integration of multilayer MoTe₂ circuit layers and the cross-sectional transmission electron microscope (TEM) image. (h) P-type I_{ds} - V_{gs} transfer characteristics are observed on two neighboring devices within different layers, suggesting the synthesis of the top layers does not impact the performance of the bottom layers. (d)-(h) are reproduced with permission from Ref. [46], © Zhang, Q. et al., under exclusive licence to Springer Nature Limited 2019.

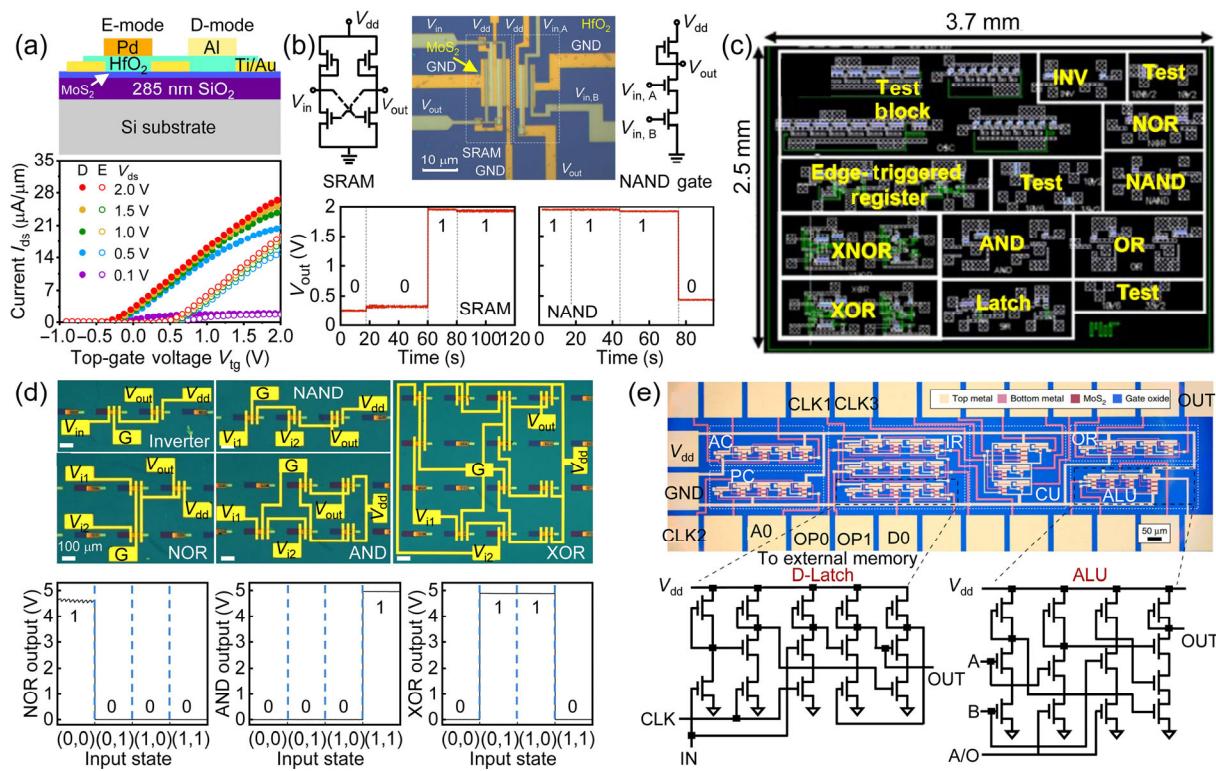


Figure 4 (a) Schematic illustration of the MoS₂ device under enhancement (E)-mode and a depletion (D)-mode using different top gate electrodes, as well as the corresponding I_{ds} - V_{tg} transfer characteristics of MoS₂ FETs. (b) NAND logic and the SRAM circuit diagram, optical image and the input–output relationship. (a) and (b) are reproduced with permission from Ref. [47], © American Chemical Society 2012. (c) Layout of the test chip using the CVD grown MoS₂ circuits (reproduced with permission from Ref. [20], © American Chemical Society 2016). (d) Optical images of inverter, NAND, NOR, AND, and XOR logic functions fabricated from solution-processed MoS₂ transistors, as well as the logic input–output relationship (reproduced with permission from Ref. [16], © Springer Nature Limited 2018). (e) Optical image of 1-bit MoS₂ microprocessor with circuit schematics of D-Latch and ALU (reproduced with permission from Ref. [18], © Wachter, S. et al. 2017).

which is comparable higher than conventional organic transistor used for thin film transistor (TFT) application [16]. In addition, the solution-based MoS₂ film offers an appealing path to fabricate 2D transistors on flexible substrates using low-temperature processes (e.g., spin coating, screen printing or inkjet printing) with low processing cost and large film size. With high stability, logic NAND, NOR, AND and XOR have been demonstrated using gate-first technique by integrating 3, 3, 5 and 11 MoS₂ transistors, respectively, and demonstrating the desired logic function (Fig. 4(d)). Furthermore, the successful realization of different logic functions enables the demonstration of more complex half-adder, corresponding to the addition of two one-bit binary numbers.

Take a step further, 1-bit microprocessor based NMOS MoS₂ technology is recently demonstrated [18], representing the most complex logic circuit from 2D transistor. The processor composes 115 MoS₂ transistors with all basic building blocks of a typical microprocessor, including D-Latch, arithmetic logic unit (ALU), accumulator (AC), instruction register (IR), control unit (CU), program counter (PC), and output register (OR), as shown in Fig. 4(e). The processor demonstrates correct logic result with a series of input operations, confirming the ability of cascade logic functionals based on 2D transistor. Furthermore, benefited from the uniform CVD synthesized MoS₂ used, 80% of the fabricated ALU is functional, which is a decent yield considering the high circuit complexity, suggesting the potential for fully functional multi-bit microprocessors based on 2D NMOS technology.

3 CMOS logic inverter and integrated circuit

Compared to NMOS logic functions, CMOS technology based

on 2D semiconductors becomes another promising approach for logic circuits owing to its low power consumption and high tolerance to external noise. A CMOS inverter can be achieved by connecting a PMOS and an NMOS transistors in series. When the low input voltage is applied, PMOS is turned on while NMOS is turned off, resulting in high output voltage close to V_{dd} . On the other hand, with high input voltage, NMOS is turned on and PMOS is turned off, leading to low output voltage close 0 V. As stated above, the key challenge for 2D CMOS technology is the polarity control of 2D semiconductors, which is not an easy task for such atomic thin lattice. To this end, various approaches have been demonstrated for creating complementary MOSFETs, including using different 2D channel materials, substitutional doping, charge transfer doping, contact engineering, as well as electrostatic doping.

3.1 Different 2D channel materials

A simple strategy to create CMOS function is utilizing different 2D materials as the channel, where one material is used for NMOS and a different material is used for PMOS. As shown in Fig. 5(a), a MoS₂ flake (~ 6 nm thick) and a WSe₂ flake are exfoliated on top of typical Si/SiO₂ substrate separately, and then contacted with different work function metals (Ti for MoS₂ and Pt for WSe₂) to achieve NMOS and PMOS [48], respectively. By connecting the two transistors in series, an inverter is demonstrated with desired logic behavior, as shown in Fig. 5(b). Beyond MoS₂ and WSe₂, this simple strategy has been demonstrated for other combinations between different p-type (such as BP, MoTe₂, WSe₂, MoSe₂) and n-type (such as MoS₂, ReS₂, WS₂) 2D semiconductors [49–53].

Alternatively, different 2D semiconductors (in-plane heterostructure) can be epitaxially grown using CVD method [54–58],

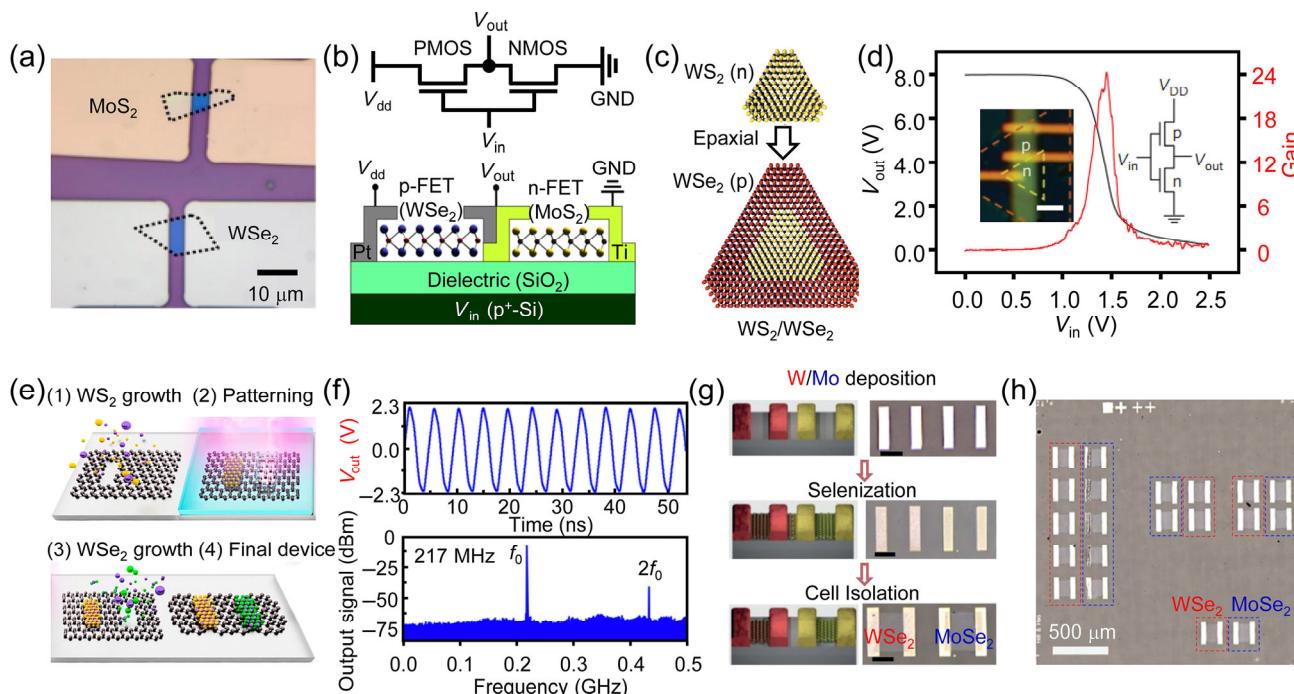


Figure 5 (a) Optical image of two different 2D transistors obtained by mechanical exfoliation method, where WSe₂ is used as PMOS and MoS₂ as NMOS. (b) CMOS inverter diagram and cross-section schematic by connecting these two transistors in series. (a) and (b) are reproduced with permission from Ref. [48], © American Chemical Society 2015. (c) Schematic of lateral CVD epitaxial growth of WS₂-WSe₂ heterostructures. (d) VTC and voltage gain of CMOS inverter based on CVD grown WS₂-WSe₂ heterostructures (WSe₂ used as PMOS and WS₂ used NMOS) and the corresponding inverter optical image. (c) and (d) are reproduced with permission from Ref. [55], © Macmillan Publishers Limited 2014. (e) In-plane epitaxial CVD growth of graphene-WS₂-graphene-WSe₂-graphene heterostructures, where graphene could be used as the contact for different 2D channels. (f) Circuits made from the CVD growth heterostructures, including five-stage ring oscillator with oscillation frequency at 217 MHz. (e) and (f) are reproduced with permission from Ref. [59], © American Chemical Society 2020. (g) Schematics and optical images of fabrication process for location-selective CVD growth with different pre-deposited metal pads. (h) A representative optical image of WSe₂ and MoSe₂ using location-selective growth. (g) and (h) are reproduced with permission from Ref. [60], © Wiley-VCH Verlag GmbH & Co. KGaA 2019.

representing a more scalable approach to assemble different 2D materials on a given substrate. For example, WS₂/WSe₂ heterojunction is achieved through *in-situ* modulation of the vapor-phase reactants during the CVD process, as shown in Fig. 5(c). The I_{ds} - V_{gs} transfer characteristics of each regions demonstrate expected n-type and p-type device characteristic with an electron and hole mobility of 16 and 82 cm²/(V·s), respectively, suggesting its potential for logic applications. As shown in Fig. 5(d), through a patterning process of the WS₂/WSe₂ heterostructures and following top-gate ALD process, logic inverter (based on PMOS and NMOS in series) is demonstrated with voltage gain of 24, at bias voltage of 8 V [55]. Notably, recent literatures [56, 57] have reported controllable approaches to CVD synthesizing complex multi-heterostructures or superlattice (such as alternating WS₂/WSe₂/WS₂/WSe₂/WS₂) using reverse flow CVD approaches, paving the road for more scalable and complex logic circuit using different 2D materials. Furthermore, the in-plane epitaxial growth of different 2D semiconductors can be applied on metallic graphene, where patterned graphene serves as a guiding template for site-selective growth of graphene/WS₂/graphene (NMOS) and graphene/WSe₂/graphene (PMOS) heterostructures, resulting in the growth of 2D contact and semiconductors at the same time (Fig. 5(e)). Based on this technique, CMOS logic inverter, NAND, SRAM, and five-stage CMOS ring oscillator are demonstrated with the highest oscillation frequency of ~0.2 GHz and propagation delay of 0.46 ns (Fig. 5(f)) [59]. Besides high scalability, the CVD approaches used here (compared to previous exfoliation approaches) show obvious advantages of uniform channel thickness down to the monolayer, which is essential for low power CMOS application and further channel length scaling.

Towards practical application, the precisely control of the 2D flake location is of great importance for circuit fabrication. Previous approach to integrate different 2D materials is largely based on random mechanical exfoliation process or random nucleation process during CVD growth. Recently, a bottom-up metal-guided selective growth method is reported [60], allowing the precise deposition of specific 2D channels onto desired locations that are controlled by the pre-patterned metal pads. For example, transition metal (Mo and W) pads are first pre-fabricated through conventional photolithographically and metal deposition process, as shown in Fig. 5(g). After selenization process, the grown MoSe₂ and WSe₂ are found to confine along W and Mo metal pads (Figs. 5(g) and 5(h)) [60], leading to the growth of different 2D materials at the same time, with high location controllability. With further isolation process, the grown WSe₂ and MoSe₂ transistors are measured to p-type and n-type, respectively, resulting in well-behaved inverter with high scalability and location-controllability.

Besides connecting two planar 2D transistors (NMOS and PMOS) in series, CMOS logic can also be realized by stacking two vertical transistors (with opposite polarity) layer-by-layer in the vertical direction, representing the 3D monolithic CMOS integration. This kind of vertical CMOS does not consume additional planar space besides what is needed for bottom transistor, holding great promise for complex CMOS circuit with small device area and thus high integration density. As shown in Figs. 6(a)–6(e), MoS₂ transistors (NMOS) and WSe₂ transistors (PMOS) are layer-by-layer transferred and fabricated in the vertical direction. They are separated by gate electrodes and ZrO₂ layer, which not only acts as the insulating spacing layer, but also as the high-k dielectric for both transistors. Within this approach, 3D monolithic CMOS

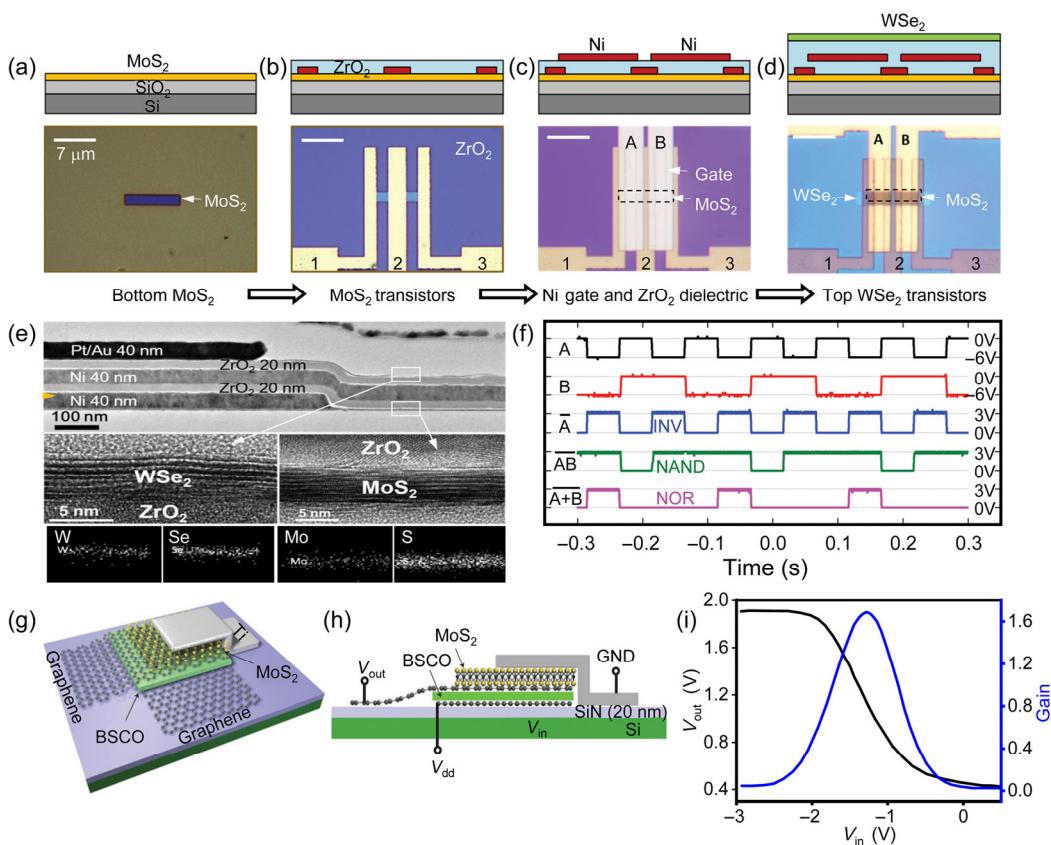


Figure 6 (a)–(d) Fabrication processes of CMOS monolithic integrated of different 2D transistors, which are fabricated layer-by-layer and connected through via holes. (e) TEM image of 3D CMOS structure and enlarged view of MoS₂ and WSe₂ regions. (f) Switching waveforms of INV, 2-input NAND, and NOR fabricated through the monolithic integration. (g)–(f) are reproduced with permission from Ref. [61], © Wiley-VCH Verlag GmbH & Co. KGaA 2016. (g) and (h) Schematic view and cross-sectional illustration of a CMOS inverter by vertically stacking graphene, MoS₂ and BSCO. With weak screen effect of graphene, the bottom gate could modulate the both PMOS and NMOS at the same time. (i) The corresponding VTC and voltage gain of vertical vdW inverter. (g)–(i) are reproduced with permission from Ref. [62], © Macmillan Publishers Limited 2013.

functions are demonstrated with static logic function (Fig. 6(f), INV, NOR, NAND) and analog functions such as amplifier [61]. Compared with previous 3D monolithic CMOS technology using conventional bulk Si, the technique of using layered semiconductors demonstrate obvious advantages with low processing temperature. The active channel materials (MoS₂, WSe₂) can be pre-fabricated and transferred layer-by-layer within temperature $< 200^{\circ}\text{C}$, compatible with various back-end-of-line (BEOL) process. Furthermore, the vertical stacking of different 2D materials can also be realized using graphene as the contact electrode [62–64]. For example, a complementary vertical inverter was created by vertically stacking the layered 2D MoS₂ (n-type), 2D graphene (metallic) and 2D Bi₂Sr₂Co₂O₈ (p-type), as shown in Figs. 6(g) and 6(h) [62]. With single atomic thickness, finite density of states (DOS) and weak screening effect, graphene exhibits a field-tunable work-function and partial electrostatic transparency. Hence, the bottom gate electrical field could penetrate through graphene, modulating both PMOS and NMOS at the same time without additional gate electrode and leading to the demonstration of vertical inverter (Fig. 6(i)).

3.2 Substitution doping and surface charge transfer doping

Selective doping represents an effective route to control the polarity of various 2D semiconductors and to achieve the CMOS functions. As stated above, conventional ion implantation doping approaches are difficult to apply on the ultra-thin 2D semiconductors. To overcome this challenge, gentle doping strategies have been demonstrated for 2D semiconductors, and

can be largely categorized into two approaches: the element substitutional doping (anion or cation) and the surface charge transfer doping (SCTD).

In typical 2D TMDCs, the metal atoms of each layer are sandwiched by outer chalcogenide atoms, as shown in Fig. 7(a) [65], where the ionic elements can be substituted by exterior atoms to n-dope or p-dope 2D semiconductors, depending on the valence electrons of the exterior atoms. The anion atom (non-metal) substitutional doping can be more favorably realized than cation substitutional doping, because the anion in TMDC is exposed to their surface, where the dopants can diffuse or bond through the surface vacancy or defect sites. For example, nitrogen (N) doping can be realized through plasma process, where the WS₂ transistor is exposed to nitrogen radicals such as ionized nitrogen and atomic nitrogen, as shown in Fig. 7(b). The doping concentration can be controlled by the plasma power and the kinetic energy of the ionized nitrogen is designed to keep very low, hence the surface damage of plasma process can be minimized, enabling effective p-type doping of monolayer WS₂ transistors (Figs. 7(c) and 7(d)) [66]. On the other hand, the substitute doping of metal dopants (cation) can be achieved through *in-situ* growth method. Nb element (five electrons) has been used for p-dope TMD materials by replacing Mo or W with six valance electrons [65, 67–69], and similarly, Re with seven valance electrons could be used to n-dope TMD materials [70]. Various substitutional doping approaches have been applied for 2D semiconductors, as summarized in Table 1, and CMOS logic inverter based on this technique has been demonstrated [65].

Alternatively, SCTD has recently attracted considerable

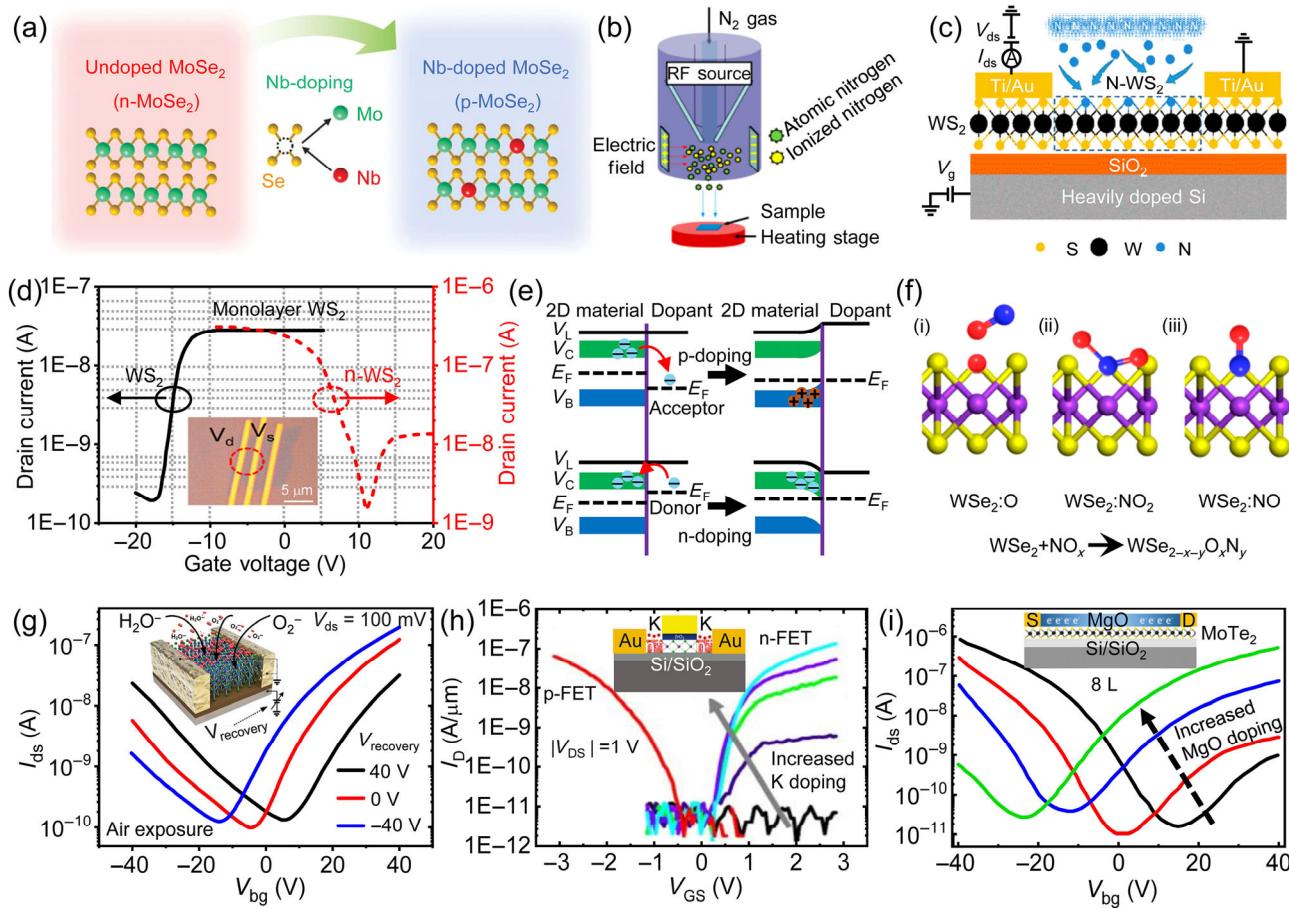


Figure 7 (a) Schematics illustration of cation substitutional doping of 2D semiconductors (reproduced with permission from Ref. [65], © Wiley-VCH Verlag GmbH & Co. KGaA 2015). (b) and (c) Schematic diagram of the anion substitutional doping process to 2D semiconductors using nitrogen plasma treatment. (d) I_d - V_g transfer characteristics of the pristine monolayer WS_2 and nitrogen-doped WS_2 FETs, demonstrating clear p-type doping. (b)–(d) are reproduced with permission from Ref. [66], © American Chemical Society 2018. (e) Schematic band diagram before and after p- and n-type SCTD (reproduced with permission from Ref. [71], © Wiley-VCH Verlag GmbH & Co. KGaA 2016). (f) Schematics illustration of SCTD between gaseous NO_x and defects of Se at the WSe_2 surface, where p-type degenerate doping of WSe_2 FET is realized by NO_x chemisorption surface treatment (reproduced with permission from Ref. [72], © American Chemical Society 2014). (g) The control MoTe_2 transistor behavior using different gate bias voltage ($V_{recovery}$). Inset shows the schematic view of air exposure of MoTe_2 transistor with the absorption of water or oxygen in the p-type doping process (reproduced with permission from Ref. [73], © Wiley-VCH Verlag GmbH & Co. KGaA 2018). (h) SCTD by depositing thin K layers on top of WSe_2 FET, where the n-doping concentration increases with depositing time (reproduced with permission from Ref. [75], © American Chemical Society 2014). (i) Polarity control by integrating thin layer MgO on top of MoTe_2 FET, where the polarity is gradually changed from p-type to n-type with increasing MgO thickness (reproduced with permission from Ref. [79], © Wiley-VCH Verlag GmbH & Co. KGaA 2018).

interests for reliable doping of 2D semiconductors. SCTD approach utilizes surface charge transfer between 2D semiconductors and the dopant materials, which is in great contrast to the substitutional doping method with external dopants to 2D lattice and therefore potential lattice change or damage. Within SCTD approach, built-in potential is typically generated between the 2D and doping layer owing to their energy difference, leading to the band bending and charge transfer in between. For example, a schematic energy diagram for acceptor and donor behavior before and after p- or n-type SCTD process is illustrated in Fig. 7(e) [71]. When the 2D material displays higher Fermi level (E_F) compared to that of the dopant layer, electrons are moved from the semiconductor to the surface dopants until reaching E_F equilibrium, leading to the p-type doping of 2D semiconductor. Similarly, n-type SCTD is realized when the 2D material exhibiting lower E_F than dopants.

Various SCTD approaches of 2D semiconductors have been demonstrated and summarized in Table 1. Depending on the dopant materials, they generally categorized into gaseous doping, metals or metal compounds doping, as well as organic molecules doping. Gas doping is based on the gas adsorption on

the 2D surface, and can be controlled through the processing temperature (with different adsorption energy). For example, the p-type degenerate doping of WSe_2 FET is realized by NO_x chemisorption surface treatment at 150°C , where the doping mechanism can be largely attributed to the formation of $\text{WSe}_{2-x-y}\text{O}_x\text{N}_y$ (such as NO_2 or NO for SCTD and O for substitution, Fig. 7(f)) species between NO_x and defects of Se vacancy at the WSe_2 surface [72]. Furthermore, the gas molecules adsorption can also be modulated by using an additional back gate voltage or electrothermal processes for devices, where the absorbed dopants such as O_2 or H_2O molecules can be desorbed from the MoTe_2 surface adsorbents. For example, MoTe_2 transistor is p-doped with the absorption of water or oxygen, and by an annealing doping process, the polarity of MoTe_2 transistor can be switched from p-type to n-type (Fig. 7(g)) [73]. This precisely controllable doping technique can be applied in same MoTe_2 flake for the demonstration of various CMOS logic functions such as inverter, NAND and NOR, revealing the potential of adsorption doping in microelectronic devices.

On the other hand, metals or metal compounds can be used as the dopants material and integrated on top of 2D semicon-

Table 1 Doping approaches of 2D semiconductors^a

Doping type	Dopant	Type	2D channel	Material method	Ref.
Substitution doping	Nb	p-type	MoS ₂	CVD	[67]
	Nb	p-type	MoS ₂	ME	[68]
	Nb	p-type	MoSe ₂	ME	[65]
	Nb	p-type	WS ₂	CVD	[69]
	P	p-type	MoS ₂	ME	[94]
	W	p-type	MoSe ₂	CVD	[95]
	Mn/Cr	p-/n-type	MoS ₂	CVD	[96]
Anion	Zn	p-type	MoS ₂	CVD	[97]
	Se	n-type	WS ₂	CVD	[98]
	N	p-type	WS ₂	ME	[66]
	Re	n-type	MoS ₂	CVD	[70]
Gas	Se	n-type	SnS ₂	ME	[99]
	NO ₂	p-type	WSe ₂	ME	[72, 100]
	Cl	n-type	WS ₂ /MoS ₂	ME	[101]
	O ₂	p-type	MoTe ₂	ME	[85]
SCTD	O ₂ /H ₂ O	p-type	MoTe ₂	ME	[73]
	K	n-type	WSe ₂	ME	[74, 75]
	K	n-type	BP	ME	[102]
	Cu	n-type	BP	ME	[77]
	Al	n-type	BP	ME	[103–105]
	Al	n-type	MoTe ₂	ME	[76]
	AuCl ₃	p-type	MoS ₂	ME	[81–83]
	ATO	n-type	MoS ₂	ME	[106]
	Al ₂ O ₃	n-type	MoTe ₂	ME	[80]
	Al ₂ O ₃	n-type	MoTe ₂	CVD	[107]
	IGZO	p-type	MoS ₂	ME	[108]
	MgO	n-type	BP	ME	[78]
Organic molecules	MgO	n-type	MoTe ₂	ME	[79]
	MoO ₃	p-type	WSe ₂	ME	[109]
	BV	n-type	MoS ₂	ME	[82, 84]
	BV	n-type	MoTe ₂	ME	[85]
Organic molecules	PDPP3T	n-type	MoS ₂	ME	[52]
	OTS	p-type	WSe ₂	ME	[90]
	MEA/FDT	n-/p-type	MoS ₂	ME	[87]
	OTS/APTES	p-/n-type	WSe ₂ /MoS ₂	ME	[91]
	F ₄ TTCNQ-PMMA	p-type	WSe ₂	ME	[92]
	PPh ₃	n-type	MoS ₂	ME	[93]
	PFS/AHAPS	p-/n-type	WSe ₂	ME	[89]
	MB	p-type	MoS ₂	ME	[110]
	HAT-CN	p-/n-type	MoTe ₂ /MoS ₂	ME	[111]
	NADH	n-type	MoS ₂	ME	[112]
	MMA/PMMA	p-type	PtSe ₂	CVD	[113]
	4-NBD/DETA	p-/n-type	WSe ₂	CVD	[114]

^aME: mechanical exfoliation; PDPP3T: poly(diketopyrrolopyrrole-terthiophene); MEA: mercaptoethylamine; FDT: 1H,1H,2H,2H-perfluorodecanethiol; PMMA: poly(methyl methacrylate); PFS: trichloro(1H,1H,2H,2H-perfluoroctyl)silane; AHAPS: N-[3-(trimethoxysilyl)propyl]ethylenediamine; MB: tris(4-bromophenyl)ammonium methyl hexachloroantimonate; HAT-CN: hexaaazatriphenylenehexacarbonitrile; NADH: nicotinamide adenine dinucleotide; MMA: methyl methacrylate; 4-NBD: 4-nitrobenzenediazonium tetrafluoroborate; DETA: diethylenetriamine.

ductors through vacuum thermal/e-beam deposition. For example, by thermal depositing low work function K on the channel of WSe₂, the original p-type transistor is switched to well-behaved n-type device [74, 75]. More importantly, the doping concentration can be controlled through depositing time and thus film thickness (Fig. 7(h)), leading to the demonstration of high-performance CMOS inverter [75]. Similarly, depositing low work function metal Al and Cu have also been demonstrated to effectively

dope MoTe₂ [76] and BP [77], respectively. Within this technique, low deposition rate and short deposition time (on the scale of second) are normally utilized, to maintain the deposited dopant is functioned as the adatom rather than the continuous metal film to short the channel. In addition to the metal dopants, metal oxide can also be used to dope the 2D host material. For example, it has been demonstrated that evaporated MgO is an insulator material with negative electron affinity, which could

reduce the work function and n-dope the 2D semiconductors [78, 79]. The doping concentration and transistor threshold voltage can be further modulated through the thickness of deposited MgO, as shown in Fig. 7(i). Based on this technique, the CMOS inverter is realized on an 8-layer thick MoTe₂ device, with the voltage gain of 26 [79]. Similarly, the n-type of MoTe₂ is also realized by the deposition of Al₂O₃ through ALD process [80]. On the other hand, metal compounds of p-type dopants have been widely used for modulating the doping polarity. AuCl₃ with higher positive reduction potential, is the most prevalent p-type dopants for 2D layered materials [81–83].

SCTD of organic molecules on 2D materials is generally controlled by the electron withdrawing or donating groups in molecules, and can be achieved through the simple spin-coating process, holding the potential for the low cost and large-scale doping method. For example, the strongly reductive benzyl viologen (BV) is demonstrated to n-dope the MoS₂ [82, 84]. Since each BV molecule could donate 2 electrons to MoS₂, high doping concentration (sheet density of $\sim 1.2 \times 10^{13} \text{ cm}^{-2}$) approaching degeneration is achieved [84]. Similarly, n-dope using BV is also reported for other 2D semiconductors such as MoTe₂, demonstrating lateral MoTe₂ p-n junction with ideality factor of 1.2 [85]. Furthermore, the profuse functional groups in organic materials can tailor the charge transfer with 2D host materials. Among those organic molecule's functional

groups, –SH, –OH, –NH₂, and benzyl as n-type dopants donate electrons to 2D host materials [84, 86–88], and –CF₃ is likely to induce hole-doping because of high electronegativity of the F element [87, 89]. Based on this SCTD approaches, various organic chemical materials have been used to dope 2D semiconductors, including octadecyltrichlorosilane (OTS, n-dope [90]), 3-aminopropyltriethoxysilane (APTES, n-dope [91]), tetrafluoro-tetracyanoquinodimethane (F₄TCNQ, p-dope [92]), and triphenylphosphine (PPh₃, n-dope [93]), are also summarized in Table 1.

3.3 Contact engineering

Metals with different work function could be used to modulate the Schottky barrier height (SBH) at the metal–2D junctions, leading to the control of majority carrier type. For example, Al metal has a low work function of 4.1 eV, closing to the energy of WSe₂ conduction band, and similarly, Au has a high work function ~ 5.1 eV, matching well with the valance band of WSe₂. Hence, by simply depositing Al or Au on to WSe₂, PMOS and NMOS devices are observed for multilayer WSe₂, leading to the demonstration of well-behaved inverter, as shown in Figs. 8(a) and 8(b) [115]. However, due to the high-energy metal deposition process and corresponding damage to the delicate 2D channel, strong Fermi level pinning (FLP) effect and largely Schottky barrier is typically observed

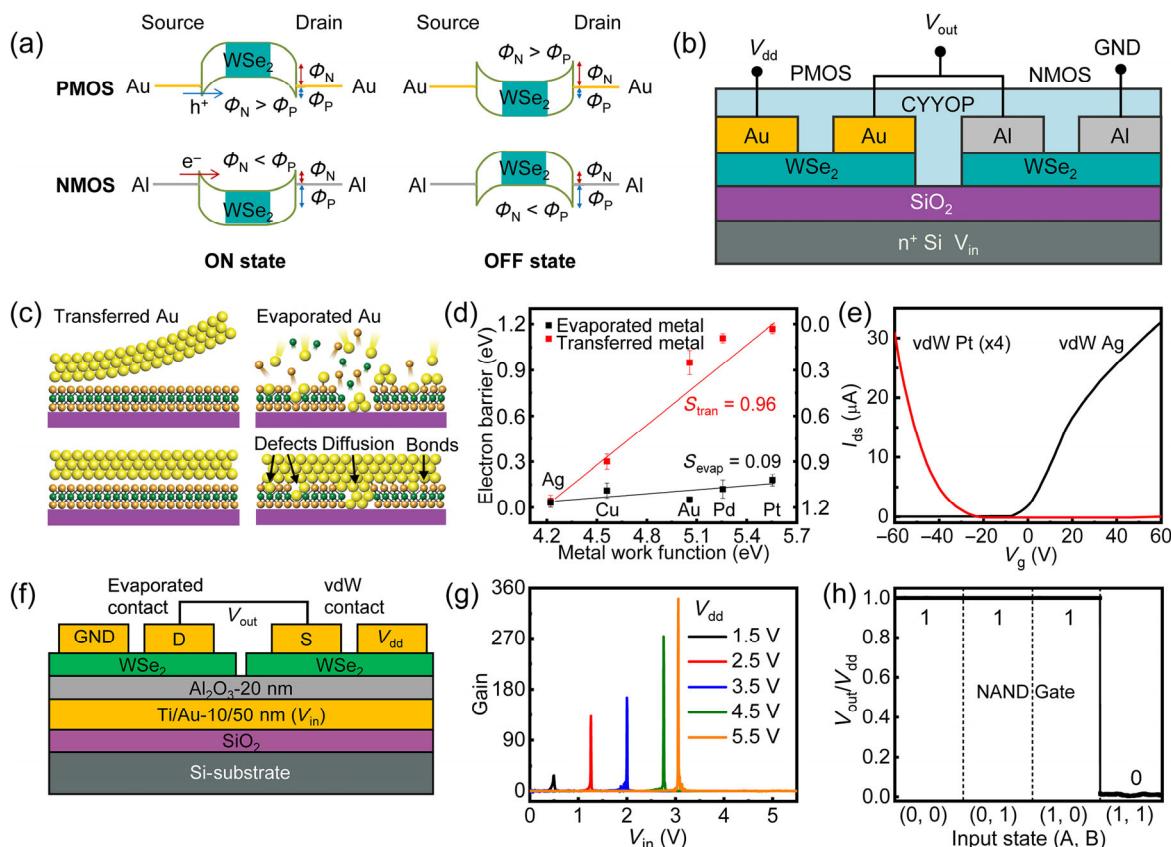


Figure 8 (a) Energy band diagram of WSe₂ p-type and n-type FETs using metal electrodes with different work function. (b) Schematic illustration of the WSe₂ CMOS inverter with Au and Al contact electrodes. Reproduced with permission from Ref. [115], © IOP Publishing, Ltd 2016. (c) Cross-sectional views of the MoS₂ transistors by using vdW Au electrodes and conventional e-beam deposited Au electrodes, where vdW metal–semiconductor interfaces feathers atomically clean and sharp interfaces with minimized surface states. (d) The relationship between SBH and metal work function for MoS₂ transistors using both vdW metals and conventional evaporated metals, where the vdW metal–MoS₂ junction shows highly tunable barrier height approaching Schottky-Mott limit. (e) I_{ds} – V_{gs} transfer characteristics of MoS₂ transistor using vdW Pt and Ag metals, demonstrating the control of device polarity using different metal work functions. (c)–(e) are reproduced with permission from Ref. [33], © Macmillan Publishers Limited 2018. (f) Schematic of WSe₂ inverter fabricated by using same metal Au electrodes with different metallization approaches, where vdW integration method leads to PMOS and evaporation method results in NMOS. (g) The corresponding inverter voltage gains under different bias voltage. (h) The input–output logic functions of NAND and NOR gates fabricated by vdW integration and evaporation Au electrodes on WSe₂, respectively. (f)–(h) are reproduced with permission from Ref. [123], © Kong, L. et al. 2020.

regardless of the metal work function used [116–118]. The strong FLP effect poses two severe limitations for the development of high-performance CMOS inverter based on this approach.

First, the SBH changes little with the metal work function, hence, large Schottky barrier is typical observed regardless of metal work function used, leading to large contact resistances, low driving current and undesired device performance. To alleviate this problem, the use of different metals (to achieve polarity control) is typically assisted with channel chemical doping or contact region doping to reduce the Schottky barrier width and to achieve ohmic contact. For example, with the $\text{F}_4\text{TCNQ-PMMA}$ (p-dopant) on top of WSe_2 channel, high performance CMOS devices are achieved [92] with Ag and Pt metal contacts, respectively. Second, since the SBH only changes a finite value with different metal work functions, this polarity control strategy is largely limited to ambipolar 2D semiconductors [119–121] such as WSe_2 , MoTe_2 , BP, where the Fermi level is located within the bandgap middle. To reduce the Fermi level pinning effect and to achieve highly designable band-alignment for more 2D semiconductors, vdW metal–semiconductor junction has been recently developed [33, 34, 122]. Within this approach, 3D metals (with atomic flat surface as well as different work functions) are pre-fabricated on a sacrifice wafer, and then physically laminated on top of 2D semiconductors (Fig. 8(c)). Because the high energy metal deposition process is only conducted on the sacrifice wafer, the previous fabrication induced damage to delicate 2D lattice is minimized, leading atomically clean and electrically sharp vdW interfaces. Therefore, the measured SBH changes linearly with the metal work function, approaching that defined by Schottky-Mott rule, as shown in Fig. 8(d). Using this method, the polarity of MoS_2 transistors can be simply switched by vdW integrating metals with different work functions, and at the same time, with high device performance. For example, by selecting vdW integrating metals (Ag or Pt) with work function matching MoS_2 conduction or valence band edge,

high two-terminal electron peak mobility ($260 \text{ cm}^2/(\text{V}\cdot\text{s})$) and hole peak mobility ($175 \text{ cm}^2/(\text{V}\cdot\text{s})$) are demonstrated at room temperature (Fig. 8(e)) [29], respectively. This technique provides a doping-free method to control the polarity of MoS_2 , which is normally believed to be an n-type 2D semiconductor and is hard to switch its majority carrier type only using different contact metals. Besides vdW integrating 3D metal, 2D graphene has also been utilized as the vdW electrode to de-pin the metal semiconductor junctions, leading to the switch of device majority carrier [39]. However, this method may need the assistance of additional gate electrode to modulate the work function of graphene, posing a limitation for practical application.

Although the contact engineering (based on different metals) has demonstrated desired polarity control, this approach involved two different metals, which would greatly complicate the fabrication process. To overcome this limitation, a polarity control strategy is recently demonstrated by using same contact metal gold and same channel materials, but different metal integration methods. By vdW integrating Au electrode, robust PMOS characteristic is observed in multilayer WSe_2 transistors, in great contrast to the NMOS fabricated on the same WSe_2 flake using conventional deposited Au contacts, as shown in Fig. 8(f). With the ability to control polarity of WSe_2 transistors using same contact metal, logic inverter is demonstrated with a highest voltage gain of 340 (at V_{dd} of 5.5 V, Fig. 8(g)) and total noise margin over 90%. Furthermore, this contact integration strategy is also extended to realize more complex logic functions such as NAND and NOR, as shown in Fig. 8(h) [123]. To further increase the voltage gain, high-k dielectric with thinner thickness should be used to enhance the gate controllability towards the channel. In addition, the reduction of contact resistance and the balance between PMOS and NMOS are also beneficial for the gain improvement.

3.4 Electrostatic doping and polarity control

Another approach to enable polarity control and CMOS functions

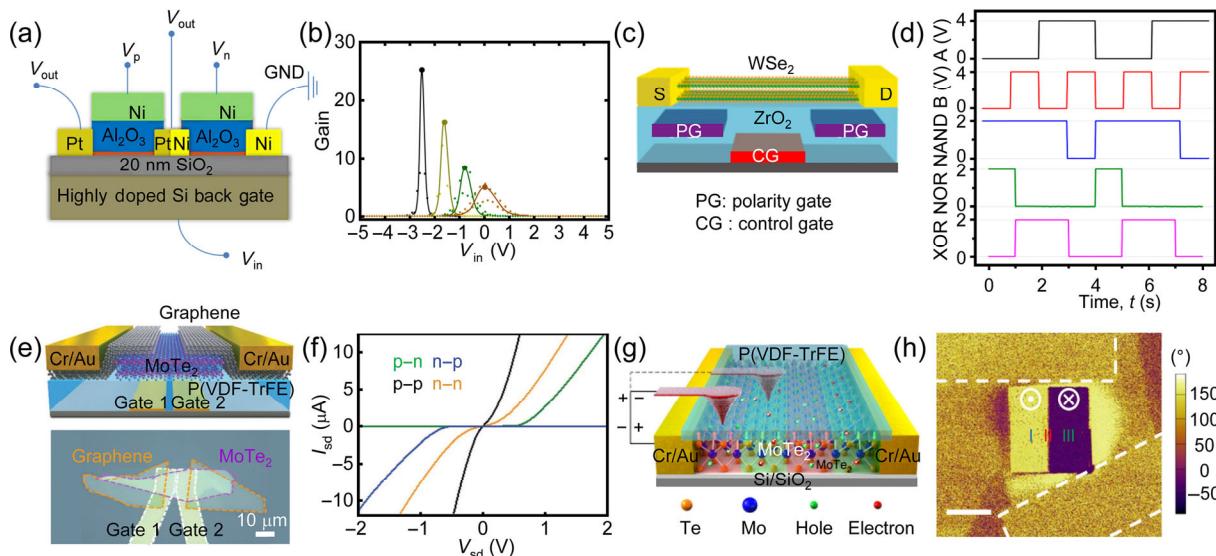


Figure 9 (a) The electrostatic doping of WSe_2 transistors using two control gate electrodes, where top gate voltages are used to modulate transistor polarity individually and to achieve CMOS inverter function. (b) Voltage gain of corresponding WSe_2 inverter with various control voltage difference. (a) and (b) are reproduced with permission from Ref. [124], © AIP Publishing LLC 2014. (c) The schematic illustration of WSe_2 transistor polarity control using CG and PG. (d) The 2-input logic functions of the NAND, NOR, and XOR gates using WSe_2 transistors with CG and PG. (c) and (d) are reproduced with permission from Ref. [125], © American Chemical Society 2018. (e) Ferroelectric (using PVDF as the dielectric layer) modulations of the MoTe_2 transistor structure (upper) and corresponding device optical image. (f) I_{ds} - V_{ds} output curves by using localized bottom gate to dope different regions. (e) and (f) are reproduced with permission from Ref. [126], © Wiley-VCH Verlag GmbH & Co. KGaA 2020. (g) Probe-controlled ferroelectric domains of the MoTe_2 lateral homojunction, using the AFM tip rather than fixed gate electrodes. (h) The PFM phase diagram of different MoTe_2 region, demonstrating the effective tip modulation of device polarity. (g) and (h) are reproduced with permission from Ref. [127], © Wu, G. J. et al., under exclusive licence to Springer Nature Limited 2020.

is electrostatic doping of 2D semiconductors. As shown in Fig. 9(a), two split control gates (CG, also termed polarity gate: PG) are deposited on top of 2D transistors. During device operation, opposite voltages are applied on the two control gates, allowing to define spatially controlled p-type region and n-type regions individually (under gate electrodes) and leading to the demonstration of high-performance CMOS inverters. Importantly, the doping concentration and threshold voltage of each region (either p-type or n-type) can be precisely controlled by polarity gate voltage, offering another degree of freedom to design the behavior of resulting CMOS logic function. For example, by changing the voltage difference between two control gates, the inverter switching voltage and inverter gain can be modulated, as shown in Fig. 9(b) [124]. Based on similar electrostatic doping concept, functional and complete CMOS logic functions have been demonstrated, including inverter, NAND, NOR, 2-input XOR, 3-input XOR, and majority (MAJ), as shown in Figs. 9(c) and 9(d) [125]. Owing to the highly re-configurable device operation using electrostatic gate, the device structure could realize specific functions with fewer transistors than conventional CMOS design. For example, the XOR-2 logic is realized with only four polarity-controllable devices, in contrast to 8 transistors required using conventional CMOS design.

On the other hand, similar to contact doping (discussed in Section 3.3), there still remains two limitations for split-gate electrostatic doping approaches. First, to utilize this doping scheme, the 2D semiconductor needs to be electrical switched between n- and p-type, where contacts should be able to inject both electron and hole depending on the control gate voltage. Hence, this approach is largely limited to ambipolar 2D transistors, such as WSe₂, MoTe₂, BP [119–121]. Second, the fabrication of additional control gates (as well as gate dielectric) is required, not only complicating the device fabrication process, but also requiring a fixed potential applied on the gate electrode to maintain the majority carrier type.

To avoid additional voltage used for the control gate, the transistor polarity can be modulated through ferroelectric materials, which takes advantage of the nonvolatility of electrostatic fields at the interface between ferroelectric and 2D semiconductor. For example, by using poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) as the ferroelectric material and additional gate electrode to control its polarization direction, the polarity of MoTe₂ channel can be switched between n-type to p-type (Figs. 9(e) and 9(f)) [126]. Importantly, the ferroelectric electrical fields and majority carrier type still remain by removing control gate voltage, greatly simplifying the device operation and demonstrating advantages over the previous electrostatics doping approach. Furthermore, to avoid the existence of physical control gate electrode (for poling the ferroelectric) and to simplify the device fabrication process, tip-based modulation of ferroelectric domains is demonstrated with highly controlled shapes and sizes. As shown in Fig. 9(g), a conductive AFM tip is used to program the ferroelectric poly(vinylidene fluoride) (PVDF) up and down, thus fabricating a lateral p-n-p-n junction structure in MoTe₂, which can be verified through piezoresponse force microscopy (PFM) phase diagram (Fig. 9(h)) [127].

4 Outlook

Although lots of advancements have been demonstrated for device polarity control and the realization of complex 2D CMOS function, challenges still remain for its practical application. One important issue is the stability of polarity control technique, particular for chemical doping approaches based

on surface absorption. For example, in the p-doped WSe₂ transistor by NO_x, the on-state current density is reduced ~ 72% after 36 h of air exposure [72], which can be largely attributed to the desorption of physical absorbed NO_x. Although the stability could be greatly improved using more stable chemicals (such as OTS with –CH₃ groups) or hydrophobic PPh₃ organic polymer (PPh₃ with hydrophobic C–H bonds), on-current decrease is still observed with 31% drop for OTS-doping (after 3 days) and 6% for PPh₃-doping (after 14 days) [90, 128]. Similarly, the contact engineering approach (for polarity control) also shows poor stability. For example, MoTe₂ transistors have been fabricated with Au as the contact and BN as the encapsulation layer, where PMOS device characteristic is observed for the as-fabricated device. Interestingly, after simple thermal annealing at 100 °C in inert gases, the polarity of the device is changed from p-type to n-type, which is explained by the formation of Au-MoTe₂ composite (with a lower work function compared to that of bare Au) upon thermal annealing [129]. With further increasing the temperature, the instability of logic device is expected to be more severe, limiting the large current driving operation (with strong joule heating and high local temperature) as well as following fabrication processes.

Scalability and uniformity are also important for large-scale fabrication and for demonstrating complex CMOS circuit or microprocessor. Although exfoliating two different 2D flakes has been demonstrated to achieve various logic functions, the approach is inherent not scalable. Similarly, tip-based polarization of ferroelectric dielectric approach may also face scalability issue, where the relatively slow tip movement and limited tip scanning region and speed may limit the number/yield of fabricated transistors. To this end, CVD approach has demonstrated wafer-scale 2D semiconductors [17, 30], but the quality is typically inferior compared to the exfoliated counterparts. Moreover, since the CVD approach is based on non-uniform gas flux, the uniformity of grown material across the whole wafer (e.g., 4-inch wafer) needs further statistics check and quality analysis. With these challenges solved, there seems no major hurdles for further scaling up the 2D semiconductors, and fabricating more complex logic devices and integrated circuits. Given the short history and already demonstrated MoS₂ microprocessors, we believe that logic circuit research on 2D semiconductors is just at the beginning and will continue to expand towards practical application.

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