ELC 2137 Lab 4: Subtractor

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Summary

This lab was an extension of the previous adders lab, in which a family of logic chips was used to design logic circuits. The full adder and two-bit adder were reproduced, and we were charged with determining what needed to be added to the two-bit adder circuit to convert it to a subtractor circuit. As shown in Figure 2, three XOR gates were needed for the conversion from a two-bit adder circuit to a subtractor circuit. Like the previous circuits, the subtractor circuit was built and tested. The constructed circuit can be found in Figure 1, and the expected and actual results can be found in Figure 3.

Q&A

1. Why did we use two full adders instead of a half adder and a full adder?

   The half adder only has two inputs whereas the full adder has three. There are six possible inputs for the subtractor circuit (A1, B1, A2, B2, Cin, and M), so using two full adders simplifies the circuits. The subtractor circuit was built from a two bit adder circuit, which only has five inputs. An additional input location was necessary to complete the subtractor circuit, as M was added as an input. As shown in Figure 2, M takes the place of Cin, so only five inputs are used. It is possible, however, to build a subtractor circuit with Cin and M as separate inputs, and it would be easier to do so with two full adders instead of a half hald and a full adder.

2. How many input combinations would it take to exhaustively test the adder/subtractor?

   With the M and Cin as separate switches/inputs, there are 2^6 possibilities and with M and Cin as one switch there are 2^5 possiblities.

3. Why were the combinations given in the truth table chosen?

   The combinations in the truth table were given because they represent all the possible outputs from the circuit. Even though the full truth table has eight different inputs, there are only six unique outputs from the circuit because some inputs produce identical outputs.

4. Do the results from your adder/subtractor math what you would expect from theory? Explain any discrepancies.

   Initially, the results from the circuit provided an inverted value for the borrow bit due to the overflow of the operation. However, this issue was rectified via inverting the MSB when using the subtractor operation. Inverting the MSB required an additional exclusive-or gate to be

added to the end of the circuit, which then allowed the theoretical and experimental results to coincide.

Results

The connections in some of the switches on the blue box were problematic, so we had to incorporate additional wires and switches to let the adder/subtractor circuit function properly. We also used two additional XOR gates instead of one for the M connections.

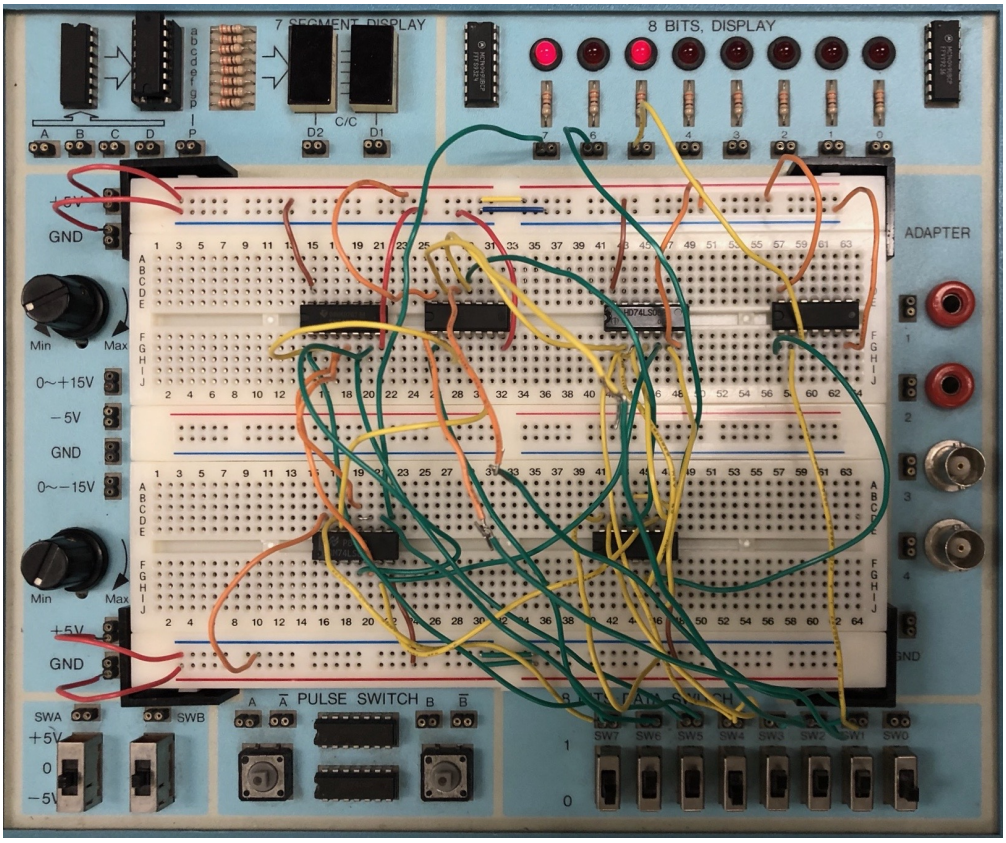
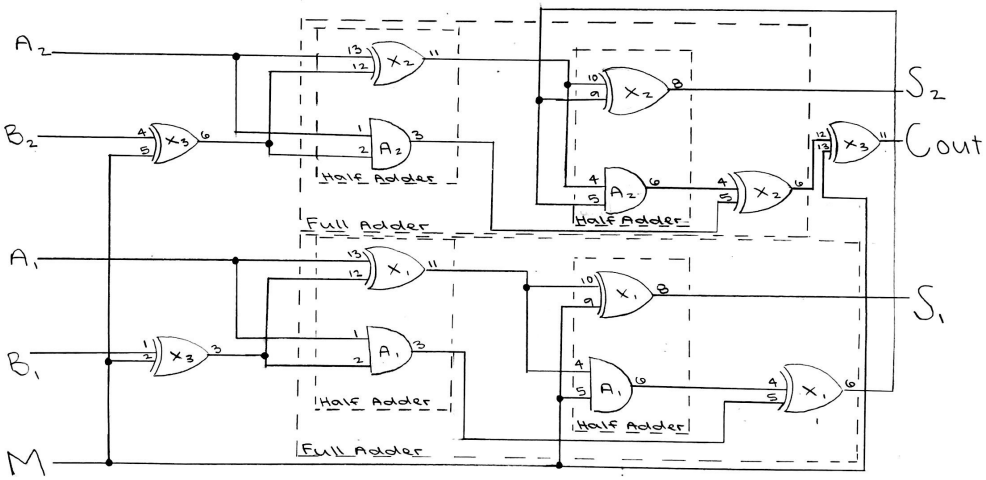


Figure 1: Assembled Subtractor Circuit



Ref. Des.	5V	GND
A_1	14	7
X_1	14	7
A_2	14	7
X_2	14	7
X_3	14	7

Figure 2: Two Bit Adder/Subtractor Schematic

Circuit Demonstration Page

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Instructor Signatures

Separate Full Adders

Two-Bit Adder

Adder/Subtractor

Inputs		Expected Results			Actual Results
A	B	B 2's comp	Sub Cout S1 S0	Dec	Sub
00	01	11	1 11	-1	1 1 1
00	10	10	1 10	-2	1 1 0
00	11	01	1 01	-3	1 0 1
01	01	11	0 00	0	0 0 0
10	01	11	0 01	1	0 0 1
10	00	00	0 10	2	0 1 0

Figure 3: In-Class Circuit Demonstration