



## 1. Description

### 1.1. Project

Project Name	CubeMX-UFBGA176+25
Board Name	custom
Generated with:	STM32CubeMX 6.16.1
Date	02/02/2026

### 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H725/735
MCU name	STM32H725IGKx
MCU Package	UFBGA176
MCU Pin number	201

### 1.3. Core(s) information

Core(s)	Arm Cortex-M7
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### 3. Pins Configuration

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PB8	I/O	I2C4_SCL	
A3	VDDLDO	Power		
A4	VCAP	Power		
A5	PB6	I/O	TIM4_CH1	
A6	PB3(JTDO/TRACESWO)	I/O	TIM2_CH2	
A7	PG11	I/O	ETH_TX_EN	
A8	PG9	I/O	FDCAN3_TX	
A9	PD3	I/O	SPI2_SCK	
A10	PD1 *	I/O	GPIO_Output	FPGA_CRESET_B
A11	PA15(JTDI)	I/O	SPI3_NSS	
A12	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
A13	VDDLDO	Power		
A14	VCAP	Power		
A15	VSS	Power		
B1	PE4	I/O	SPI4_NSS	
B2	PE3	I/O	USART10_TX	
B3	PB9	I/O	SPI2_NSS	
B4	PE0	I/O	UART8_RX	
B5	PB7	I/O	USART1_RX	
B6	PB4(NJTRST)	I/O	TIM3_CH1	
B7	PG13	I/O	SPI6_SCK	
B8	PD7	I/O	OCTOSPIM_P1_IO7	
B9	PD5	I/O	USART2_TX	
B10	PD2	I/O	UART5_RX	
B11	PC12	I/O	UART5_TX	
B12	PH14	I/O	FDCAN1_RX, UART4_RX	
B13	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
B14	PA8	I/O	RCC_MCO_1	
B15	PA12	I/O	USB_OTG_HS_DP	
C1	PC13	I/O	GPIO_EXTI13	EXTI13_WIFI
C2	VSS	Power		
C3	PE2	I/O	USART10_RX	
C4	PE1	I/O	UART8_TX	
C5	BOOT0	Boot		
C6	PB5	I/O	TIM3_CH2	

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
C7	PG14	I/O	SPI6_MOSI	
C8	PG10	I/O	FDCAN3_RX	
C9	PD4	I/O	GPIO_EXTI4	EXTI4_EMERGENCY_STOP
C11	PC11	I/O	SPI3_MISO	
C12	PC10	I/O	SPI3_SCK	
C13	PH13	I/O	FDCAN1_TX, UART4_TX	
C14	PA10	I/O	USB_OTG_HS_ID	
C15	PA11	I/O	USB_OTG_HS_DM	
D1	PC15-OSC32_OUT	I/O	GPIO_EXTI15	EXTI15_RESERVED
D2	PC14-OSC32_IN	I/O	GPIO_EXTI14	EXTI14_FPGA_CDONE
D3	PE5	I/O	SPI4_MISO	
D4	PDR_ON	Power		
D5	VDD	Power		
D6	VSS	Power		
D7	PG15 *	I/O	GPIO_Input	DIGITAL_IN_2
D8	PG12	I/O	OCTOSPIM_P2_NCS	
D9	PD6	I/O	USART2_RX	
D10	VSS	Power		
D11	VDD	Power		
D12	PH15 *	I/O	GPIO_Input	DIGITAL_IN_1
D13	PA9	I/O	USART1_TX	
D14	PC8	I/O	TIM8_CH3	
D15	PC7	I/O	TIM8_CH2	
E1	VSS	Power		
E2	VBAT	Power		
E3	PE6	I/O	SPI4_MOSI	
E4	VDD	Power		
E12	VDD	Power		
E13	PC9	I/O	TIM8_CH4	
E14	PC6	I/O	TIM8_CH1	
E15	VDD50USB	Power		
F1	VLXSMPS	Power		
F2	VSSSMPS	Power		
F3	PF1	I/O	TIM23_CH2	
F4	PF0	I/O	TIM23_CH1	
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F9	VSS	Power		
F10	VSS	Power		
F12	VSS	Power		
F13	VDD33USB	Power		
F14	PG6	I/O	OCTOSPIM_P1_NCS	
F15	PG5	I/O	TIM1_ETR	TIM1_ETR_FPGA
G1	VDDSMPS	Power		
G2	VFBSMPS	Power		
G3	PF2	I/O	TIM23_CH3	
G4	VDD	Power		
G6	VSS	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G12	PG8	I/O	TIM8_ETR	TIM8_ETR_FPGA
G13	PG7 *	I/O	GPIO_Output	SPI5_NSS_2
G14	PG4 *	I/O	GPIO_Output	SPI4_NSS_2
G15	PG2 *	I/O	GPIO_Output	SPI3_NSS_2
H1	PF6	I/O	OCTOSPIM_P1_IO3	
H2	PF4	I/O	OCTOSPIM_P2_CLK	
H3	PF5 *	I/O	GPIO_Output	SPI6_NSS_SW_1
H4	PF3	I/O	TIM23_CH4	
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H12	VDD	Power		
H13	PG3 *	I/O	GPIO_Output	SPI2_NSS_2
H14	PD14	I/O	TIM4_CH3	
H15	PD13	I/O	TIM4_CH2	
J1	PH0-OSC_IN	I/O	RCC_OSC_IN	
J2	PF8	I/O	SPI5_MISO	
J3	PF7	I/O	TIM17_CH1	PWM_OUT_C1_BUZZER
J4	PF9	I/O	SPI5_MOSI	
J6	VSS	Power		
J7	VSS	Power		
J8	VSS	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J9	VSS	Power		
J10	VSS	Power		
J12	PD15	I/O	TIM4_CH4	
J13	PD11	I/O	OCTOSPIM_P1_IO0	
J14	VSS	Power		
J15	PD12	I/O	OCTOSPIM_P1_IO1	
K1	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
K2	VSS	Power		
K3	PF10	I/O	OCTOSPIM_P1_CLK	
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K12	VSS	Power		
K13	PD9	I/O	USART3_RX	
K14	PB15	I/O	SPI2_MOSI	
K15	PB14	I/O	SPI2_MISO	
L1	NRST	Reset		
L2	PC0	I/O	ADC3_INP10	ANALOG_IN_6
L3	PC1	I/O	ETH_MDC	
L4	VREF-	Power		
L12	VDD	Power		
L13	PD10	I/O	GPIO_EXTI10	EXTI10_FPGA
L14	PD8	I/O	USART3_TX	
L15	PB13	I/O	ETH_TXD1	
M1	PC2	I/O	OCTOSPIM_P1_IO2	
M2	PC3	I/O	OCTOSPIM_P1_IO6	
M4	VDDA	Power		
M5	VDD	Power		
M6	VSS	Power		
M7	PC5	I/O	ETH_RXD1	
M8	PB1	I/O	TIM3_CH4	
M9	VDD	Power		
M10	VSS	Power		
M11	PH7	I/O	I2C3_SCL	
M12	PE14	I/O	TIM1_CH4	
M13	PH11	I/O	TIM5_CH2	

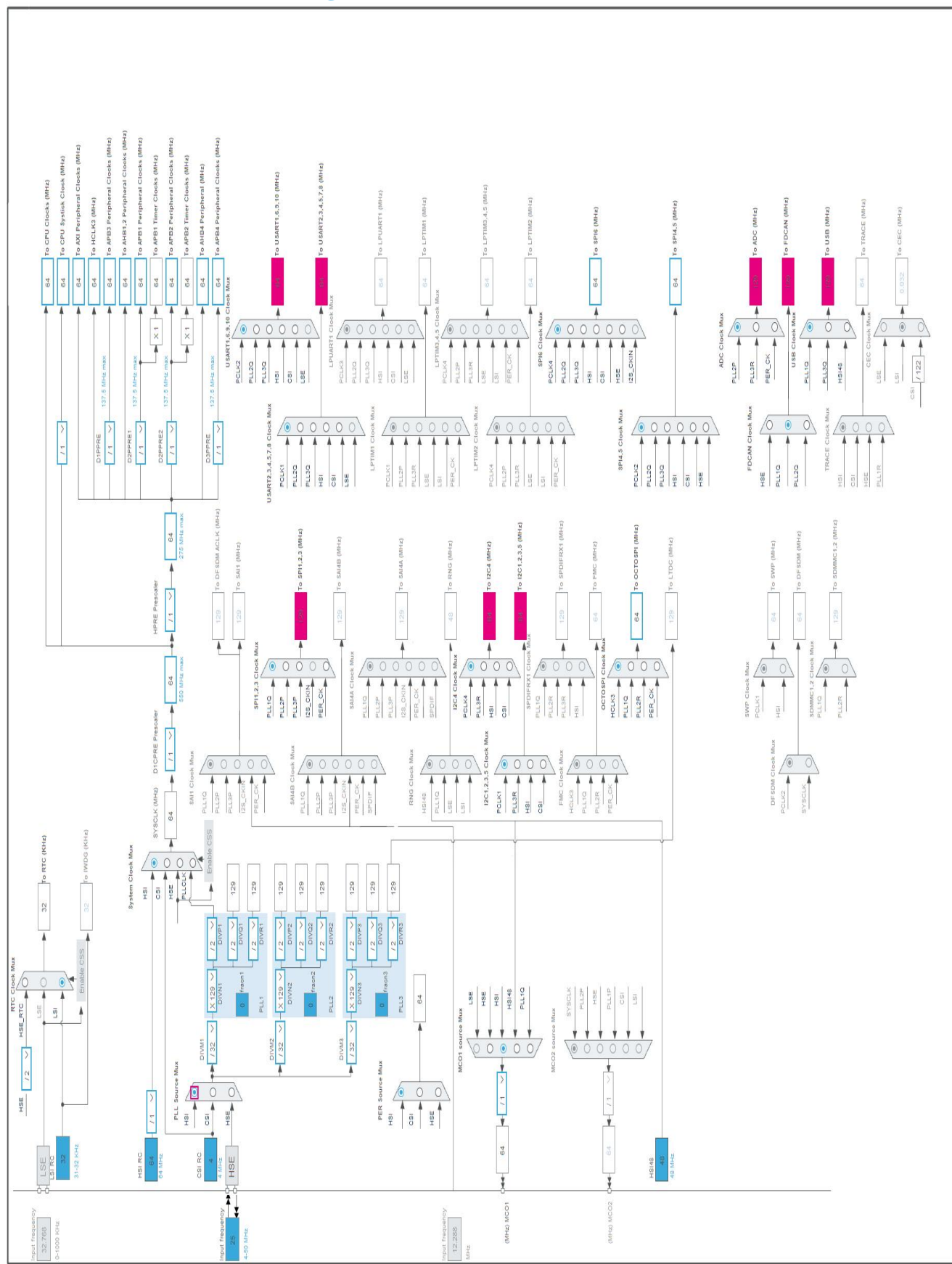
Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
M14	PH9	I/O	DAC1_EXTI9, GPIO_Input	EXTI9_DAC
M15	PB12	I/O	ETH_TXD0	
N1	PC2_C	I/O	ADC3_INP0	ANALOG_IN_3
N2	PC3_C	I/O	ADC3_INP1	ANALOG_IN_4
N3	VSSA	Power		
N4	PH2	I/O	OCTOSPIM_P1_IO4	
N5	PA3	I/O	TIM5_CH4	
N6	PA7	I/O	ETH_CRSDV	
N7	PF11	I/O	TIM24_CH1	
N8	PE8	I/O	UART7_TX	
N9	PG1	I/O	UART9_TX	
N10	PF15	I/O	I2C4_SDA	
N11	PF13	I/O	TIM24_CH3	
N12	PB10	I/O	TIM2_CH3	
N13	PH8	I/O	I2C3_SDA	
N14	PH10	I/O	TIM5_CH1	
N15	PH12	I/O	TIM5_CH3	
P1	PA0	I/O	TIM2_CH1	
P2	PA1	I/O	ETH_REF_CLK	
P3	PA1_C	I/O	ADC1_INP1	ANALOG_IN_1
P4	PH4	I/O	ADC3_INP15	ANALOG_IN_5
P5	PA4	I/O	DAC1_OUT1	
P6	PA5	I/O	DAC1_OUT2	
P7	PB2	I/O	SPI3_MOSI	
P8	PG0	I/O	UART9_RX	
P9	PE7	I/O	UART7_RX	
P10	PB11	I/O	TIM2_CH4	
P11	PF12	I/O	TIM24_CH2	
P12	PE12	I/O	SPI4_SCK	
P13	PE13	I/O	TIM1_CH3	
P15	PH6	I/O	SPI5_SCK	
R1	VSS	Power		
R2	PA2	I/O	ETH_MDIO	
R3	PA0_C	I/O	ADC1_INP0	ANALOG_IN_2
R4	PH3	I/O	OCTOSPIM_P1_IO5	
R5	PH5	I/O	SPI5_NSS	
R6	PC4	I/O	ETH_RXD0	
R7	PA6	I/O	SPI6_MISO	
R8	PB0	I/O	TIM3_CH3	



Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R9	PE10 *	I/O	GPIO_Output	SPI6_NSS_SW_2
R10	PF14	I/O	TIM24_CH4	
R11	PE9	I/O	TIM1_CH1	
R12	PE11	I/O	TIM1_CH2	
R13	VCAP	Power		
R14	VDDLDO	Power		
R15	VSS	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H725/735
MCU	STM32H725IGKx
Datasheet	DS13311_Rev1

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

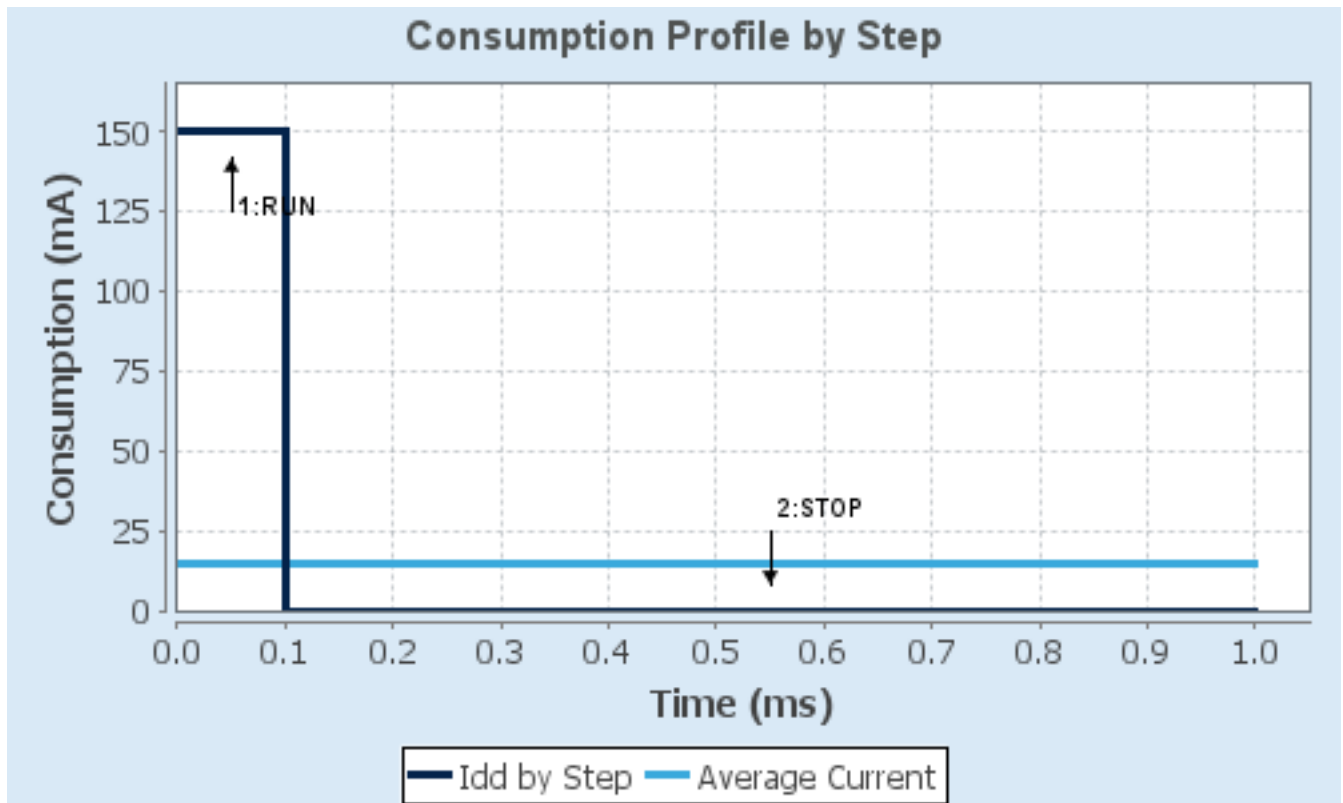
#### 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0: Scale0/Boost	SVOS3: System-Scale3/SMPs-LDO
<b>D1 Mode</b>	DRUN	DSTANDBY
<b>D2 Mode</b>	DRUN	DSTANDBY
<b>D3 Mode</b>	DRUN	DSTOP
<b>Fetch Type</b>	SRAM1/FlashMode-ON/Cache	NA
<b>CPU Frequency</b>	550 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	LSE LowDrive RTC
<b>Clock Source Frequency</b>	8 MHz	32.768 kHz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	150 mA	2.5 µA
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	1177.0	0.0
<b>Ta Max</b>	107.9	125
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	15 mA
Battery Life	1 day, 17 hours	Average DMIPS	1177.0 DMIPS

#### 1.6. Chart



## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	CubeMX-UFBGA176+25
Project Folder	D:\Users\Hydra\Documents\DipTrace\Projects\MakerPnPControl\CubeMX
Toolchain / IDE	EWARM V8.50
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_DAC1_Init	DAC1
5	MX_ETH_Init	ETH
6	MX_FDCAN3_Init	FDCAN3
7	MX_SPI2_Init	SPI2
8	MX_SPI3_Init	SPI3
9	MX_SPI4_Init	SPI4
10	MX_SPI5_Init	SPI5
11	MX_TIM1_Init	TIM1

Rank	Function Name	Peripheral Instance Name
12	MX_TIM2_Init	TIM2
13	MX_TIM5_Init	TIM5
14	MX_TIM8_Init	TIM8
15	MX_TIM12_Init	TIM12
16	MX_TIM14_Init	TIM14
17	MX_TIM15_Init	TIM15
18	MX_TIM16_Init	TIM16
19	MX_TIM17_Init	TIM17
20	MX_TIM23_Init	TIM23
21	MX_TIM24_Init	TIM24
22	MX_UART5_Init	UART5
23	MX_UART7_Init	UART7
24	MX_UART8_Init	UART8
25	MX_UART9_Init	UART9
26	MX_USART1_UART_Init	USART1
27	MX_USART2_UART_Init	USART2
28	MX_USART3_UART_Init	USART3
29	MX_USART10_UART_Init	USART10
30	MX_USB_OTG_HS_USB_Init	USB_OTG_HS
31	MX_ADC1_Init	ADC1
32	MX_ADC3_Init	ADC3
33	MX_FDCAN1_Init	FDCAN1
34	MX_I2C3_Init	I2C3
35	MX_OCTOSPI1_Init	OCTOSPI1
36	MX_RTC_Init	RTC
37	MX_TIM3_Init	TIM3
38	MX_TIM4_Init	TIM4
39	MX_TIM6_Init	TIM6
40	MX_TIM7_Init	TIM7
41	MX_SPI6_Init	SPI6
42	MX_I2C4_Init	I2C4
43	MX_OCTOSPI2_Init	OCTOSPI2

### 3. Peripherals and Middlewares Configuration

#### 3.1. ADC1

mode: IN0

IN1: IN1 Single-ended

##### 3.1.1. Parameter Settings:

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##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler	Asynchronous clock mode divided by 4
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	1
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

##### ADC\_Injected\_ConversionMode:

Enable Injected Conversions	Disable
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##### Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false
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##### Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false
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##### Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false
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### 3.2. ADC3

mode: IN0

IN1: IN1 Single-ended

IN10: IN10 Single-ended

IN15: IN15 Single-ended

mode: Vbat Channel

mode: Temperature Sensor Channel

mode: Vrefint Channel

#### 3.2.1. Parameter Settings:

##### **ADC\_Settings:**

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Scan Conversion Mode	Disabled
Data Alignment	Right alignment
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

##### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	Oversampling ratio 2x
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Sampling Mode	Normal
<u>Rank</u>	1
Channel	<b>Channel Vrefint *</b>
Sampling Time	2.5 Cycles
Offset Number	No offset
Offset Sign	Offset Sign Negative

##### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions	Disable
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#### Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

#### Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

#### Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

### 3.3. CORTEX\_M7

#### 3.3.1. Parameter Settings:

##### Speculation default mode Settings:

Speculation default mode Enabled \*

##### Cortex Interface Settings:

CPU ICache Disabled

CPU DCache Disabled

##### Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers

##### Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled

MPU Region Base Address 0x0 \*

MPU Region Size 4GB

MPU SubRegion Disable 0x87 \*

MPU TEX field level level 0

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access DISABLE

MPU Shareability Permission ENABLE

MPU Cacheable Permission DISABLE

MPU Bufferable Permission DISABLE

##### Cortex Memory Protection Unit Region 1 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 2 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

**Cortex Memory Protection Unit Region 6 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 7 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 8 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 9 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 10 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 11 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 12 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 13 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 14 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 15 Settings:**

MPU Region Disabled

### 3.4. DAC1

**OUT1 connected to: both external pin and on chip analog peripherals**

**OUT2 connected to: both external pin and on chip analog peripherals**

**mode: External Trigger**

#### 3.4.1. Parameter Settings:

**DAC Out1 Settings:**

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
On chip peripheral(s)	not yet connected

**DAC Out2 Settings:**

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None

User Trimming	Factory trimming
On chip peripheral(s)	not yet connected

### 3.5. DEBUG

#### Debug: Serial Wire

### 3.6. ETH

#### Mode: RMII

##### 3.6.1. Parameter Settings:

#### General : Ethernet Configuration:

Warning	Ethernet RX and Tx descriptors needs to be placed in a RAM memory accessible by the dedicated Ethernet DMA
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	<b>0x30000080 *</b>
Rx Descriptor Length	4
First Rx Descriptor Address	<b>0x30000000 *</b>
Rx Buffers Address	<b>0x30000100 *</b>
Rx Buffers Length	1536

### 3.7. FDCAN1

#### mode: Activated

##### 3.7.1. Parameter Settings:

#### Clock Calibration Unit:

Clock Calibration	Disable
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#### Bit Timings Parameters:

Nominal Prescaler	16
Nominal Time Quantum	<b>124.03100775193798 *</b>
Nominal Time Seg1	1
Nominal Time Seg2	1
Nominal Time for one Bit	<b>372 *</b>
Nominal Baud Rate	<b>2687500 *</b>



## I2C: I2C

### 3.10.1. Parameter Settings:

#### Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

#### Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

## 3.11. MEMORYMAP

mode: Activated

## 3.12. OCTOSPI1

Mode: Quad SPI

Clock: Port1 CLK

Chip Select: Port1 NCS

Data [3:0]: Port1 IO[3:0]

### 3.12.1. Parameter Settings:

#### Generic:

Fifo Threshold	1
Dual Quad mode	Disable
Memory Type	Micron
Device Size	32
Chip Select High Time	1
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported

Clock Prescaler	1
Sample Shifting	None
Delay Hold Quarter Cycle	Disable
Chip Select Boundary	0
Delay Block	Disable
Maximum Transfer	0
Refresh Rate	0

### 3.13. OCTOSPI2

**Mode: Quad SPI**

**Clock: Port2 CLK**

**Chip Select: Port2 NCS**

**Data [3:0]: Port1 IO[7:4]**

#### 3.13.1. Parameter Settings:

**Generic:**

Fifo Threshold	1
Dual Quad mode	Disable
Memory Type	Micron
Device Size	32
Chip Select High Time	1
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	1
Sample Shifting	None
Delay Hold Quarter Cycle	Disable
Chip Select Boundary	0
Delay Block	Disable
Maximum Transfer	0
Refresh Rate	0

### 3.14. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**mode: Master Clock Output 1**

#### 3.14.1. Parameter Settings:

**Power Parameters:**

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

**RCC Parameters:**

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	64

**System Parameters:**

VDD voltage (V)	3.3
Flash Latency(WS)	1 WS (2 CPU cycle)

**PLL range Parameters:**

PLL1 input frequency range	Between 2 and 4 MHz
PLL2 input frequency range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

### 3.15. RTC

**mode: Activate Clock Source****3.15.1. Parameter Settings:****General:**

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

### 3.16. SPI2

**Mode: Full-Duplex Master****Hardware NSS Signal: Hardware NSS Output Signal****3.16.1. Parameter Settings:****Basic Parameters:**

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First



**Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>64.5 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.17. SPI3

**Mode: Full-Duplex Master****Hardware NSS Signal: Hardware NSS Output Signal**3.17.1. Parameter Settings:**Basic Parameters:**

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>64.5 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern

Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.18. SPI4

**Mode: Full-Duplex Master**

**Hardware NSS Signal: Hardware NSS Output Signal**

#### 3.18.1. Parameter Settings:

**Basic Parameters:**

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>32.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.19. SPI5

## Mode: Full-Duplex Master

### Hardware NSS Signal: Hardware NSS Input Signal

#### 3.19.1. Parameter Settings:

##### Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

##### Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	<b>32.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

##### Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Input Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

## 3.20. SPI6

### Mode: Full-Duplex Master

#### 3.20.1. Parameter Settings:

##### Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

##### Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	<b>32.0 MBits/s *</b>
Clock Polarity (CPOL)	Low

Clock Phase (CPHA)	1 Edge
<b>Advanced Parameters:</b>	
CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.21. SYS

**Timebase Source: SysTick**

### 3.22. TIM1

**Slave Mode: Trigger Mode**

**Trigger Source: ETR1**

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

**Channel3: Input Capture direct mode**

**Channel4: Input Capture direct mode**

#### 3.22.1. Parameter Settings:

##### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable
Slave Mode Controller	Trigger Mode

##### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

**Trigger:**

Trigger Polarity	non inverted
Trigger Prescaler	Prescaler not used
Trigger Filter (4 bits value)	0

**Input Capture Channel 1:**

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

**Input Capture Channel 2:**

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

**Input Capture Channel 3:**

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

**Input Capture Channel 4:**

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

### 3.23. TIM2

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

**Channel3: Input Capture direct mode**

**Channel4: Input Capture direct mode**

#### 3.23.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

#### Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

### 3.24. TIM3

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

**Channel3: Input Capture direct mode**

**Channel4: Input Capture direct mode**

#### 3.24.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

#### Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

### 3.25. TIM4

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

**Channel3: Input Capture direct mode**

**Channel4: Input Capture direct mode**

#### 3.25.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

#### Input Capture Channel 1:

Polarity Selection	Rising Edge
--------------------	-------------

IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

### 3.26. TIM5

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

**Channel3: Input Capture direct mode**

**Channel4: Input Capture direct mode**

#### 3.26.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

#### Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division



Input Filter (4 bits value) 0

#### Input Capture Channel 2:

Polarity Selection Rising Edge

IC Selection Direct

Prescaler Division Ratio No division

Input Filter (4 bits value) 0

#### Input Capture Channel 3:

Polarity Selection Rising Edge

IC Selection Direct

Prescaler Division Ratio No division

Input Filter (4 bits value) 0

#### Input Capture Channel 4:

Polarity Selection Rising Edge

IC Selection Direct

Prescaler Division Ratio No division

Input Filter (4 bits value) 0

### 3.27. TIM6

**mode: Activated**

#### 3.27.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value ) 65535

auto-reload preload Disable

##### Trigger Output (TRGO) Parameters:

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

### 3.28. TIM7

**mode: Activated**

#### 3.28.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value ) 65535

auto-reload preload Disable

#### Trigger Output (TRGO) Parameters:

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

### 3.29. TIM8

#### Slave Mode: Trigger Mode

#### Trigger Source: ETR1

#### Channel1: Input Capture direct mode

#### Channel2: Input Capture direct mode

#### Channel3: Input Capture direct mode

#### Channel4: Input Capture direct mode

#### 3.29.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value) 0  
Counter Mode Up  
Counter Period (AutoReload Register - 16 bits value ) 65535  
Internal Clock Division (CKD) No Division  
Repetition Counter (RCR - 16 bits value) 0  
auto-reload preload Disable  
Slave Mode Controller Trigger Mode

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)  
Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)  
Trigger Event Selection TRGO2 Reset (UG bit from TIMx\_EGR)

##### Trigger:

Trigger Polarity non inverted  
Trigger Prescaler Prescaler not used  
Trigger Filter (4 bits value) 0

##### Input Capture Channel 1:

Polarity Selection Rising Edge  
IC Selection Direct  
Prescaler Division Ratio No division  
Input Filter (4 bits value) 0

##### Input Capture Channel 2:

Polarity Selection Rising Edge  
IC Selection Direct  
Prescaler Division Ratio No division  
Input Filter (4 bits value) 0

#### Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

### 3.30. TIM12

#### Channel1: Output Compare No Output

#### Channel2: Output Compare No Output

##### 3.30.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### Clear Input:

Clear Input Source	Disable
--------------------	---------

#### Output Compare No Output Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

#### Output Compare No Output Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

### 3.31. TIM14

**mode: Activated**

#### 3.31.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

### 3.32. TIM15

**Channel1: Output Compare No Output**

**Channel2: Output Compare No Output**

#### 3.32.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

**Break And Dead Time management - BRK Configuration:**

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

**Break And Dead Time management - Output Configuration:**

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable

Off State Selection for Idle Mode (OSSI) Disable  
Lock Configuration Off

#### Output Compare No Output Channel 1:

Mode Frozen (used for Timing base)  
Pulse (16 bits value) 0  
Output compare preload Disable  
CH Polarity High  
CH Idle State Reset

#### Output Compare No Output Channel 2:

Mode Frozen (used for Timing base)  
Pulse (16 bits value) 0  
Output compare preload Disable  
CH Polarity High  
CH Idle State Reset

### 3.33. TIM16

**mode: Activated**

#### 3.33.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value) 0  
Counter Mode Up  
Counter Period (AutoReload Register - 16 bits value ) 65535  
Internal Clock Division (CKD) No Division  
Repetition Counter (RCR - 8 bits value) 0  
auto-reload preload Disable

### 3.34. TIM17

**mode: Activated**

**Channel1: PWM Generation CH1**

#### 3.34.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value) 0  
Counter Mode Up  
Counter Period (AutoReload Register - 16 bits value ) 65535  
Internal Clock Division (CKD) No Division  
Repetition Counter (RCR - 8 bits value) 0

auto-reload preload                      Disable

**Break And Dead Time management - BRK Configuration:**

BRK State                                  Disable

BRK Polarity                              High

BRK Filter (4 bits value)              0

BRK Sources Configuration

- Digital Input                          Disable

- COMP1                                  Disable

- COMP2                                  Disable

- DFSDM                                  Disable

**Break And Dead Time management - Output Configuration:**

Automatic Output State                Disable

Off State Selection for Run Mode (OSSR)    Disable

Off State Selection for Idle Mode (OSSI)    Disable

Lock Configuration                      Off

**PWM Generation Channel 1:**

Mode                                      PWM mode 1

Pulse (16 bits value)                  0

Output compare preload                Enable

Fast Mode                                Disable

CH Polarity                              High

CH Idle State                            Reset

### 3.35. TIM23

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

**Channel3: Input Capture direct mode**

**Channel4: Input Capture direct mode**

#### 3.35.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)        0

Counter Mode                            Up

Counter Period (AutoReload Register - 32 bits value )    4294967295

Internal Clock Division (CKD)            No Division

auto-reload preload                      Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)            Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO            Reset (UG bit from TIMx\_EGR)

#### Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

### 3.36. TIM24

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

**Channel3: Input Capture direct mode**

**Channel4: Input Capture direct mode**

#### 3.36.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

#### Input Capture Channel 1:

Polarity Selection	Rising Edge
--------------------	-------------

IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

### 3.37. UART5

#### Mode: Asynchronous

##### 3.37.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable



Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

### 3.38. UART7

#### Mode: Asynchronous

##### 3.38.1. Parameter Settings:

###### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

###### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

###### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

### 3.39. UART8

#### Mode: Asynchronous

##### 3.39.1. Parameter Settings:

###### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

**Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 3.40. UART9

### Mode: Asynchronous

#### 3.40.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

**Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

### 3.41. USART1

#### Mode: Asynchronous

##### 3.41.1. Parameter Settings:

###### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

###### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

###### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

### 3.42. USART2

## Mode: Asynchronous

### 3.42.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 3.43. USART3

## Mode: Asynchronous

### 3.43.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

### 3.44. USART10

#### Mode: Asynchronous

##### 3.44.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

### **3.45. USB\_OTG\_HS**

**Internal FS Phy: OTG/Dual\_Role\_Device**

### **3.46. VREFBUF**

**VREFBUF Mode: External voltage reference**

**\* User modified value**

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1_C	ADC1_INP1	Analog mode	No pull-up and no pull-down	n/a	ANALOG_IN_1
	PA0_C	ADC1_INP0	Analog mode	No pull-up and no pull-down	n/a	ANALOG_IN_2
ADC3	PC0	ADC3_INP10	Analog mode	No pull-up and no pull-down	n/a	ANALOG_IN_6
	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull-down	n/a	ANALOG_IN_3
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	ANALOG_IN_4
	PH4	ADC3_INP15	Analog mode	No pull-up and no pull-down	n/a	ANALOG_IN_5
DAC1	PH9	DAC1_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EXTI9_DAC
	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
ETH	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	High	
FDCAN1	PH14	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH13	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN3	PG9	FDCAN3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	FDCAN3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C3	PH7	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PH8	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C4	PB8	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF15	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
OCTOSPI1	PG6	OCTOSPI1_P1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF6	OCTOSPI1_P1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
		IO3				
	PD11	OCTOSPIM_P1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD12	OCTOSPIM_P1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF10	OCTOSPIM_P1_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2	OCTOSPIM_P1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
OCTOSPI2	PD7	OCTOSPIM_P1_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG12	OCTOSPIM_P2_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	OCTOSPIM_P2_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	OCTOSPIM_P1_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH2	OCTOSPIM_P1_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	OCTOSPIM_P1_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PA8	RCC_MCO_1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI3	PA15(JTDI)	SPI3_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI4	PE4	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI5	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH6	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH5	SPI5_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI6	PG13	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	



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IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM1	PG5	TIM1_ETR	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM1_ETR_FPGA
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PB3(JTDO/T RACESWO)	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PB4(NJTRST)	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PH11	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH10	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH12	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG8	TIM8_ETR	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM8_ETR_FPGA
TIM17	PF7	TIM17_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_OUT_C1_BUZZER
TIM23	PF1	TIM23_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF0	TIM23_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF2	TIM23_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF3	TIM23_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM24	PF11	TIM24_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF13	TIM24_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF12	TIM24_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF14	TIM24_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART5	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	

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IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
UART7	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART9	PG1	UART9_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG0	UART9_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART10	PE3	USART10_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE2	USART10_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_HS	PA12	USB_OTG_HS_DP	n/a	n/a	n/a	
	PA10	USB_OTG_HS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	USB_OTG_HS_DM	n/a	n/a	n/a	
GPIO	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FPGA_CRESET_B
	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EXTI13_WIFI
	PD4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EXTI4_EMERGENCY_STOP
	PC15-OSC32_OUT	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EXTI15_RESERVED
	PC14-OSC32_IN	GPIO_EXTI14	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EXTI14_FPGA_CDONE
	PG15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIGITAL_IN_2
	PH15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIGITAL_IN_1
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI5_NSS_2
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI4_NSS_2
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI3_NSS_2
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI6_NSS_SW_1
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_NSS_2
	PD10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EXTI10_FPGA
	PH9	GPIO_Input	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EXTI9_DAC
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI6_NSS_SW_2



## 4.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM15_UP	DMA1_Stream0	Memory To Peripheral	<b>Medium *</b>
TIM6_UP	DMA1_Stream1	Memory To Peripheral	Low
TIM7_UP	DMA1_Stream2	Peripheral To Memory	Low

### TIM15\_UP: DMA1\_Stream0 DMA request Settings:

Mode: **Circular \***  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Half Word  
 Memory Data Width: Half Word

### TIM6\_UP: DMA1\_Stream1 DMA request Settings:

Mode: Normal  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Half Word  
 Memory Data Width: Half Word

### TIM7\_UP: DMA1\_Stream2 DMA request Settings:

Mode: Normal  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Half Word  
 Memory Data Width: Half Word

## 4.3. BDMA configuration

nothing configured in DMA service

#### **4.4. MDMA configuration**

nothing configured in DMA service

## 4.5. NVIC configuration

### 4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream2 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
PVD/AVD through EXTI Line detection Interrupt		unused	
Tamper and TimeStamp interrupts through the EXTI line		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
EXTI line4 interrupt		unused	
ADC1 and ADC2 global interrupts		unused	
FDCAN1 interrupt 0		unused	
FDCAN1 interrupt 1		unused	
EXTI line[9:5] interrupts		unused	
TIM1 break interrupt		unused	
TIM1 update interrupt		unused	
TIM1 trigger and commutation interrupts		unused	
TIM1 capture compare interrupt		unused	
TIM2 global interrupt		unused	
TIM3 global interrupt		unused	
TIM4 global interrupt		unused	
SPI2 global interrupt		unused	
USART1 global interrupt		unused	
USART2 global interrupt		unused	
USART3 global interrupt		unused	
TIM8 break interrupt and TIM12 global interrupt		unused	
TIM8 update interrupt and TIM13 global interrupt		unused	
TIM8 trigger and commutation interrupts and TIM14 global interrupt		unused	

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM8 capture compare interrupt		unused	
TIM5 global interrupt		unused	
SPI3 global interrupt		unused	
UART5 global interrupt		unused	
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts		unused	
TIM7 global interrupt		unused	
Ethernet global interrupt		unused	
Ethernet wake-up interrupt through EXTI line 86		unused	
FDCAN calibration unit interrupt		unused	
I2C3 event interrupt		unused	
I2C3 error interrupt		unused	
FPU global interrupt		unused	
UART7 global interrupt		unused	
UART8 global interrupt		unused	
SPI4 global interrupt		unused	
SPI5 global interrupt		unused	
SPI6 global interrupt		unused	
OCTOSPI1 global interrupt		unused	
I2C4 event interrupt		unused	
I2C4 error interrupt		unused	
TIM15 global interrupt		unused	
TIM16 global interrupt		unused	
TIM17 global interrupt		unused	
HSEM1 global interrupt		unused	
ADC3 global interrupt		unused	
OCTOSPI2 global interrupt		unused	
UART9 global interrupt		unused	
USART10 global interrupt		unused	
FDCAN3 interrupt 0		unused	
FDCAN3 interrupt 1		unused	
TIM23 global interrupt		unused	
TIM24 global interrupt		unused	

#### 4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream2 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true

\* User modified value



## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

Middleware											
System Core	Analog	Timers		Connectivity		Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Other
BDMA	ADC1	RTC	TIM1	ETH	FDCAI1				DEBUG		
CORTEX_M7	ADC3	TIM2	TIM3	FDCAI3	I2C3						
DMA	DAC1	TIM4	TIM5	I2C4	OCTOSPI1						
GPIO	VREFBUF	TIM6	TIM7	OCTOSPI2	SPI2						
MDMA		TIM8	TIM12	SPI3	SPI4						
IVVIC		TIM14	TIM15	SPI5	SPI6						
RCC		TIM16	TIM17	UART5	UART7						
SYS		TIM23	TIM24	UART8	UART9						
				USART1	USART2						
				USART3	USART10						
				USB_HS							

## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip">https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32h7-svd.zip">https://www.st.com/resource/en/svd/stm32h7-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h72x-3x_line_product-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h72x-3x_line_product-overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/brstm32h7.pdf">https://www.st.com/resource/en/brochure/brstm32h7.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32h7rs.pdf">https://www.st.com/resource/en/flyer/flstm32h7rs.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-">https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-</a>

stmicroelectronics.pdf

Application Notes [https://www.st.com/resource/en/application\\_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf)

Application Notes [https://www.st.com/resource/en/application\\_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf)

Application Notes [https://www.st.com/resource/en/application\\_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf)

Application Notes [https://www.st.com/resource/en/application\\_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf)

Application Notes [https://www.st.com/resource/en/application\\_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf)

Application Notes [https://www.st.com/resource/en/application\\_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf)

Application Notes [https://www.st.com/resource/en/application\\_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf)

Application Notes [https://www.st.com/resource/en/application\\_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf)

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