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TODO
* FPGA power sequencing.
* FPGA oscillator.
* FPGA flash programming port (CDONE/CRESET/SPI)
* ESP32 power supplies and boot control.
* LEDs for power rails.
* RGB LED output, for up-lights
* Replace RGB leds with SK6812 RGBW leds.
* Rearrange ADC mux inputs, read PORT 1/3 on ADC CH1/2 and then PORT 2/4 on CH1/2?
* 2x vacuum sensors.
* Head RS422 (non-isolated power).
* Expansion port - in progress.
* Analog mux (2x1 in 4 out).
* CAN termination jumpers.
* Check courtyards of components.
* Route MCU MCO to FPGA
* Diode footprints/model
* Add footprints for weak pull-ups on flash chip WP HOLD
* upgrade OT1-6 mosfets to use SiZ270DT
* signal for TIM1_ETR and TIM8_ETR to Ports 1 and 3 respectively.
* signal for TIM16_CH1 and TIM17_CH1 to Port 2 and 4 respectively.

TODO - for FPGA direct SRAM programming, if needed
* Add footprints for resistor between flash MISO/MOSI
* Add 0 ohm resistor inline on flash CS to FPGA.

REVIEW
* ICE FPGA harware checklist.
* Footprint and pinout for every component.
* Name and check every net.

MAYBE
* external memory for the FPGA - since FPGA is to be memory mapped, CPU could share it.
* connector for front-panel USB socket - should probably go to raspberry-pi - need a small break-out PCB in that case.
* Consider using 2 bit bus switch instead of for HEAD_COMMS jumpers.
* reverse polarity protection, need multiple high-current fets like SUD50P06-15-GE3.
* VUSB sense input.

DONE
* Additional 5V rail for onboard and up-lights.
* FPGA power supplies.
* Raspberry Pi 5 power connector
* Connector for Logic analyzer - 20 pin shrouded header
* Supercap/RTC osc - deleted.
* Models for JST-XH (e.g 'B4B-XH-A(LF)(SN)')
* Ethernet PHY
* MOSFET + connector for external ethernet link leds.

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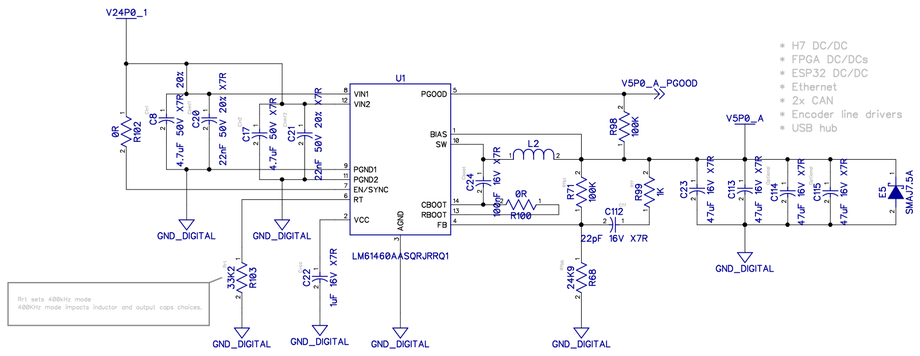
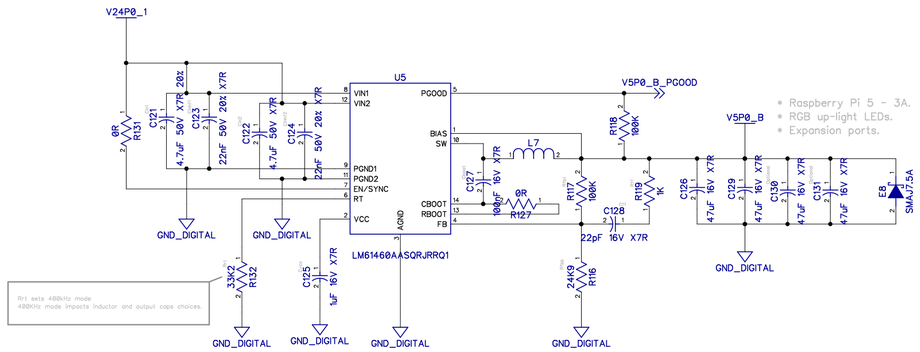
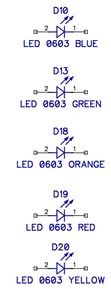
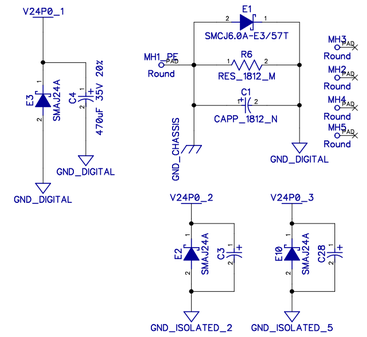
Main 5V power



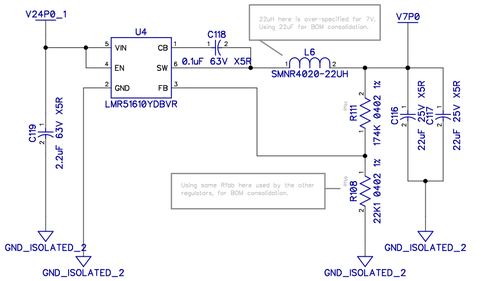
Secondary 5V power



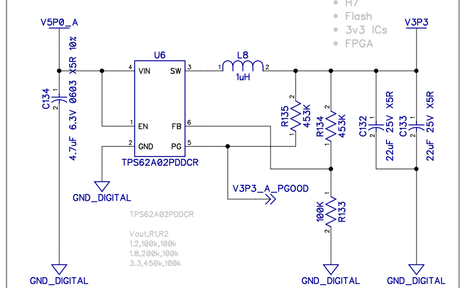




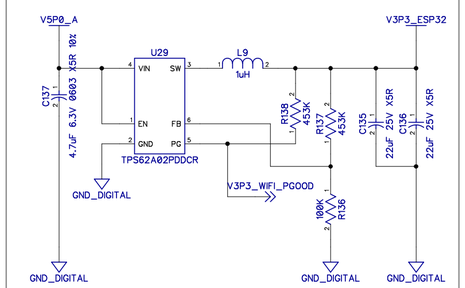
7V supply for the head.



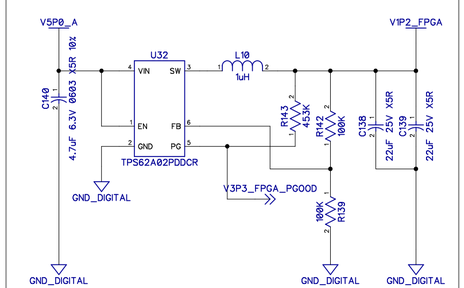
Main 3v3 supply ~ 2A



ESP32/Wifi 3v3 supply ~ 2A



FPGA 1v2 supply ~ 2A



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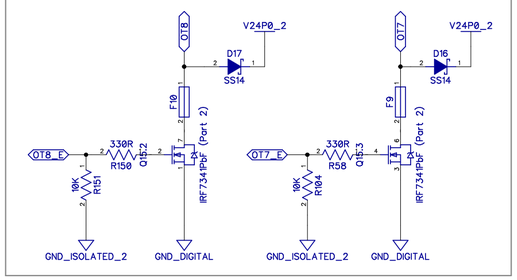
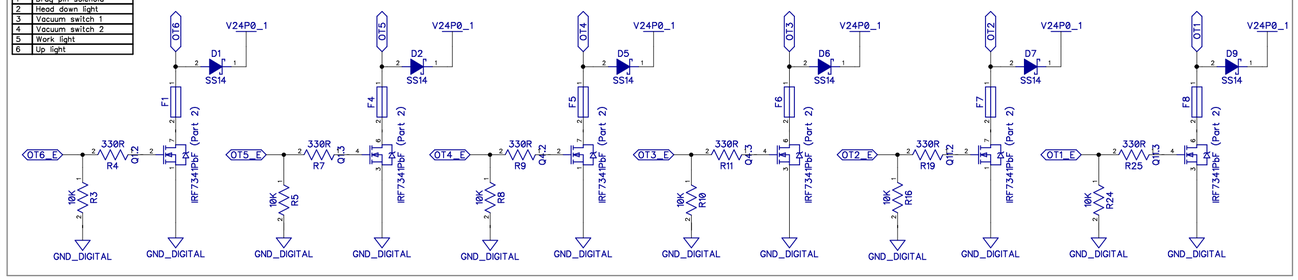
PM3/4 outputs

Not populated on CHMT48VB

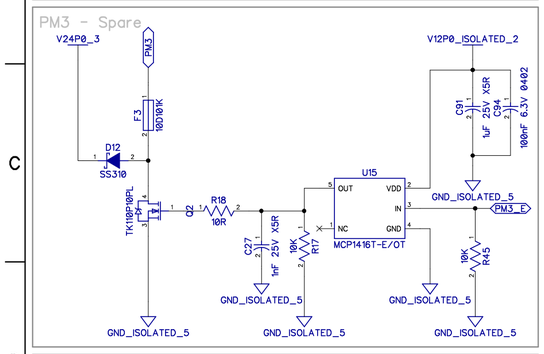


OT1-6 Outputs

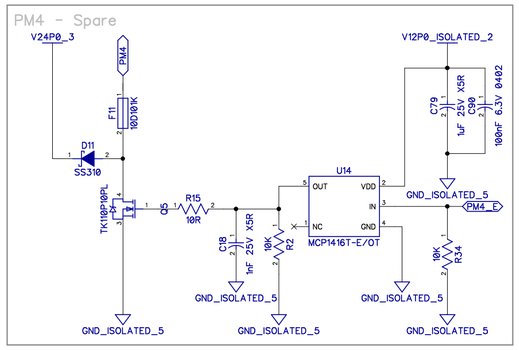
OT	CHMT48VB
1	Drag pin solenoid
2	Head down light
3	Vacuum switch 1
4	Vacuum switch 2
5	Work light
6	Up light



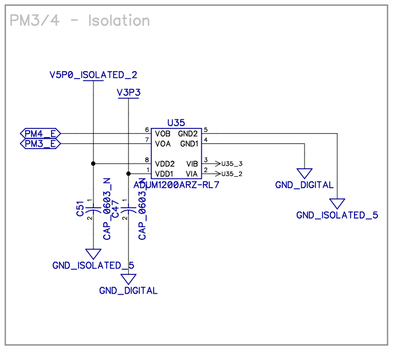
PM3 - Spare

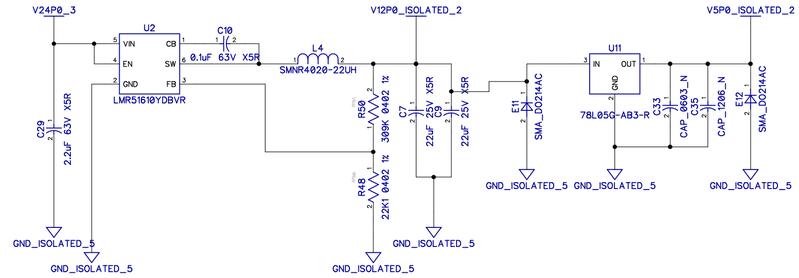


PM4 - Spare

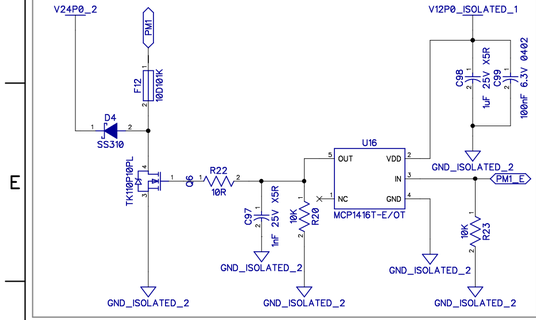


PM3/4 - Isolation

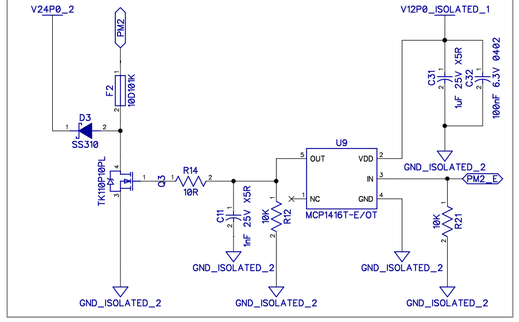




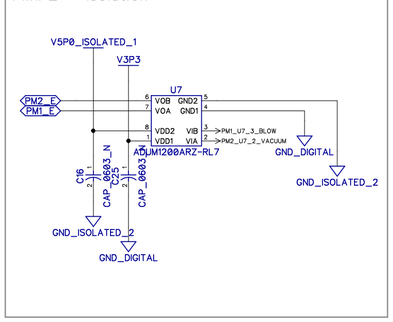
PM1 - Blow

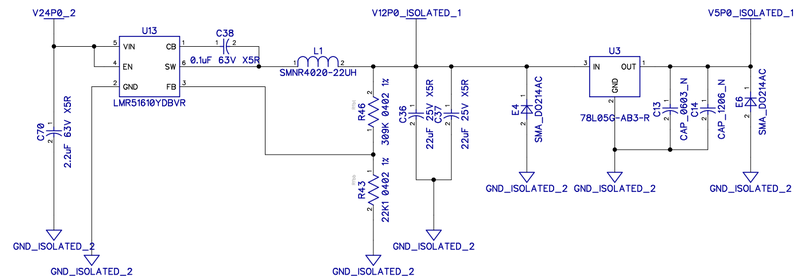


PM2 - Vacuum



PM1/2 - Isolation





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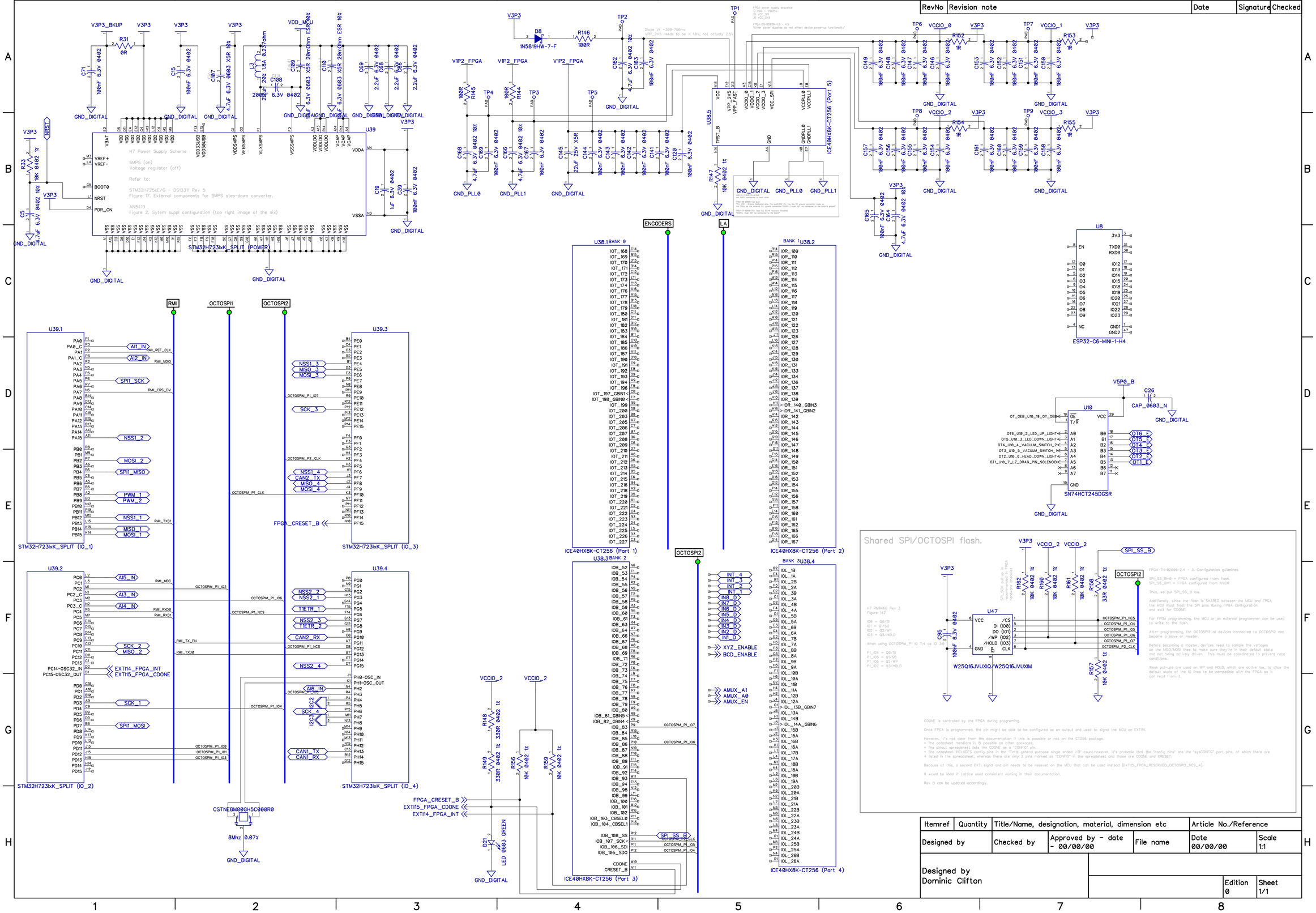

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Pull-down to select INT polarity.
Refer to MICROCHIP LAN8742A-CZ-TR datasheet.

See:
• 3.8.1.5 REGOFF and LED1 Polarity Selection
• 3.8.1.6 nINTSEL and LED2 Polarity Selection

REGOFF = 0
nINTSEL = 0

NX2016SA-25MHZ-STD-CZS-2

LAN8742AI-CZ-TR

H1102NLT

USBLC6-4SC6

PSM712-LF-177

ADM2587EBRWZ

Head comms via RS422

7 Port USB 2 hub.

Up-stream port: A PC or SoC (Raspberry Pi)

Downstream ports:
1-4) Ports 1-4
4-7) H7, FPGA, ESP32

TE2.1-CQFP48A

FD-CAN1 8Mbps (For Ports)

+5V CAN voltage. Always on.

TCAN1044AVDRBRQ1

Pin compatible devices, note VIO requirement.

TCAN1044AVDRBRQ1
TCAN1057AVDRBRQ1
MCP2558FDT-H/MF

CAN1 termination

I2C Pull-Ups

I2C MUX

PCA9545APW,118

FD-CAN2 8Mbps (For Head)

+5V CAN voltage. Always on.

TCAN1044AVDRBRQ1

Pin compatible devices, note VIO requirement.

TCAN1044AVDRBRQ1
TCAN1057AVDRBRQ1
MCP2558FDT-H/MF

CAN2 termination

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Connectors

Organized by physical layout.

Connectors are oriented with pin 1 as they are on the actual PCB.

NOTE: double check with a multimeter to be sure!

Pin 1 locations taken from corresponding datasheets. e.g. JST VH, JST XH, etc.

For logic analyzer debugging.

20 pin female headers

0.127mm pitch
4.8mm width (inc terminals)
3.8mm width (body)
13.1mm length (10*1.27 + 0.4mm)
4.5-4.7mm height
~4.3mm pin insertion depth

Alternatives:
C2684738 - XKB X1312 - X1321FVS-2x10-C43D48
C37328894 - Bossie BX - BX-PM1.27-2-10PU-W

Debug (Same pinout as on ST Nucleo boards)

* SWD
* NRST
* SWO
* SWD

NO ST JTAG

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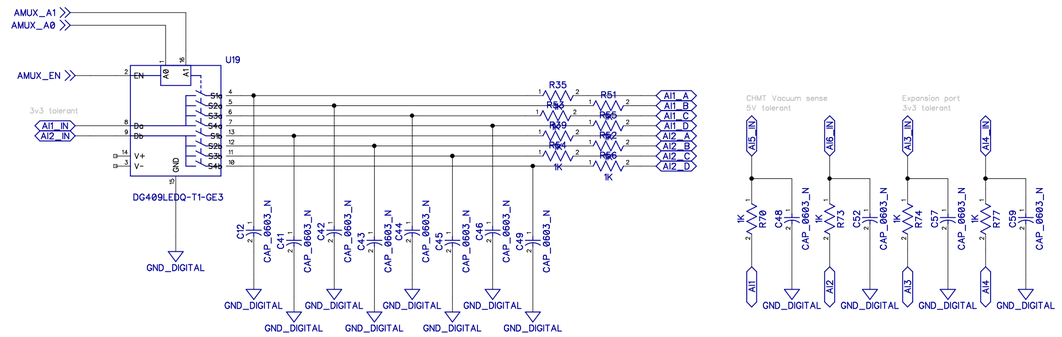

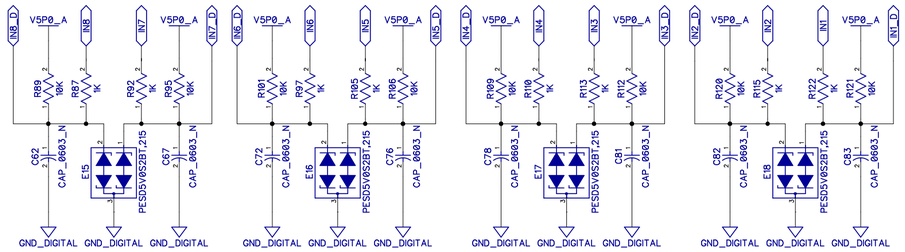

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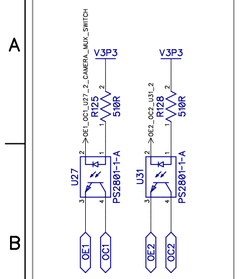
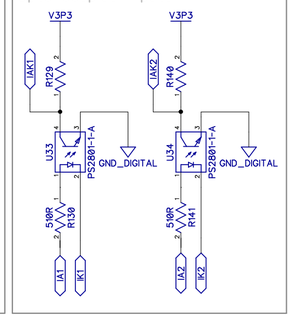
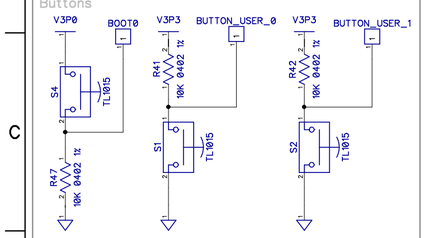
Opto-coupled outputs



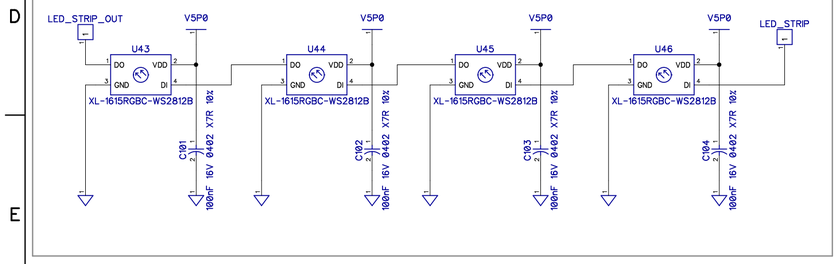
Opto-coupled inputs



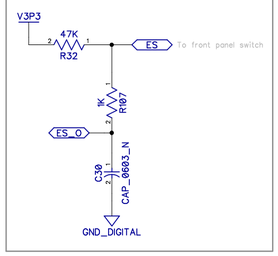
Buttons

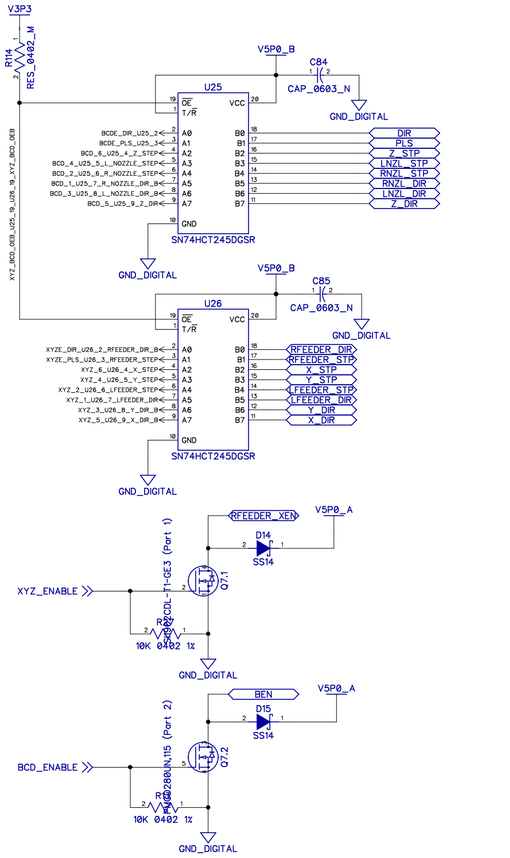


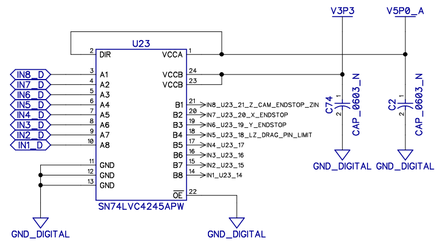
RGB Status LEDs

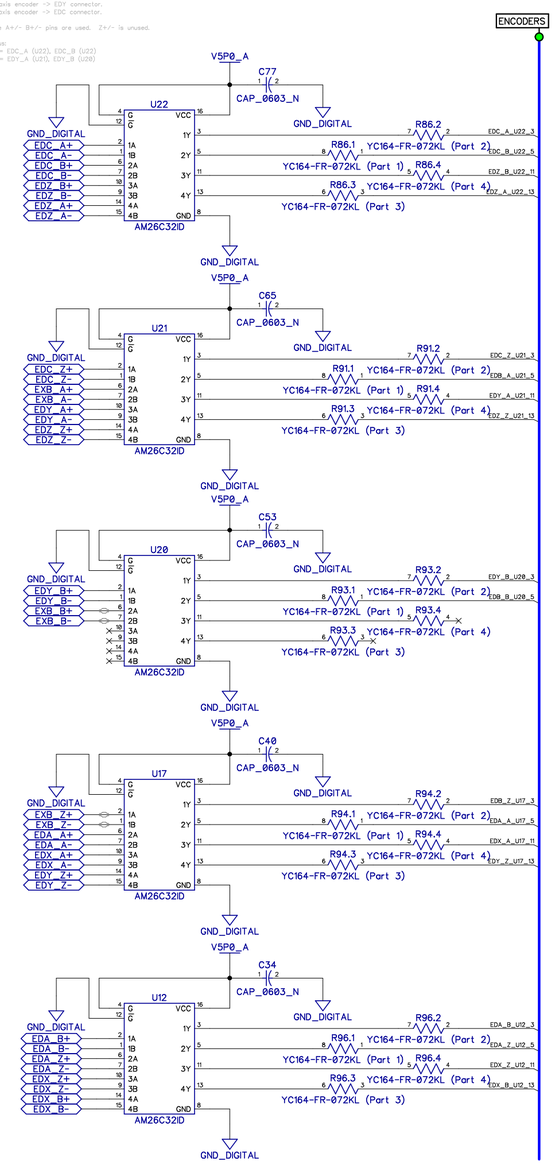


Emergency Stop









CHMT-48VB has 2 differential encoders on X and Y.

Cables are 6 pin shielded cable.
Y axis encoder -> EDY connector.
X axis encoder -> EDC connector.

The A+/- B+/- pins are used. Z+/- is unused.

Thus:
X = EDC_A (U22), EDC_B (U22)
Y = EDY_A (U21), EDY_B (U20)

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