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TODO
* Check courtyards of components.
* Diode footprints/model

MAYBE
* Upgrade OT1-6 Dual MOSFETs
* Connector for front-panel USB socket - should probably go to raspberry-pi - need a small break-out PCB in that case.

DONE
* 2xI2C mux SDA/SDC/INT signals on a header
* Used 8xI2C mux INT signals.
* Load-cell amplifier (HX717)
* VUSB sense input.
* Additional 5V rail for onboard and up-lights.
* Raspberry Pi 5 power connector
* Supercap/RTC osc - deleted.
* Models for JST-XH (e.g 'B4B-XH-A(LF)(SN)')
* Ethernet PHY
* MOSFET + connector for external ethernet link leds.
* 3V3 power from core board
* LEDs for power rails.
* RGB LED output, for up-lights
* 2x vacuum sensors.
* Head RS422 (non-isolated power).
* Analog mux (2x1 in 4 out).

NO
* reverse polarity protection, need multiple high-current fets like SUD50P06-15-GE3.

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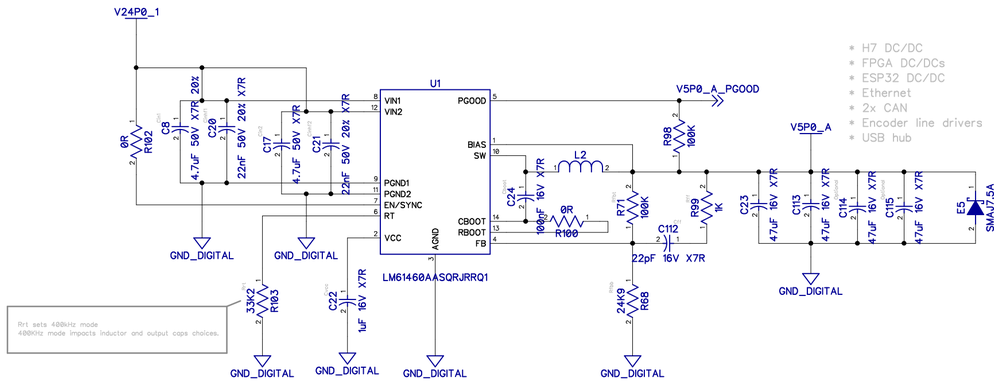
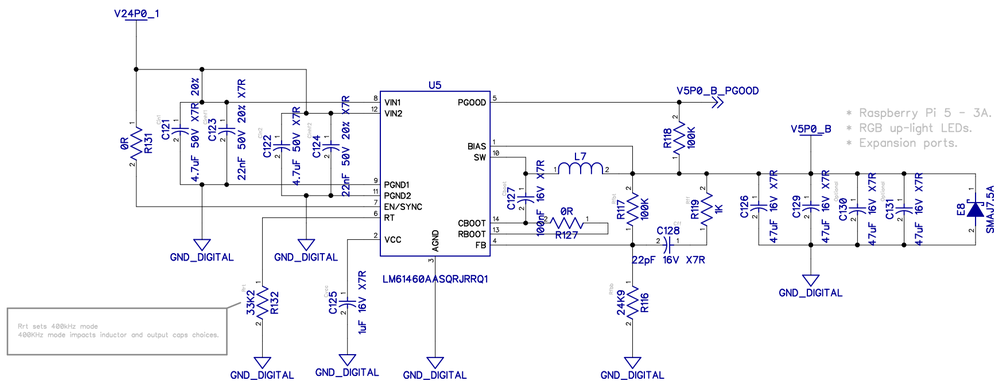
Designed by Dominic Clifton				Edition 0	Sheet 1/1

RevNo	Revision note	Date	Signature	Checked

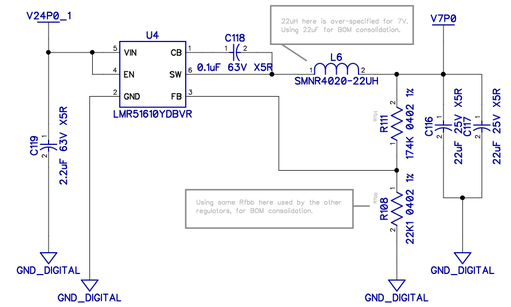
Main 5V power



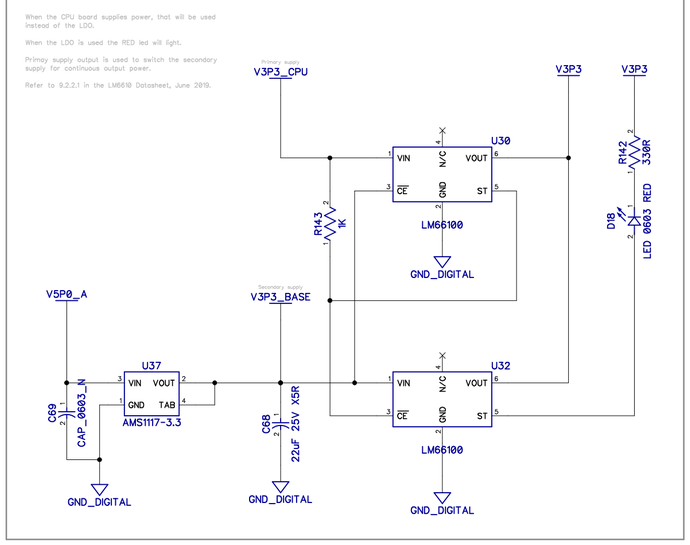
Secondary 5V power

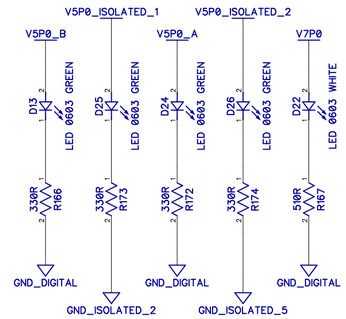


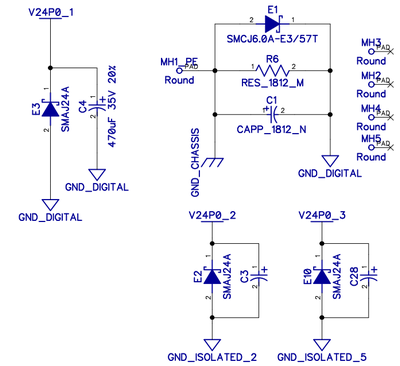
7V supply for the head ~ 1A



3V3 supply + supply ORing with continuous supply output







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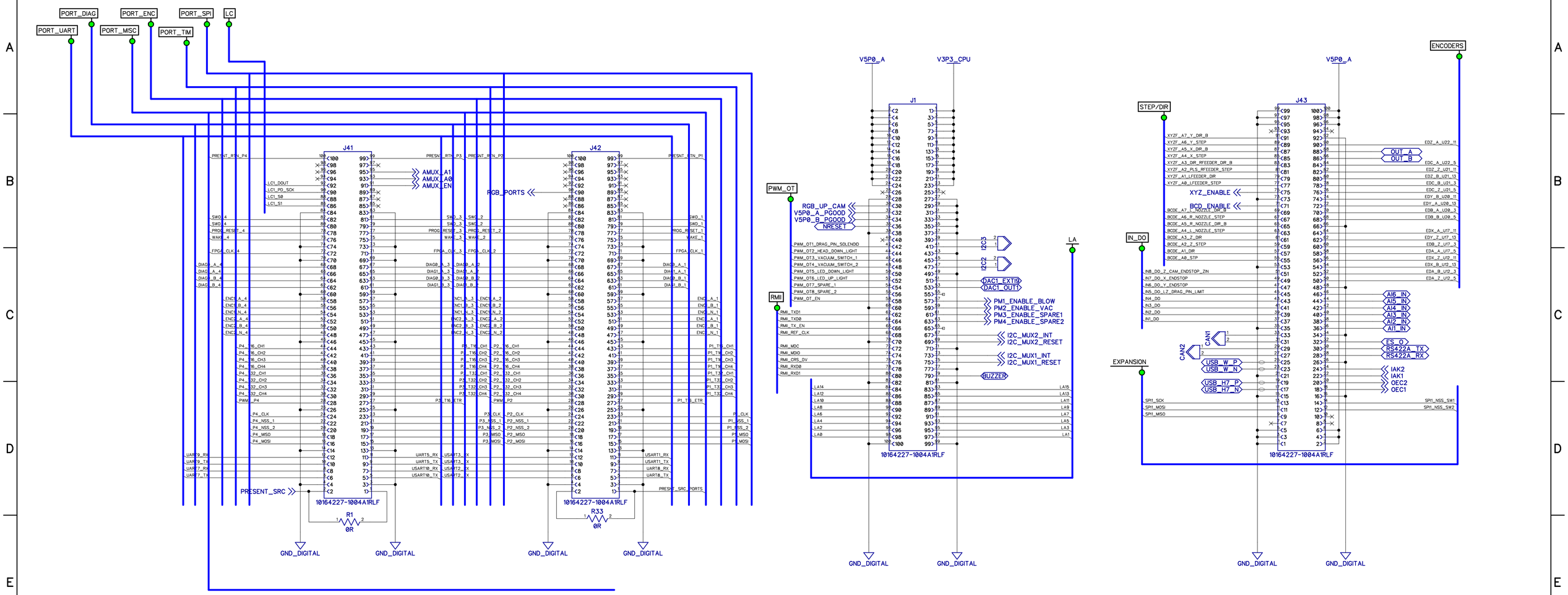

Card detection system

A pull-up to 3v3 is generated on the core board, signal is called PRESENT_SRC.
On the core board, this signal comes in on the left hand connector, pin 2.
The base board then routes this to pin 1 on the same connector.
The core board then routes pin 1 from the left connector to pin 2 on the right connector as PRESENT_THROUGH.
The base board this routes this under the right connector from pin 2 to pin 1.
The base board then routes this same signal from pin 1 on the right connector to each of the ports, as PRESENT_SRC_PORTS (aka PRESENT_BASE_RTN).
The port expansion cards then route the signal back to the FPGA on PRESENT_RTN_P1/2/3/4.

The FPGA then has 5 input pins.
One for pin 1 on right connector.
Then one for each PORT_RTN signal.

The FPGA can then detect correct seating of the core board.
The FPGA can then detect 4 different port expansion card correct seatings.

The pins chosen ensure each connector or expansion
card must be fully seated at both ends of the connector or slot.

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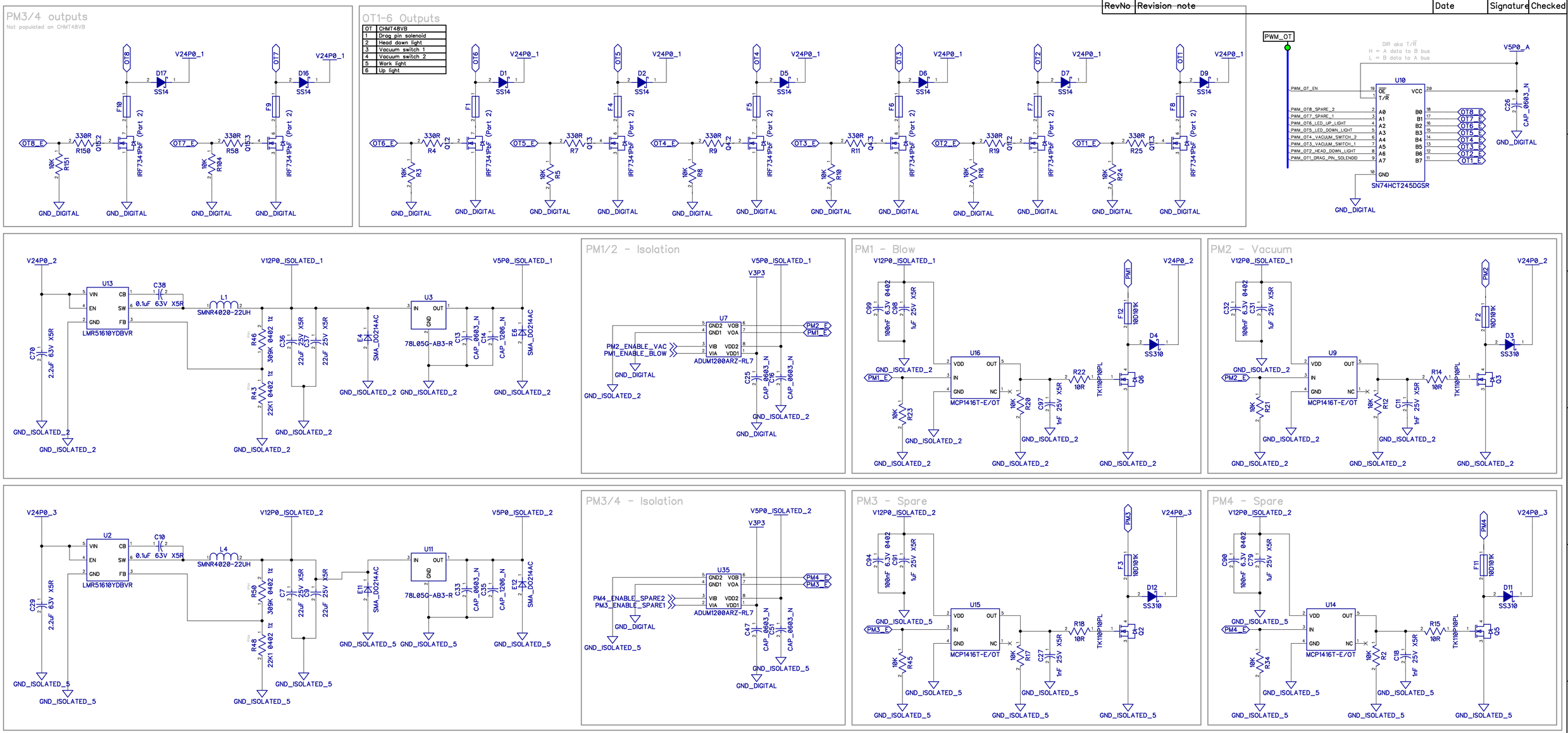

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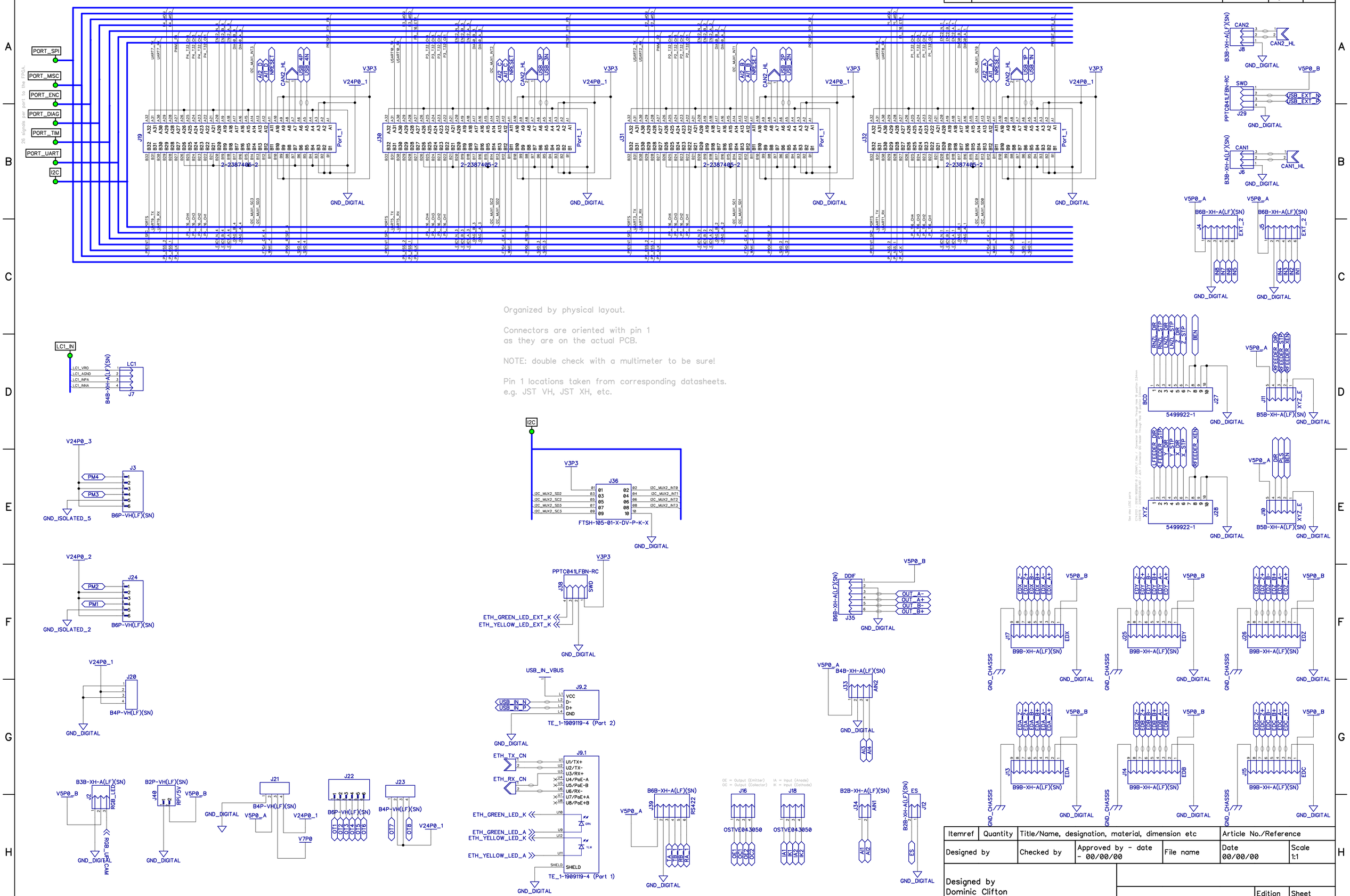

Organized by physical layout.

Connectors are oriented with pin 1
as they are on the actual PCB.

NOTE: double check with a multimeter to be sure!

Pin 1 locations taken from corresponding datasheets.
e.g. JST VH, JST XH, etc.

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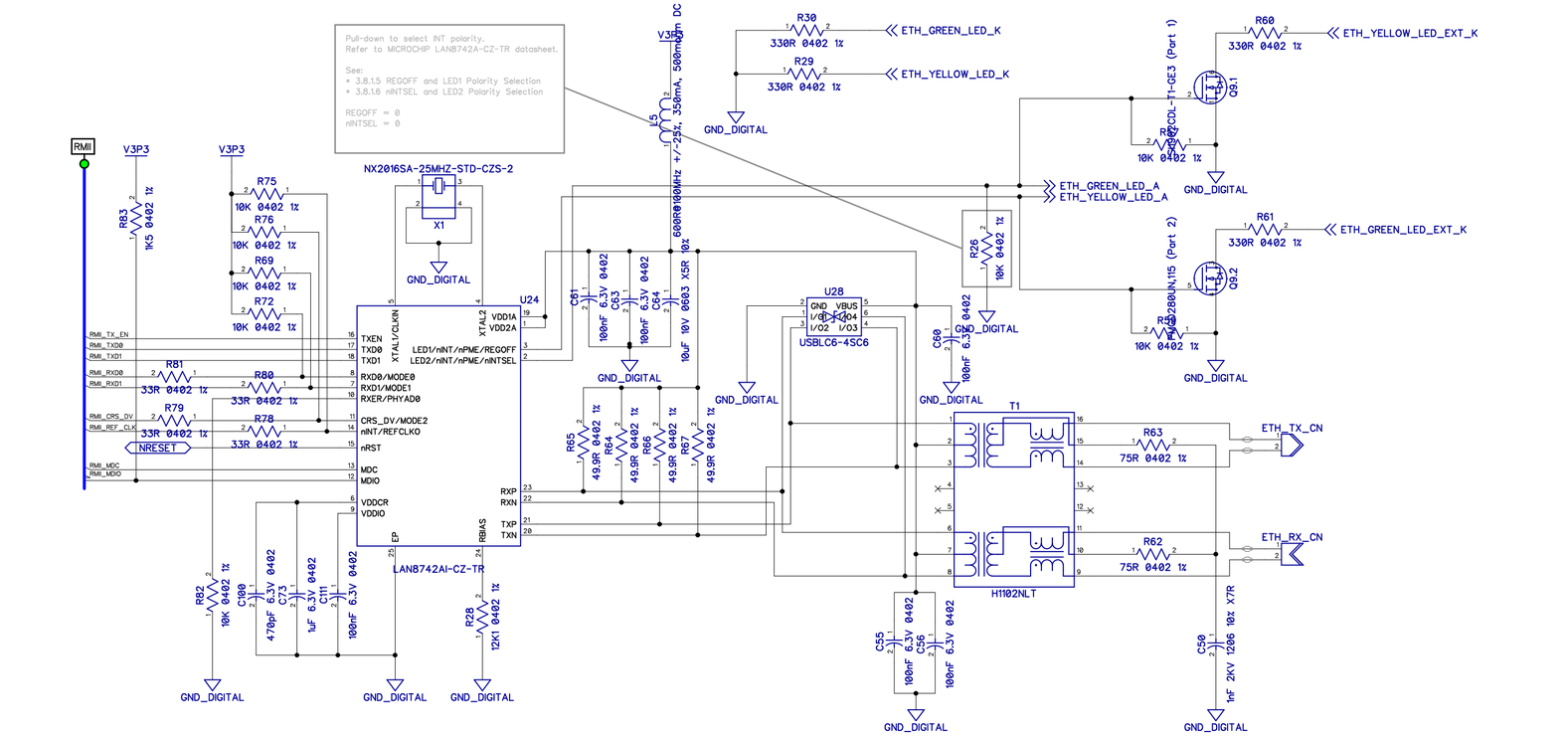
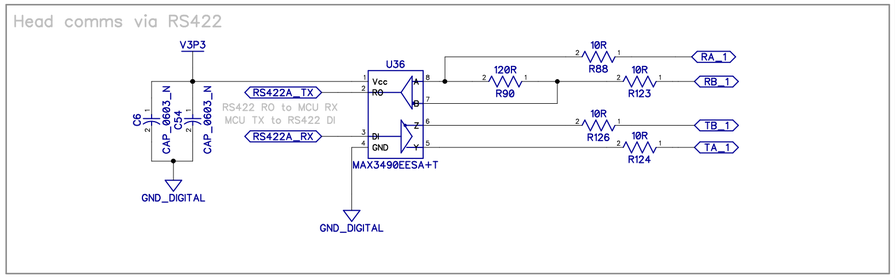
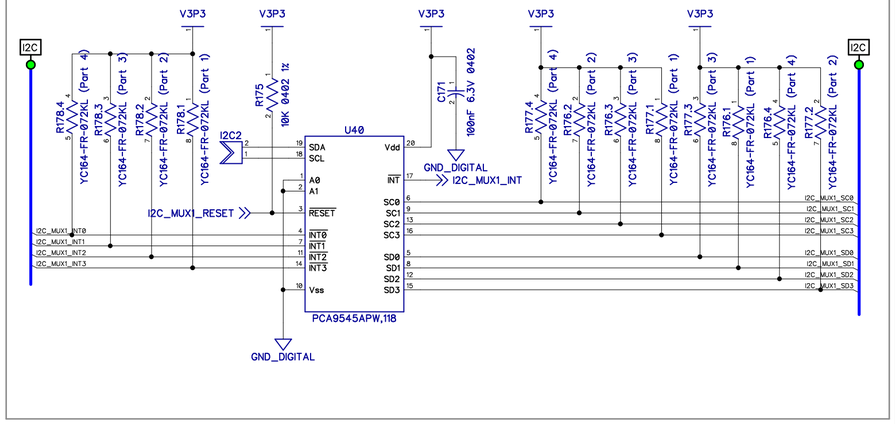


Head comms via RS422



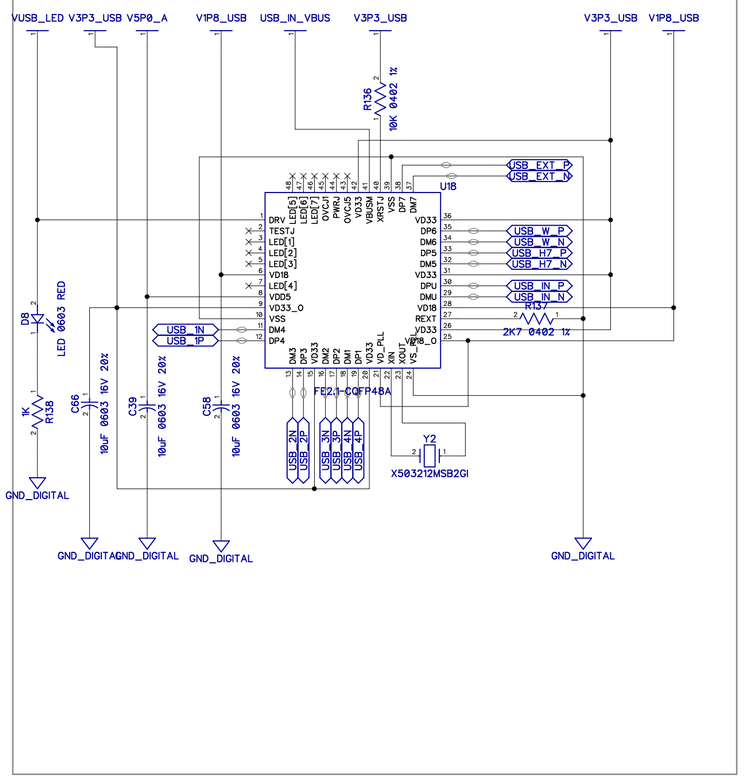
I2C MUX 1 (Ports)



7 Port USB 2 hub.

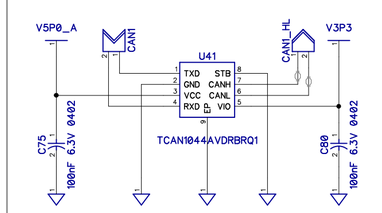
Up-stream port: A PC or SoC (Raspberry Pi)

Downstream ports:
1-4) Ports 1-4
4-7) H7, FPGA, ESP32



FD-CAN1 8Mbps

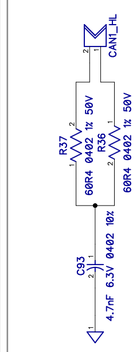
+5V CAN voltage. Always on.



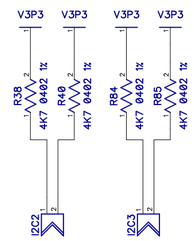
Pin compatible devices, note VIO requirement.

TCAN1044AVDRBRQ1
TCAN1057AVDRBRQ1
MCP2558FDT-H/MF

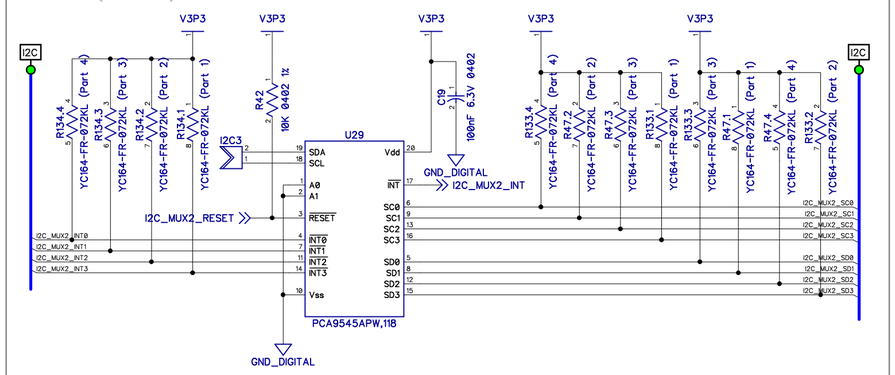
CAN1 termination



I2C Pull-Ups

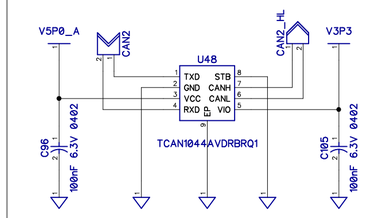


I2C MUX (Sensors)



FD-CAN2 8Mbps

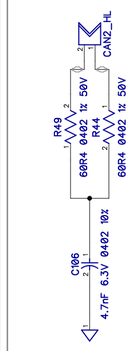
+5V CAN voltage. Always on.



Pin compatible devices, note VIO requirement.

TCAN1044AVDRBRQ1
TCAN1057AVDRBRQ1
MCP2558FDT-H/MF

CAN2 termination



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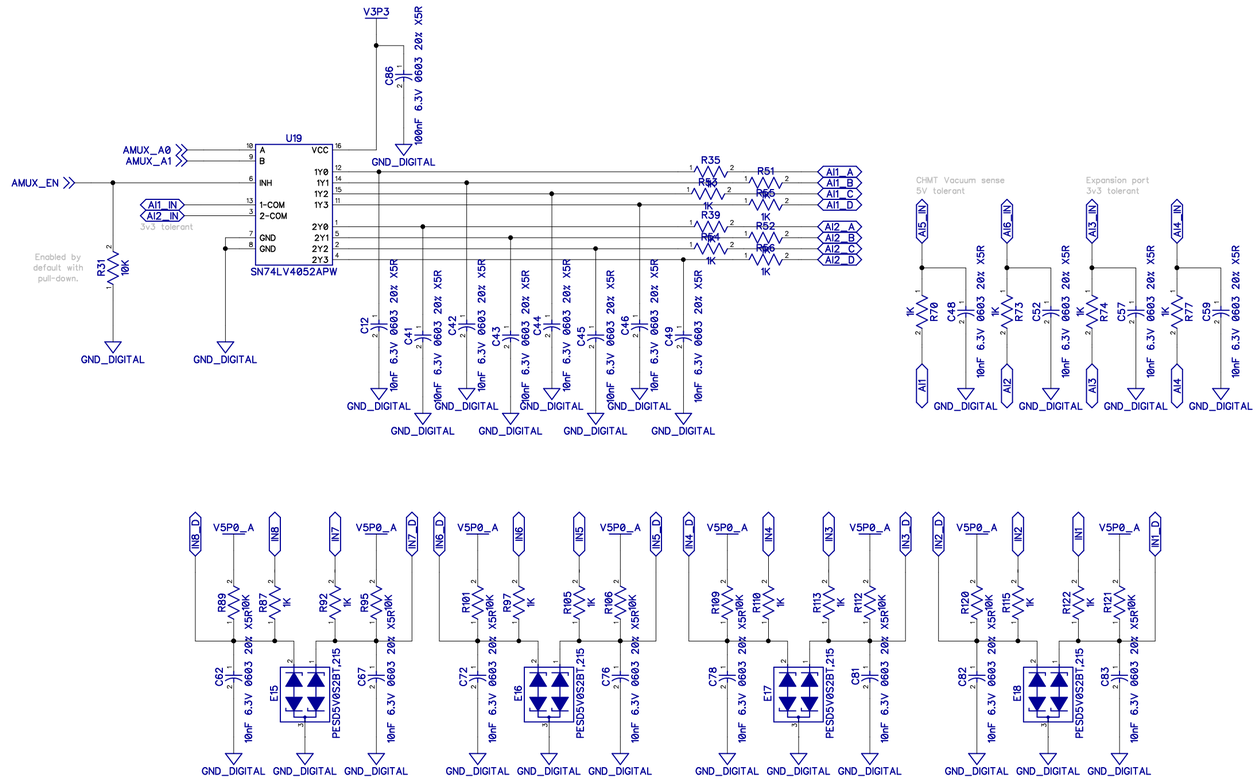

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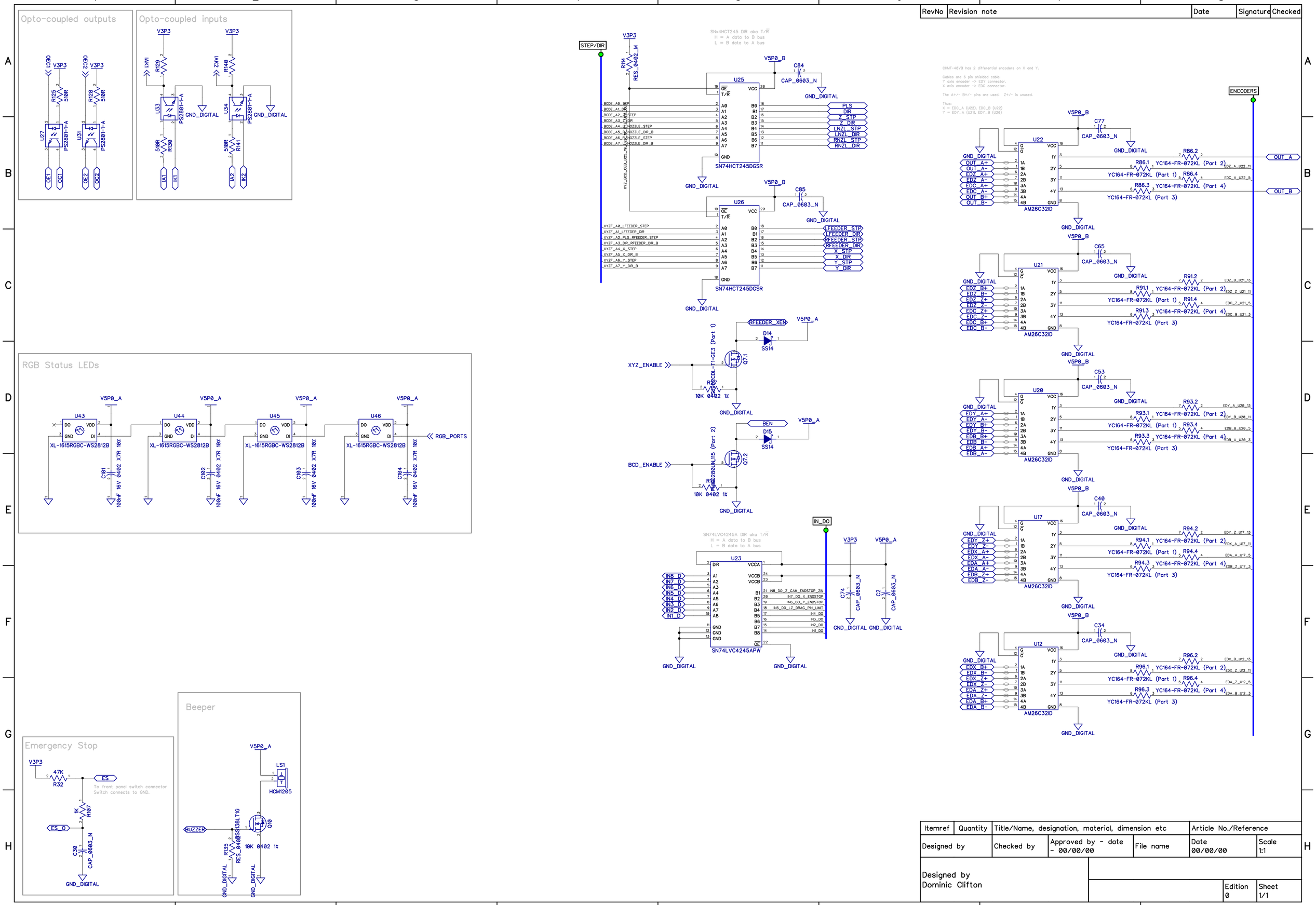

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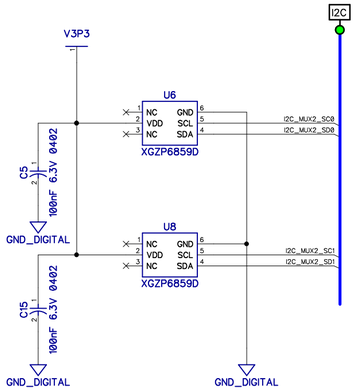

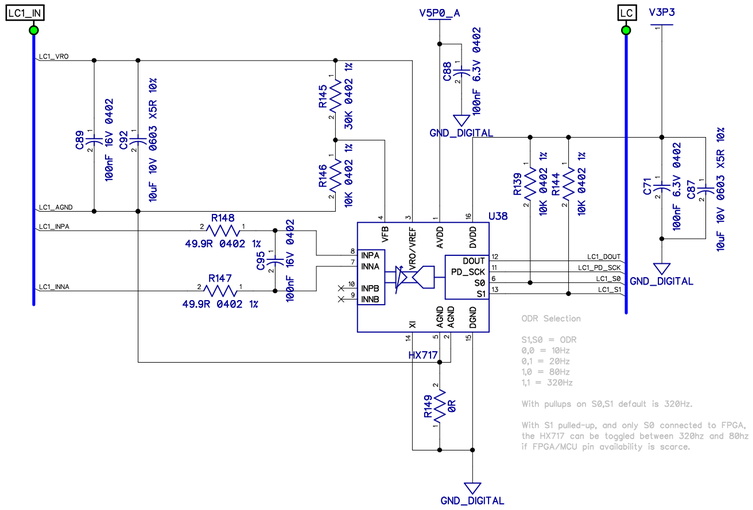

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