Appendix

<filename.v> ⇒ replace this appropriate verilog file name with .v extension
<top module name> ⇒ replace the name with correct top module name
<techfile.lib> ⇒ replace with proper techfile with .lib extension (here skywater tech file **sky130_fd_sc_hd_tt_025C_1v80.lib**)

Commands

#Load modules from a Verilog file to the current design
read_veriloq <filename.v>

#check, expand and clean up design hierarchy(elaborate the design hierarchy)
hierarchy -check -top <top module name>

#Convert "processes" (the internal representation of behavioral Verilog code) into multiplexers and registers.
proc

#Perform some basic optimizations and cleanups
opt

#Analyze and optimize finite state machines.
fsm

#Perform some basic optimizations and cleanups
opt

#Analyze memories and create circuits to implement them
memory

#Perform some basic optimizations and cleanups
opt

#Map coarse-grain RTL cells (adders, etc.) to fine-grain logic gates (AND, OR, NOT, etc.).
techmap

#Perform some basic optimizations and cleanups
opt

#Map registers to available hardware flip-flops from lib
dfflibmap -liberty <techfile.lib>

#Perform some basic optimizations and cleanups
opt

#Map logic to available hardware gates
abc -liberty <techfile.lib>

#remove unused cells and wires
clean

#print some statistics
stat -liberty <techfile.lib>

#write gate level netlist in verilog\
write_verilog <filename.v>

#write the .blif file
write_blif <filename.blif>

#To see the block diagram at any point
show
Or
show <filename>