# TITAN MICRO™ ELECTRONICS 14x4 LCD Driver TM1621D

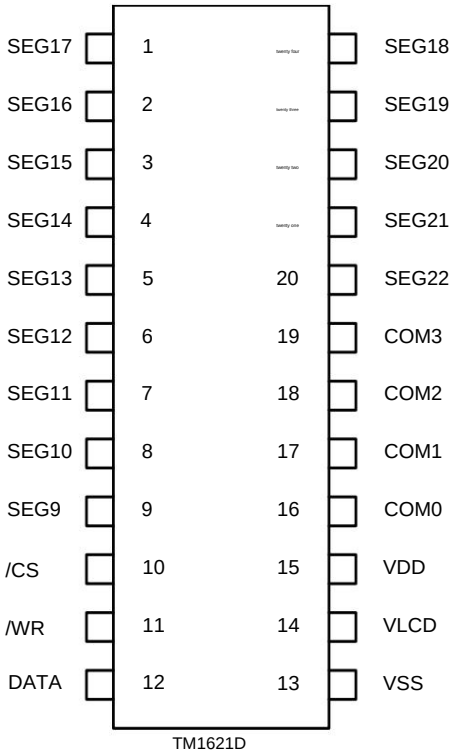
Characteristic description

TM1621D is a 56-point, memory-mapped and multi-functional LCD driver. The software configuration feature of TM1621D makes it suitable for A variety of LCD applications, including LCD modules and display subsystems. The communication sequence between the main controller and TM1621D is simple, and TM1621D also has a power-saving command to reduce system power consumption.

Features ÿ

- Operating voltage 2.4~5.2V ÿ
- Embedded 256KHz RC oscillator ÿ Optional
- 1/2 or 1/3 bias and 1/2, 1/3 or 1/4 duty cycle ÿ On-chip time base frequency
- Sources ÿ Power saving
- commands can be used to reduce power
- consumption ÿ A 14x4 LCD driver ÿ An
- embedded 14x4 bit display RAM memory ÿ Three-wire serial
- interface ÿ On-chip LCD drive
- frequency source ÿ Software configuration
- features ÿ Data mode and
- command mode instructions ÿ Two data access
- modes ÿ Provide VLCD pin for
- adjusting LCD operating voltage ÿ Package type: SOP24

Pin information




TM1621D

Pin Description

| Pin No. | Pin Name | I/O | Functional description |
|---|---|---|---|
| 10 | /CS | I | Chip select input, connected to a pull-up resistor. When /CS is high level, the data and commands written to TM1621D are invalid, and the serial interface circuit is reset; when /CS is low level and used as an input, the data and commands written to |
| 11 | /WR | I | TM1621D are valid WRITE pulse input, connected to a pull-up resistor. On the rising edge of the /WR signal, the data on the DATA line is written to TM1621D. |
| 12 | DATA | I/O | Serial data input/output with external pull-up resistor |
| 13 | VSS | I | Negative power supply, |
| 14 | VLCD | | ground I LCD power input I |
| 15 | VDD | | Positive power supply |
| 16ÿ19 | COM0ÿCOM3 | O | Common output port of LCD |
| 1ÿ9<br>20ÿ24 | SEG9ÿSEG22 | O | LCD segment output port |

In the dry season or in a dry environment, a large amount of static electricity is likely to be generated, and electrostatic discharge may damage the integrated circuit. Tianwei Electronics recommends that all appropriate preventive measures be taken for the integrated circuit. If improper operation and welding may cause ESD damage or Performance drops, chips don't work properly.

Absolute Maximum Ratings Range

| parameter | | scope | unit |
|---|---|---|---|
| VDD logic supply voltage | | VSS-0.3ÿVSS+5.5 | V |
| VIN logic input voltage | | VSS-0.3ÿVDD+0.3 | V |
| Topr operating temperature range | | -25ÿ+75 | ÿ |
| Tstg Storage Temperature Range | | -50ÿ+120 | ÿ |
| ESD | Human Body Model | 4000 | V |
| | (HBM) Machine Model (MM) | 400 | V |

Symbol description of DC

| electrical parameters | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | VDD | condition | | | | |
| VDD operating voltage | | | 2.4 | | 5.2 | V |
| IDD operating current | 3V | On-chip RC | | 150 | 300 | uA |
| | 5V | oscillator without load | | 300 | 600 | uA |
| IDD operating current | 3V | Crystal oscillator without load | | 60 | 120 | uA |
| | 5V | | | 120 | 240 | uA |
| IDD operating current | 3V | External clock | | 100 | 200 | uA |
| | 5V | source without load | | 200 | 400 | uA |
| ISTB standby current | 3V | Power saving | | 0.1 | 5 | uA |
| | 5V | mode without load | | 0.3 | 10 | uA |
| VIL input low level voltage 3V | | DATA,/WR, | 0 | | 0.6 | V |
| | 5V | /CS | 0 | | 1.0 | V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| VIH input high level voltage 3V | | | DATA,/WR, /CS | 2.4 | | 3.0 | V |
| | | 5V | | 4.0 | | 5.0 | V |
| IOL1 DATA | 3V VOL=0.3V | | | 0.5 | 1.2 | | mA |
| | 5V VOL=0.5V | | | 1.3 | 2.6 | | mA |
| IOH1 DATA | 3V VOH=2.7V | | | -0.4 | -0.8 | | mA |
| | 5V VOH=4.5V | | | -0.9 | -1.8 | | mA |
| IOL2 LCD common port leakage current 3V VOL=0.3V 5V | | | | 80 | 150 | | uA |
| | VOL=0.5V | | | 150 | 250 | | uA |
| IOH2 LCD common port source current 3V VOH=2.7V | | | | -80 | -120 | | uA |
| | 5V VOH=4.5V | | | -120 | -200 | | uA |
| IOL3 LCD segment pin leakage current 3V VOL=0.3V | | | | 60 | 120 | | uA |
| | 5V VOL=0.5V | | | 120 | 200 | | uA |
| IOH3 LCD segment pin source current 3V VOH=2.7V | | | | -40 | -70 | | uA |
| | 5V VOH=4.5V | | | -70 | -100 | | uA |
| RPH pull-up resistor | | 3V | DATA,/WR, /CS | 40 | 80 | 150 | Kohm |
| | | 5V | | 30 | 60 | 100 | Kohm |

Symbol description of AC

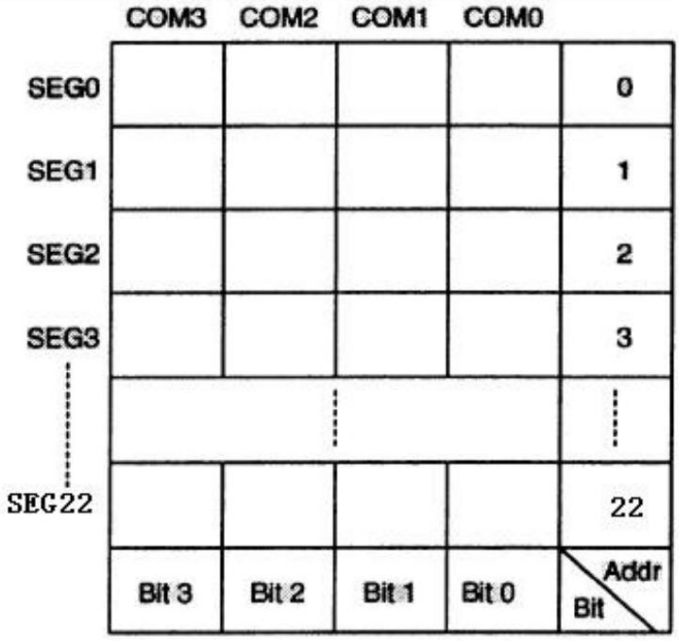
| electrical characteristics | | Test Conditions | | Min Typ Max | | value | unit |
|---|---|---|---|---|---|---|---|
| | | On-chip RC oscillator | | | | | |
| fSYS1 | System Clock 3V | | for VDD condition | | 256 | | KHz |
| | | 5V | | | 256 | | KHz |
| fSYS2 | System Clock 3V | | crystal oscillator | | 32.768 | | KHz |
| | | 5V | | | 32.768 | | KHz |
| fSYS3 | System Clock 3V | | external clock source | | 256 | | KHz |
| | | 5V | | | 256 | | KHz |
| fLCD | LCD clock | | On-chip RC oscillator | | fSYS1/1024 | | Hz |
| | | | crystal oscillator | | fSYS2 /128 | | Hz |
| wxya | COM Clock | | n: Number of COMs | | n/ fLCD | | |
| fCLK | Period Serial Data Clock 3V | | | | | 300 | KHz |
| | | 5V | | | | 500 | KHz |
| TT | DATA pin input 3V | | | | | 2 | us |
| | output delay time 5V | | | | | 1 | us |

System

structure 1. Display memory

(RAM) Static display memory (RAM) stores the displayed data in the format of 23x4 bits, but only SEG9~SEG22

Should the display memory be useful. The data in RAM is directly mapped to the LCD driver.




RAM 映象图

2. System oscillator

TM1621D system clock is used to generate LCD drive clock. On-chip RC oscillator (256KHz) generates the clock source. implement The SYS DIS command can stop the system clock and LCD bias generator. The SYS DIS command is only applicable to the on-chip RC oscillator. When the system clock stops working, the LCD will display blank. The LCD OFF command is used to turn off the LCD bias generator. When the LCD bias generator is turned off, the SYS DIS command can be used to reduce the system power consumption. At this time, SYS DIS is a power-saving command. When the system starts to power on, TM1621D is in SYS DIS state.

3. LCD driver TM1621D

is a 56 (14x4) point LCD driver, which can be configured by software as 1/2 or 1/3 LCD driver bias and 2, 3 or 4 common ports. This feature makes TM1621D suitable for Various LCD applications. The LCD driving clock is generated by frequency division of the system clock, and the frequency value of the LCD driving clock is kept at 256Hz. LCD driver related commands refer to the table below. Name Command Code

| Function Description LCD OFF 10000000010X Turn off LCD output | | |
|---|---|---|
| | | |
| LCD ON 10000000011X Turn on LCD output | | |
| BIAS&COM 1000010abXcX c=0: optional 1/2 bias | | c=1: optional 1/3 bias ab=00: optional 2 common ports<br>ab=01: optional 3 common ports<br>ab=10: optional 4 public ports |

Bold 100 means "100", indicating the command mode type. If consecutive commands are executed, except for the first command, the mode type codes of other commands will be ignored. The LCD OFF command disables the LCD bias voltage generator, thus turning off the LCD display; the LCD ON command enables the LCD bias voltage generator, thereby turning on the LCD display. BIAS&COM is the command related to LCD module, which can make TM1621D compatible with most LCD modules.



4. The command

format of TM1621D can be set by software. The commands of the two modes can configure TM1621D and transmit the data displayed on the LCD. The configuration mode of TM1621D is called command mode, and the type code is 100. The command mode includes a system configuration command, a system frequency selection command, an LCD configuration command and an operation command. The following table is the data and command mode type code table.

| Operation Mode | Type Code |
|---|---|
| WRITE data | 101 |
| COMMAND command | 100 |

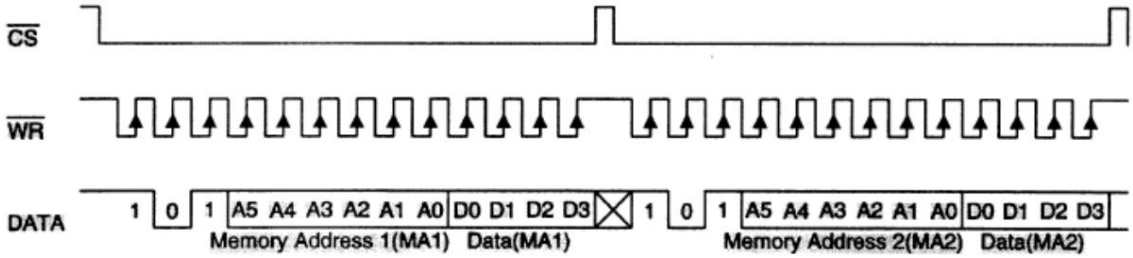
The mode command should be run before the data or command is transmitted, if the continuous command is executed, the command mode code is 100, which will be ignored. When the system is in discontinuous command mode or discontinuous address data mode, the pin /CS should be set to "1", and the previous operating mode will be reset. When pin /CS returns "0", the new operation mode type code should run first.

5. Interface

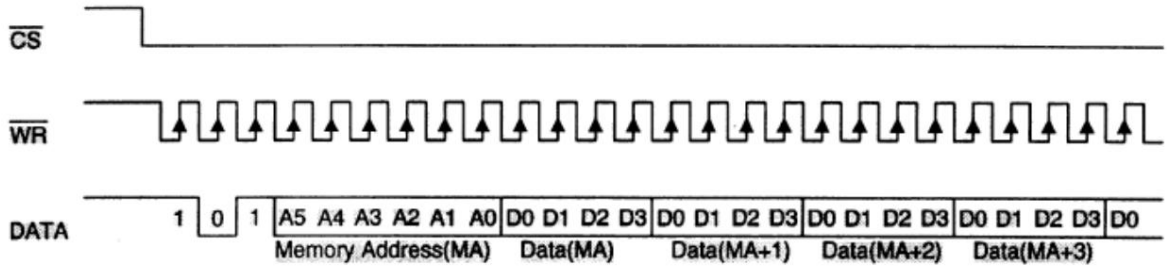
TM1621D only has three pins for interface. The pin /CS is used to initialize the serial interface circuit and end the communication between the main controller and TM1621D. When the pin /CS is set to "1", the data and commands between the main controller and TM1621D are invalid and initialized. Before generating mode command or mode conversion, the serial interface of TM1621D must be initialized with a high level pulse. The pin DATA is a serial data input/output pin, and read/ write data and write commands are performed through the pin DATA. The pin /WR is the write clock input pin, and the data, address and command on the pin DATA are written into TM1621D at the rising edge of the /WR signal.

6. Timing diagram

WRITE mode (command code 101)



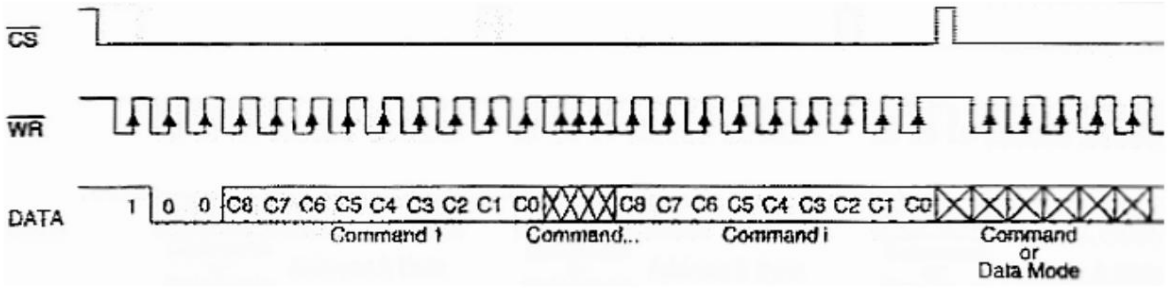

WRITE mode (write consecutive addresses)





command mode (command code 100)




Command

| Overview Command Name | Command Code | D/C function description | Reset default on power-up |
|---|---|---|---|
| WRITE | 101 a5a4a3a2a1a0d0d1d2d3 | D write data to RAM | |
| SYS DIS | 10000000000X | C Turn off the system oscillator and LCD bias generator | Y |
| SYS EN | 10000000001X | C Turn on the system oscillator | |
| LCD OFF | 10000000010X | C Turn off the LCD bias generator | Y |
| LCD ON | 10000000011X | C Turn on the LCD bias generator | |
| XTAL 32K | 100000101XXX | C system clock source crystal oscillator | |
| RC 256K | 100000110XXX | C System clock source On-chip RC oscillator Y | |
| BIAS1/2 | 1000010abX0X | C LCD 1/2 bias option ab=00: 2 common ports ab=01: 3 common ports ab=10: 4 common ports | |
| BIAS 1/3 | 1000010abX1X | C LCD 1/3 bias option ab=00: 2 common ports ab=01: 3 common ports ab=10: 4 common ports | |
| TOPT | 10011100000X | C test mode | |
| NORMAL | 10011100011X | C Norma mode Note: | Y |

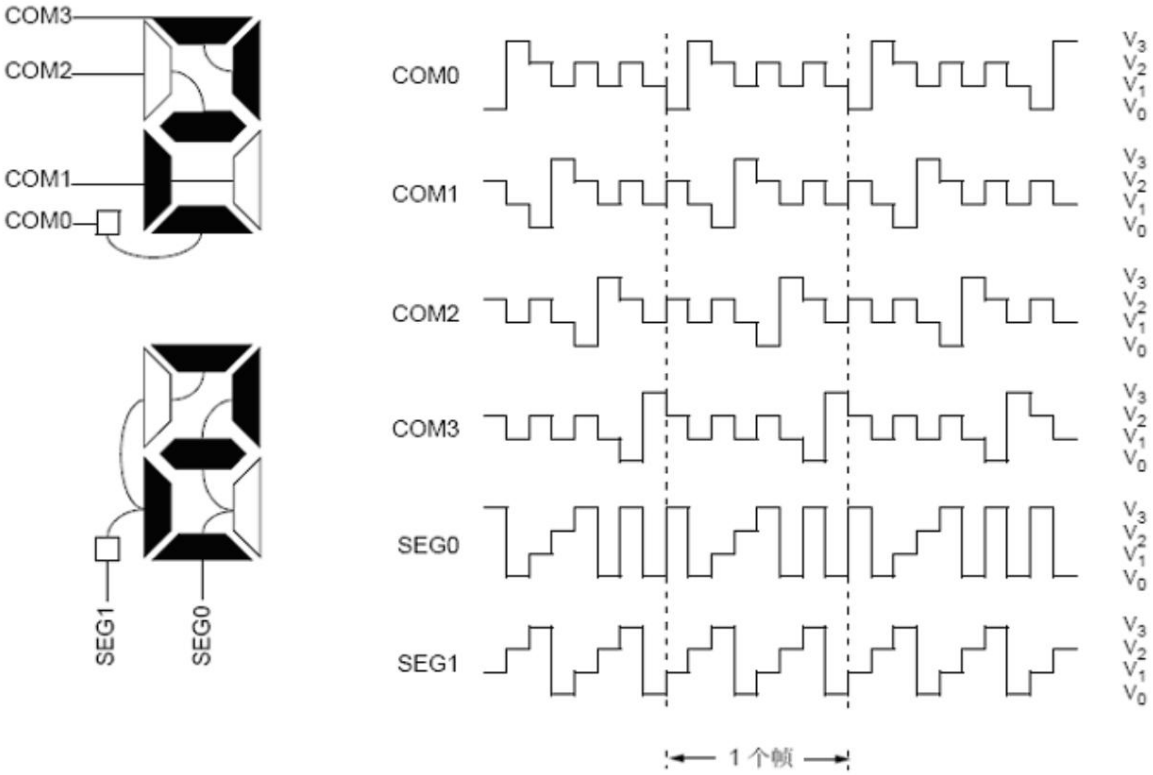
X: 0 or 1; a5~a0: RAM address; d3~d0: RAM data

All bold numbers in D/C data/

command mode, ie 101 and 100, are mode command codes. 100 is the command mode type code. If you run consecutive commands, except the first command, the mode type codes of other commands will be ignored. It is recommended to initialize TM1621D with the main controller after power-on reset, because if power-on reset fails, TM1621D will not work normally.

The pin driving waveform

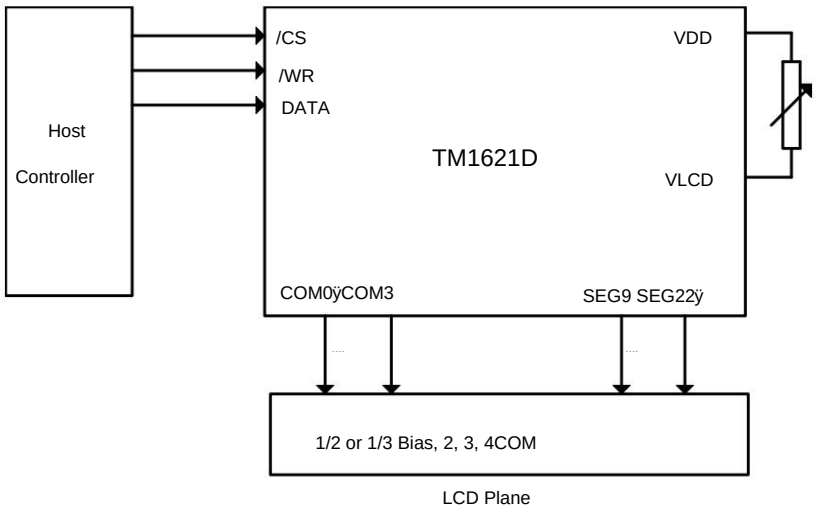
shows the waveform showing "2" under 1/3 bias driving using 1/4 multiplexing:




V3=VDD (VDD is LCD supply voltage)
V2=2/3VDD
V1=1/3VDD
V0=0

Peripheral Application Block

Diagram The main controller and TM1621D form a display system, see the figure below.



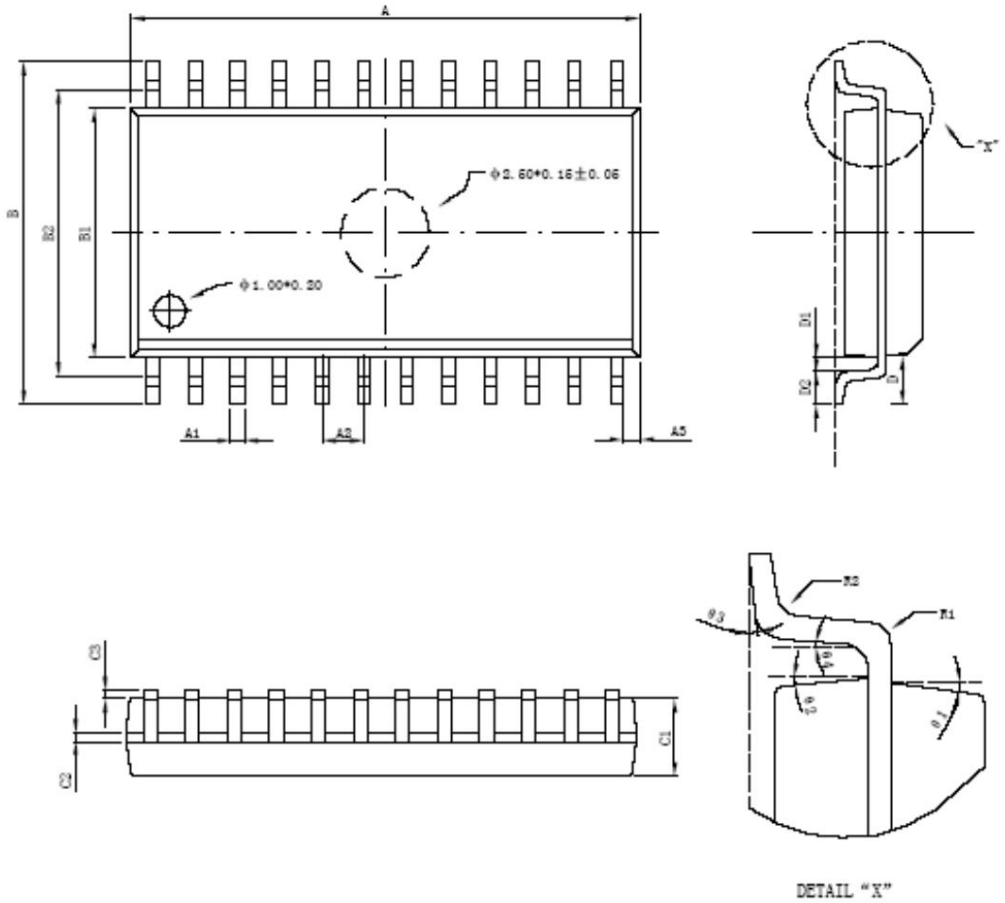
Note: 1. The voltage of the VLCD pin must be lower than the voltage of the VDD pin;

2. The VR resistor is used to adjust the display grayscale of the LCD screen. When VDD=5V and VLCD=4V, VR is generally selected as 15Kÿ (± 20%).

Package Outline Drawing

SOP24

| 尺寸 / 标注 | 最 小（mm） | 最 大（mm） | 尺寸 / 标注 | 最 小（mm） | 最 大（mm） |
|---|---|---|---|---|---|
| A | 15.28 | 15.48 | C4 | 0.86TYP | |
| A1 | 0.406TYP | | D | 1.34TYP | |
| A2 | 1.27TYP | | D1 | 0.33TYP | |
| A3 | 0.50TYP | | D2 | 0.70 | 0.90 |
| B | 9.90 | 10.50 | R1 | 0.25TYP | |
| B1 | 7.42 | 7.62 | R2 | 0.25TYP | |
| B2 | 8.7TYP | | θ1 | 7° TYP | |
| C1 | 2.13 | 2.23 | θ2 | 7° TYP | |
| C2 | 0.204 | 0.33 | θ3 | 4° TYP | |
| C3 | 0.10 | 0.25 | θ4 | 10° TYP | |



revision

| history | issue date | Release of the official |
|---|---|---|
| V1.0 | 2012-03-20 | version of the revised introduction |
| | | |
| | | |