Nucleo144 H7 SMPS with STLINK V3

MB1363

H755ZIQ

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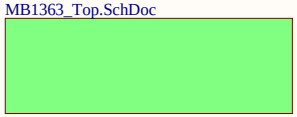
Sheet 9: ST-LINK V3E SWD

U_MB1363_Top
MB1363_Top.SchDoc



Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

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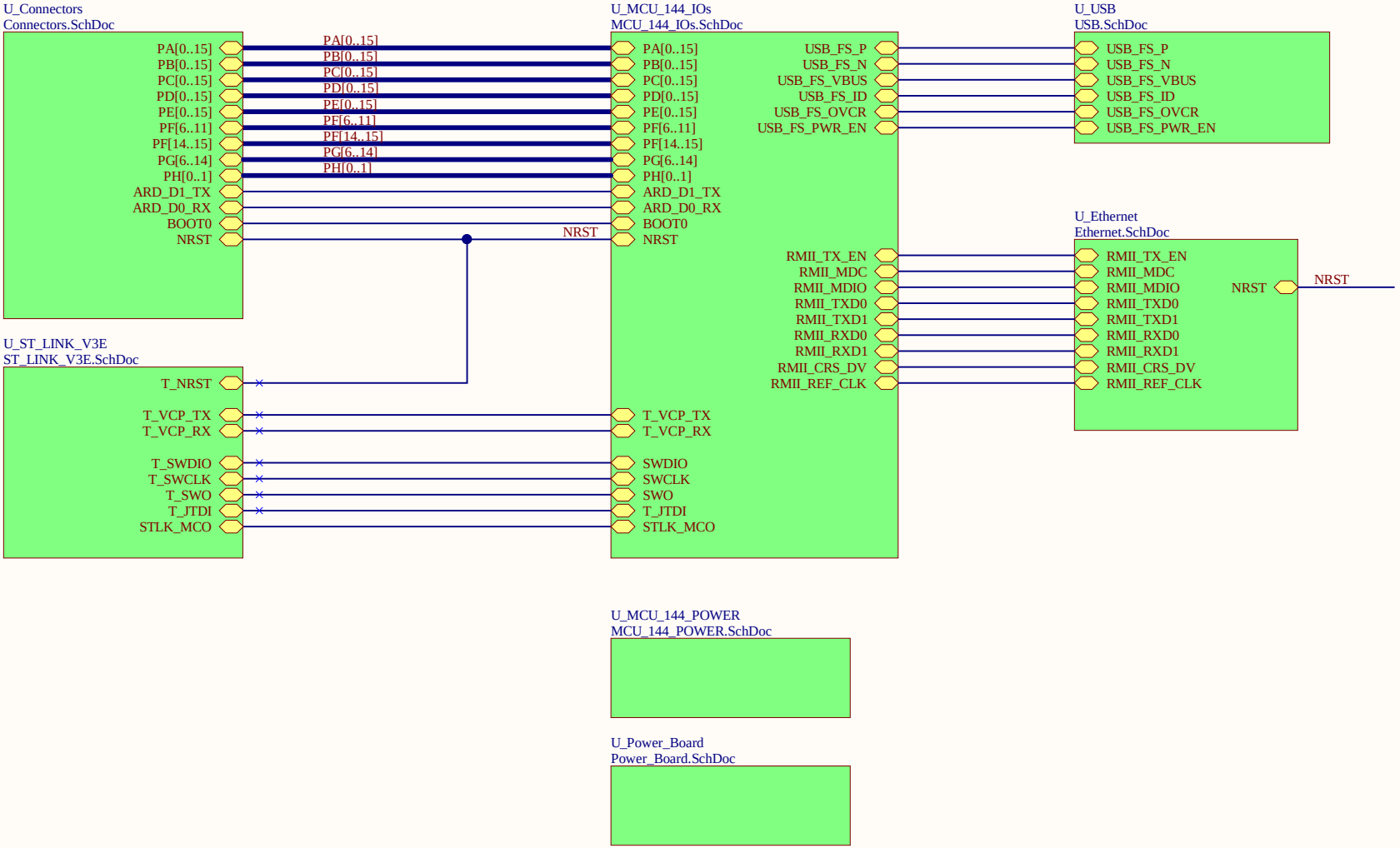
Title: **Project overview**		
Project: **Nucleo144 H7 SMPS with STLINK V3**		
Variant: H755ZIQ		
Revision: D-01		Reference: MB1363
Size: A4	Date: 09-OCT-19	Sheet: 1 of 9

life.augmented



Title: **MB1363 Top: hierarchical view**		
Project: **Nucleo144 H7 SMPS with STLINK V3**		
Variant: H755ZIQ		
Revision: D-01		Reference: MB1363
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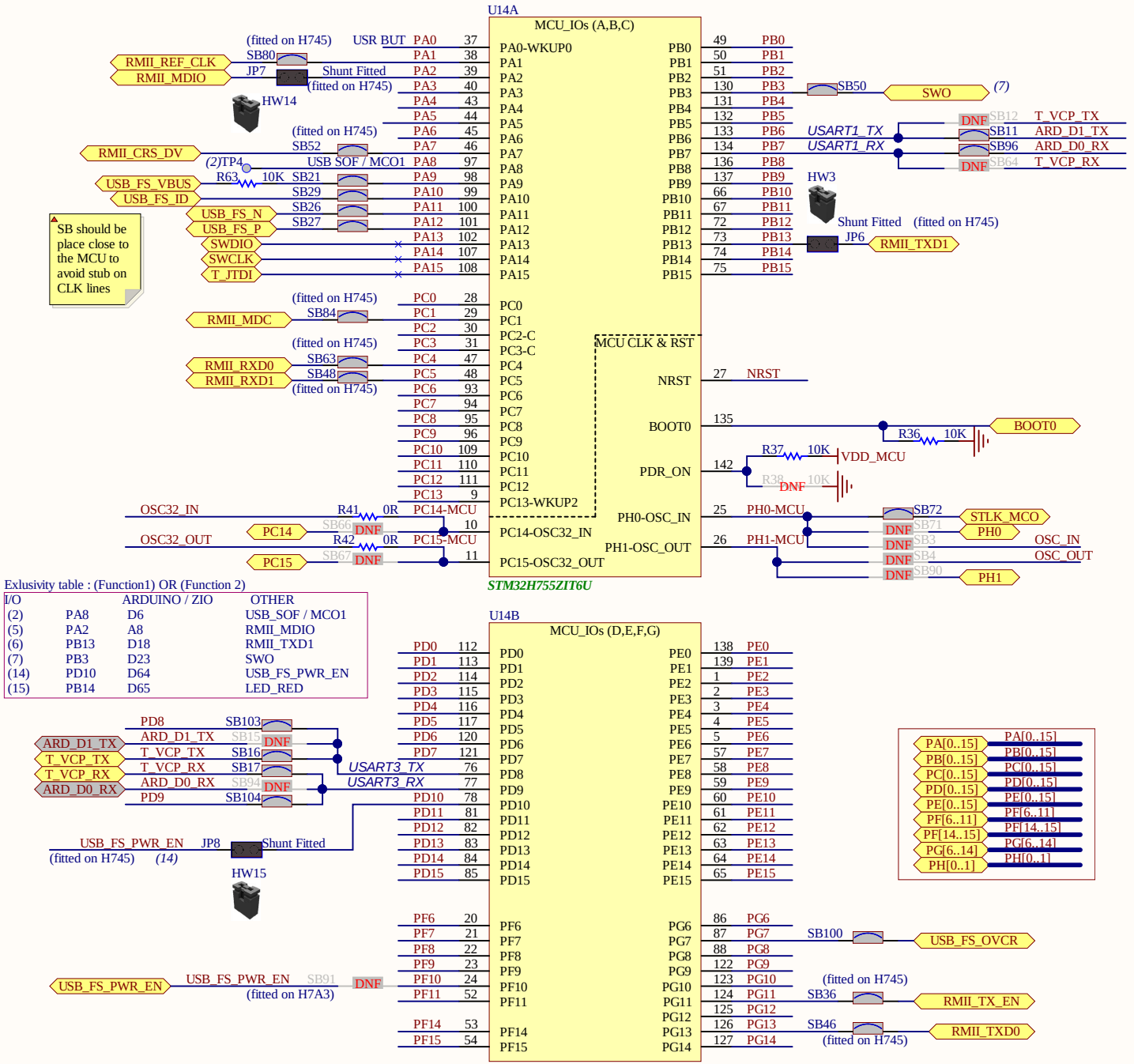
MCU IO CLK and RST



Exlusivity table : (Function1) OR (Function 2)

I/O	ARDUINO / ZIO	OTHER
(2)	PA8	D6	USB_SOF / MCO1
(5)	PA2	A8	RMII_MDIO
(6)	PB13	D18	RMII_TXD1
(7)	PB3	D23	SWO
(14)	PD10	D64	USB_FS_PWR_EN
(15)	PB14	D65	LED_RED

Title:	**MCU 144 I/Os**	
Project:	**Nucleo144 H7 SMPS with STLINK V3**	
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MCU PWR SUPPLIES

IDD Measurement
VDD — IDD — JP4 — VDD_MCU
Shunt Fitted
HW12

U14C
MCU_PWR

VDD_MCU	71	VDD_1	
	106	VDD_2	
	13	VDD_3	
	19	VDD_4	
	32	VDD_5	
	42	VDD_7	
	56	VDD_10	
	79	VDD_15	
	129	VDD_27	
	144	VDD_29	
	92	VDD_30	
	7	VDD_33	
		VSS_1	69
		VSS_2	104
		VSS_3	12
		VSS_4	18
		VSS_5	33
		VSS_7	41
		VSS_10	55
		VSS_13	141
		VSS_15	80
		VSS_24	118
		VSS_27	128
		VSS_30	89
		VSS_33	6
VDD_SMPS_IN	16	VDDSD	
VDD_SMPS_OUT	15	VLXSD	
VFBSD	17	VFBSD	
		VSSSD	14
VCAP	68	VCAP1	
	103	VCAP2	
	140	VCAP3	
VDD_LDO	70	VDDLDO_1	
	105	VDDLDO_2	
	143	VDDLDO_3	
3V3 — SB18	90	VDD50_USB	
3V3 — SB19	91	VDD33_USB_1	
VDD_MCU — SB32	119	VDD_MMC_1	
		VSSA	34
	36	VDDA	
VREFP	35	VREFP	
VDD_MCU — SB83	8	VBAT	

STM32H755ZIT6U

VDD_MCU — R40 0R — VDDA
DNF C62 100nF
DNF C61 100nF
R39 0R
VDD_MCU — SB32
VREFP
VDD_MCU — SB83 — VBAT
SB68
AGND

SMPS MCU Supply Config

Supply Config 1 : LDO only (SMPS OFF, LDO ON)

Disconnect 3V3_SMPS_IN from 3V3_MCU
Connect 3V3_SMPS_IN to GND
Connect VDD_SMPS_IND_OUT to GND
Connect VDD_LDO to 3V3_MCU
2 x 2.2uF near VCAP plans/pins

VDD_MCU — SB25 DNF — VDD_LDO
VFBSD — R33 DNF 0R
VDD_SMPS_IN — SB74 DNF
2x2.2uF instead of 2x100nF near VCAP pins / plan

Supply Config 2 : Internal SMPS only (SMPS ON, LDO OFF)

Default config

Connect VDD_SMPS_IN to VDD_MCU
Connect VDD_SMPS_IND_OUT to VCAP1/2/3

VCAP — R35 0R — VFBSD
VDD_MCU — SB92 — VDD_SMPS_IN
Cin near VDDSD pin
Cin — C68 10uF — C65 10uF — VSSSD
VDD_SMPS_OUT — L1 2.2uH, 1.2A L — VDD_SMPS_IND_OUT
C64 220pF Cfilt
Cfilt & L near VLXSD
C75 10uF Cout
COUT near L
SB79
1V2_MCU — SB75 — VCAP
near VCAP pins / plan
C58 100nF — C54 100nF
1V2_MCU — SB76 — VDD_LDO

Supply Config 3 : SMPS & LDO cascaded (SMPS & LDO ON)

Compared to config 2 :
Disconnect VDD_SMPS_IND_OUT from VCAP
Connect VDD_SMPS_IND_OUT to VDD_LDO
Add 2x100nF near VDDLDO pins/plans
Add 2x2.2uF near VCAP pins/plans (see config 1)

VDD_LDO — R34 DNF 0R — VFBSD
VDD_LDO — C51 100nF — C53 100nF
2x100nF near VDDLDO pins / plan

Supply Config 5 : external SMPS

Disconnect 1V2_MCU from VDD_SMPS_IND_OUT
Connect 1V2_MCU to 1V2_VOUTCORE (Connectors page)

MCU DECAPS

Ceramic capacitor (Low ESR, ESR<1ohm)

capa near balls

VDD_MCU — C67 4.7uF C0603 — C59 100nF — C52 100nF — C55 100nF — C49 100nF — C47 100nF — C46 100nF — C56 100nF — C57 100nF — C50 100nF — C48 100nF
VBAT — C63 1uF
VDDA — C72 1uF — C73 100nF — AGND
VREFP — C69 1uF — C71 100nF — AGND
SB61 — AGND

Title:	**MCU 144 POWER**		
Project:	**Nucleo144 H7 SMPS with STLINK V3**		
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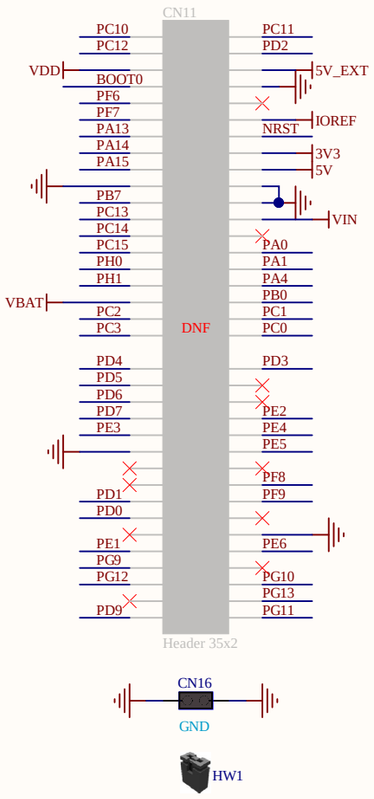
EXTENSION CONNECTORS, MCU INTERFACES

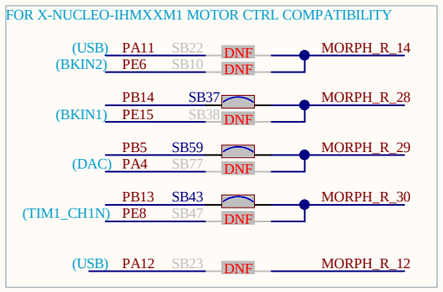
MORPHO CONNECTOR LEFT SIDE

Put the IO in BOTTOM side



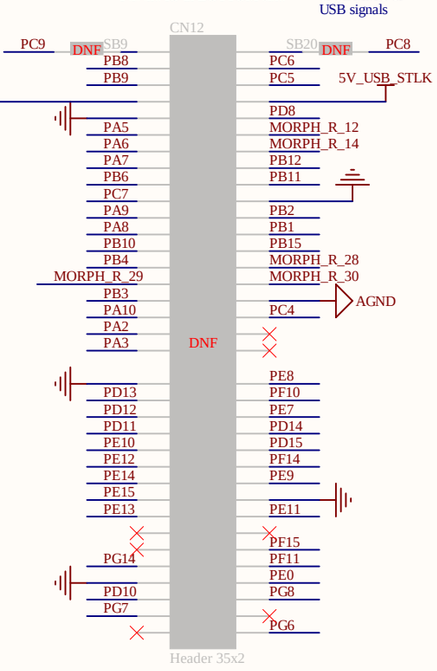
MORPHO CONNECTOR RIGHT SIDE

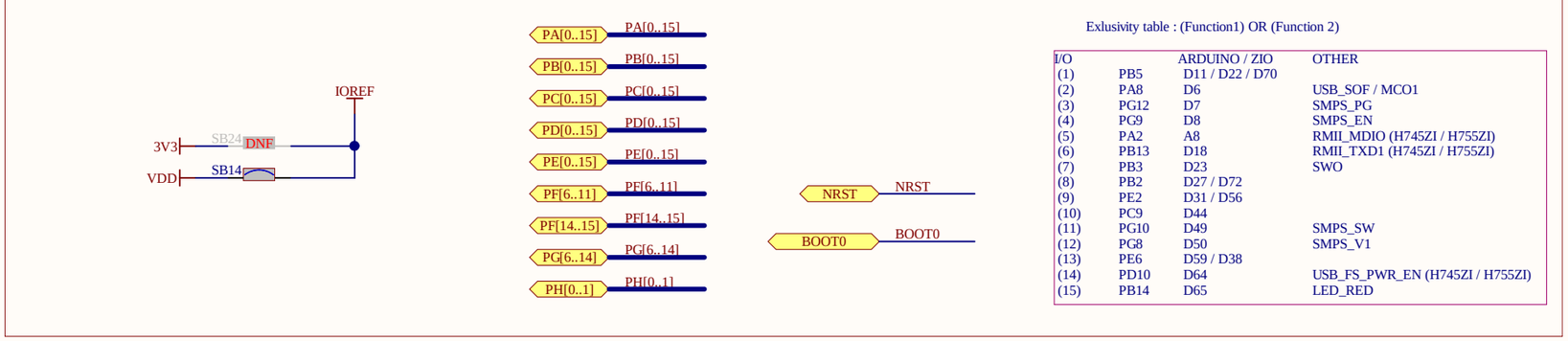
FOR X-NUCLEO-IHMXXM1 MOTOR CTRL COMPATIBILITY



Put the IO in BOTTOM side

SBxx to avoid stub of SDMMC & USB signals

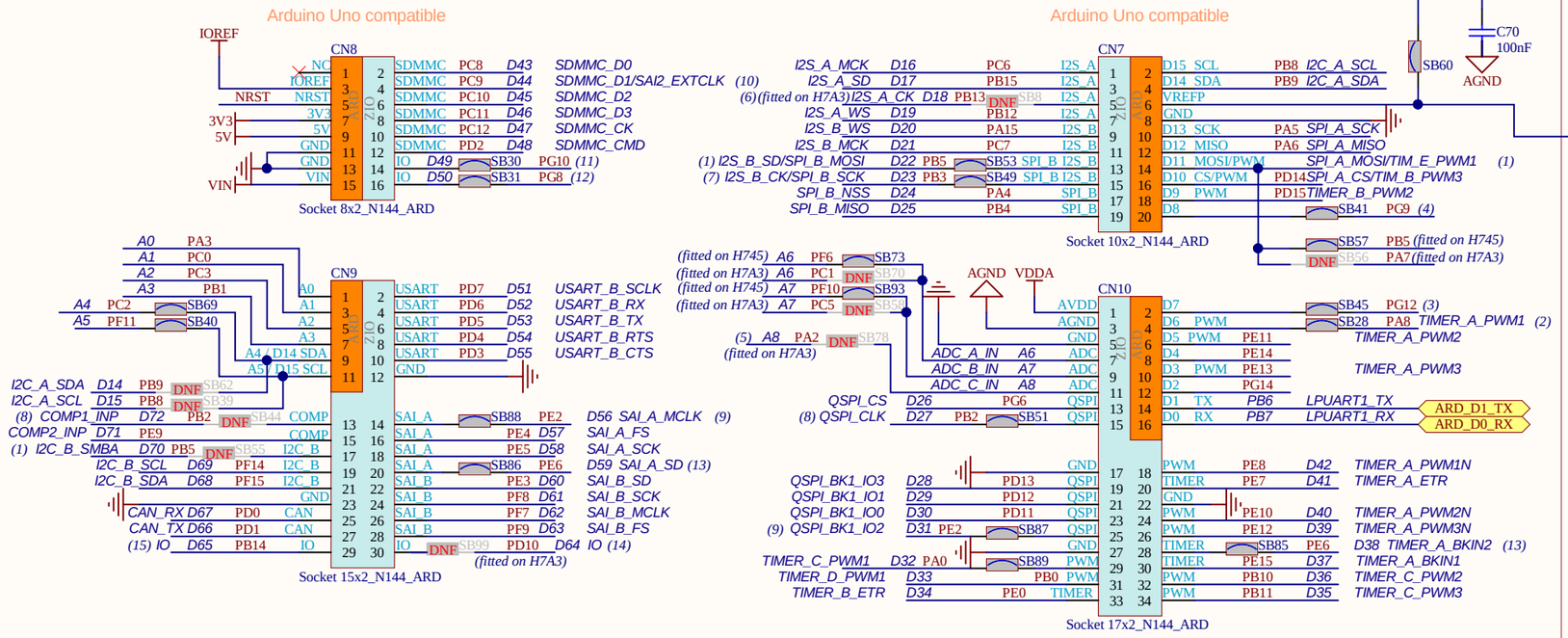




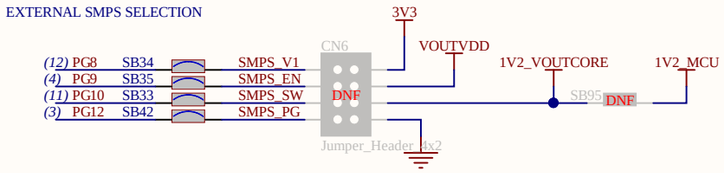
Exclusivity table : (Function1) OR (Function 2)

I/O		ARDUINO / ZIO	OTHER
(1)	PB5	D11 / D22 / D70	
(2)	PA8	D6	USB_SOF / MCO1
(3)	PG12	D7	SMPS_PG
(4)	PG9	D8	SMPS_EN
(5)	PA2	A8	RMII_MDIO (H745ZI / H755ZI)
(6)	PB13	D18	RMII_TXD1 (H745ZI / H755ZI)
(7)	PB3	D23	SWO
(8)	PB2	D27 / D72	
(9)	PE2	D31 / D56	
(10)	PC9	D44	
(11)	PG10	D49	SMPS_SW
(12)	PG8	D50	SMPS_V1
(13)	PE6	D59 / D38	
(14)	PD10	D64	USB_FS_PWR_EN (H745ZI / H755ZI)
(15)	PB14	D65	LED_RED

ZIO CONNECTOR ARDUINO UNO COMPATIBLE

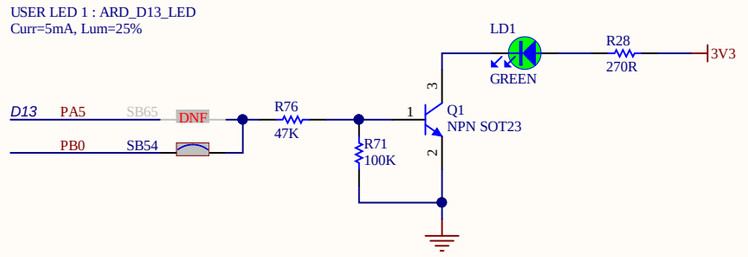


EXTERNAL SMPS SELECTION



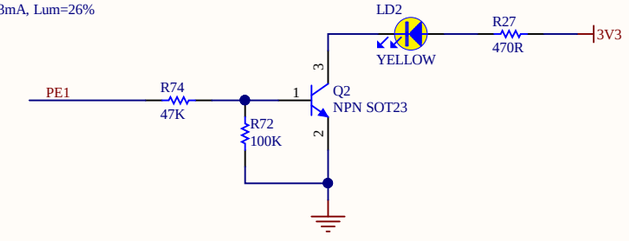
USER LED 1 : ARD_D13_LED

Curr=5mA, Lum=25%



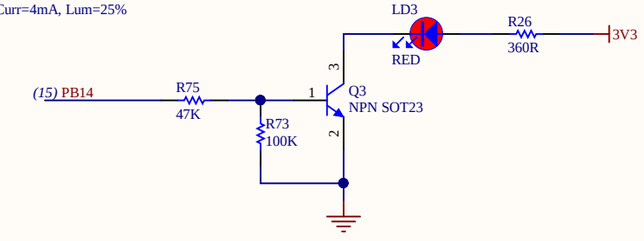
USER LED 2

Curr=3mA, Lum=26%



USER LED 3

Curr=4mA, Lum=25%



Title: **Connectors**			
Project: **Nucleo144 H7 SMPS with STLINK V3**			
Variant: H755ZIQ			
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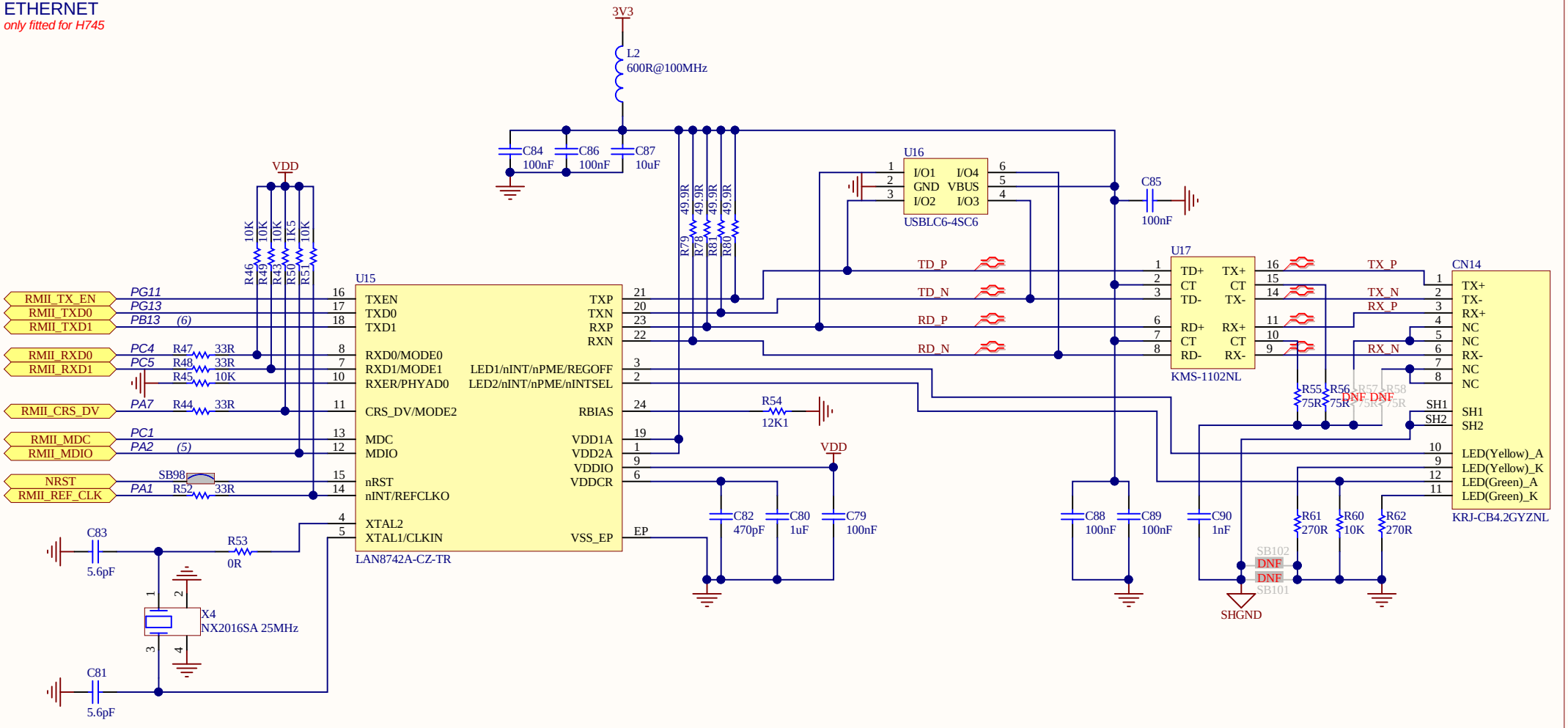
ETHERNET

only fitted for H745



Title: **Ethernet PHY with RJ45 connector**		
Project: **Nucleo144 H7 SMPS with STLINK V3**		
Variant: H755ZIQ		
Revision: D-01		Reference: MB1363
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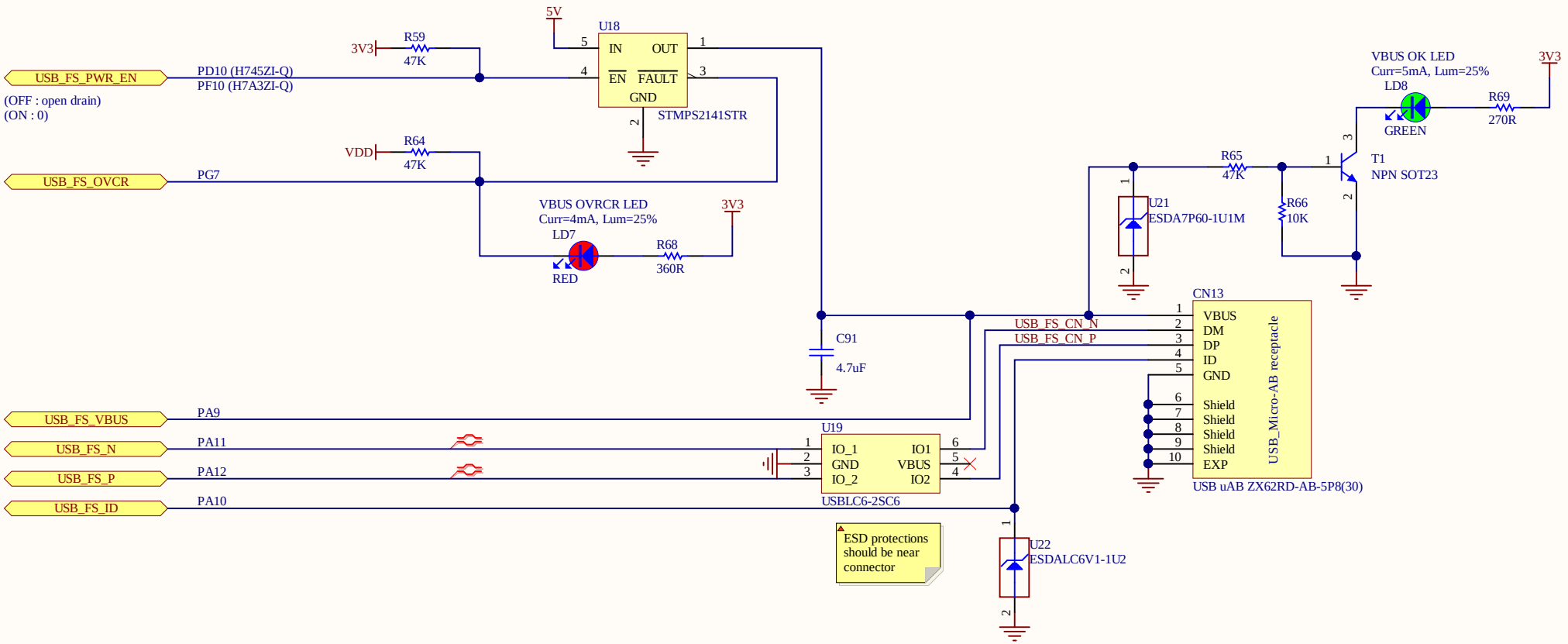
USB FS



Title: **USB**		
Project: **Nucleo144 H7 SMPS with STLINK V3**		
Variant: H755ZIQ		
Revision: D-01		Reference: MB1363
Size: A4	Date: 09-OCT-19	Sheet: 7 of 9

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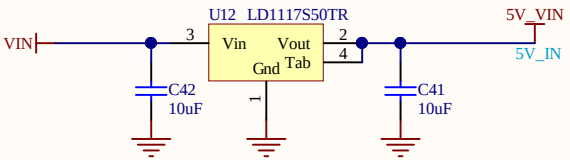
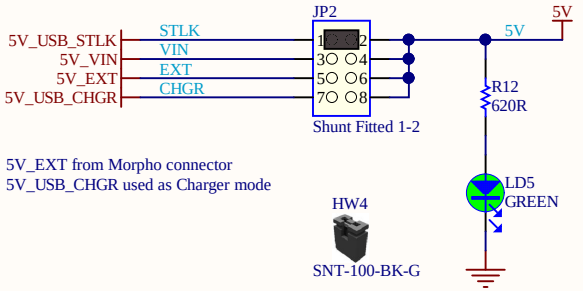
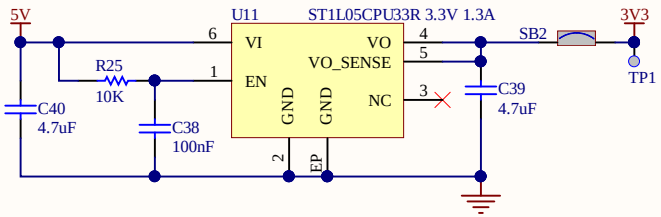
VIN / 5V PWR



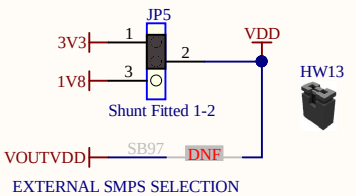
5V PWR SELECTION



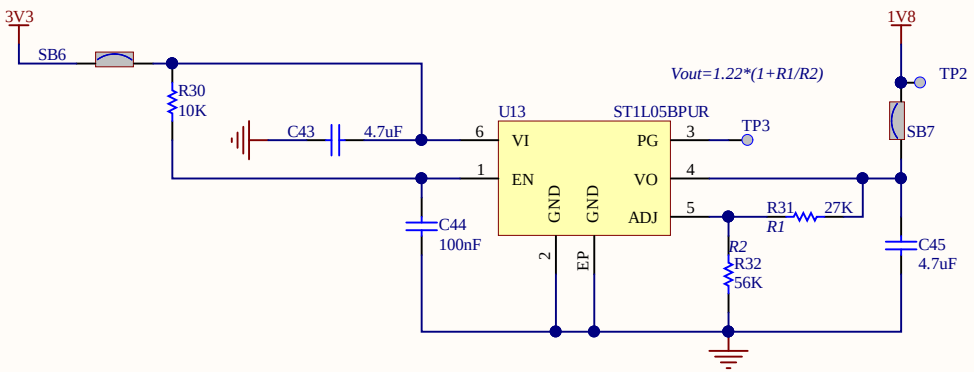
3V3 PWR



3V3/1V8 SELECTION



1V8 PWR



Title: **MAIN POWER 5V / 3V3 / 1V8**		
Project: **Nucleo144 H7 SMPS with STLINK V3**		
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STLINK_MCU

DFU CONNECTOR

CN2

DNF

Header 4x1

Connector must be on the border of the PCB

The routing of the tracks must be done on continuity from ST-LINK to 47ohm resistors and from resistors to Target MCU to avoid stub noises and EMC approach. (47ohm resistors must be very close to STDC14)

3V3_STLK

HSE CLK STLINK

X1

NZ2520SH 25MHz

R24 10K

R21 100R

C37 100nF

JP1 Shunt not fitted

NRST

C28 100nF

C7 2.2uF

R6 3K

U7A

STLK_SWDIO A15

STLK_SWCLK A14

USB_DEV_HS_N R14

USB_DEV_HS_P R15

G1

H1

J1

D6

C6

J14

J15

STLK_SWDIO/PA13

STLK_SWCLK/PA14

USB_DEV_HS_N/PB14

USB_DEV_HS_P/PB15

OSC_IN/PH0

OSC_OUT/PH1

NRST

BOOT0

PDR_ON

V12_OTGPHY

REXT_OTGPHY

T_SW_DIR/PA7 R3

T_SWDIO_IN/PH7 N12 T_SWDIO_IN level shifter 1V8/3V3

T_SWDIO_OUT/PF9 L2 T_SWDIOa level shifter 1V8/3V3

T_SWCLK/PH6 M11 T_SWCLKa

T_SWO/PD2 D12 T_SWOa level shifter 1V8/3V3

STLK_VCP_RX/PG9 C10 STLK_VCP_RX level shifter 1V8/3V3

STLK_VCP_TX/PG14 A7 STLK_VCP_TX

GNDDetect/PG5 K13 GNDDetect

T_VCC AIN/PA0 N3

T_PWR_EXT/PB1 R4 T_PWR_EXT

T_PWR_EN/PB0 R5 T_PWR_EN

STLK_LED/PA10 D15 LED_STLK

STLK_MCO/PA8 F15

T_NRST/PA6 P3 T_NRSTa

HW_TYP_0/PI4 D4

HW_TYP_1/PI5 C4

R11 47R T_SWCLK T_SWCLK

R23 47R T_VCP_RX T_VCP_RX

R20 4K7 VDD

R18 4K7

R15 2K7 5V

R14 4K7

R5 100R C5 20pF STLK_MCO STLK_MCO

R29 47R JP3 Shunt Fitted T_NRST T_NRST

HW6

ST-LINK POWER

3V3_STLK

U7B

VDD VSS VDDA VREF+ VBAT BYPASS-REG VCAP1 VCAP2

ST-LINKV3E_SWD

R22 10K

C13 2.2uF

C12 2.2uF

STDC14 Receiver

CN5

VDD

KEY

R17 100R

GNDDetect

T_VCP_RX

T_SWDIO T_SWCLK T_SWO T_JTDI T_NRST T_VCP_TX

MIPI10 on STDC14 footprint

Specific constraints for T_SWDIO and T_SWCLK (must be same length and must be Shielded).

ESD PROTECTIONS

U4 STLK_SWDIO

U3 ESDALC6V1-1U2 STLK_SWCLK

ESDALC6V1-1U2

U8 T_SWDIO T_SWCLK T_SWO T_JTDI

ESDALC6V1W5

U24 T_NRST T_VCP_TX T_VCP_RX

ESDALC6V1W5

T_JTDI

Pin attributions on ESD can be swapped for layout optimisation

LED STLK

LD4

Red

Green

LD_BICOLOR_CMS

R9 330R LED_STLK

R8 330R

3V3_STLK

3V3_STLK

C34 C8 C33 C22 C17 C15 C9 C10 100nF

C21 C25 C14 C30 C29 C31 C32 C11 100nF

C35 4.7uF C36 1uF C16 100nF

ST-LINK USB CONNECTOR

5V_USB_CHGR

C6 100pF

U6 ESDA7P60-1U1M

Capacitor close to pin 1

Matched Net Lengths [Tolerance = 2.5mm]

Impedance Constraint [Min = 85.00 Max = 95.00]

CN1 STLK

USB_Micro-B receptacle

VBUS DM DP ID GND Shield Shield Shield Shield EXP EXP

USB_DEV_HS_CN_N

USB_DEV_HS_CN_P

USB

U5 ECMF02-2AMX6 NC D- D+ GND D- D+

USB_DEV_HS_N

USB_DEV_HS_P

USB_uB_105017-0001

SW LEVEL SHIFTER FOR MCU_1V8

MCU_1V8/3V3

ST_LINK_3V3

VDD C26 100nF C27 100nF 3V3_STLK

U10

T_SWDIO T_SWO 47R R10 R13 T_SWDIOa T_SWDIO_IN T_SWOa

SN74LVC2T45DCUT

SB5 DNF

R70 100R DNF

MCU_1V8/3V3

ST_LINK_3V3

VDD C4 100nF C2 100nF 3V3_STLK

U1

VDD R4 100K

T_VCP_TX T_VCP_TX 47R R3

STLK_VCP_RX

SN74LVC2T45DCUT

SB13 DNF

5V ST-LINK PROTECTION

5V_USB_CHGR

5V_USB_STLK

U2 STMPS2151STR IN OUT EN FAULT GND

T_PWR_EN

C3 1uF

R2 1K

R1 100K

R7 10K

LD6 RED

C1 1uF

ST-LINK POWER 3V3 / 150mA

3.3 Volts ST-LINK

5V_VIN 5V_EXT 5V_USB_CHGR

BAT60JFILM D1 D2 D3

U9 LD3985M33R Vin Vout INH GND BYPASS

3V3_STLK

C18 1uF

C20 100nF

C19 10nF

C23 1uF

C24 100nF

GND

CN3 Header 2x1 16mm

HW7

CN4 Header 2x1 16mm

HW8

Title: **STLINK_V3E**			
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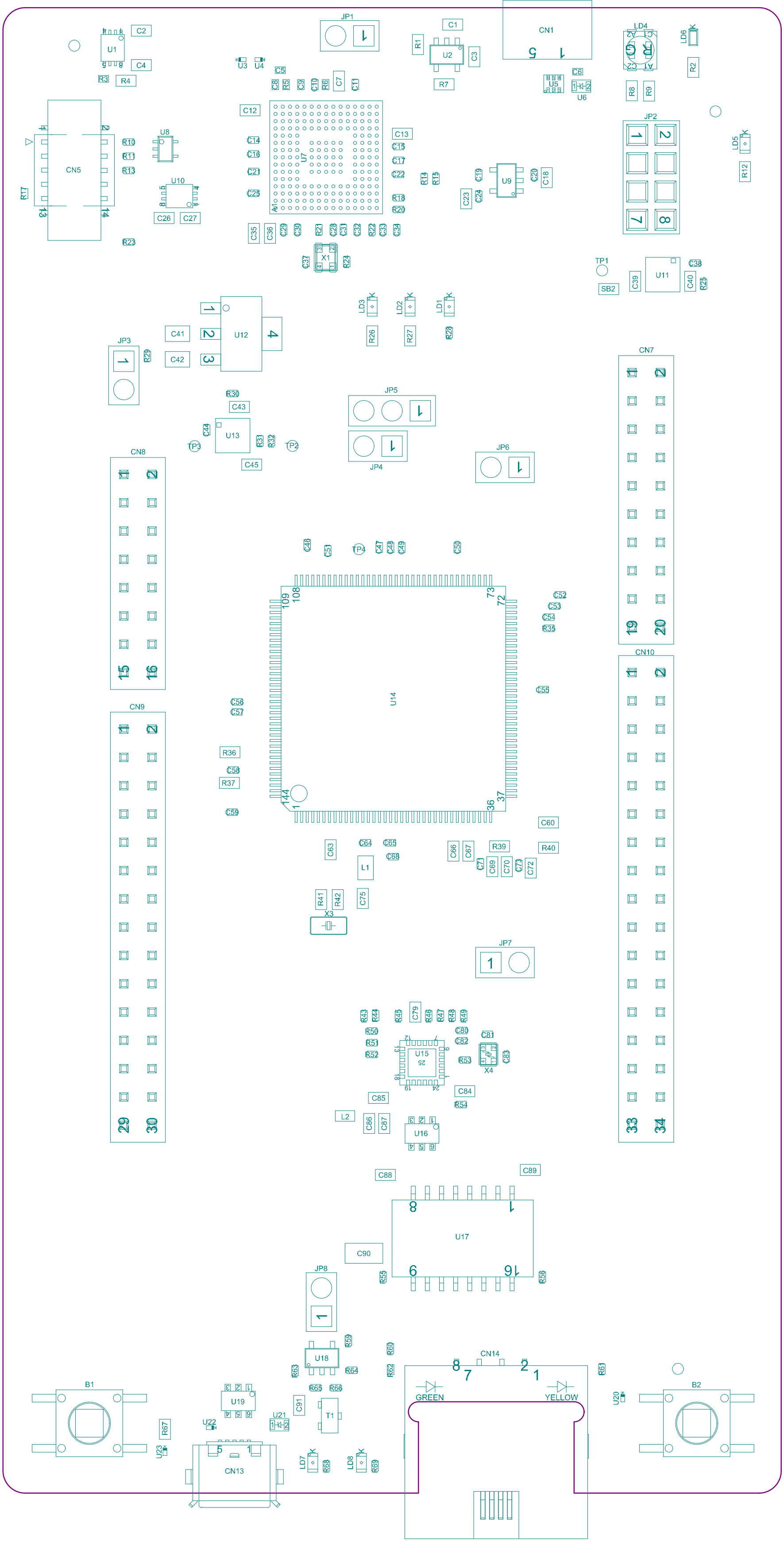

Project: Nucleo144 H7 SMPS with STLINK V3	
Layer: M14-Top Assembly	Gerber: .GM14
Variant: H755ZIQ	Ref: MB1363
Date: 09-OCT-19	Rev: D

CN4

CN3

D1 K

D2 K

D3 K

U24

Q1 Q2 Q3

R71 R72 R73

R76 R74 R75

SB6

SB7

SB11

SB14

SB16 SB103 SB17 SB18 SB19 SB21

SB26 SB27

SB31 SB28 SB29 SB30

SB34 SB32 SB33

SB35 SB36

SB37 SB43 SB40 SB41 SB42

SB45 SB46

SB51 SB48 SB49 SB50

SB54 SB52 SB53

SB57

SB59

SB63 SB60 SB61

SB68 SB69 SB72 SB73 SB75 SB76

SB80 SB79

SB84 SB82 SB83 SB85 SB86 SB87 SB88

SB89

SB93 SB92 R77

SB96

SB104

SB98

R78 R79 R80 R81

SB100

CN15

1

CN16

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Project: Nucleo144 H7 SMPS with STLINK V3	
Layer: M15-Bottom Assembly	Gerber:.GM15
Variant: H755ZIQ	Ref: MB1363
Date: 09-OCT-19	Rev: D