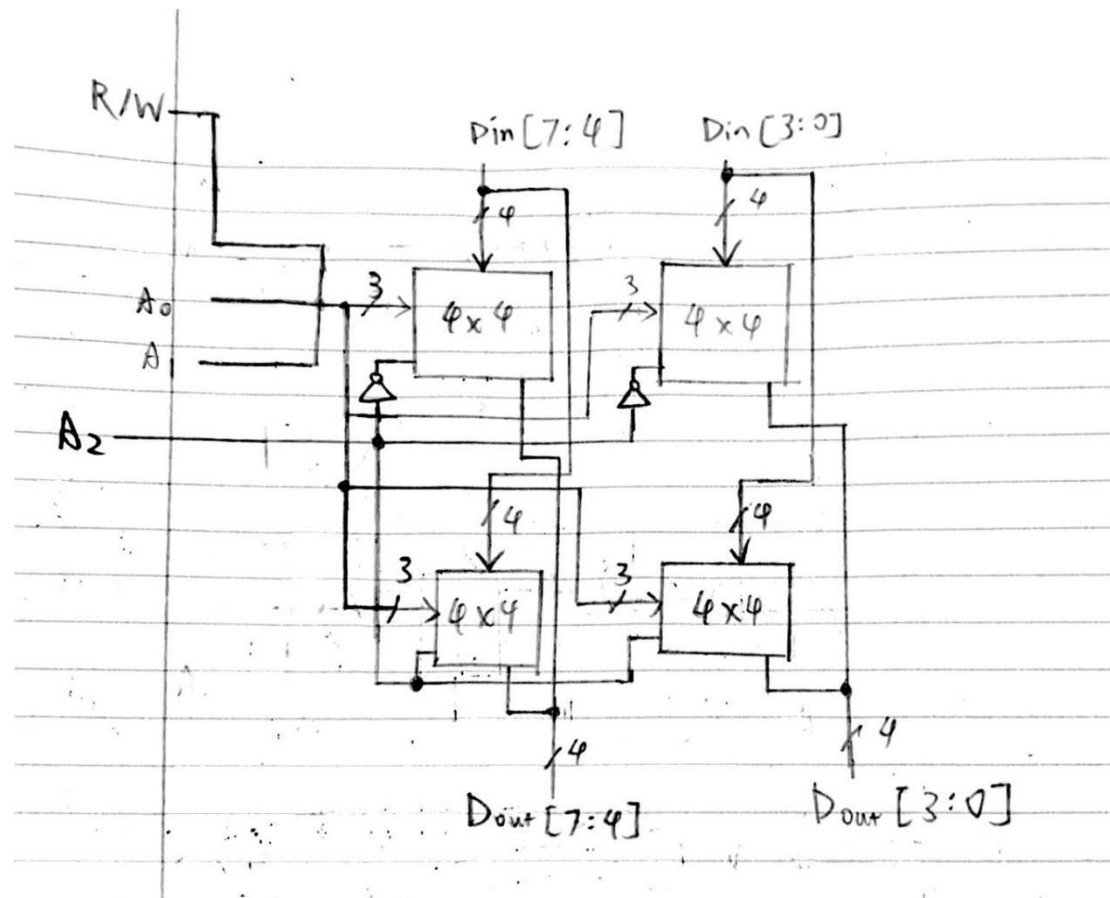
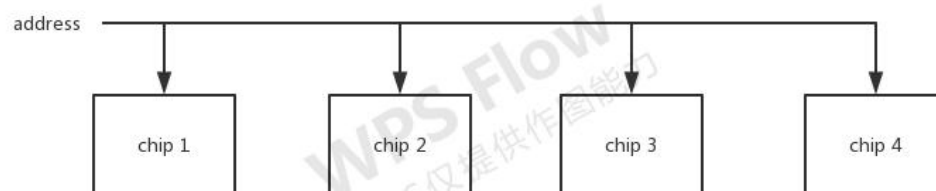


EE 371 HW2

1. a. Number of words:  $2^8 = 256$ , number of bits per word : 8  
 b. Number of words:  $2^9 = 512$ , number of bits per word: 6
- 2.

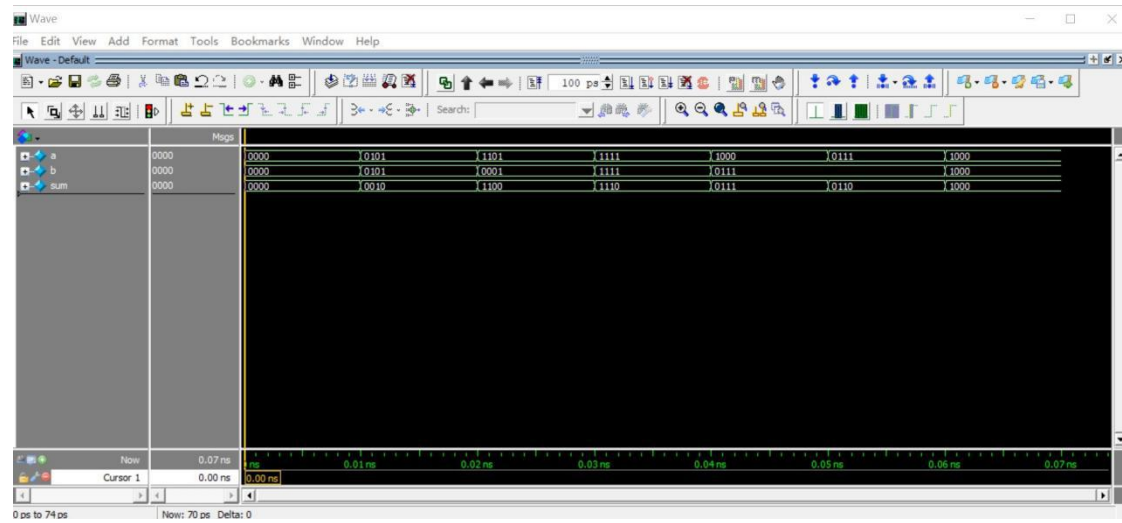


3. a. one chip is  $8M * 16 / 8 = 16M$  bytes  
 $64M / 16M = 4$   
 4 chips are needed  
 By connecting all chips in series, I can get a total capacity of  $8M * 64$ , which is 64M bytes

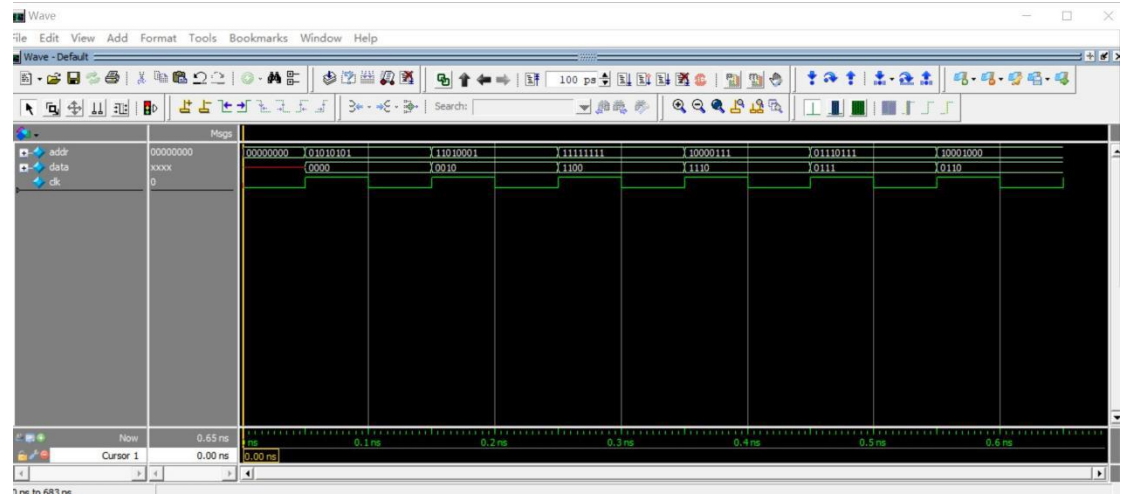


- b.  $8M = 2^3 * 2^{20} = 23$  bits
- c. All of these bits are connected to the address input
- d. 0 bits

4.



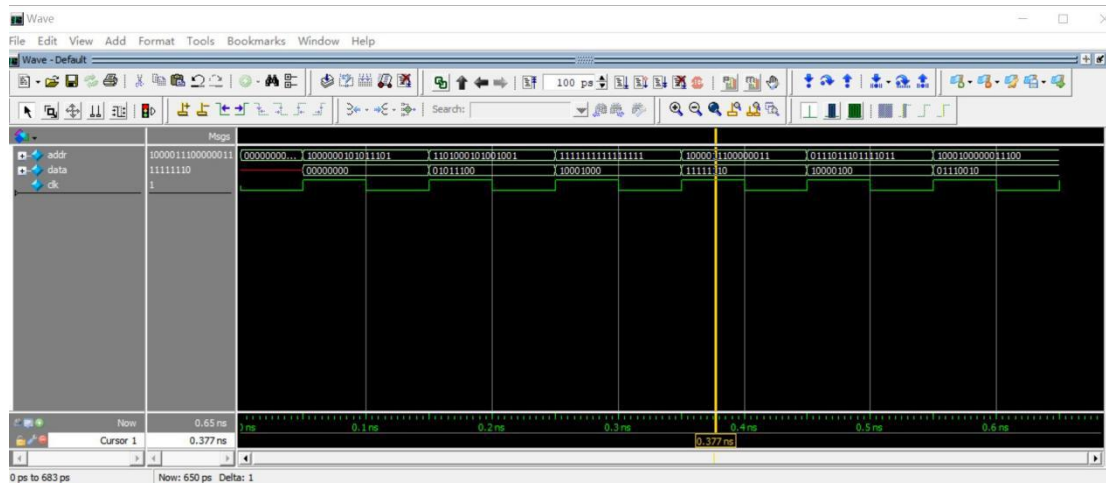
5.



4 bit ROM simulation

Table of Contents	Analysis & Synthesis Summary
<ul style="list-style-type: none"> <li>Flow Summary</li> <li>Flow Settings</li> <li>Flow Non-Default Glob</li> <li>Flow Elapsed Time</li> <li>Flow OS Summary</li> <li>Flow Log</li> <li>Analysis &amp; Synthesis <ul style="list-style-type: none"> <li>Summary</li> <li>Settings</li> <li>Parallel Compilation</li> <li>Source Files Read</li> <li>Resource Usage Sun</li> <li>Resource Utilization</li> <li>RAM Summary</li> <li>Optimization Results</li> <li>Source Assignments</li> <li>Parameter Settings l</li> <li>LPM Parameter Sett</li> <li>Post-Synthesis Netli</li> <li>Elapsed Time Per Pa</li> <li>Messages</li> </ul> </li> </ul>	<p>&lt;&lt;Filter&gt;&gt;</p> <p>Analysis &amp; Synthesis Status: Successful - Fri Oct 11 14:54:15 2019</p> <p>Quartus Prime Version: 17.0.0 Build 595 04/25/2017 SJ Lite Edition</p> <p>Revision Name: DE1_SoC</p> <p>Top-level Entity Name: sync_rom</p> <p>Family: Cyclone V</p> <p>Logic utilization (in ALMs): N/A</p> <p>Total registers: 0</p> <p>Total pins: 13</p> <p>Total virtual pins: 0</p> <p>Total block memory bits: 1,024</p> <p>Total DSP Blocks: 0</p> <p>Total HSSI RX PCSs: 0</p> <p>Total HSSI PMA RX Deserializers: 0</p> <p>Total HSSI TX PCSs: 0</p> <p>Total HSSI PMA TX Serializers: 0</p> <p>Total PLLs: 0</p> <p>Total DLLs: 0</p>

## 4 bit ROM synthesis report



## 8 bit ROM simulation

sync_rom.sv		Compilation Report - DE1_SoC
Table of Contents		Analysis & Synthesis Summary
<ul style="list-style-type: none"> <li>Flow Summary</li> <li>Flow Settings</li> <li>Flow Non-Default Glob</li> <li>Flow Elapsed Time</li> <li>Flow OS Summary</li> <li>Flow Log</li> <li>Analysis &amp; Synthesis <ul style="list-style-type: none"> <li>Summary</li> <li>Settings</li> <li>Parallel Compilation</li> <li>Source Files Read</li> <li>Resource Usage Sum</li> <li>Resource Utilization</li> <li>RAM Summary</li> <li>Optimization Results</li> <li>Source Assignments</li> <li>Parameter Settings</li> <li>LPM Parameter Sett</li> <li>Post-Synthesis Netli</li> <li>Elapsed Time Per Pa</li> <li>Messages</li> </ul> </li> </ul>		<p>&lt;&lt;Filter&gt;&gt;</p> <p>Analysis &amp; Synthesis Status Successful - Fri Oct 11 15:20:15 2019</p> <p>Quartus Prime Version 17.0.0 Build 595 04/25/2017 SJ Lite Edition</p> <p>Revision Name DE1_SoC</p> <p>Top-level Entity Name sync_rom</p> <p>Family Cyclone V</p> <p>Logic utilization (in ALMs) N/A</p> <p>Total registers 0</p> <p>Total pins 13</p> <p>Total virtual pins 0</p> <p>Total block memory bits 1,024</p> <p>Total DSP Blocks 0</p> <p>Total HSSI RX PCSs 0</p> <p>Total HSSI PMA RX Deserializers 0</p> <p>Total HSSI TX PCSs 0</p> <p>Total HSSI PMA TX Serializers 0</p> <p>Total PLLs 0</p> <p>Total DLLs 0</p>

## 8 bit ROM synthesis report

Size of question 4: 9

sign\_mag\_add.v

Compilation Report - DE1\_SoC

sync\_rom.v

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    - Resource Utilization
    - RAM Summary
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  - Source Assignments
  - Parameter Settings l
  - LPM Parameter Sett
  - Post-Synthesis Netli
  - Elapsed Time Per Pa

Analysis & Synthesis Resource Utilization by Entity

<<Filter>>

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Register
1	▼  sync_rom	0 (0)	0 (0)
1	▼  altsyncram:rom_rtl_0	0 (0)	0 (0)
1	altsyncram_h6d1:auto_generated	0 (0)	0 (0)

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Note: For table entries with two numbers listed, the numbers in parentheses indicate the number of resources of the given type used by the specific entity alone. The numbers listed outside of

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4-bit ROM size: 0

sign\_mag\_add.v

Compilation Report - DE1\_SoC

sync\_rom.v

Table of Contents

- Flow Summary
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- Flow Log
- Analysis & Synthesis
  - Summary
  - Settings
    - Parallel Compilation
    - Source Files Read
    - Resource Usage Sun
    - Resource Utilization
    - RAM Summary
  - Optimization Results
  - Source Assignments
  - Parameter Settings l
  - LPM Parameter Sett
  - Post-Synthesis Netli
  - Elapsed Time Per Pa

Analysis & Synthesis Resource Utilization by Entity

<<Filter>>

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Register
1	▼  sync_rom	0 (0)	0 (0)
1	▼  altsyncram:rom_rtl_0	0 (0)	0 (0)
1	altsyncram_h6d1:auto_generated	0 (0)	0 (0)

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Note: For table entries with two numbers listed, the numbers in parentheses indicate the number of resources of the given type used by the specific entity alone. The numbers listed outside of parentheses indicate the total resources of the given type used by the specific entity and all of its

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8-bit ROM size: 0

## Feedback

In this homework I had some trouble understanding the questions. Some questions are not very specific. For instance, question 3 did not mention how we should connect the chips. I also had much trouble working on question 5 since I did not know how to run simulation when reading from txt files.