

EDA Playground:

Concurrent Assertion: <https://www.edaplayground.com/x/4Vvu>

Classes1: <https://www.edaplayground.com/x/4ayL>

Classes2: <https://www.edaplayground.com/x/2wfB>

Randomization1: <https://www.edaplayground.com/x/56mi>

Randomization2: <https://www.edaplayground.com/x/6BLV>

18) For data arrival path, data path adds the most delay

For data required path, latch edge time adds the most delay

We can slow down the clock to meet the set up requirement. By slowing down the clock, we are increasing the data requirement time.

19) For both paths clock path adds the most delay. Hold slack does not depend on frequency, thus latch edge time does not influence the delays.

22) The fastest frequency I can set to pass setup timing is 45.4MHz

23) The latch edge time increases from 12.5ns to 22.025ns. The data required time is longer so the setup slack increases and can pass the requirement.

27) Yes. There is no unconstrained path showing in the report.

32) Fast 1200 mV OC Model has the longest slack time.

Because the hardware speed is fast, it takes less time for data to be transmitted to the output, the data arrival time is smaller, setup slack = min DRT - max DAT. Thus, the setup would be longer

Increasing the voltage speed up the circuit.

Increasing the temperature would decrease the speed of the circuit

35) Faster circuit would have smaller hold up slack. Because data transmits faster, data arrival time is smaller, hold slack = min DAT - max DRT. The data from the clock analyzer supports this expectation.