EE 371 Lab 1 Report

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I. Introduction

In this lab, I designed a parking lot occupancy system which shows the current number of vehicles in the parking lot, which is positive and cannot exceed 25. When a vehicle enters or exits the lot, the detectors are triggered and the connected LED light is turned on. The number of the vehicles in the parking lot would also be updated. When there is no vehicle in the lot, the system shows “CLEAR0” and when the parking lot is full, it shows “FULL25”.

II. Lab Procedures

To start with, I first started with breaking down the whole system into subsystems. The overall structure is presented below.

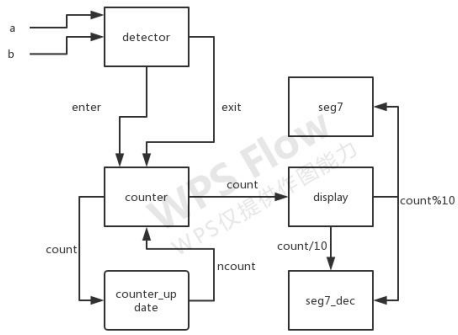

Fig 1. System Structure

Then I designed the detector module as my first step. I used a finite state machine to simulate the cases in which the vehicles pass the two detectors in sequence in the directions of entering and exiting. The state diagram is given below.

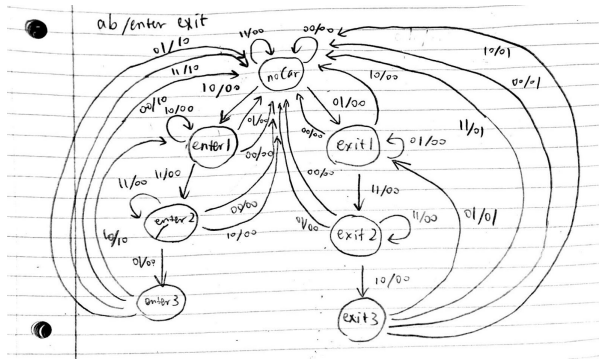

Fig 2. State Diagram

When the finite state machine reaches the final state enter 3 or exit 3, it outputs enter or exit signal which becomes the input to the counter module. The counter module increases the count when inputted enter as long as it has not reached maximum and decreases the count vice versa. The counter value is then inputted to the display which controls the hex LEDs to show the number of vehicles in the parking lot.

III. Results

The simulation meets the expectation of the system. I also notice that there is a delay of three clock periods between counter update and hex LED display update. After downloading the program onto the FPGA board, the system also worked.

IV. Problem Faced & Feedback

The lab is a relatively easy one and my major struggles are trying to remember the syntax of SystemVerilog.

And when I first programmed the display module, I used non-blocking assignment which caused the display to behave strangely: it showed patterns overlapping each other. After changing it to blocking assignment everything just worked fine. The lab cost me about 10 hours in total.

Appendix

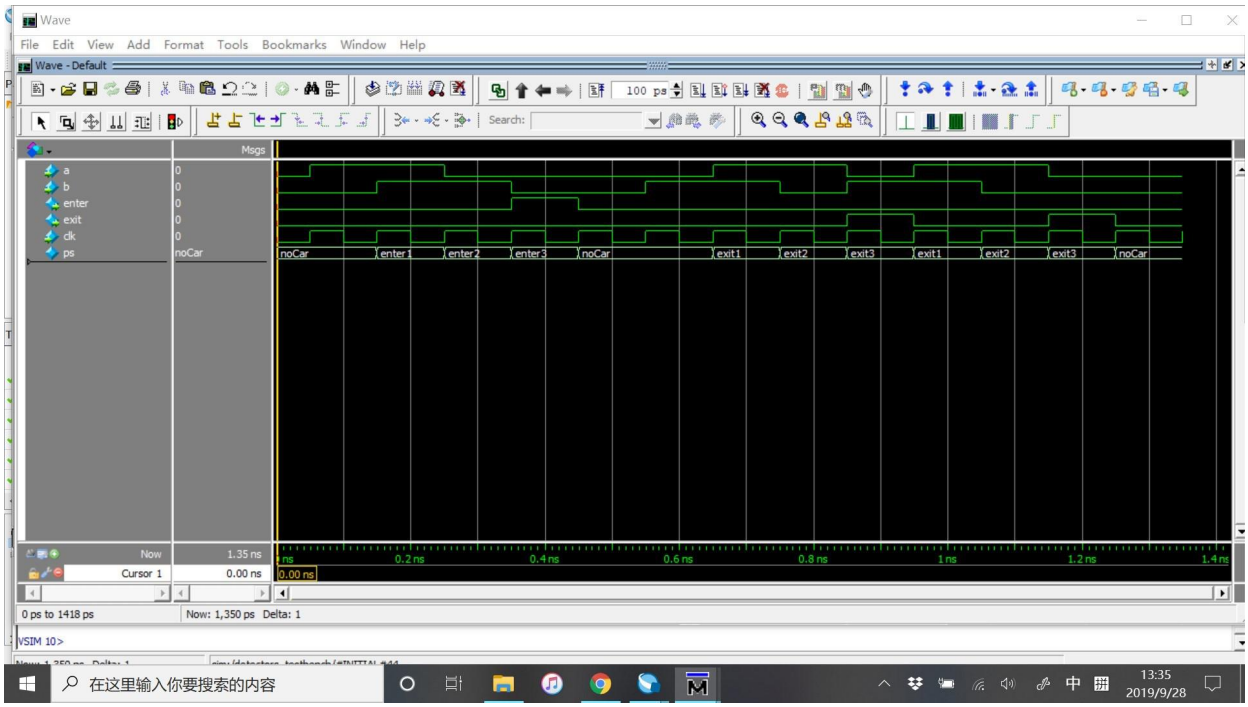

Fig 3. Detector Simulation

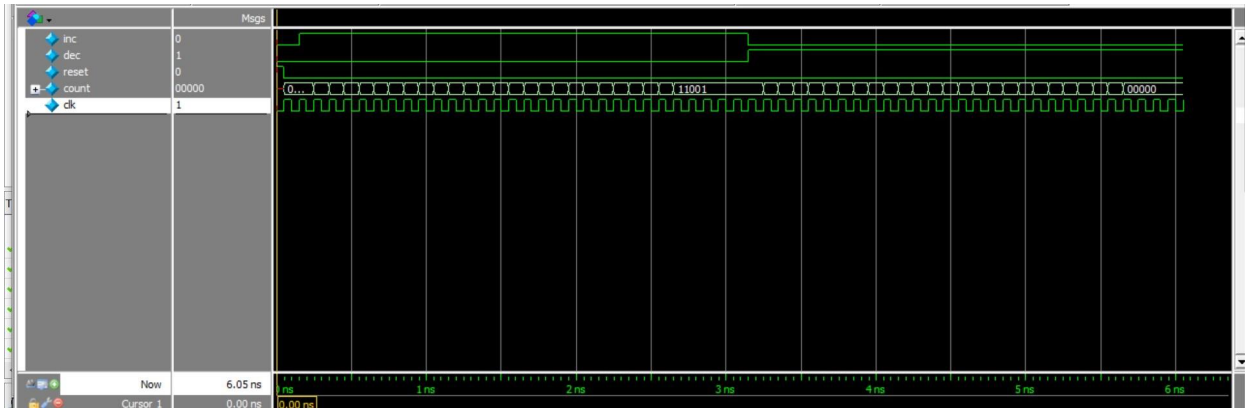

Fig 4. Counter Simulation

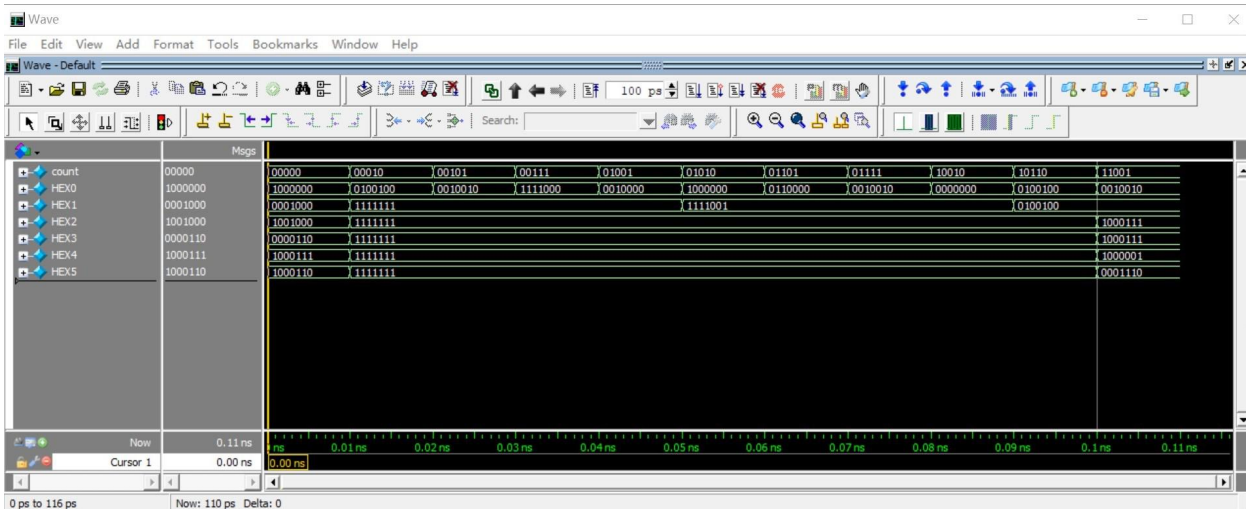

Fig 5. Display Simulation

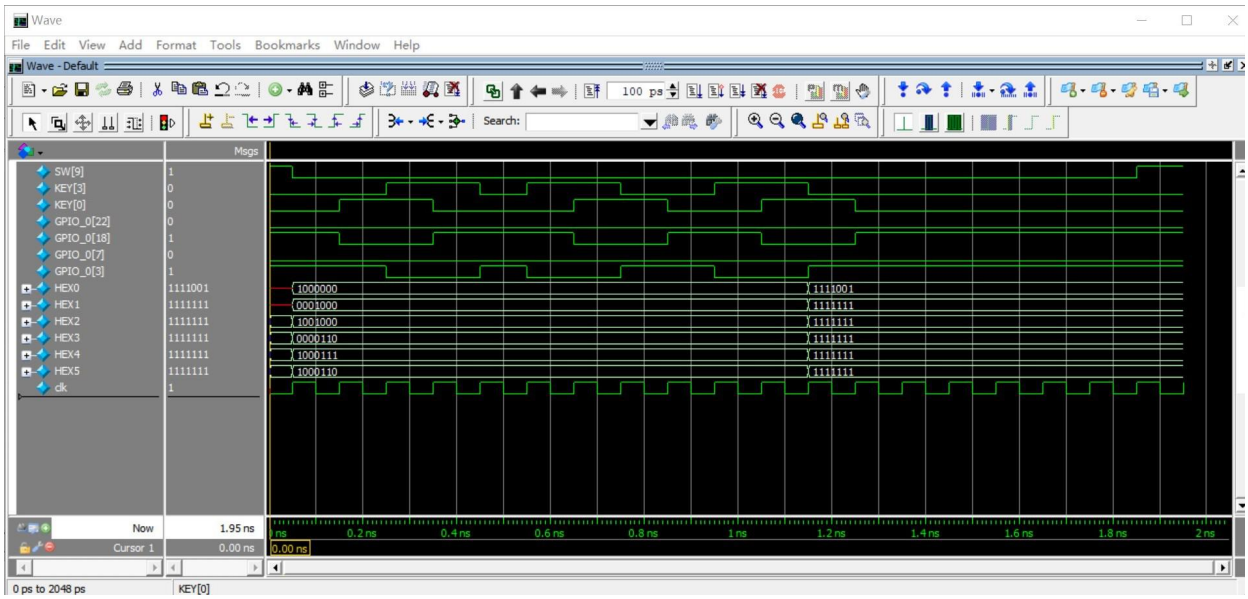

Fig 6. DE1_SoC Simulation