EE 371 HW1

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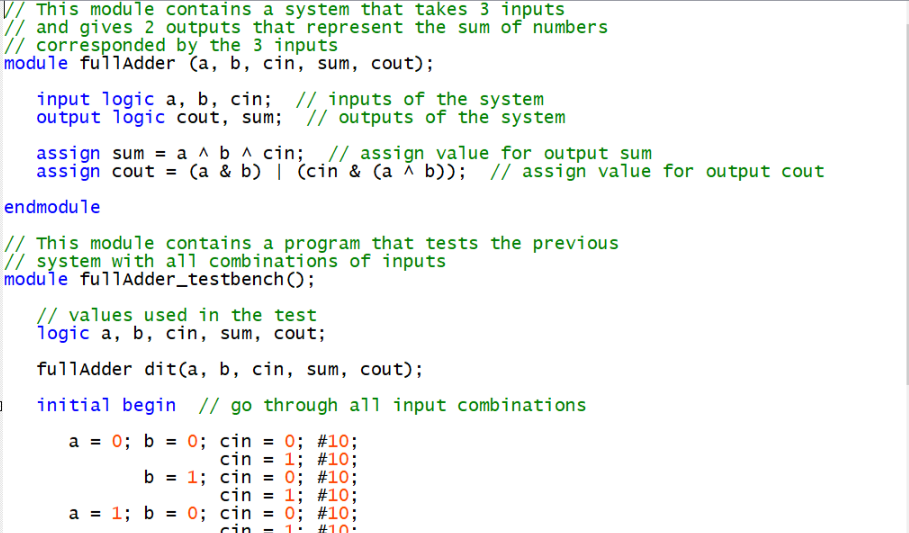
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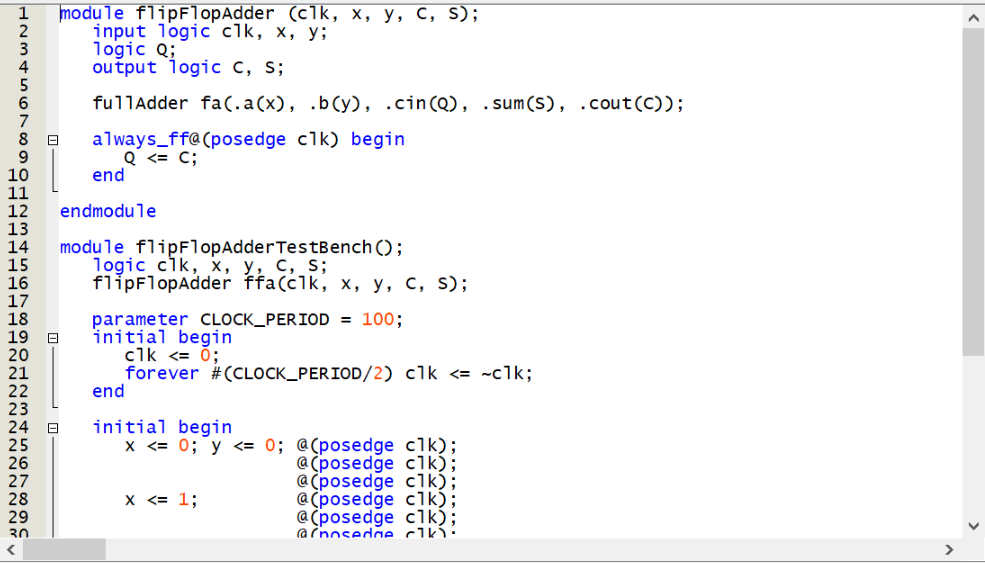
Q = 1

Q = 0

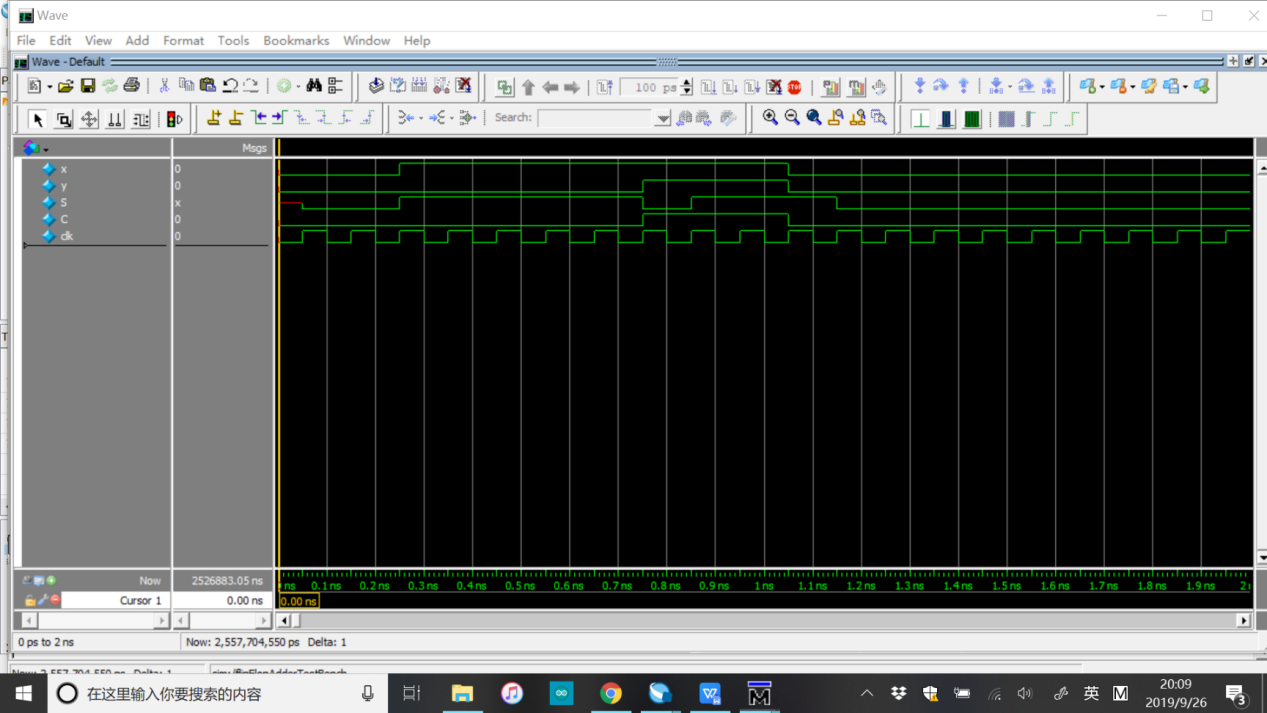
fullAdder.sv



flipFlopAdder.sv

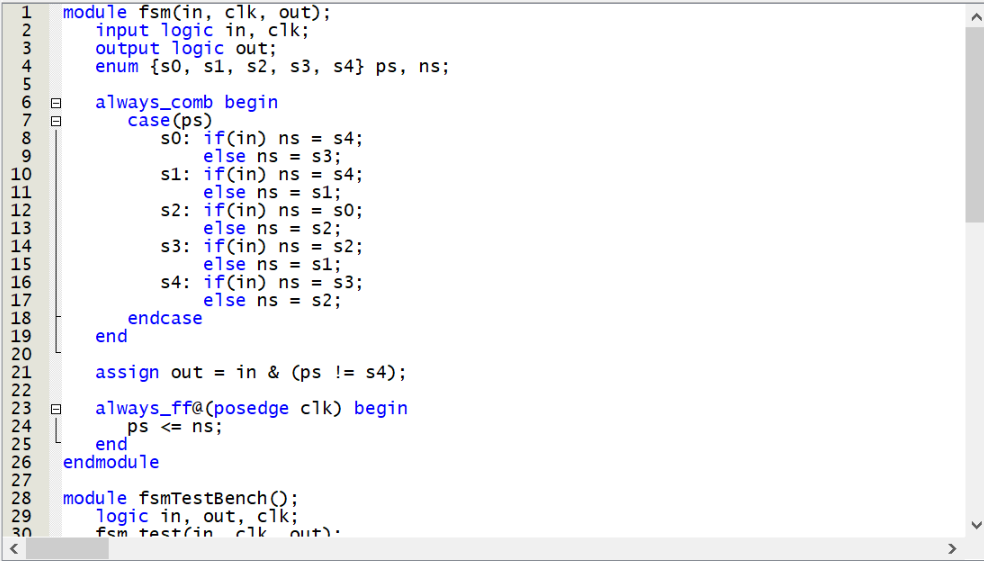


Simulation

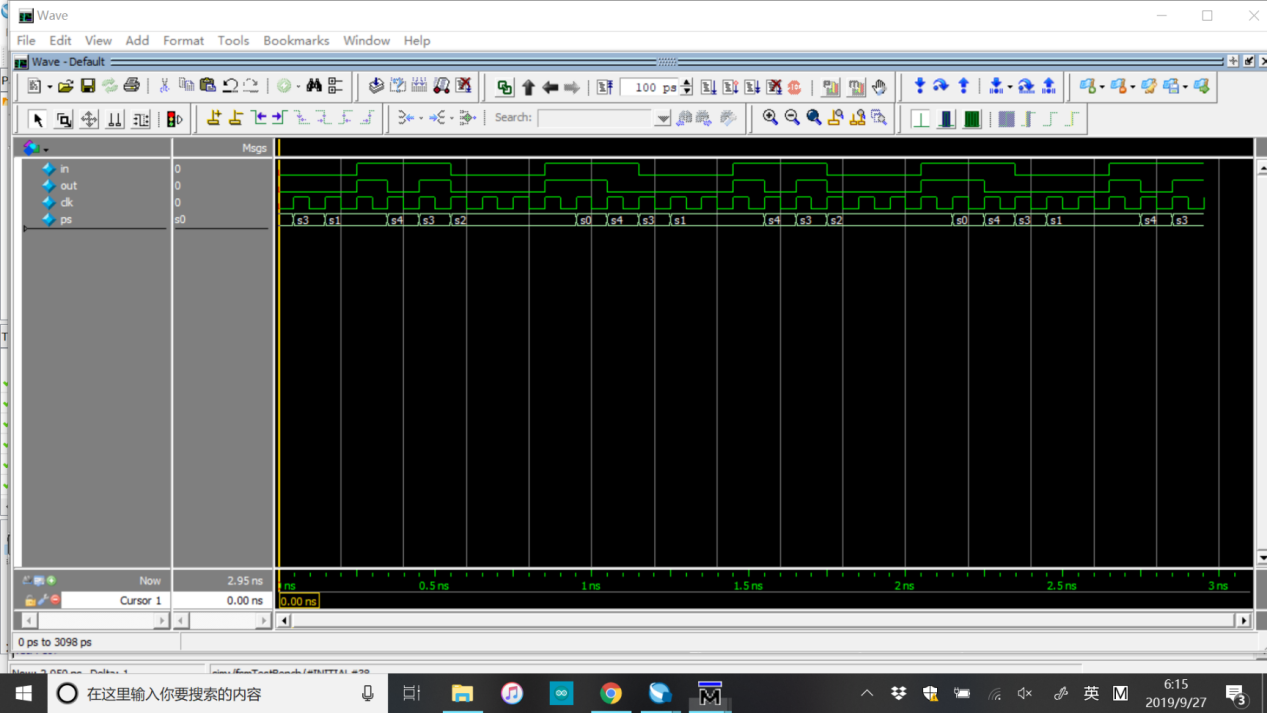


2)

fsm.sv



Simulation



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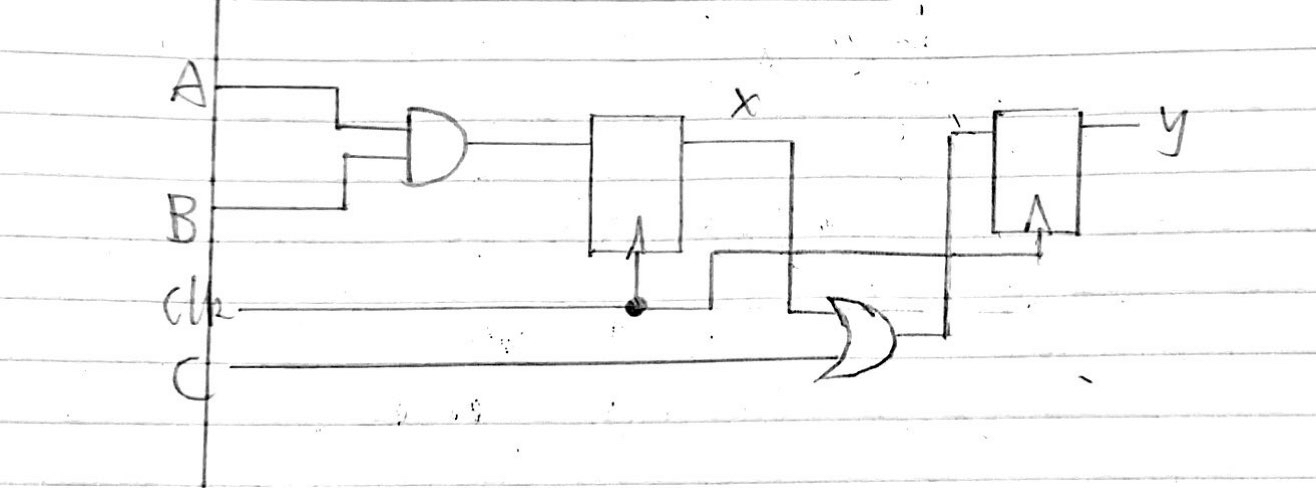
01

00

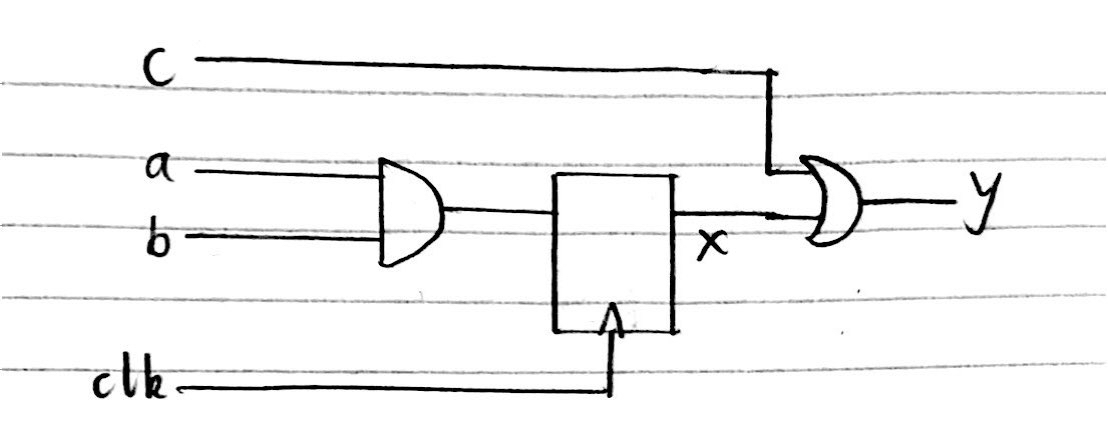
4)

Code1:

<=:

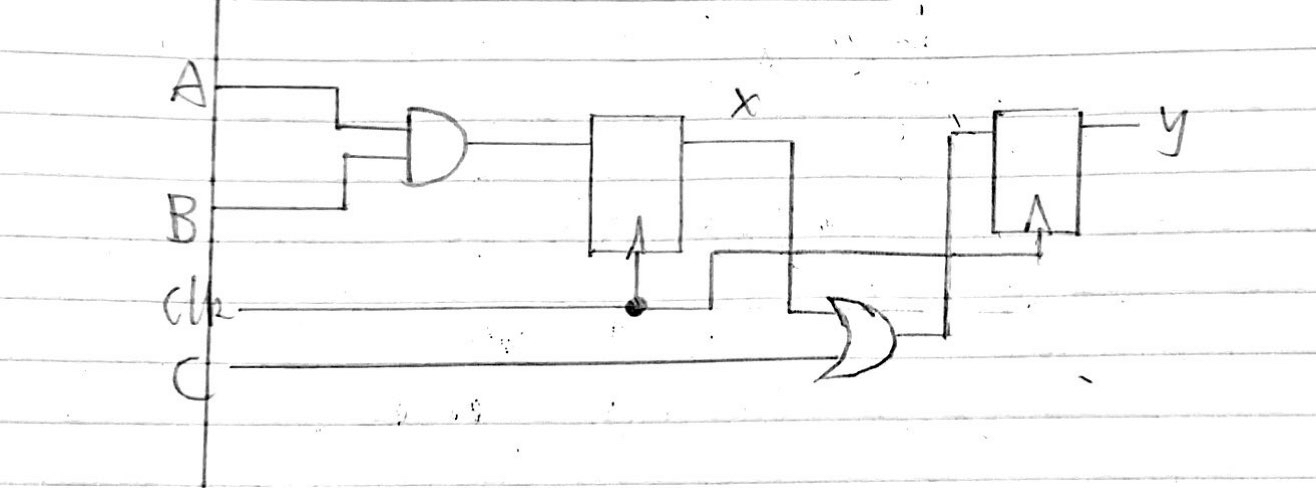


=:

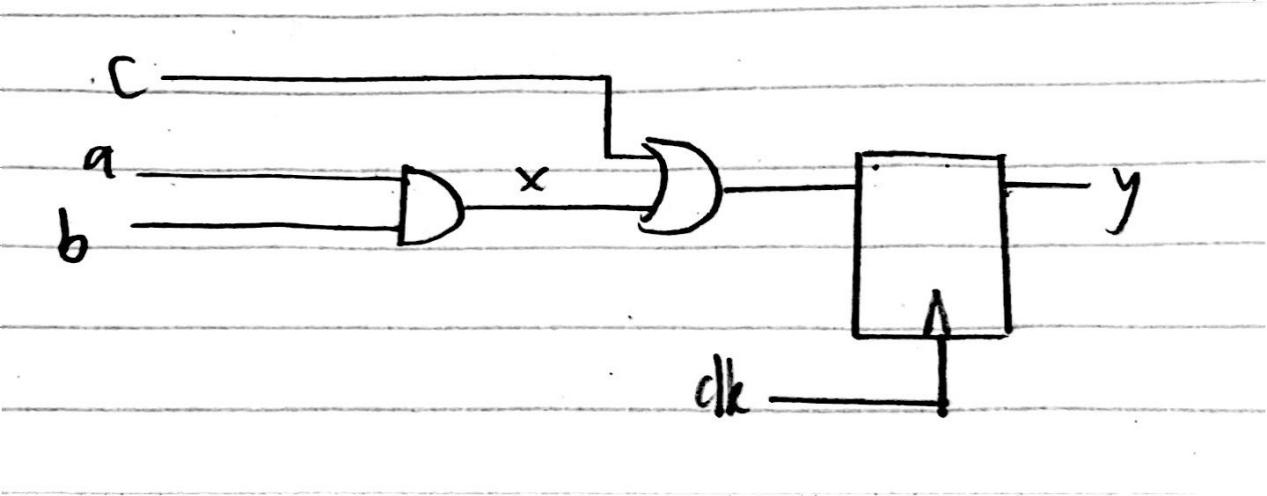


Code2:

<=:



=:



The two modules would have the same function when non-blocking assignment is used because in non-blocking assignment values are assigned simultaneously. However, they would have different functions under blocking assignment because in blocking assignment values are assigned immediately after the statement.

Feedback & Comment

I had some trouble writing the SystemVerilog codes because I kinda forget how to write them. And I also found that I can write finite state machines with logic rather than enum. I also struggled with problem 4 because I am not used to using blocking assignment with in always\_ff.