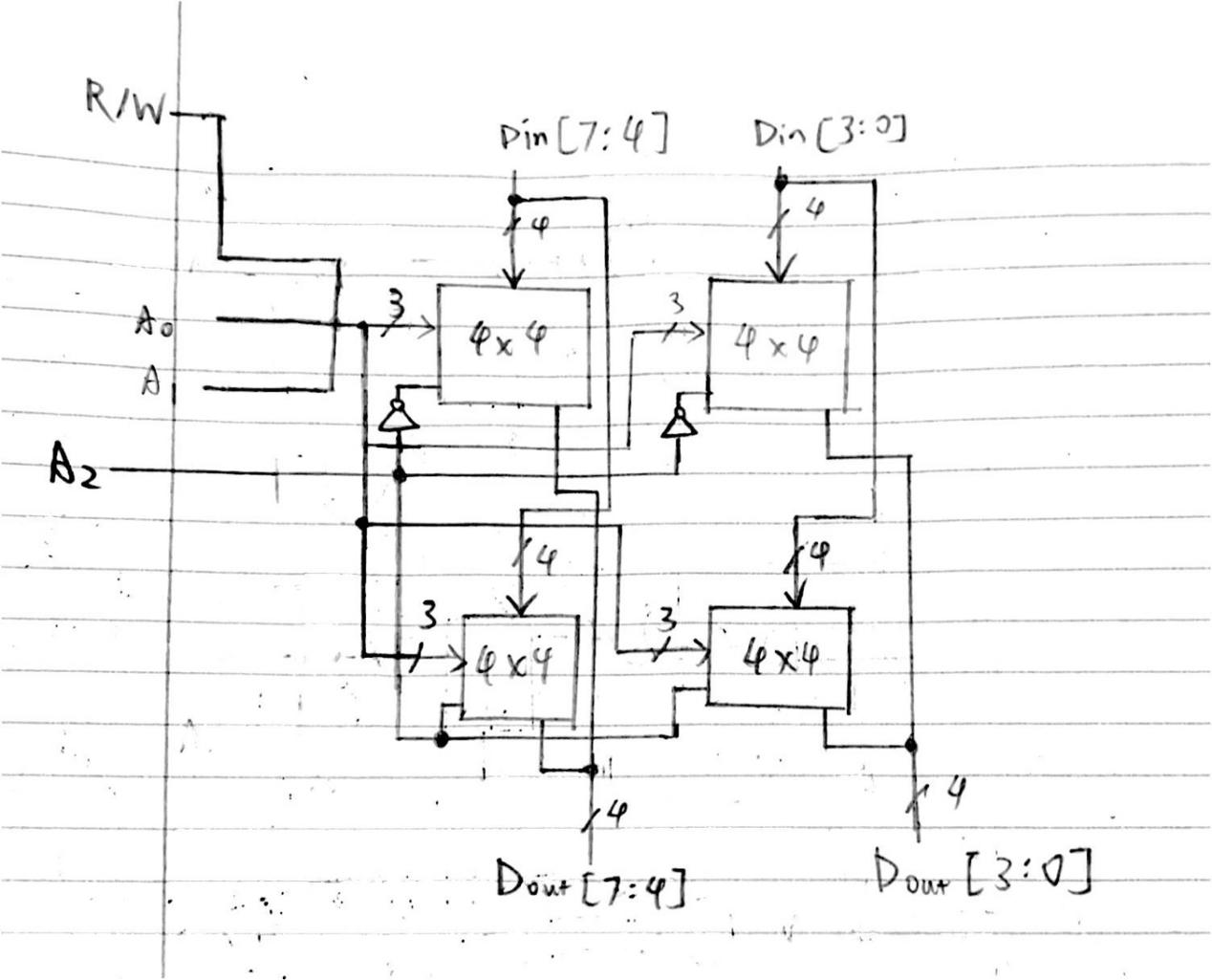
EE 371 HW2

1. a. Number of words: 28 = 256, number of bits per word : 8

b. Number of words: 29 = 512, number of bits per word: 6

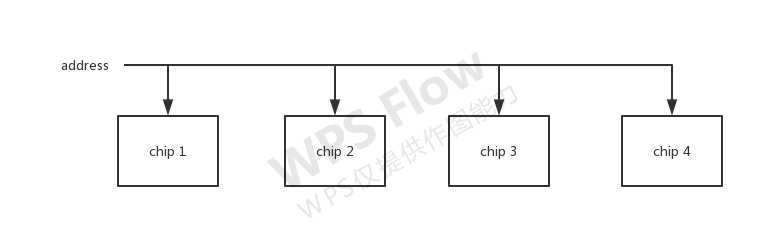
2. 

3. a. one chip is 8M \* 16 / 8 = 16M bytes

64M / 16M = 4

4 chips are needed

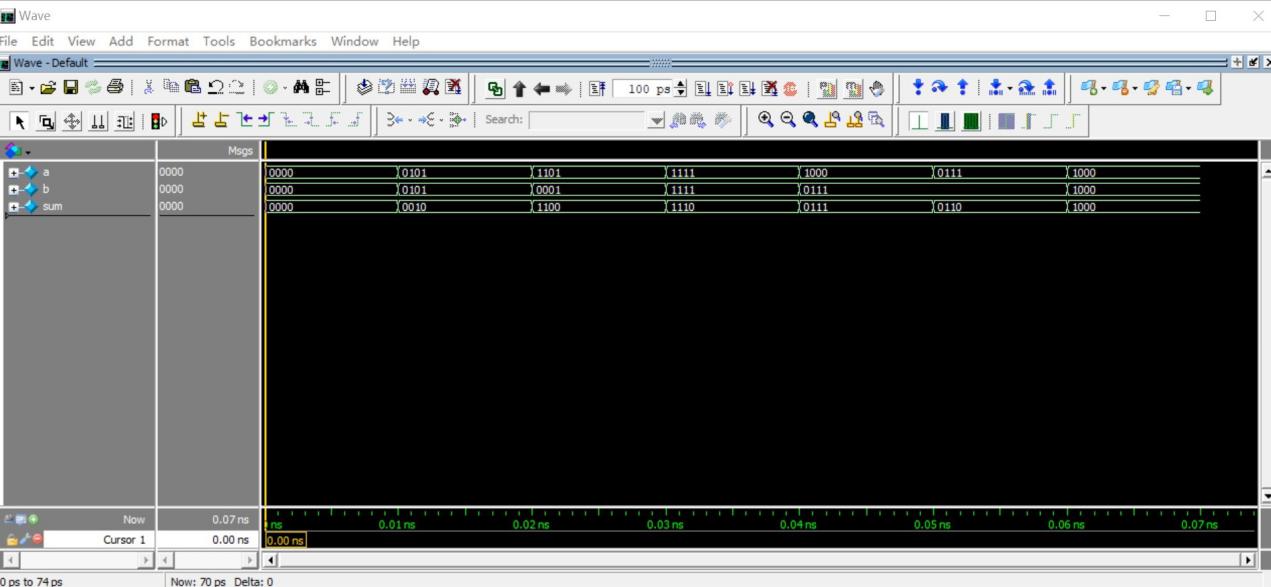
By connecting all chips in series, I can get a total capacity of 8M \* 64, which is 64M bytes



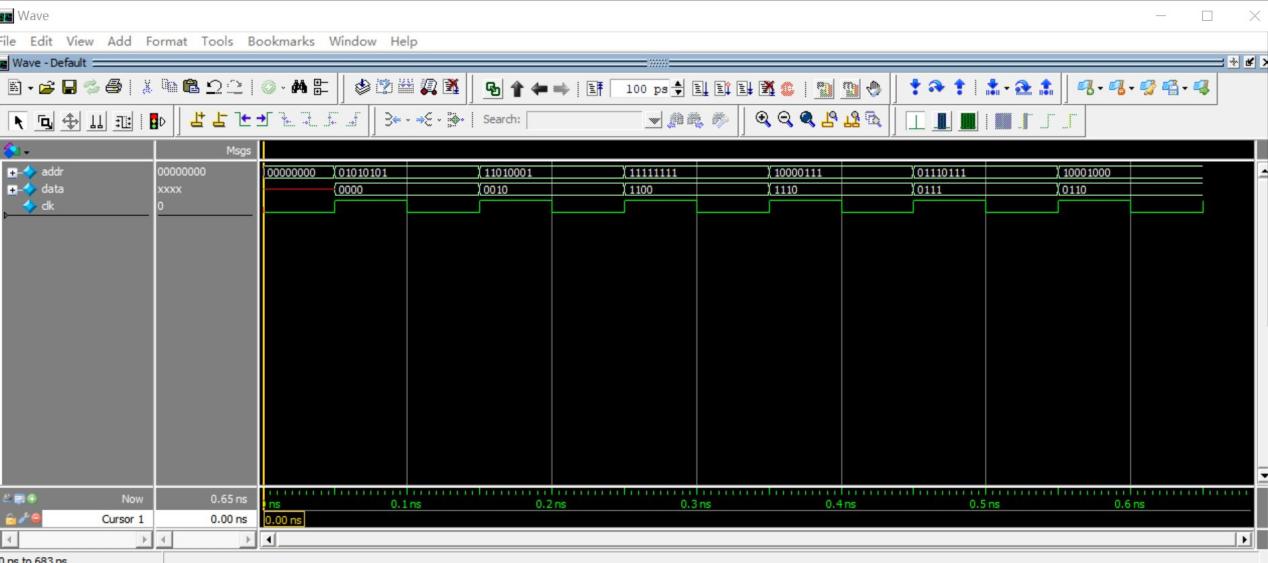
b. 8M = 23\*220 = 23 bits

c. All of these bits are connected to the address input

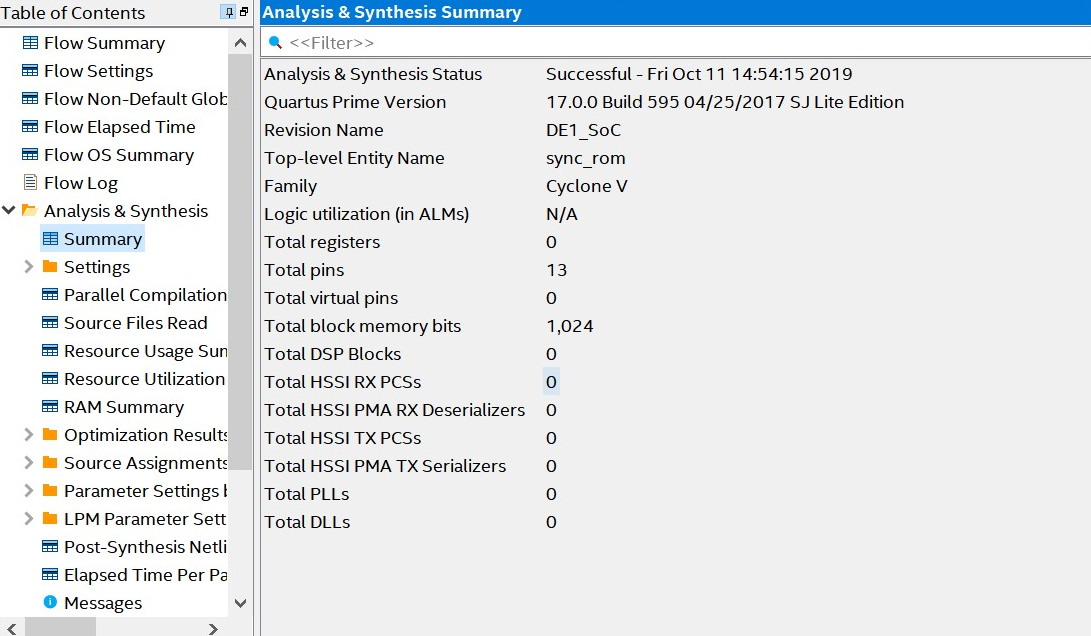
d. 0 bits



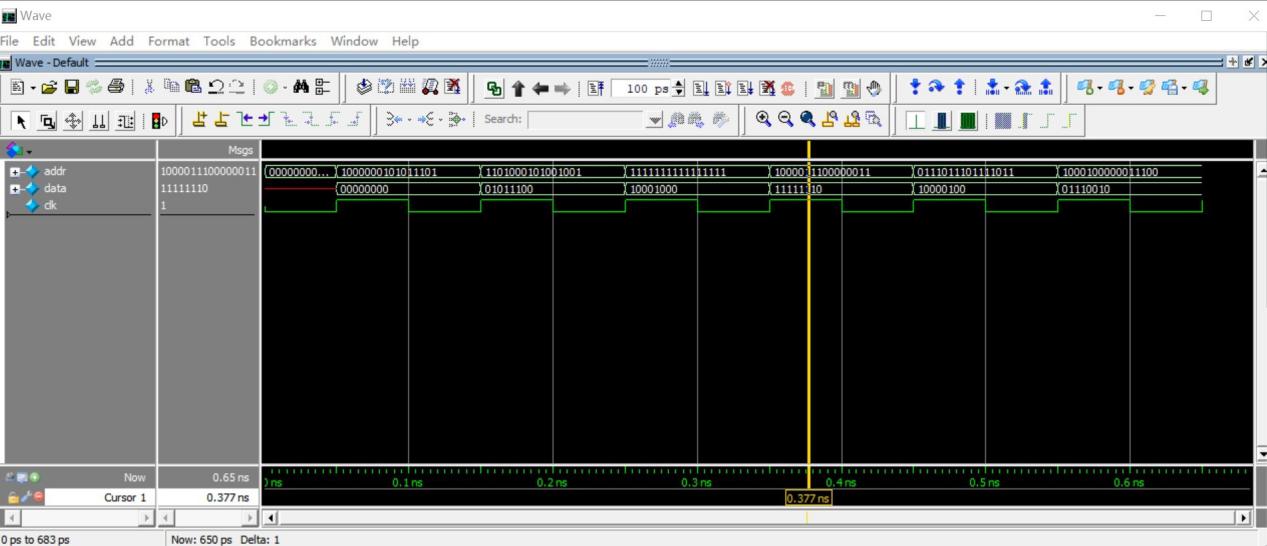
5.



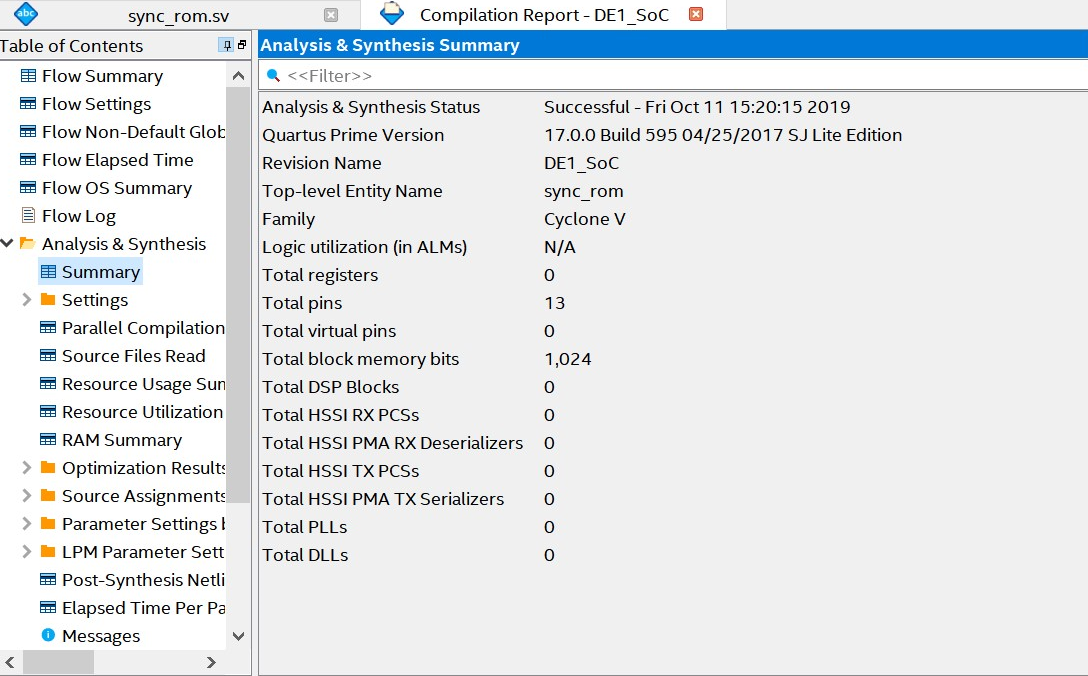
4 bit ROM simulation



4 bit ROM synthesis report

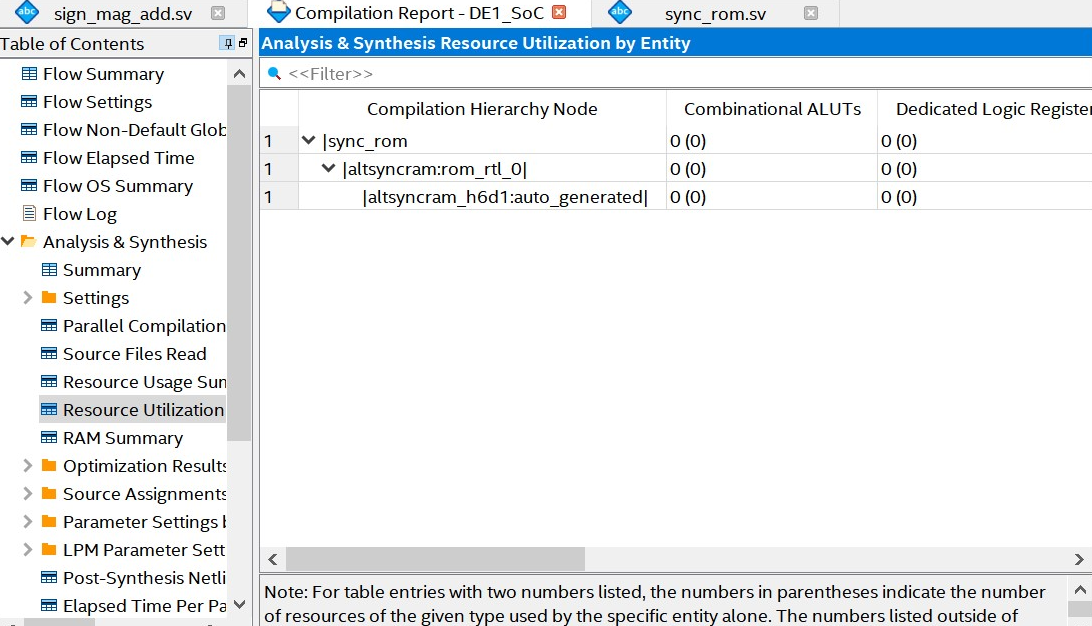


8 bit ROM simulation

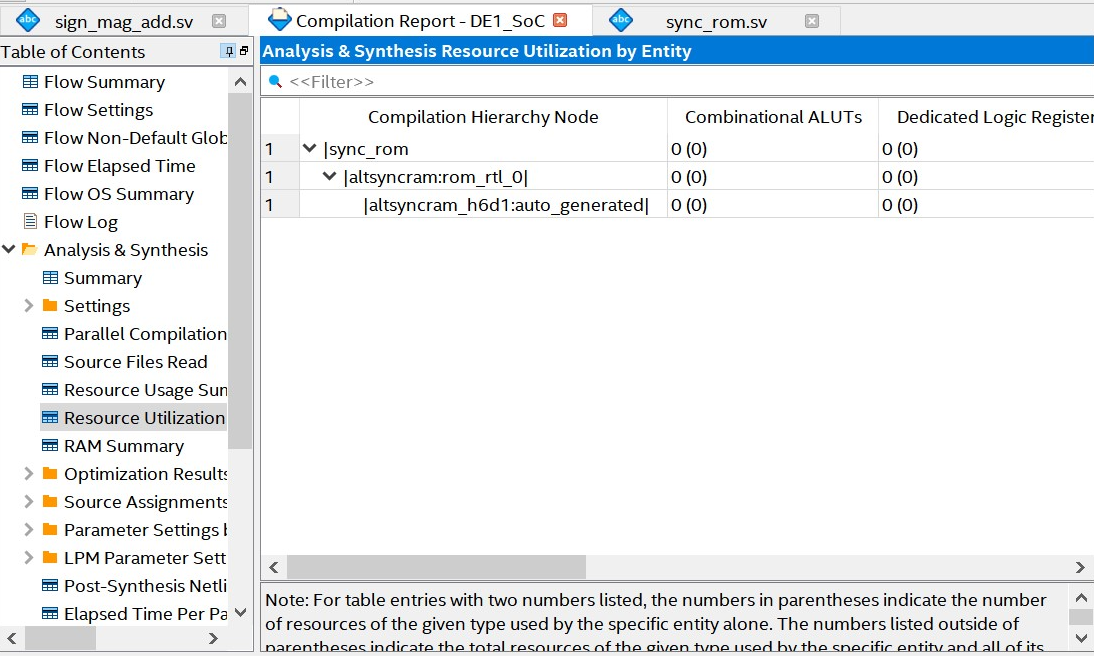


8 bit ROM synthesis report

Size of question 4: 9



1. bit ROM size: 0



8-bit ROM size: 0

Feedback

In this homework I had some trouble understanding the questions. Some questions are not very specific. For instance, question 3 did not mention how we should connect the chips. I also had much trouble working on question 5 since I did not know how to run simulation when reading from txt files.