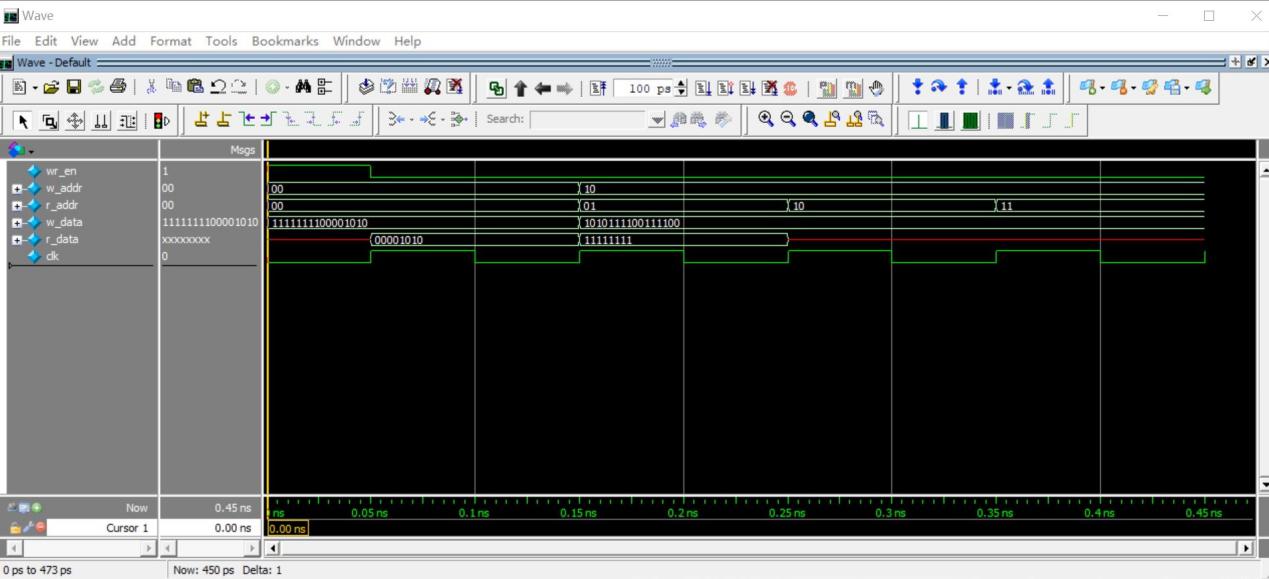
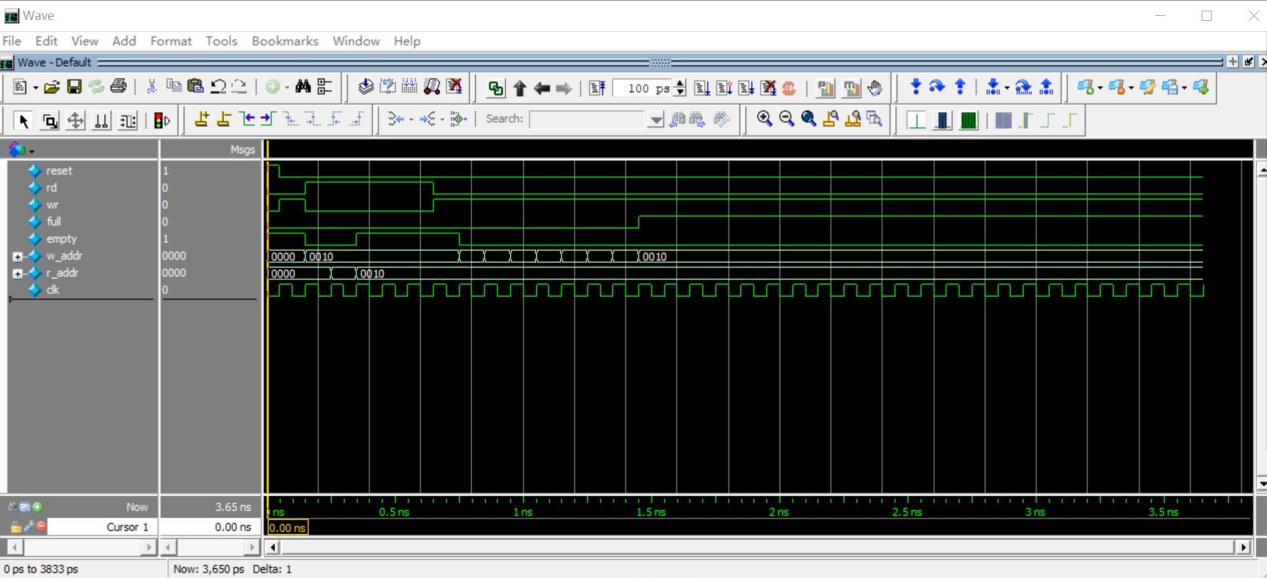


I changed the internal logic rp1a, rp1b, rp2a, rp2b, rp3a, rp3b and used them as addresses in normal state and cycling state. I set port 3 to read only from the second half (less significant half) from the given address.

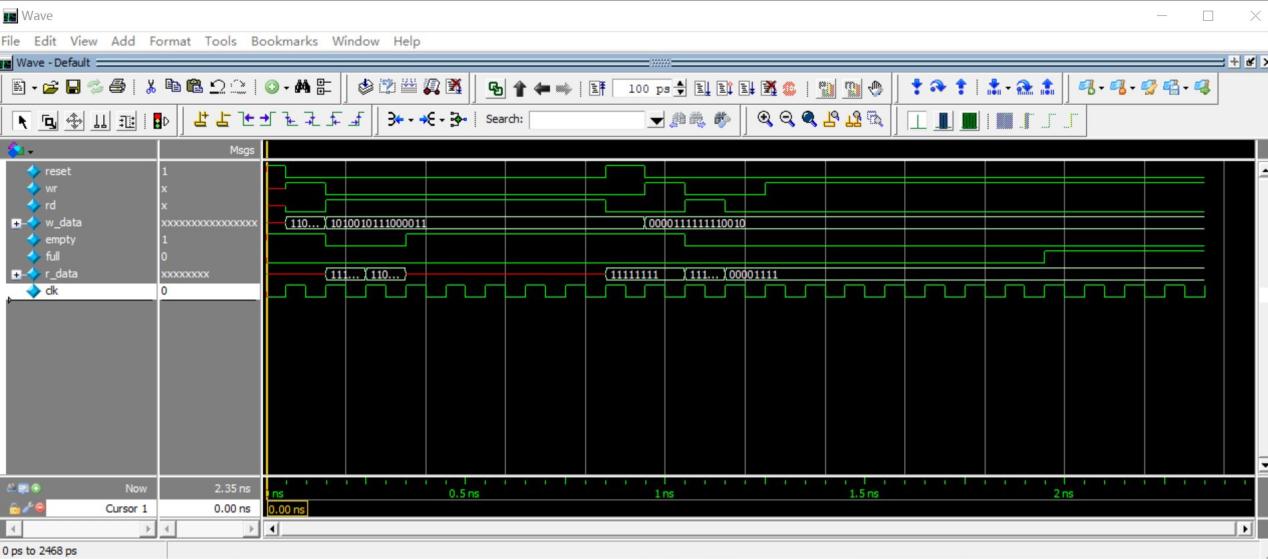
2.



reg\_file testbench



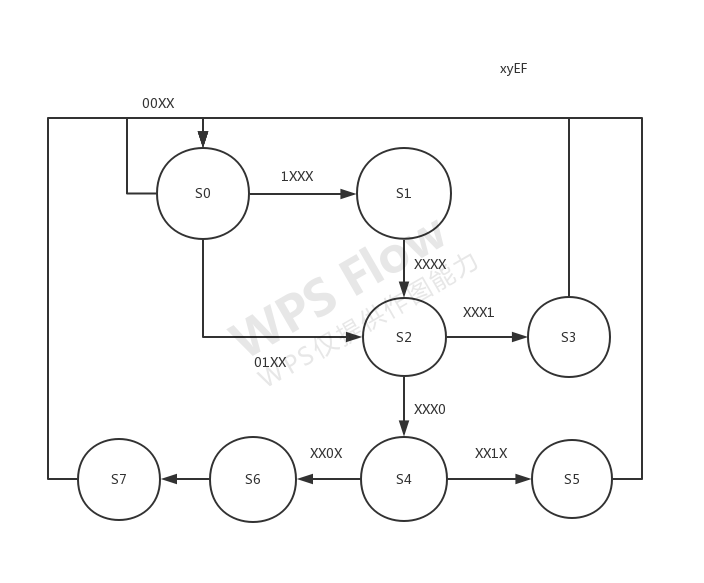
fifo\_ctrl testbench



fifo testbench

I used the 8-bit data width and 4-bit address width just like the default value from the provided code. I set the write port to write 2 addresses at the same time and when a new data is written, the address pointer increments by 2. The logic to check full is also changed because one writing fills two slots at the same time, I need to check both write address and the next one address to see if any of them meets the read address. In this way, I modified the FIFO so that its writing port is twice as wide as the reading port.

3.



Feedback

I found this homework a little hard, mainly because it is pretty vague on the specifics. Though in fact it did not take me too much time to modify the code, probably just 2 hours to finish everything.